

PSpice Model BRT (Bias Resistor Transistor) KEC KRC101

Model Information

 Model
 A macro model based on Gummel-Poon model

 Call Name
 MDC_KRC101_PS

 Pin Assign
 1:E 2:C 3:B

 File List
 Model Library
 MDC_KRC101_PS01.lib

 Model Report
 MDC_KRC101_PS.pdf (this file)

Verified Simulator Version Note

PSpice version 16.6

References

The information which was used for modeling is as follow:

[Data Sheet]

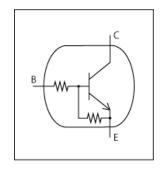
Date/Version
Product name
Company name
Characteristics

No:2 KRC101 KEC Corporation IcVi[OFF],IcVi[ON],hFEIc[Temp],tr,tstg,tf

Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Collector-emitter voltage (DC)	0	to	50	V
Base current (DC)	0	to	0.0018	А
Temperature	-55	to	150	deg C

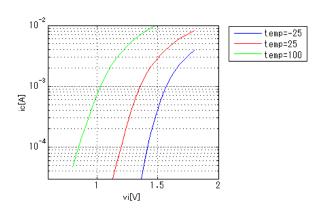




Simulation results are following. Explanatory notes — : simulated

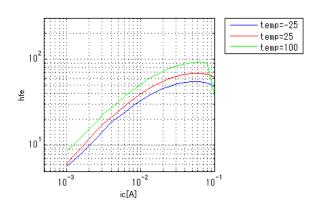
lcVi[OFF]

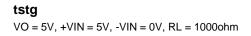
Vce = 5V

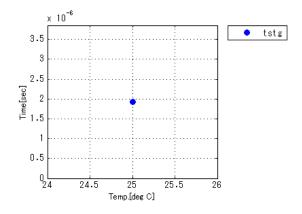


hFElc[Temp]

Vce = 5V



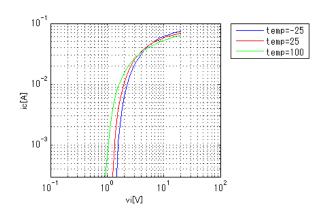




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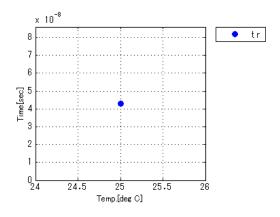
lcVi[ON]

Vce = 0.2V

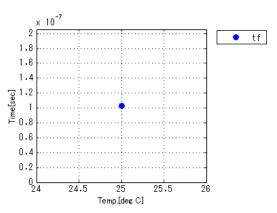


tr VO = 5V + V

VO = 5V, +VIN = 5V, -VIN = 0V, RL = 1000 hm



tf VO = 5V, +VIN = 5V, -VIN = 0V, RL = 1000ohm





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