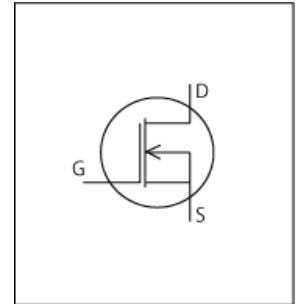


# LTspice Model

## NMOS

## STM

## STD8N60DM2



### Model Information

**Model** A macro model based on BSIM3 model  
**Call Name** MDC\_STD8N60DM2\_LT  
**Pin Assign** 1:G 2:D 3:S  
**File List** Model Library MDC\_STD8N60DM2\_LT01.lib  
 Model Report MDC\_STD8N60DM2\_LT.pdf (this file)

**Verified Simulator Version** LTspice version XVII  
**Note**

### References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version Rev 3 - September 2018
- Product name STD8N60DM2
- Company name STMicroelectronics N.V.
- Characteristics IdVds[Vgs], IdVgs[Temp], VgsQg[Vdd], VdsQg[Vdd], Rds(on)Id[Vgs], CapacitanceVds[Cname], NormVthTemp[Id], NormRds(on)Temp[Vgs], NormBvTemp{Ir}, VsdIs[Temp], SwitchingIdd[Tname], Trrlf[Ir], Qrrlf[Ir], Trrlf[Ir]2, Qrrlf[Ir]2SwitchingWaveform, TrWaveform

### Simulation Range

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	600	V
Gate-source voltage (DC)	-25	to	25	V
Temperature	-55	to	150	deg C

## MOSFET

○ : Implemented  
× : Not Implemented  
— : Not applicable

Model Functions Table

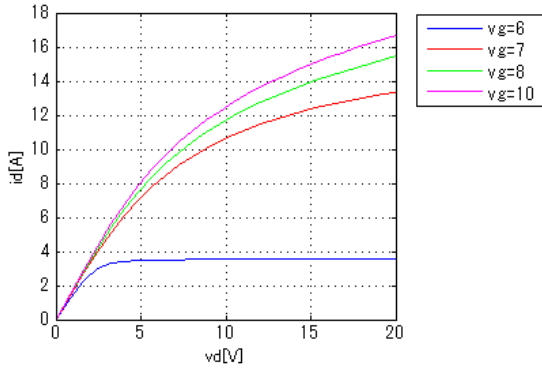
RANK=1

Functions	RANK	Implemented
ID-VDS-VGS	1	○
ID-VGS(Temp)	1	○
RDS(on)	1	○
Capacitance	1	○
Gate Charge	1	○
IS-VSD(Forward)	1	○
Reverse recovery	1	○
Switching(Typ.)	1	○
Bv	1	○
Yfs	1	—
Vth	1	○

Simulation results are following.  
 Explanatory notes — : simulated

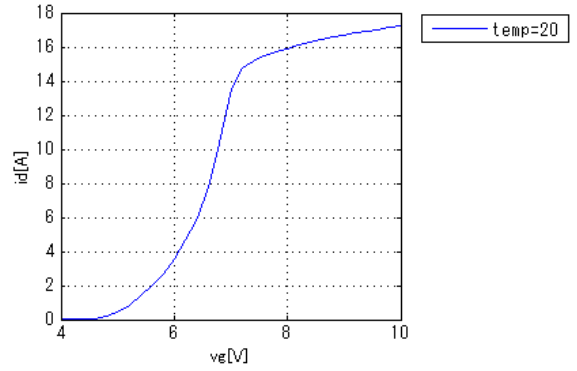
**IdVds[Vgs]**

Temp = 25degC



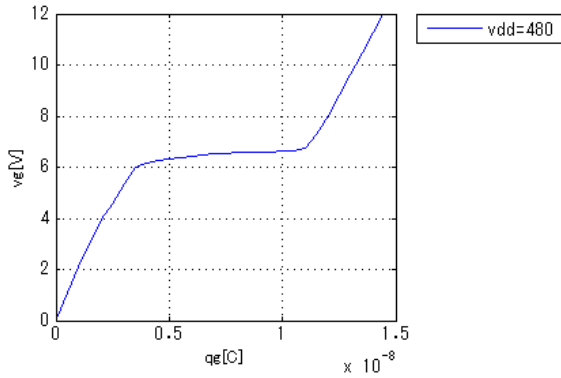
**IdVgs[Temp]**

Vds = 20V



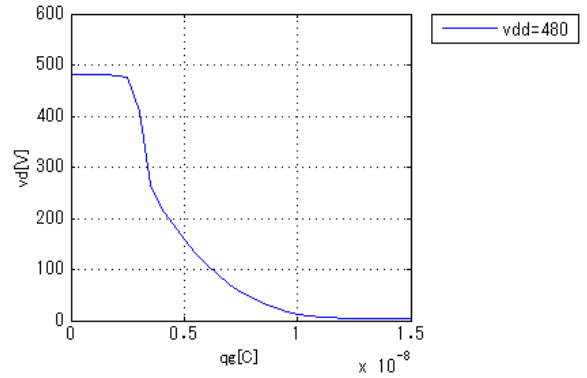
**VgsQg[Vdd]**

Id = 8A



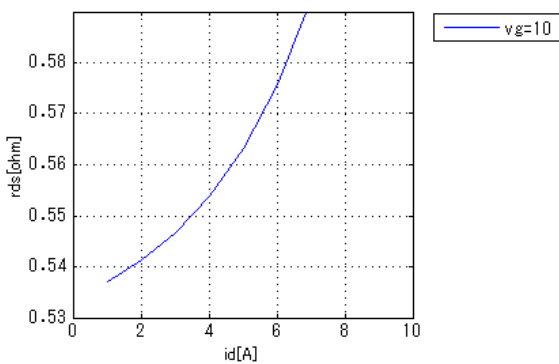
**VdsQg[Vdd]**

Id = 8A



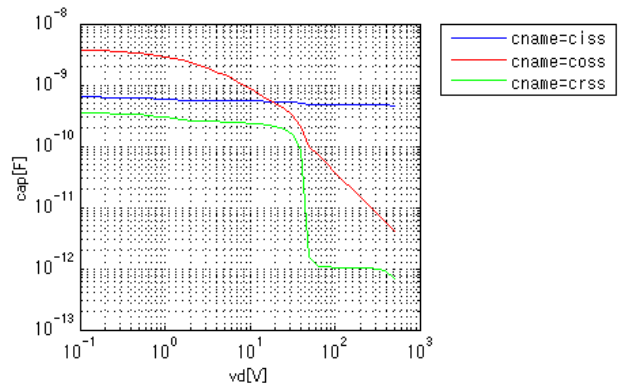
**Rds(on)Id[Vgs]**

Temp = 25degC



**CapacitanceVds[Cname]**

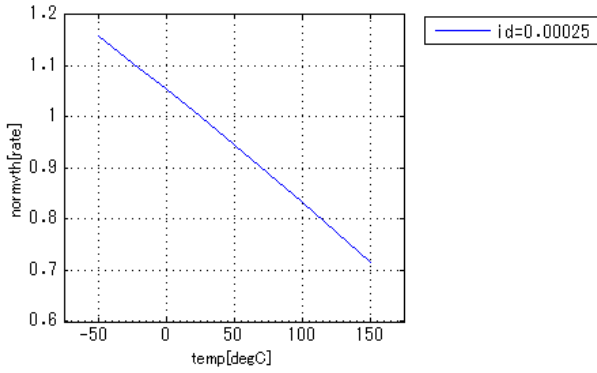
freq = 1000000Hz



Simulation results are following.  
 Explanatory notes — : simulated

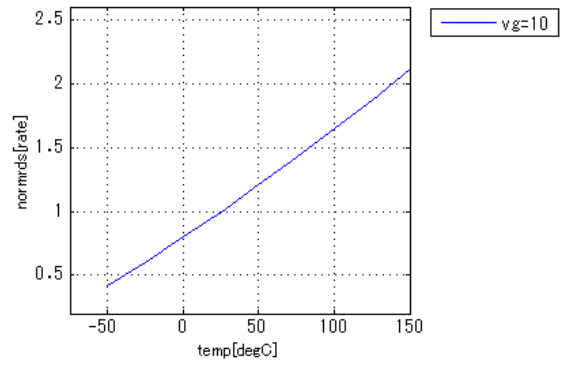
**NormVthTemp[Id]**

Vd = Vg

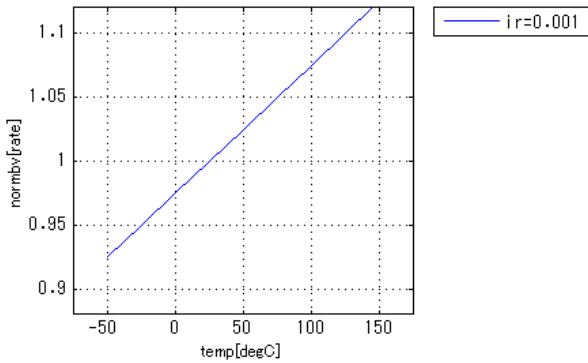


**NormRds(on)Temp[Vgs]**

Id = 4A

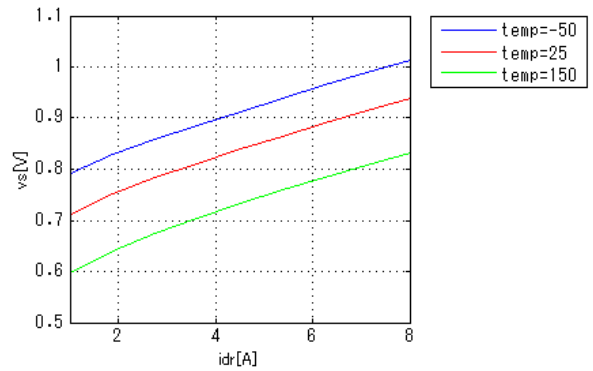


**NormBvTemp{Ir}**



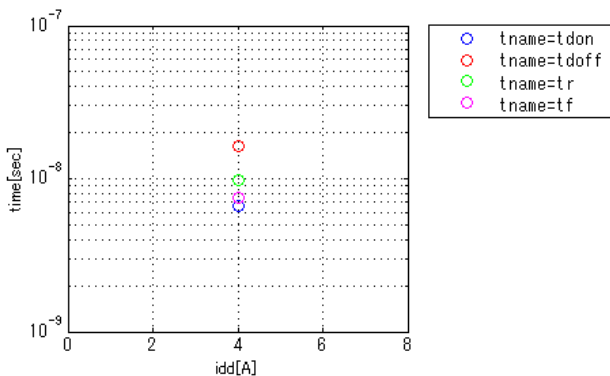
**Vsdlis[Temp]**

vg = 0V



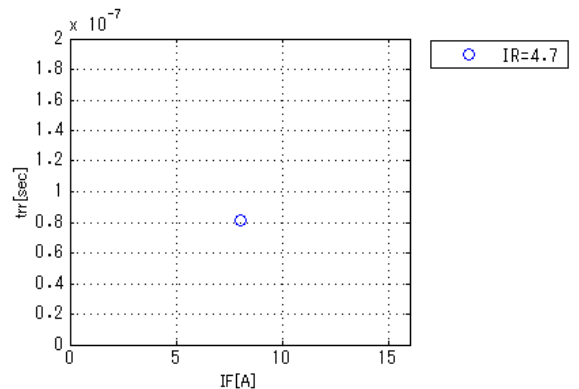
**SwitchingIdd[Tname]**

vgg = 10V, vdd = 300V, RGG = 4.7ohm



**TrrIf[Ir]**

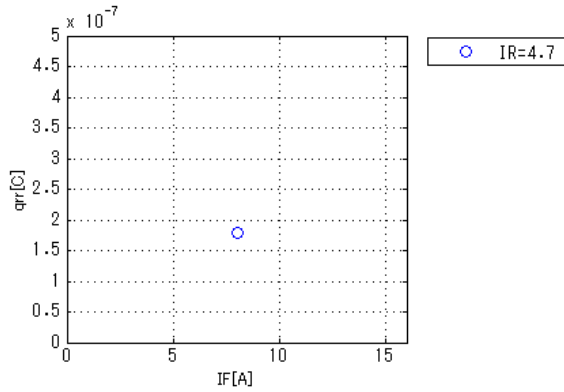
vdd = 60V, didt = 100A/us, Temp = 25degC



Simulation results are following.  
 Explanatory notes — : simulated

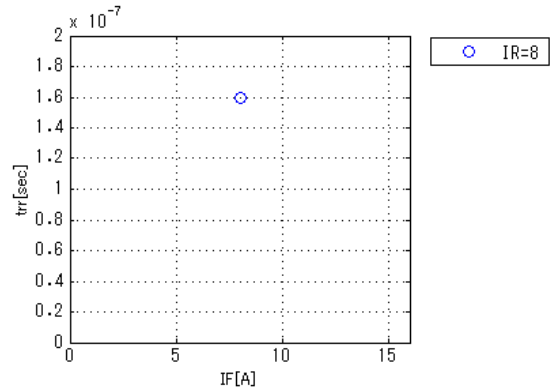
**Qrrlf[Ir]**

vdd = 60V, didt = 100A/us, Temp = 25degC



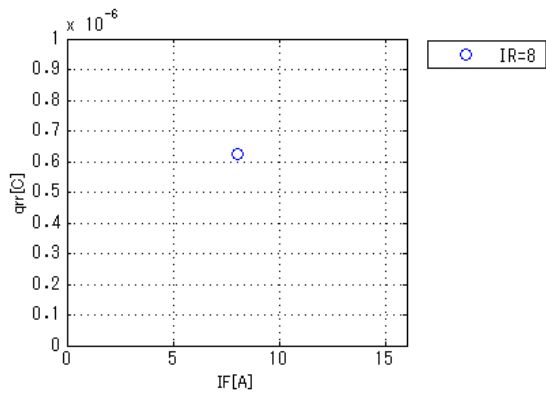
**Trrlf[Ir]2**

vdd = 60V, didt = 100A/us, Temp = 150degC



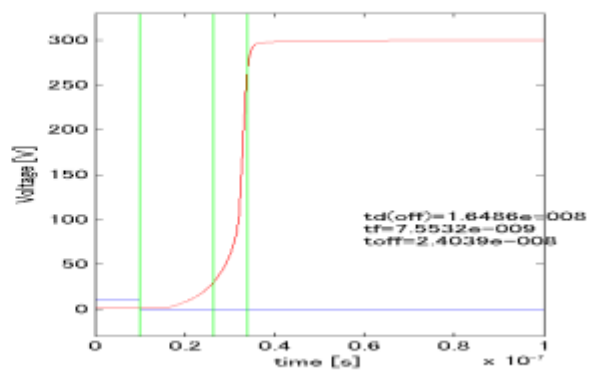
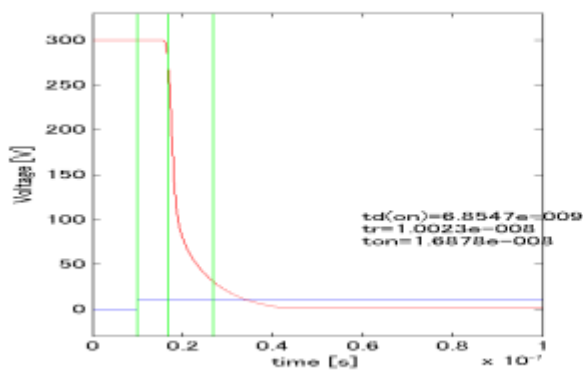
**Qrrlf[Ir]2**

vdd = 60V, didt = 100A/us, Temp = 150degC



**Switching Waveform ( Blue : INPUT Red : OUTPUT )**

v<sub>gg</sub> = 10V, v<sub>dd</sub> = 300V, R<sub>GG</sub> = 4.7ohm, I<sub>DD</sub> = 4A

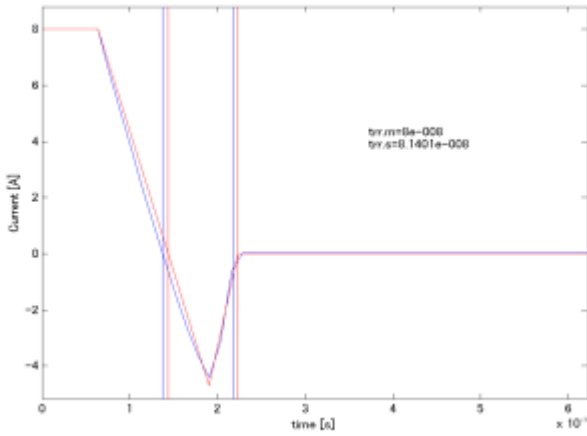


Simulation results are following.

Explanatory notes — : simulated

### Trr Waveform ( Red : Datasheet Blue : Simulation )

vdd = 60V, didt = 100A/us, Temp = 25degC, If = 8A



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