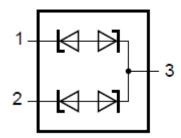


LTspice Model ESD Protection Diode Nexperia PESD5V0L2BT



Model Information

Model	A macro model based on general SPICE diode model			
Call Name	MDC_PESD5V0L2BT_LT			
Pin Assign	1:cathode1 2:cathode2 3:double cathode			
File List	Model Library	MDC_PESD5V0L2BT_LT01.lib		
	Model Report	MDC_PESD5V0L2BT_LT.pdf (this file)		

Verified Simulator Version Note

LTspice version XVII

References

The information which was used for modeling is as follow:

[Data Sheet]
Date/Version
Product name
Company name
Characteristics

Rev. 02 - 25 August 2009 PESD5V0L2BT Nexperia B.V. IrVr[Temp],CjVr,IrTemp[Vr],RdiffIr[Temp],SurgeWaveform,E SDClampingWaveform

Simulation Range

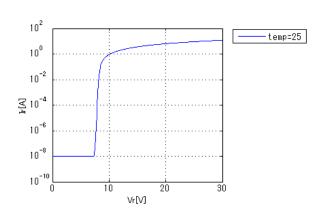
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Reverse Voltage	0	to	28	V
Temperature	-65	to	150	deg C

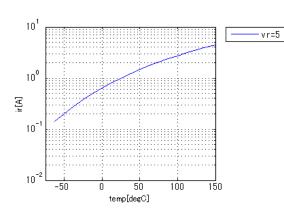


Simulation results are following. Explanatory notes -: simulated

IrVr[Temp]



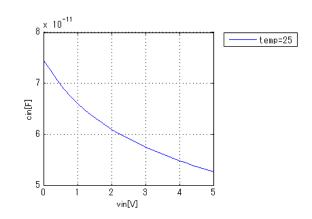
IrTemp[Vr]



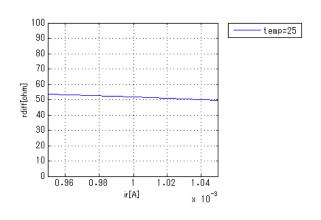
Surge Waveform

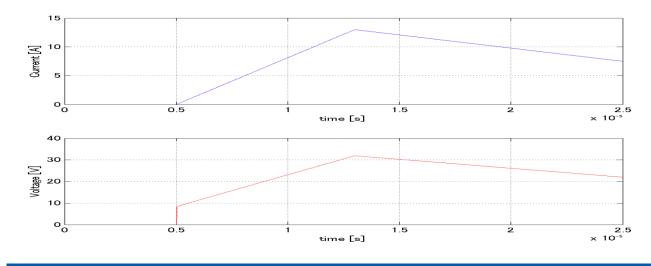
CjVr

Freq. = 1MHz



Rdifflr[Temp]



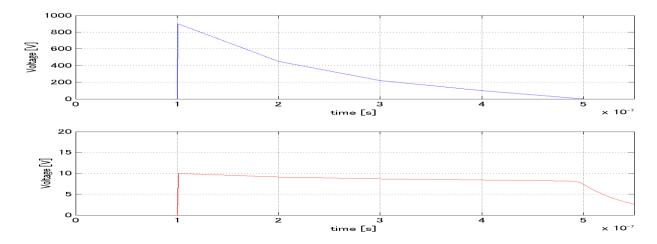


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Simulation results are following. Explanatory notes -: simulated

ESD Clamping Waveform





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