

LTspice Model LED Driver TEXAS INSTRUMENTS TPS92520QDADRQ1

Model Information

Model	A macro model
Call Name	MDC_TPS92520QDADRQ1_LT
	1:COMP1 2:UDIM1 3:PGND1A 4:PGND1B 5:VIN1A 6:VIN1B 7:AGND1 8:V5D 9:V5A 10:AGND2 11:VIN2A 12:VIN2B 13:PGND2A 14:PGND2B 15:UDIM2 16:COMP2 17:CSN2 18:CSP2 19:BST2 20:SW2B 21:SW2A 22:MOSI 23:MISO
Pin Assign	24:SCK 25:SSN 26:LHI 27:FLT 28:SW1B 29:SW1A 30:BST1 31:CSP1 32:CSN1 33:PWMPH 34:CH1EN 35:CH1INTPWM 36:CH2EN 37:CH2INTPWM 38:CH1HSILIMFL 39:CH1LSILIMFL 40:CH2HSILIMFL 41:CH2LSILIMFL 42:SLEEP 43:CH1IADJ
File List	Model Library MDC_TPS92520QDADRQ1_LT01.lib Model Report MDC_TPS92520QDADRQ1_LT.pdf(this file)
Varified Simu	

 Verified Simulator Version
 LTspice

 Note
 Strongly recommend a Maximum Timestep of 10ns during verification

 Pin33 to Pin34 are additional pins

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version	FEBRUARY 2021
Product name	TPS92520QDADRQ1
Company name	TEXAS INSTRUMENTS

[Characteristics listed]
Characteristics

PWM Operation INT PWM Dimming Sleep Mode V5D/V5A UVLO

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit	
Temperature	25	deg C	

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Model Functions Table	RANK=1	
Functions	RANK	Implemented
Control Method(PWM,PFM)	1	0
Programmable switching frequency	1	0
Soft Start	1	0
precision analog dimming	1	0
precision internal PWM dimming	1	0
Supports external PWM dimming input	1	0
UVLO	1	0
Configurable analog reference	1	0
switching frequency	1	0
PWM dimming duty cycle	1	0
Fault monitoring and reporting	1	0



Model specifications

Simulation results are following. Explanatory notes -: simulated





Additional pin information

Simulation results are following.

Explanatory notes -: simulated

No	Added Pin Name	Function
33	PWMPH	PWM phase shift setting for internal PWM generator
34	CH1EN	CH1 enable
35	CH1INTPWM	Enable internal PWM generator function for channel 1
36	CH2EN	CH2 enable
37	CH2INTPWM	Enable internal PWM generator function for channel 2
38	CH1HSILIMFL	Channel 1 high-side FET current limit fault response
39	CH1LSILIMFL	Channel 1 low-side FET current limit fault response
40	CH2HSILIMFL	Channel 2 high-side FET current limit fault response
41	CH2LSILIMFL	Channel 2 low-side FET current limit fault response
42	SLEEP	Sleep Command
43	CH1IADJ	Channel 1 Analog Current Control
44	CH2IADJ	Channel 2 Analog Current Control
45		

Additional pin settings Simulation results are following. Explanatory notes — : simulated

No	Added Pin Name	Setting
33	PWMPH	0 = 180° phase shift between internally generated PWM signals 5 = 0° phase shift between internally generated PWM signals
34	CH1EN	0 = Disable LED channel 1 5 = Enable LED channel 1
35	CH1INTPWM	0 = LED current duty cycle of channel 1 controlled by external signal connected to UDIM1 input 5 = LED current duty cycle of channel 1 controlled by internal PWM generator
36	CH2EN	0 = Disable LED channel 2 5 = Enable LED channel 2
37	CH2INTPWM	0 = LED current duty cycle of channel 2 controlled by external signal connected to UDIM2 input 5 = LED current duty cycle of channel 2 controlled by internal PWM generator
38	CH1HSILIMFL	0 = Channel 1 auto-restarts after the ILIM fault timer has expired. 5 = Channel 1 is latched off
39	CH1LSILIMFL	0 = Channel 1 auto-restarts after the ILIM fault timer has expired. 5 = Channel 1 is latched off
40	CH2HSILIMFL	0 = Channel 2 auto-restarts after the ILIM fault timer has expired. 5 = Channel 2 is latched off
41	CH2LSILIMFL	0 = Channel 2 auto-restarts after the ILIM fault timer has expired. 5 = Channel 2 is latched off
42	SLEEP	0 = Exit sleep mode and return to normal operation (SLEEP OFF). 5 = Enter sleep mode (SLEEP ON).
43	CH1IADJ	0~1023 Channel 1 Analog Current Control
44	CH2IADJ	0~1023 Channel 2 Analog Current Control



Additional parameter information

Simulation results are following.

Explanatory notes — : simulated

No	Added Parameter	Function
1	pwmdiv	The clock divider for the internal PWM generator
2	ch1pwm	Channel 1 PWM width control
3	ch2pwm	Channel 2 PWM width control
4	ch1ton	Channel 1 on-time control
5	ch2ton	Channel 2 on-time control
6	ift	The counter limit for the fault timer

Additional parameter setting

Simulation results are following. Explanatory notes — : simulated

No	Added Parameter	Function
1	pwmdiv	7 = fPWM = 1507 Hz 8 = fPWM = 1318 Hz 10 = fPWM = 1055 Hz 12 = fPWM = 879 Hz 16 = fPWM = 659 Hz 24 = fPWM = 439 Hz 49 = fPWM = 215 Hz 98 = fPWM = 108 Hz
2	ch1pwm	1~1023 Channel 1 PWM width control
3	ch2pwm	1~1023 Channel 2 PWM width control
4	ch1ton	1~43 Channel 1 on-time control
5	ch2ton	1~43 Channel 2 on-time control
6	ift	0 = 3.6 ms fault timer 1 = 7.2 ms fault timer 2 = 14.4 ms fault timer 3 = 28.8 ms fault timer



PWM Operation

Simulation results are following. Explanatory notes -: simulated





PWM Operation

Simulation results are following. Explanatory notes -: simulated



PWM Operation

Simulation results are following. Explanatory notes — : simulated

Sim result

2.04					V(vin)					
VIN										
120-	-									
5.01/2		V((v5d)				V(v5a)			
V5D)/V5A									
2.30										
V(comp2) V(comp1)										
COMP1	/COMP2			fW=462kHz						
0.01/-			4							
27V-				→	V(sw <mark>1</mark>)					
12V- SW1										
-3V			tON=706	ns			fW=449kHz			
27V-					V(sw2)					
12V- SW2						+				
-3V							/N=1.4105			
5.0V-					V(fit)					
2.5V- FLI										
0.0V					\//4\					
10mV	1 CONH)				v(csp),csi()					
SomV-V(CSP.	1,0311)									
10mV	i				V(csp2.csn2)					
	2 (SN2)									
50mV-	2,00112/1									
10mV					I(Ried1)					
TLED1		_								
0.5A-										
-0.1A	_				I(Ried2)					
ILED2	1									
0.5A-										
1.10-					I(L1)					
0.5A- IL1										
0.10										
1.1A-					I(L2)					
0.5A IL2										
0.14										
0.990ms	0.991ms	0.992ms	0.993ms	0.994ms	0.995ms	0.996ms	0.997ms	0.998ms	0.999ms	1.000



INT PWM Dimming

Simulation results are following. Explanatory notes -: simulated



INT PWM Dimming

Simulation results are following. Explanatory notes — : simulated





Sleep Mode

Simulation results are following. Explanatory notes -: simulated



Sleep Mode

Simulation results are following. Explanatory notes — : simulated



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V5D/V5A UVLO

Simulation results are following. Explanatory notes -: simulated



V5D/V5A UVLO

Simulation results are following. Explanatory notes - : simulated



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