

# LTspice Model

## IPM

### Fuji Electric

### 7MBR75XME120-50

#### Model Information

<b>Model</b>	A macro model
<b>Call Name</b>	MDC_7MBR75XME120-50_LT
<b>Pin Assign</b>	1:R1-1 2:R1-2 3:S-1 4:S-2 5:T-1 6:T-2 7:Gu 8:U-1 9:U-2 10:Gv 11:V-1 12:V-2 13:W-1 14:Gw 15:W-2 16:T1 17:T2 18:Gz 19:Gy 20:En 21:Gx 22:Gb 23:N1-1 24:N1-2 25:P1-1 26:P1-2 27:B 28:P-1 29:P-2 30:N-1 31:N-2
<b>File List</b>	Model Library MDC_7MBR75XME120-50_LT01.lib Model Report MDC_7MBR75XME120-50_LT.pdf(this file)
<b>Verified Simulator Version</b>	LTspiceXVII

#### Note

#### References

The information which was used for modeling is as follow:

##### [Data Sheet]

- Date/Version 2017/06
- Product name 7MBR75XME120-50
- Company name Fuji Electric

##### [Characteristics listed]

- Characteristics Icvcetemp[inverter],icvcevge(temp25)[inverter] ,  
icvcevge(temp175)[inverter] ,Vcevgetemp[inverter],ifvf[inverter],  
cap[inverter],vgqgvce[inverter],trr[inverter],sw[inverter] ,  
Icvcetemp[brake],icvcevge(temp25)[brake],  
icvcevge(temp175)[brake],Vcevgetemp[brake],ifvf[brake],  
cap[brake],vgqgvce[brake],sw[brake],ifvf[converter],  
Switching\_Lower[chip,module],Switching\_Upper[chip,module]

#### Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Condition	Unit
Collector-emitter voltage (DC)	0 to 1,200	V
Gate-emitter voltage (DC)	0 to 20	V
Temperature	-40~125	deg C

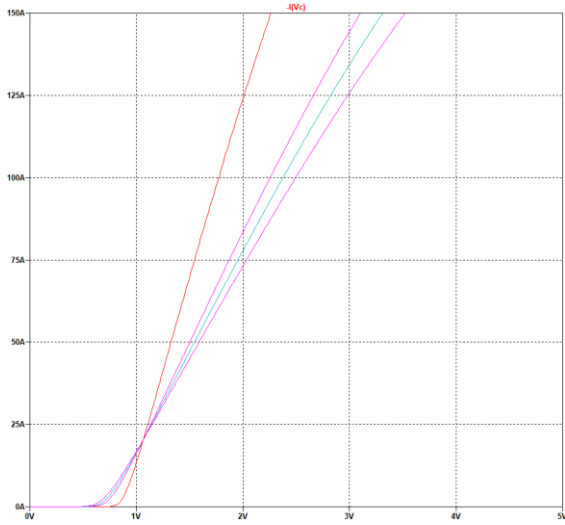
**Model Functions Table**

Functions	Implemented
Inverter	○
Brake	○
converter	○
chip,module	○
Thermistor	-

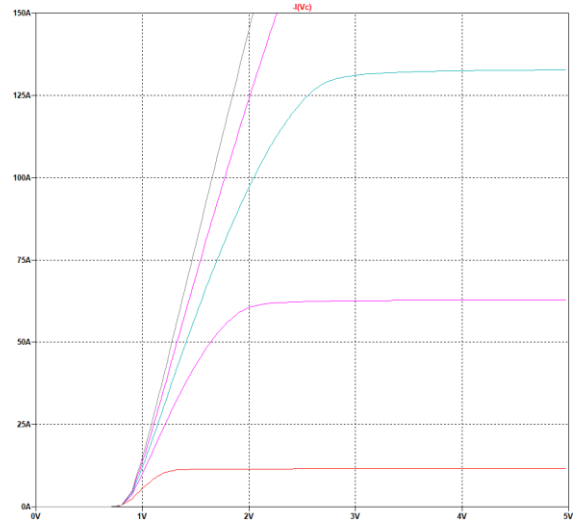
Simulation results are following.  
 Explanatory notes — : simulated

lcvcetemp[inverter],icvceve(temp25)[inverter] ,icvceve(temp175)[inverter] , Vcevgetemp[inverter]

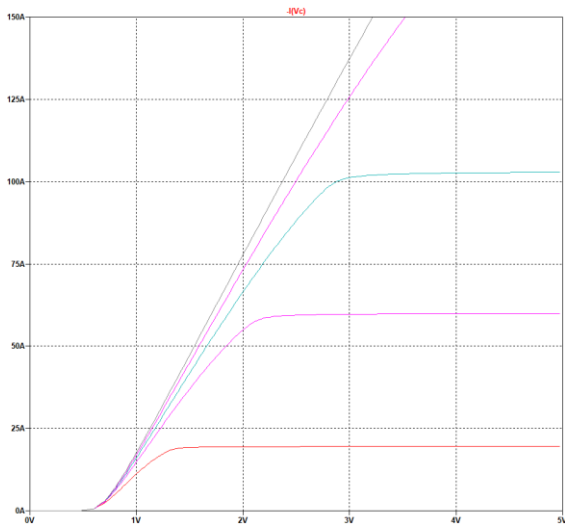
lcvcetemp[inverter]



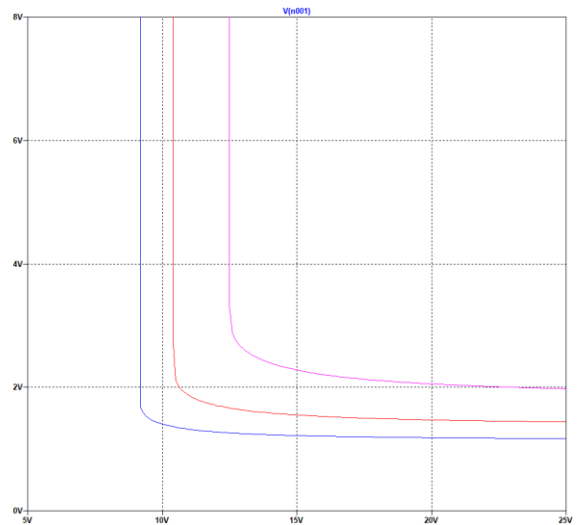
icvceve(temp25)[inverter]



icvceve(temp175)[inverter]



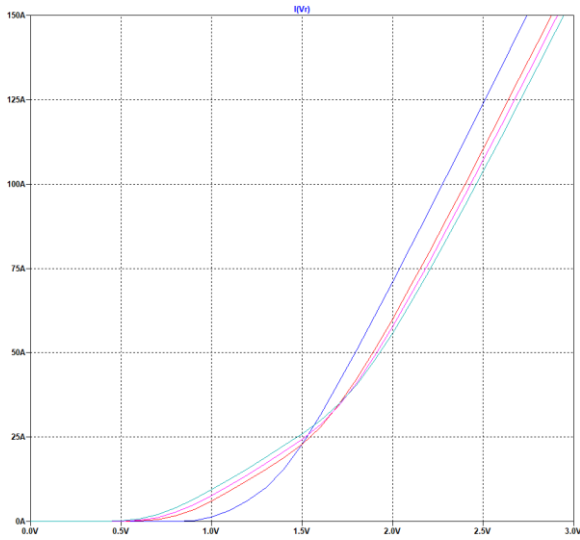
Vcevgetemp[inverter]



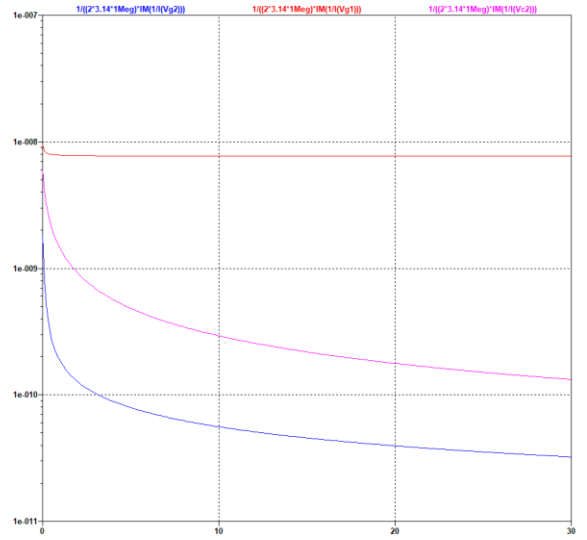
Simulation results are following.  
 Explanatory notes — : simulated

ifvf[inverter],cap[inverter],vgqgvce[inverter],trr[inverter],

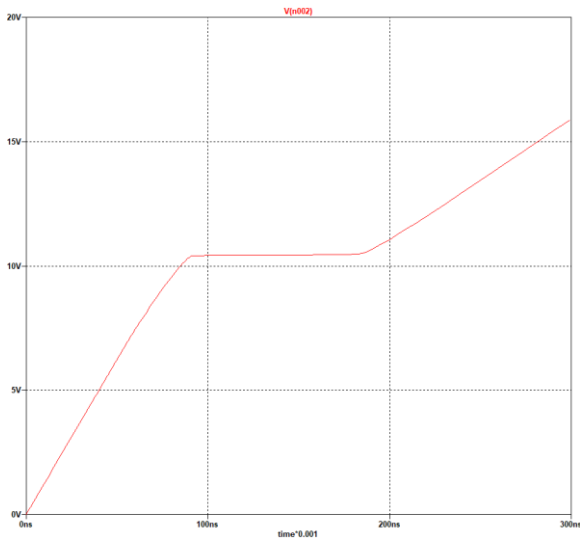
ifvf[inverter]



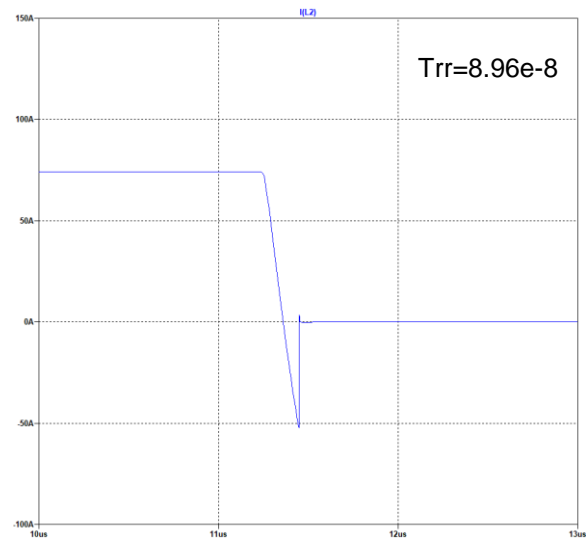
cap[inverter]



vgqgvce[inverter]



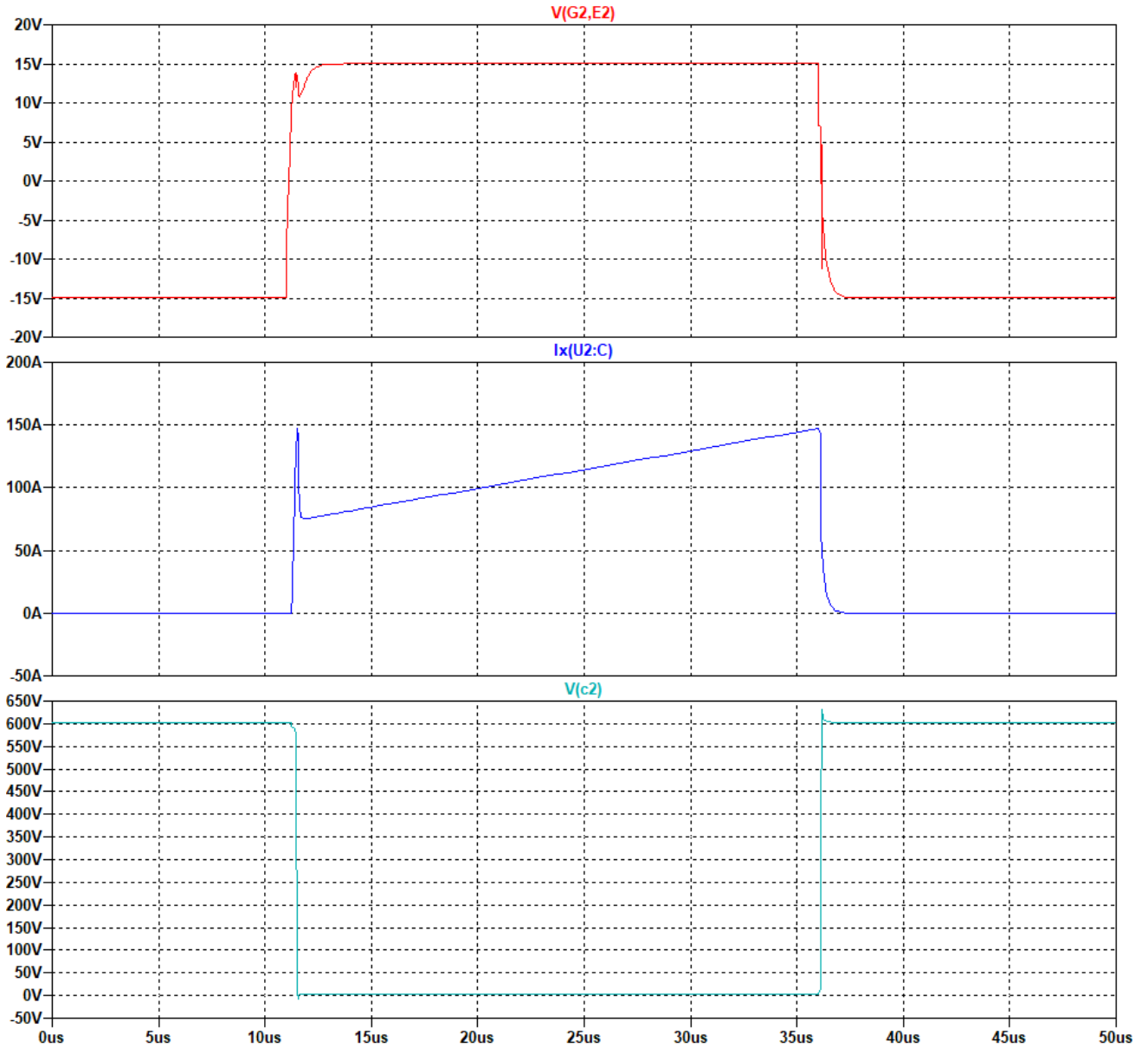
trr[inverter]



Simulation results are following.  
Explanatory notes — : simulated

sw[inverter]

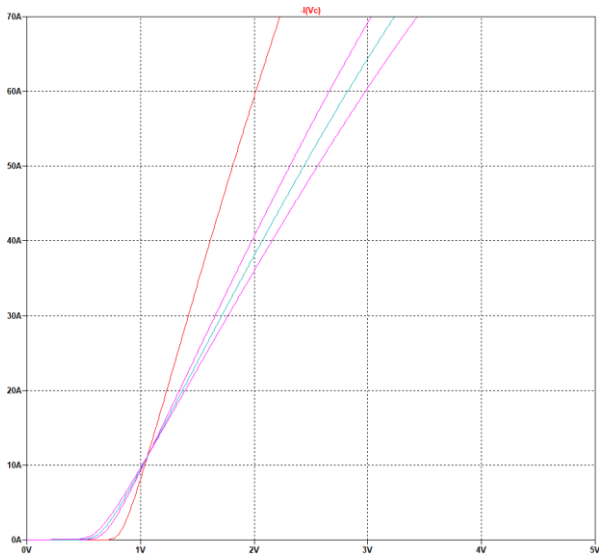
$T_d(\text{on})=4.10\text{e-}7$   $t_r=2.65\text{e-}7$   $t_d(\text{off})=1.25\text{e-}007$   $t_f=0.35\text{e-}007$



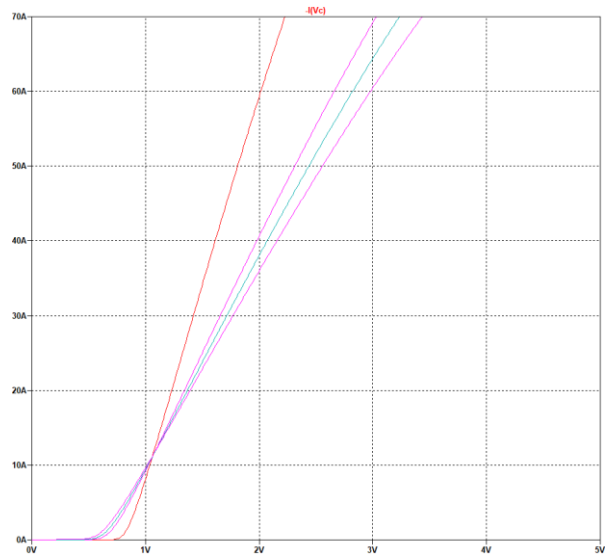
Simulation results are following.  
 Explanatory notes — : simulated

Icvcetemp[brake],icvcevge(temp25)[brake],icvcevge(temp175)[brake], VcevgeTemp[brake]

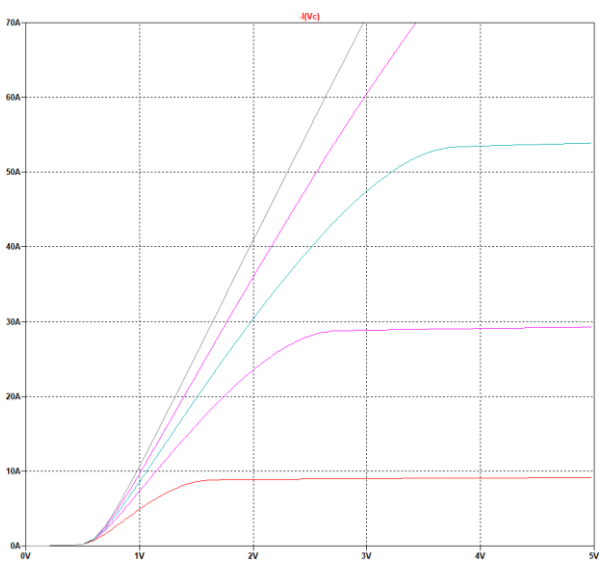
Icvcetemp[brake]



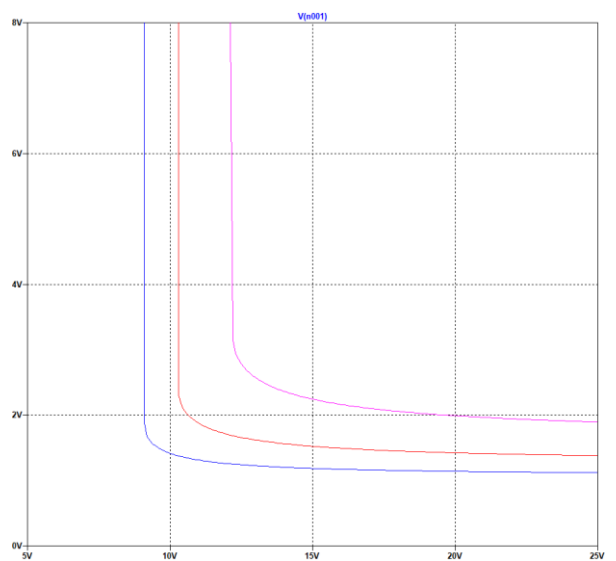
icvcevge(temp25)[brake]



icvcevge(temp175)[brake]



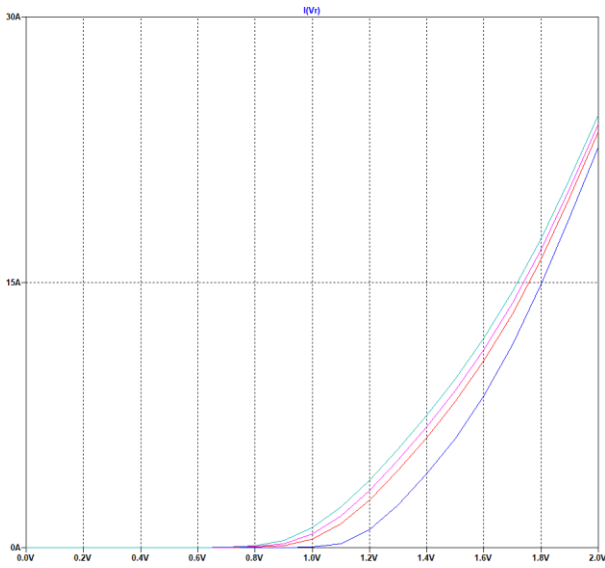
VcevgeTemp[brake]



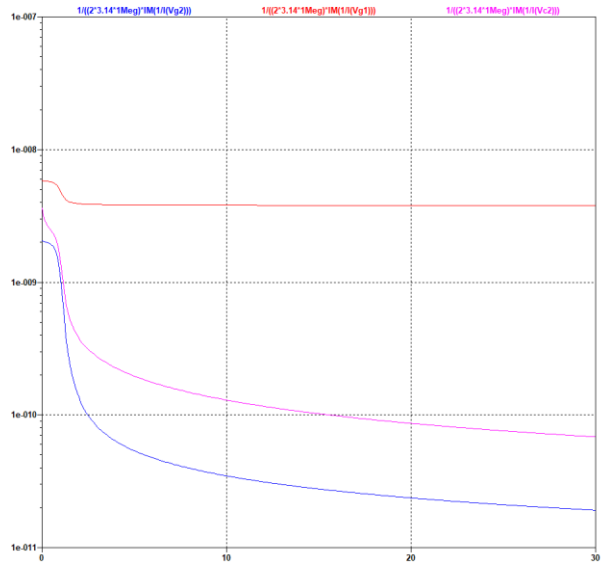
Simulation results are following.  
 Explanatory notes — : simulated

ifvf[brake],cap[brake],vgqgvce[brake]

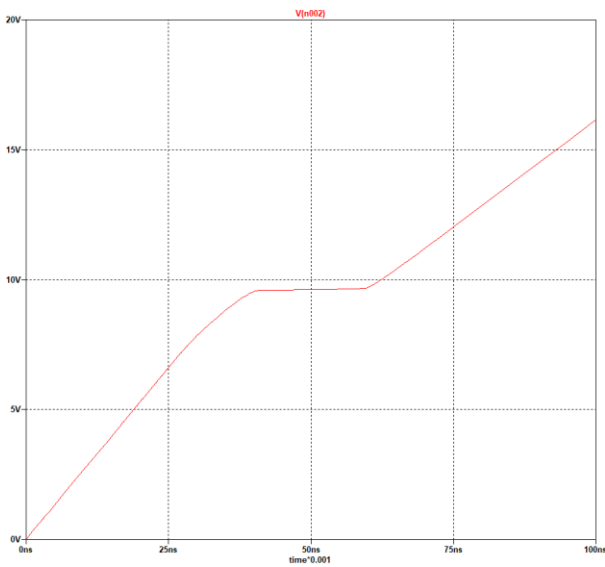
ifvf[brake]



cap[brake]



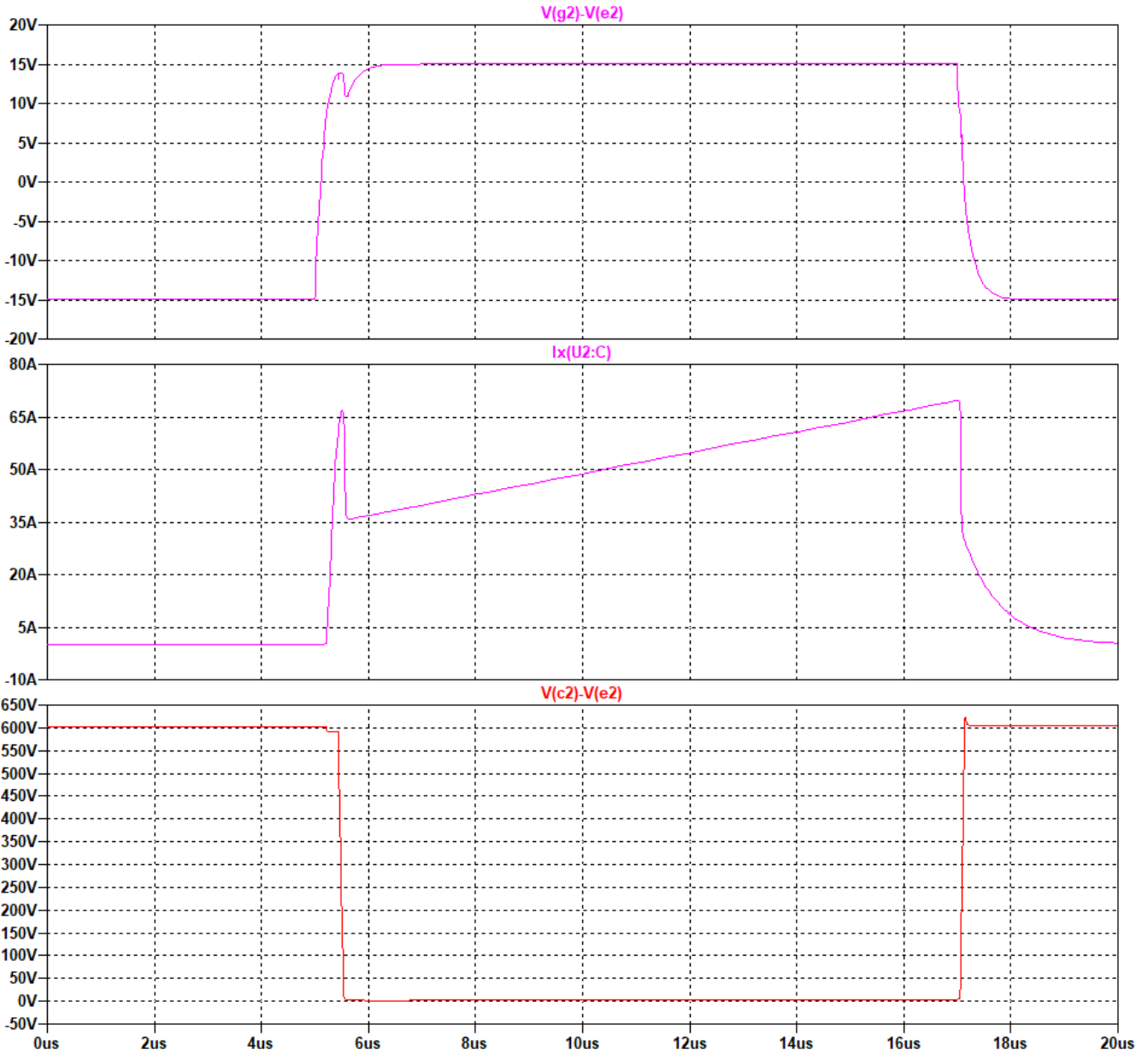
vgqgvce[brake]



Simulation results are following.  
 Explanatory notes — : simulated

sw[inverter]

$T_d(\text{on})=4.16\text{e-}7$   $t_r=3.13\text{e-}7$   $t_d(\text{off})=0.35\text{e-}007$   $t_f=0.85\text{e-}007$

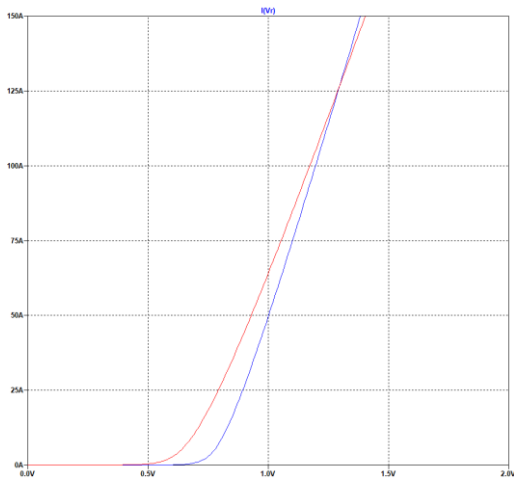




Simulation results are following.  
Explanatory notes — : simulated

ifvf[converter]

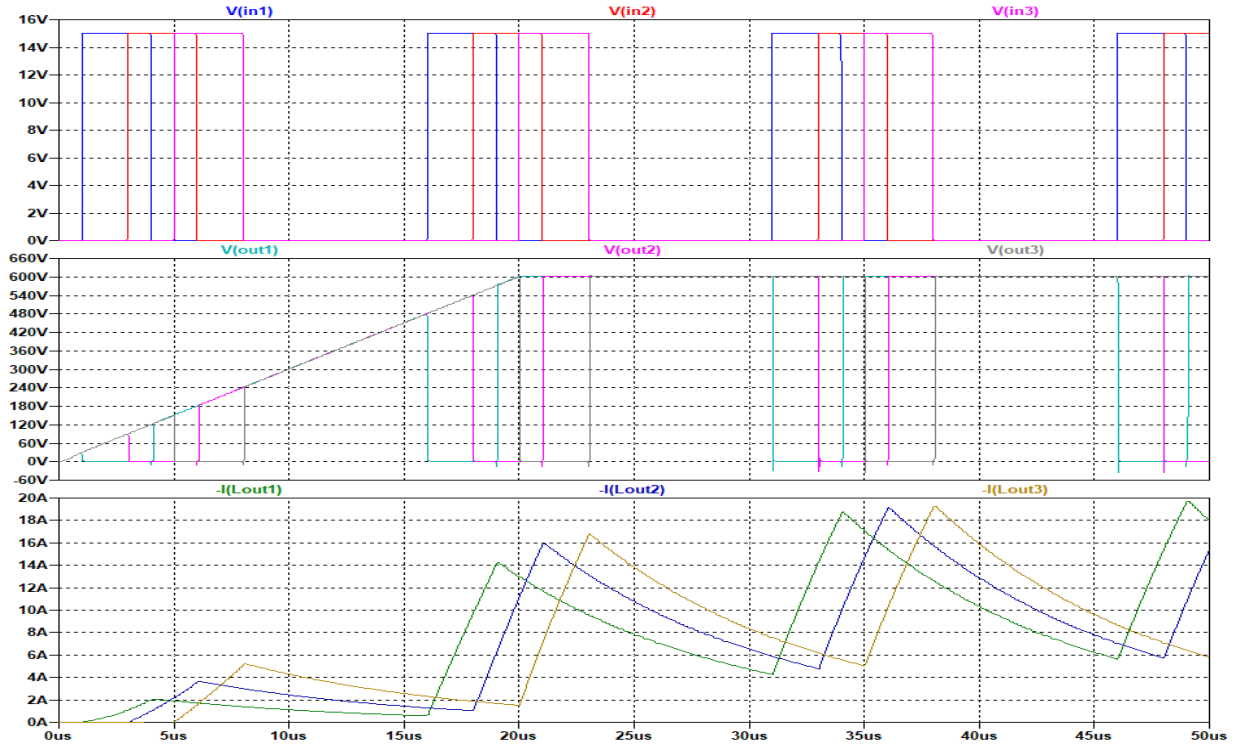
ifvf[converter]



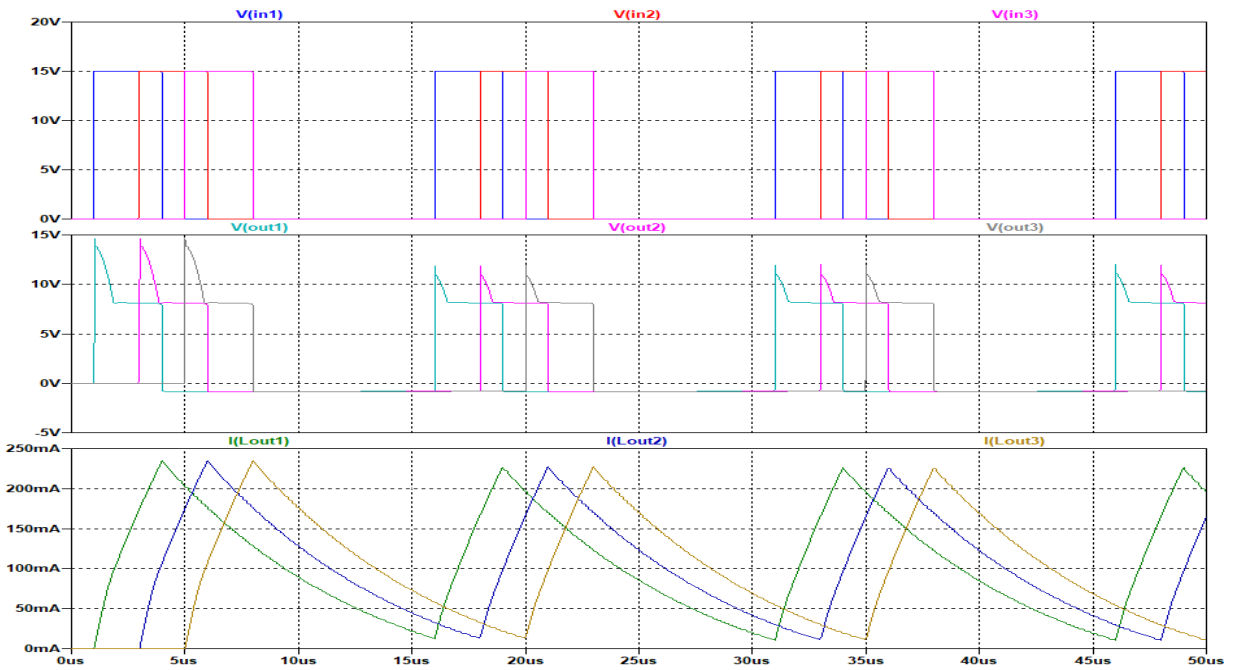
Simulation results are following.  
 Explanatory notes — : simulated

Switching\_Lower[chip,module],Switching\_Upper[chip,module]

Switching\_Lower[chip,module]



Switching\_Upper[chip,module]



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