

LTspice Model No-Opto Isolated Flyback Converter Maxim Integrated MAX17692B

Model Information

 Model
 A macro model

 Call Name
 MDC_MAX17692B_LT

 Pin Assign
 1:VIN 2:GND 3:VCC 4:SYNC/DITHER 5:RT 6:TC/VCM 7:SS 8:SET 9:COMP

 File List
 Model Library
 MDC_MAX17692B_LT01.lib

 Model Report
 MDC_MAX17692B_LT.pdf(this file)

 Verified Simulator Version
 LTspice XVII

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

Date/Version	Rev 0; 12/20
Product name	MAX17692B
Company name	Maxim Integrated

[Characteristics listed]
Characteristics	

VENR, VENF, VENSHDN, VCC, VDO VVCC-UVR, VC-UVF, fSWRT, ISS, tSS DMAXOSC, tON_MIN, tOFF_MIN, RDSON ILX-PEAK-MAX, LX-PEAK-MIN, VSET

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

ltem	Condition			Linit
	Min	Тур	Max	Unit
Supply voltage	4.2		60.0	V
Temperature		25		deg C



Model Functions Table

Functions	Implemented
Eliminates the Optocoupler and Secondary-Side Error Amplifier	0
Soft-Start	0
Frequency Dithering Supports Low-EMI, Spread-Spectrum Operation	-
Switching Frequency Synchronization to External Clock	-
Output Diode Forward Voltage Temperature Compensation	-
Hiccup Current-Limit Protection	-
Programmable EN/UVLO Threshold	0





Testbench for Line/Load regulations (Vin=24[V] Fsw=146[kHz] Vout=5[V] lout=650[mA])







Testbench for Line/Load regulations (Vin=24[V] Fsw=146[kHz] Vout=5[V] lout=650[mA])





Testbench for Line/Load regulations (Vin=24[V] -> 0[V] -> 24[V] Fsw=146[kHz] Vout=5[V] lout=650[mA])







Testbench for Line/Load regulations (Vin=24[V] Fsw=146[kHz] Vout=5[V] lout=10[mA])







Testbench for Line/Load regulations (Vin=24[V] Fsw=146[kHz] Vout=5[V] lout=10[mA])





Testbench for Line/Load regulations (Vin=24[V] Fsw=146[kHz] Vout=5[V] lout=0.5[mA])





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