

LTspice Model

Darlington Transistor Array

Texas Instruments Inc.

ULN2003ADR

Model Information

Model	A macro model	
Call Name	MDC_ULN2003ADR_LT	
Pin Assign	1:1B 2:2B 3:3B 4:4B 5:5B 6:6B 7:7B 8:E 9:COM 10:7C 11:6C 12:5C 13:4C 14:3C 15:2C 16:1C	
File List	Model Library	MDC_ULN2003ADR_LT01.lib
	Model Report	MDC_ULN2003ADR_LT.pdf(this file)
Verified Simulator Version	LTspiceXVII	

Note

References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 2019/8
- Product name ULN2003ADR
- Company name Texas Instruments Inc.

[Characteristics listed]

- Characteristics VI(on), VCE(sat), ICEX, VF, I(off), II, IR, Ci
TPLH-HL/VOH, VI(ON)_ALL, VF_ALL

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

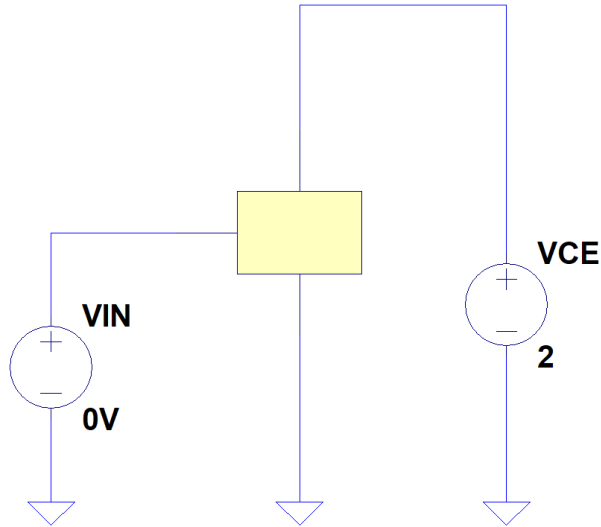
Item	Condition	Unit
Temperature	25	deg C

Model Functions Table

Functions	Implemented
VI(on)	<input type="radio"/>
VCE(sat)	<input type="radio"/>
ICEX	<input type="radio"/>
VF	<input type="radio"/>
I(off)	<input type="radio"/>
II	<input type="radio"/>
IR	<input type="radio"/>
Ci	<input type="radio"/>
TpLH-HL/VOH	<input type="radio"/>
VI(ON)_ALL	<input type="radio"/>
VF_ALL	<input type="radio"/>

VI(on) Testbench

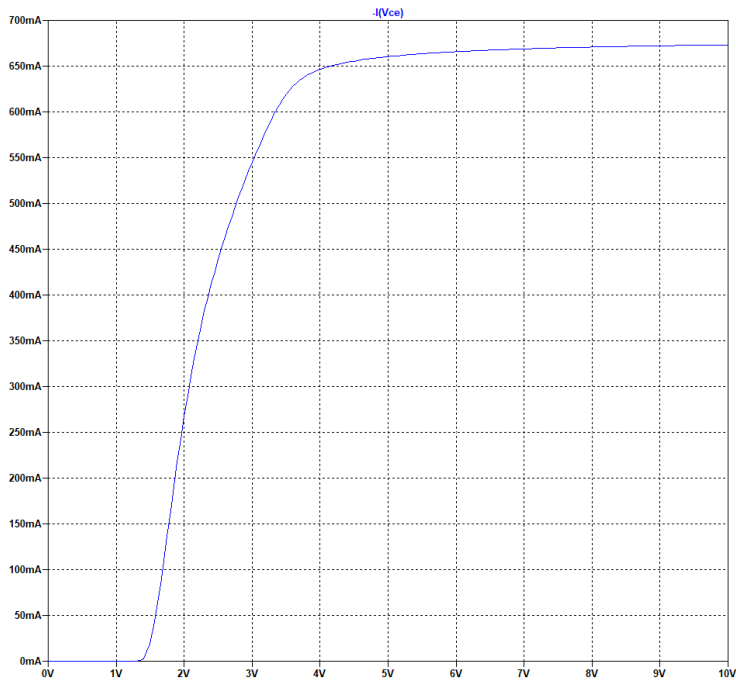
Referred to Data Sheet



```
.dc VIN 0 10 0.1
.lib ULN2003ADR.lib
```

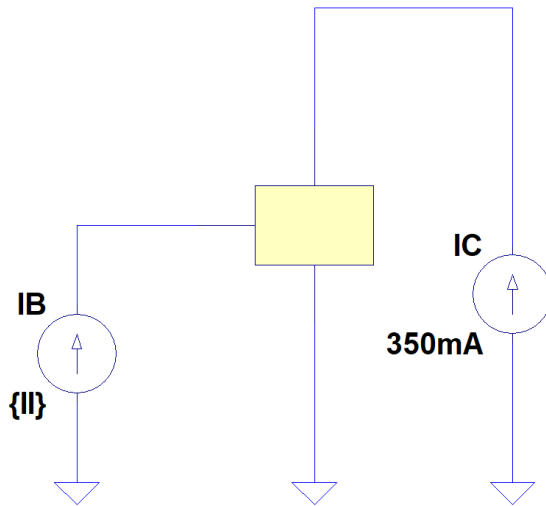
Simulation results are following.
 Explanatory notes — : simulated

VI(on)



VCE(sat) Testbench

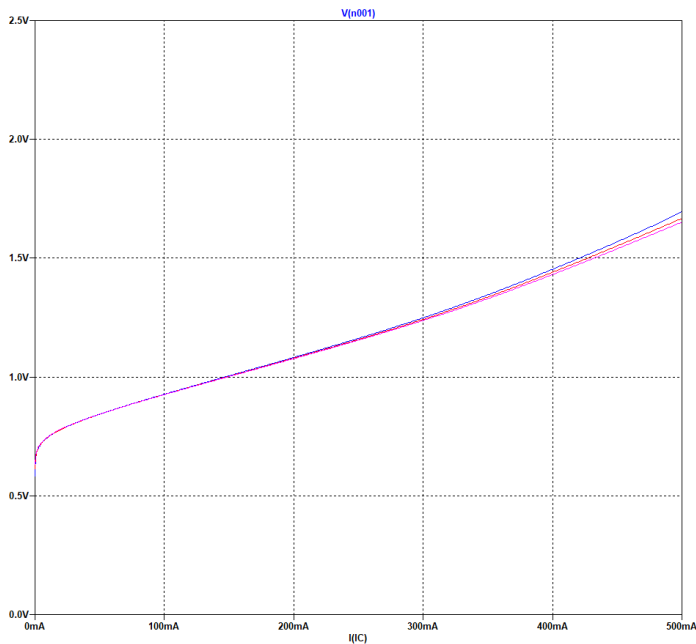
Referred to Data Sheet



```
.step param II list 250u 350u 500u
.dc IC 0 500m 0.1m
.lib ULN2003ADR.lib
```

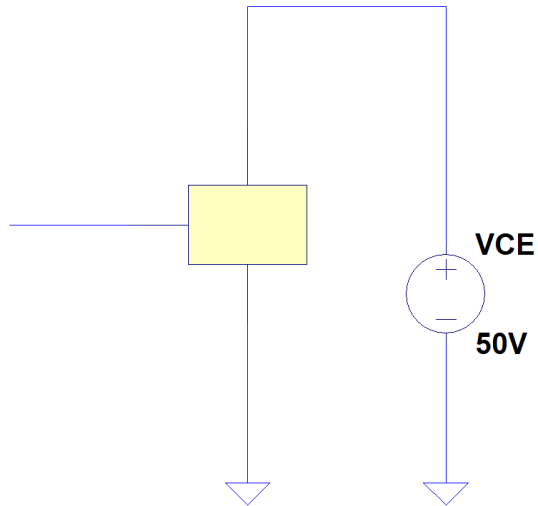
Simulation results are following.
 Explanatory notes — : simulated

VCE(sat)



ICEX Testbench

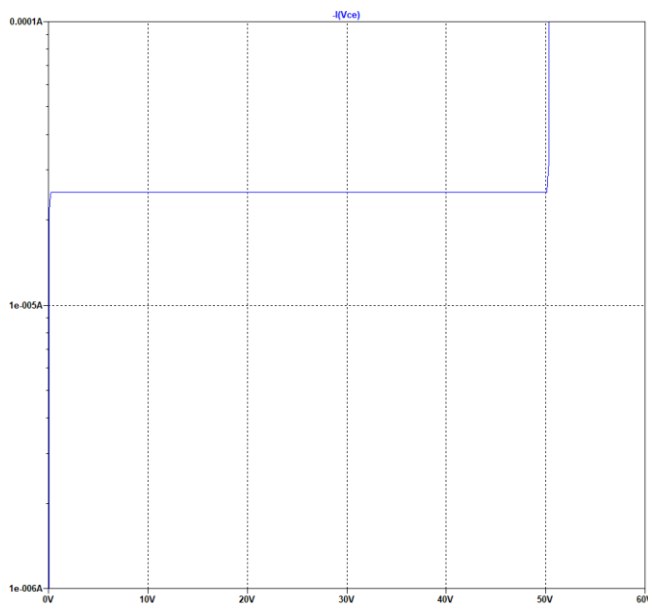
Referred to Data Sheet



```
.dc VCE 0 60 0.1
.lib ULN2003ADR.lib
```

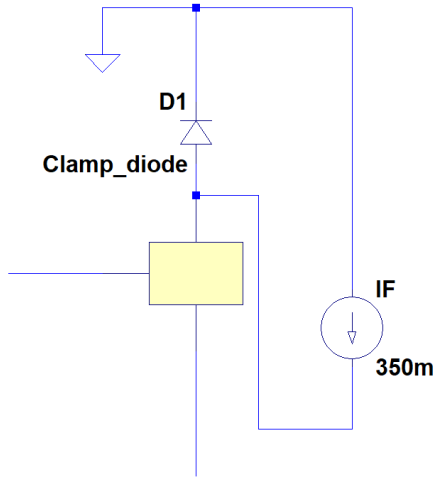
Simulation results are following.
 Explanatory notes — : simulated

ICEX



VF Testbench

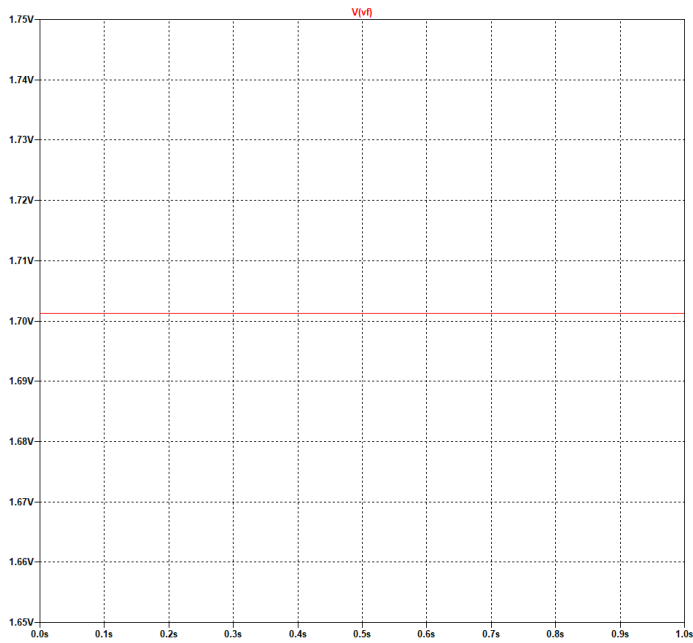
Referred to Data Sheet



```
.tran 1
.lib ULN2003ADR.lib
.lib Clamp_diode.lib
```

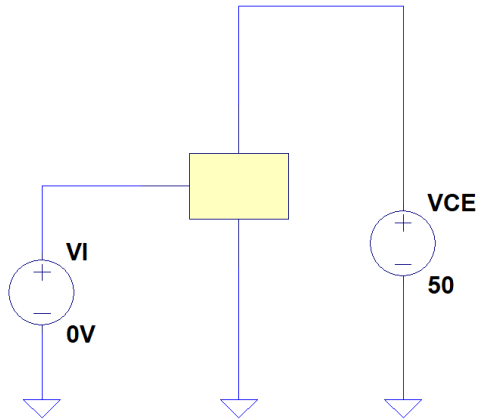
Simulation results are following.
 Explanatory notes — : simulated

VF



II(off) Testbench

Referred to Data Sheet

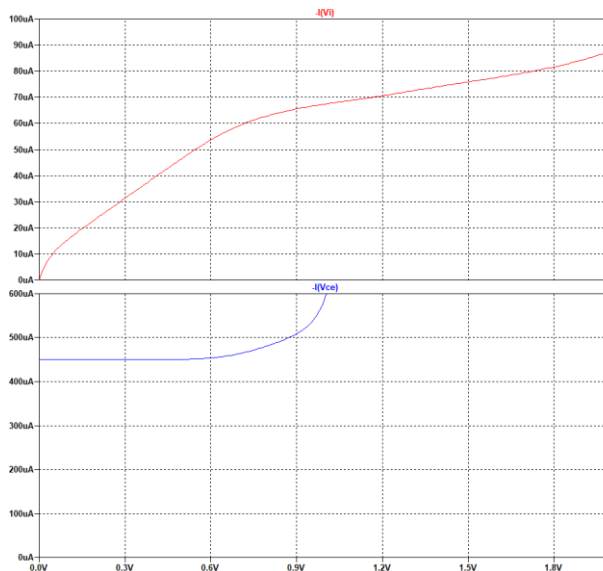


```
.dc VI 0 2 0.01
.lib ULN2003ADR.lib
.temp 70

.meas II(off) FIND -I(Vi) WHEN -(Vce)=500u RISE=1
```

Simulation results are following.
 Explanatory notes — : simulated

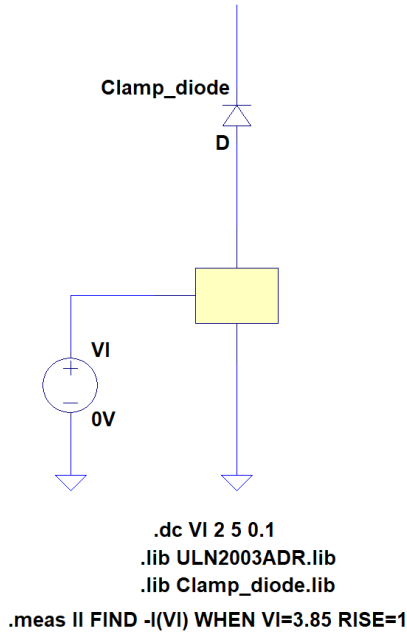
II(off)



```
meas II(off) FIND -I(Vi) WHEN -(Vce)=500u RISE=1
II(off) -I(Vi)=6.49442e-005 at 0.873678
```

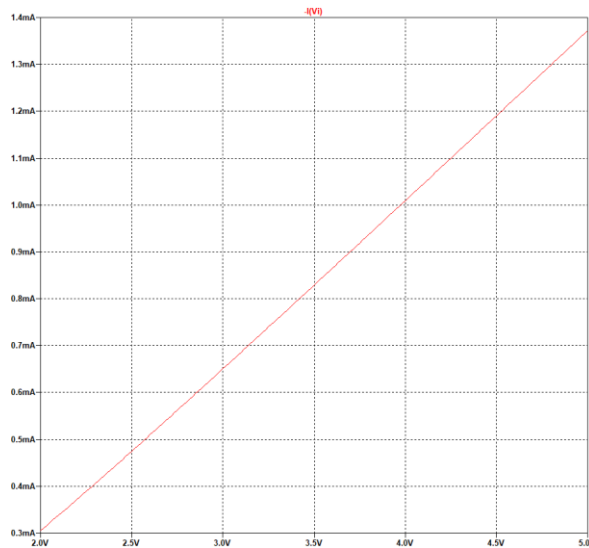
II Testbench

Referred to Data Sheet



Simulation results are following.
 Explanatory notes — : simulated

II

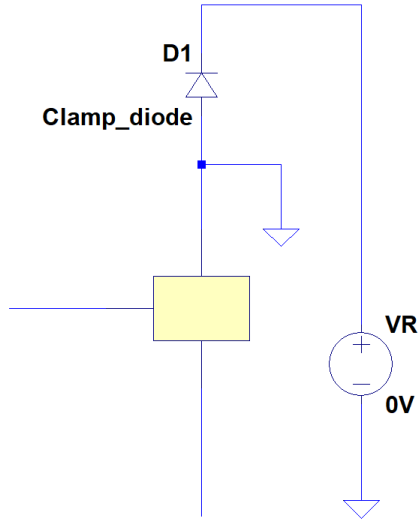


```

.meas II FIND -I(VI) WHEN VI=3.85 RISE=1
II: -I(VI)=0.0009551 22 at 3.85
    
```


IR Testbench

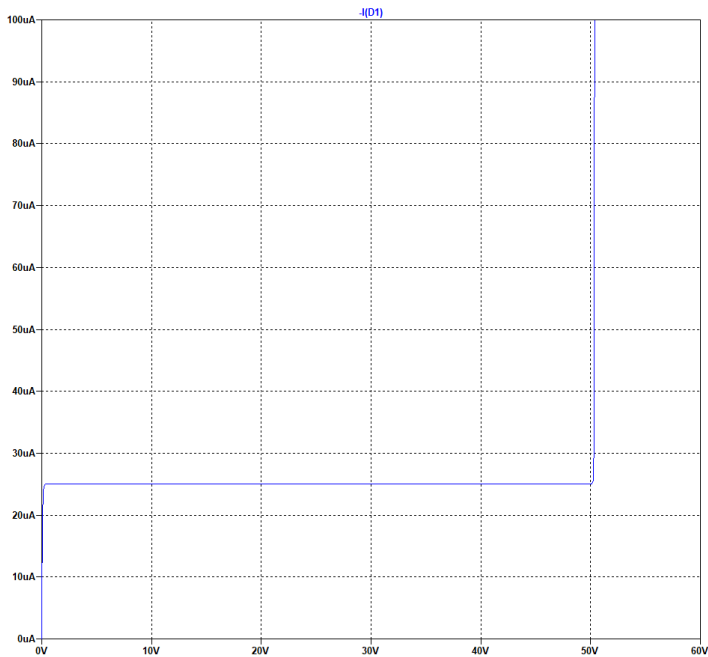
Referred to Data Sheet



```
.dc VR 0 60 0.01
.lib ULN2003ADR.lib
.lib Clamp_diode.lib
```

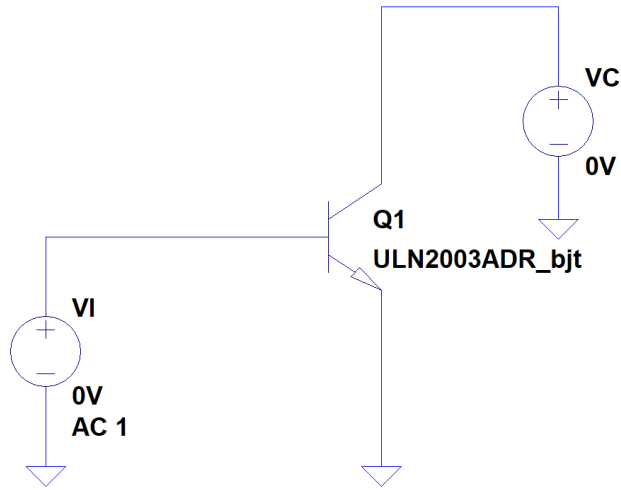
Simulation results are following.
 Explanatory notes — : simulated

IR



Ci Testbench

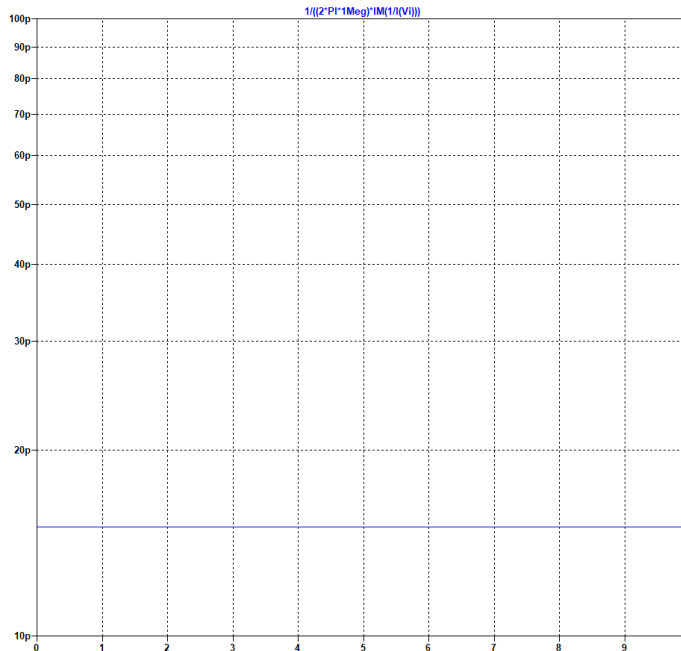
Referred to Data Sheet



```
.ac dec 1 1Meg 1Meg
.step param VI 0 10 0.1
.lib ULN2003ADR_bjt.lib
```

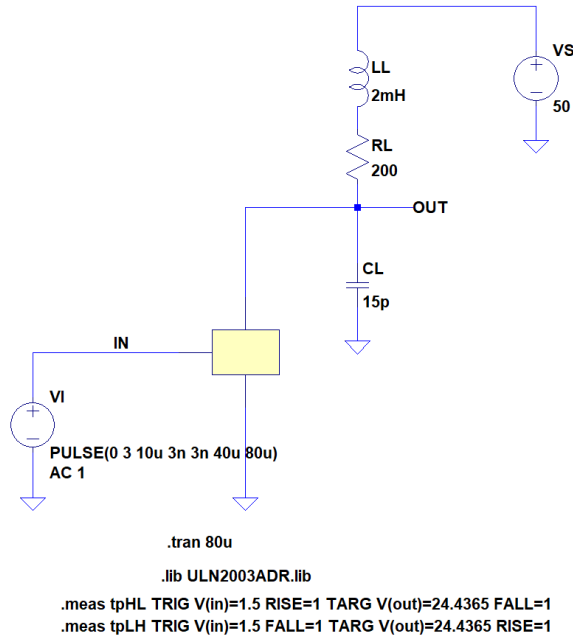
Simulation results are following.
 Explanatory notes — : simulated

Ci



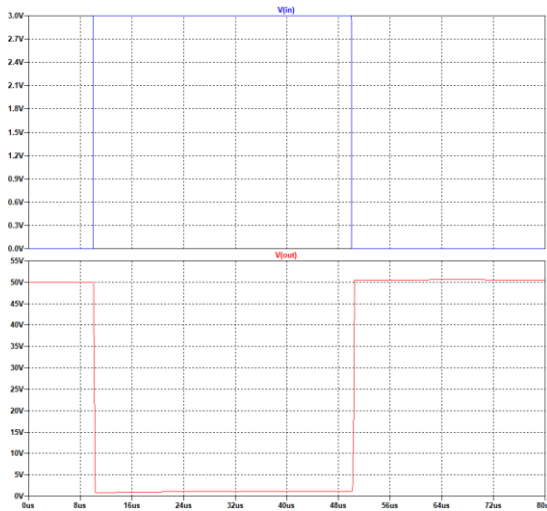
tpLH-HL/VOH Testbench

Referred to Data Sheet



Simulation results are following.
 Explanatory notes — : simulated

tpLH-HL/VOH



VOH

Cursor 1	
V(out)	
Horz: 39.955006us	Vert: 1.1268496V
Cursor 2	
Horz: -- N/A --	Vert: -- N/A --
Diff(Cursor2 - Cursor1)	
Horz: -- N/A --	Vert: -- N/A --
Freq: -- N/A --	Slope: -- N/A --

tpHL

```

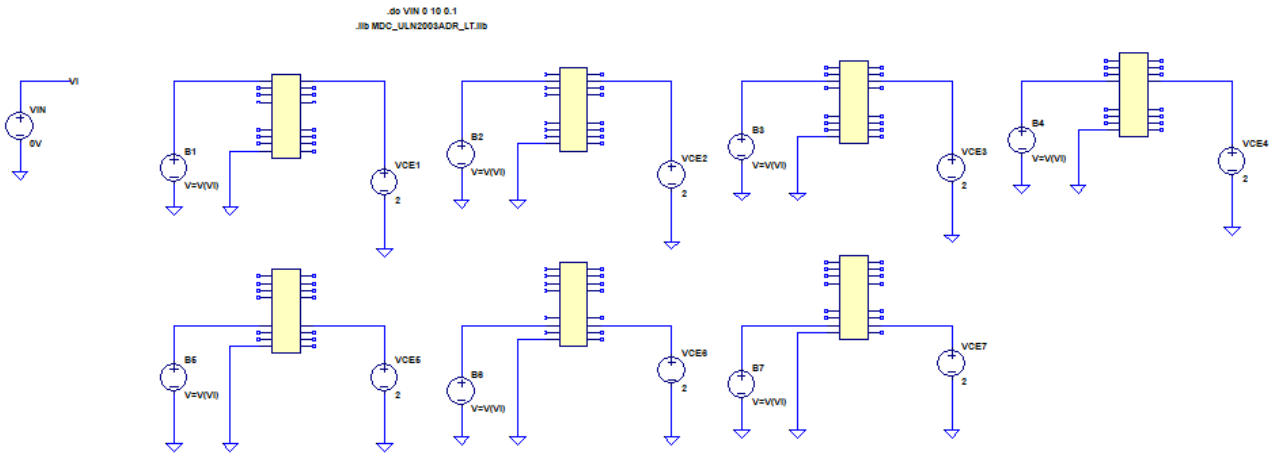
.meas tpHL TRIG V(in)=1.5 RISE=1 TARG V(out)=24.4365 FALL=1
tpHL=2.00921e-007 FROM 1.00015e-005 TO 1.02024e-005
    
```

tpLH

```

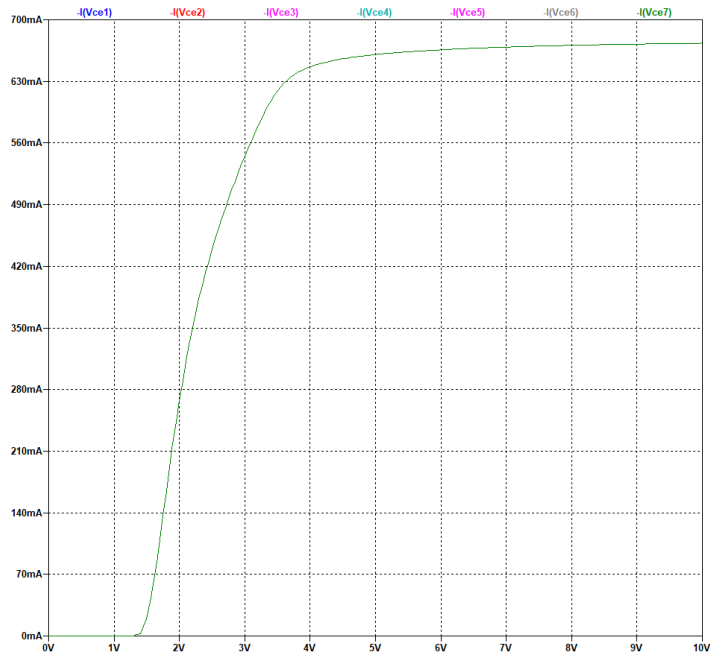
.meas tpLH TRIG V(in)=1.5 FALL=1 TARG V(out)=24.4365 RISE=1
tpLH=3.57238e-007 FROM 5.00045e-005 TO 5.03617e-005
    
```

VI(ON)_ALL Testbench
 Referred to Data Sheet



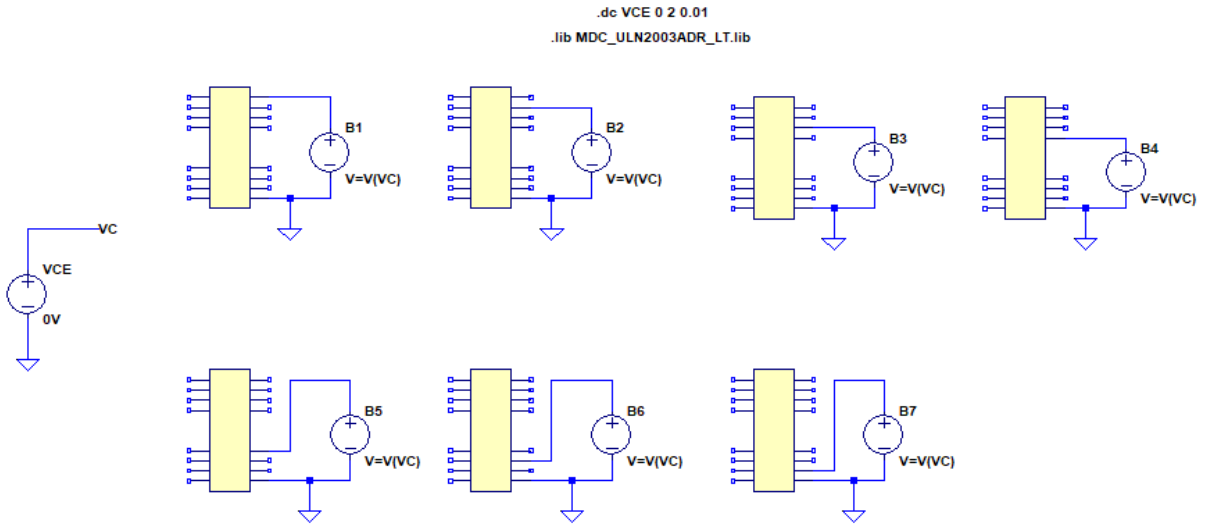
Simulation results are following.
 Explanatory notes — : simulated

VI(ON)_ALL



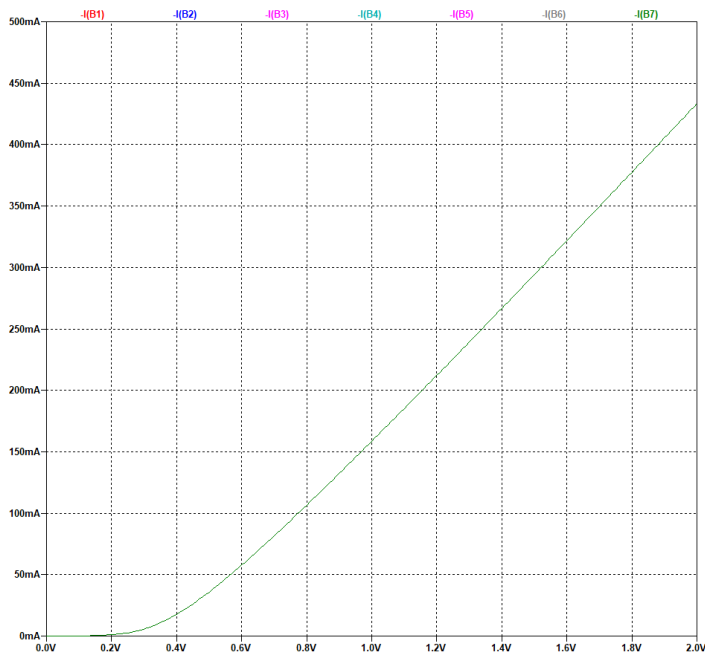
VF_ALL Testbench

Referred to Data Sheet



Simulation results are following.
Explanatory notes — : simulated

VF_ALL



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