

LTspice Model NMOS+NMOS RENESAS UPA3753GR-E1-AX

Model Information

A macro model based on BSIM3 model

Call Name MDC_UPA3753GR-E1-AX_LT Pin Assign 1:S 2G 3S 4:G 5:D 6:D 7:D 8:D

MDC_UPA3753GR-E1-AX_LT01.lib File List Model Library

Model Report MDC_UPA3753GR-E1-AX_LT.pdf (this file)

Verified Simulator Version

Note

LTspice version XVII

References

The information which was used for modeling is as follow:

Company name

[Data Sheet]

Date/Version Rev. 1.00

Product name UPA3753GR-E1-AX

Renesas Electronics Corporation Characteristics IdVds[Vgs],IdVgs[Temp],VthTemp[Id],Rds(on)Id[Vgs],Rds(on

)Vgs[Id],Rds(on)Temp[Vgs],Crss,Coss,Ciss,VdsQg[Vdd],Vgs

Qg[Vdd],IsVsd[Vgs],tdon,tdoff,tf,tr

Simulation Range

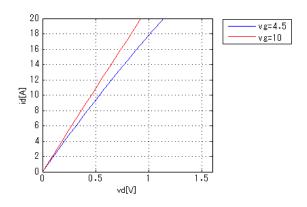
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

Item	Range			Unit
	Min.		Max.	
Drain-source voltage (DC)	0	to	60	V
Gate-source voltage (DC)	0	to	20	V
Temperature	-55	to	150	deg C



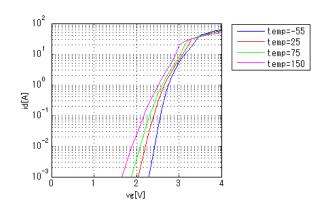
IdVds[Vgs]

Temp. = 25deg C



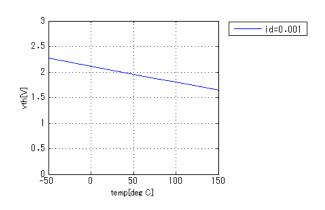
IdVgs[Temp]

Vds = 10V

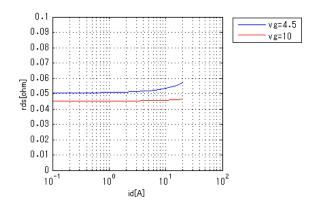


VthTemp[Id]

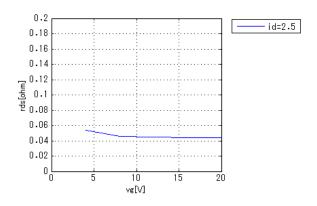
Vds = 10V



Rds(on)Id[Vgs]

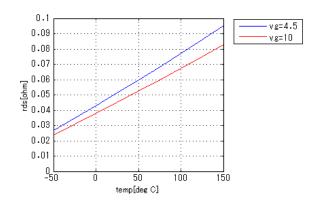


Rds(on)Vgs[Id]



Rds(on)Temp[Vgs]

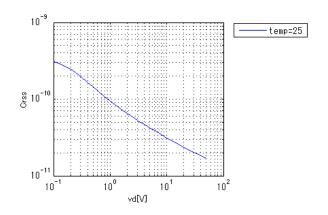
Id = 2.5A





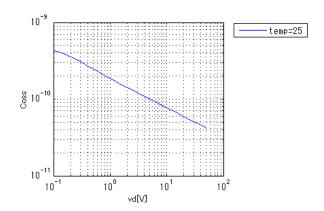
Crss

Freq. = 1MHz



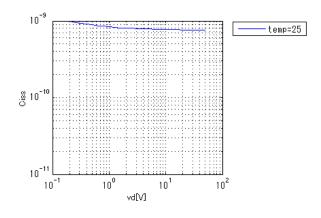
Coss

Freq. = 1MHz



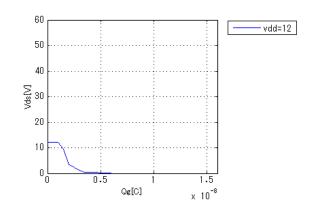
Ciss

Freq. = 1MHz



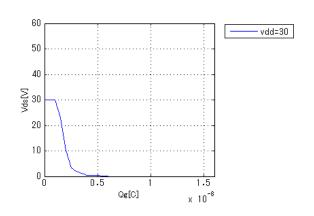
VdsQg[Vdd]

Id = 5A



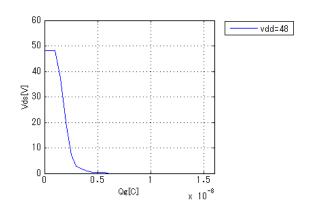
VdsQg[Vdd]

Id = 5A



VdsQg[Vdd]

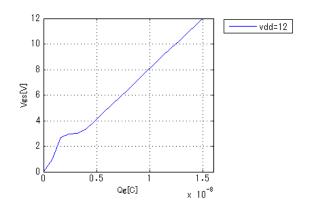
Id = 5A





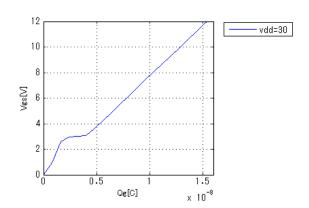
VgsQg[Vdd]

Id = 5A



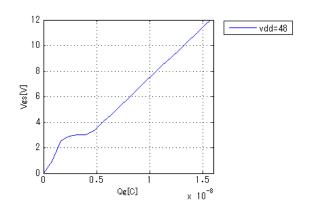
VgsQg[Vdd]

Id = 5A

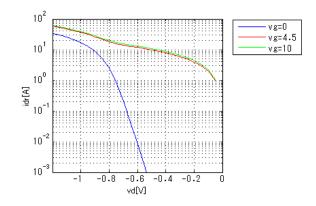


VgsQg[Vdd]

Id = 5A

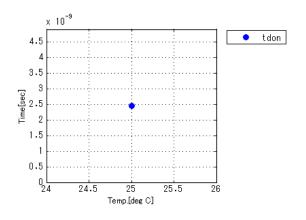


IsVsd[Vgs]



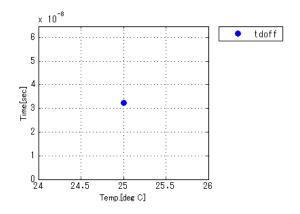
tdon

Vdd = 30V, Id = 2.5A, +Vg = 10V, -Vg = 0V, Rg = 100hm



tdoff

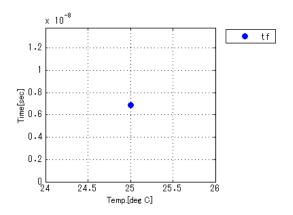
Vdd = 30V, Id = 2.5A, +Vg = 10V, -Vg = 0V, Rg = 100hm





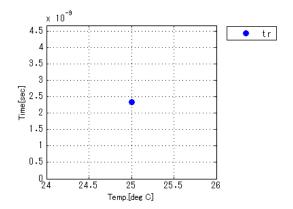
tf

Vdd = 30V, Id = 2.5A, +Vg = 10V, -Vg = 0V, Rg = 10ohm



tr

Vdd = 30V, Id = 2.5A, +Vg = 10V, -Vg = 0V, Rg = 10ohm





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