

LTspice Model

Logic IC

Toshiba Corporation

74VHC244FT

Model Information

Model A macro model
Call Name MDC_74VHC244FT_LT
Pin Assign 1:1_G 2:1A1 3:2Y4 4:1A2 5:2Y3 6:1A3 7:2A2 8:1A4 9:2Y1 10:GND 11:2A1 12:1Y4
 13:2A2 14:1Y3 15:2A3 16:1Y2 17:2A4 18:1Y1 19:2_G 20:Vcc
File List Model Library MDC_74VHC244FT_LT01.lib
 Model Report MDC_74VHC244FT_LT.pdf(this file)

Verified Simulator Version LTspice 17.1.15

Note

References

The information which was used for modeling is as follow:

- [Data Sheet]
- Date/Version
 - Product name 74VHC244FT
 - Company name Toshiba Corporation

- [Characteristics listed]
- Characteristics Vih, Vil, Voh, Vol, Ioz, Iin, Icc
 tpLH, tpHL, tpLZ, tpZL, tpHZ, tpZH
 Cin, Cout

Simulation Condition

This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

| Item | Condition | | | Unit |
|----------------------|-----------|-----|-----|-------|
| | Min | Typ | Max | |
| Power Supply Voltage | 2.0 | | 5.5 | V |
| Temperature | | 25 | | deg C |

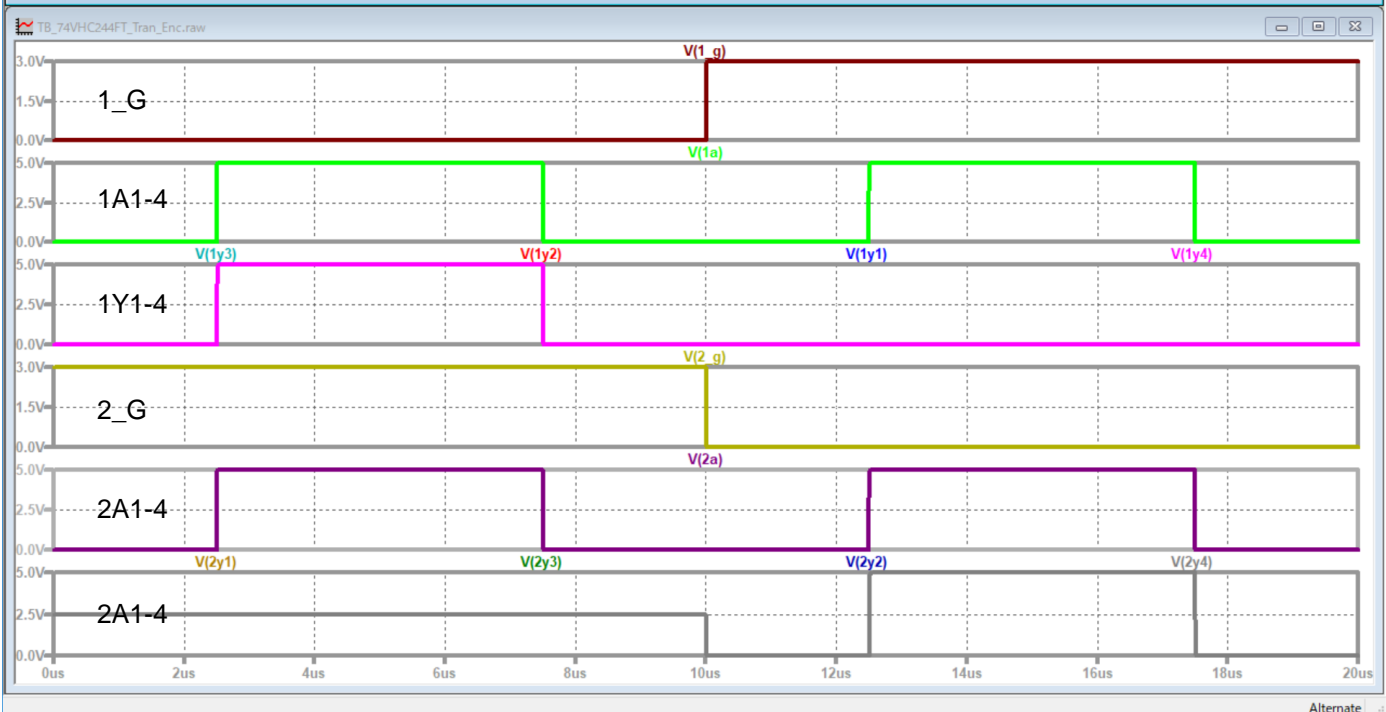
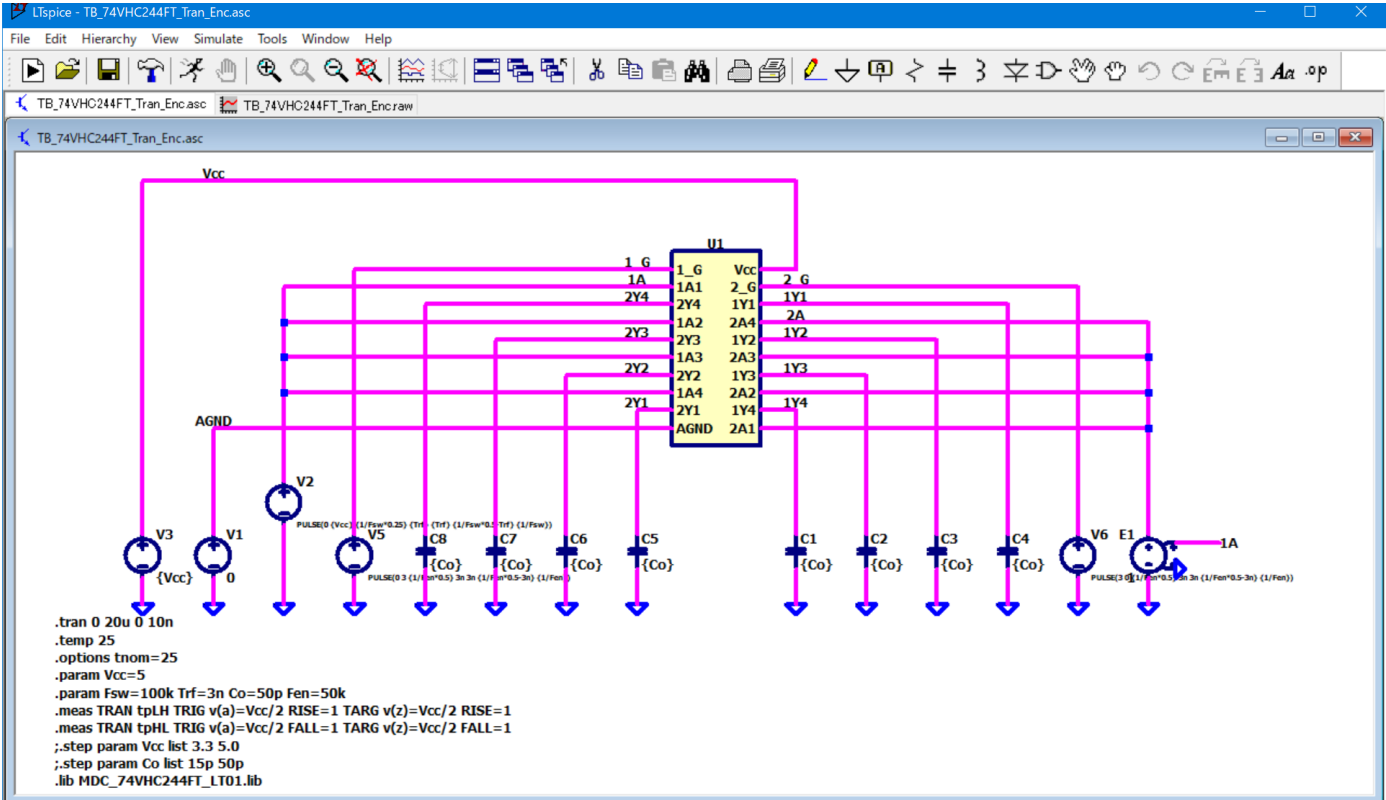
Logic Gate

○ : Implemented
 × : Not Implemented
 — : Not applicable

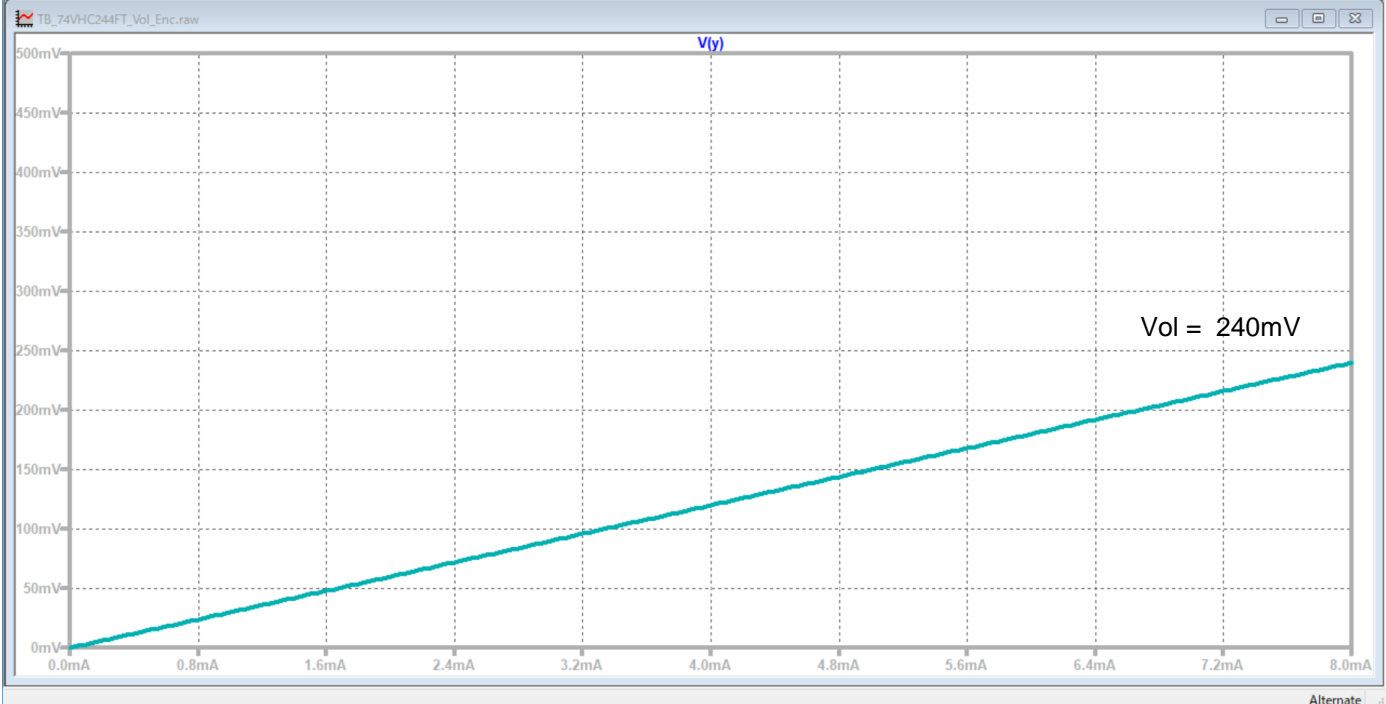
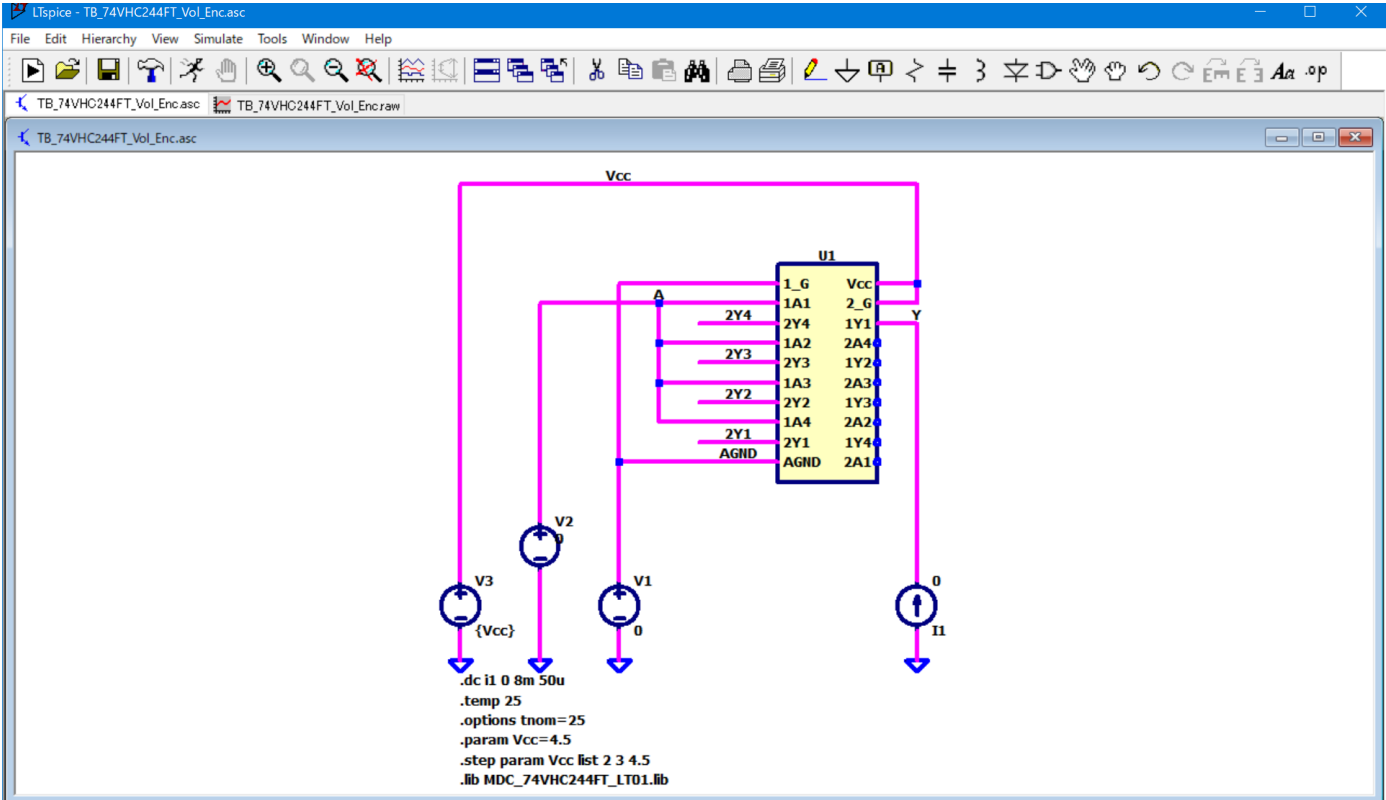
Model Functions Table
RANK=2

| Functions | RANK | Implemented |
|------------------------|------|-------------|
| Truth Table | 1 | ○ |
| Propagation Delay | 1 | ○ |
| CMOS/Open Drain Output | 1 | ○ |
| Schmitt trigger | 1 | ○ |
| Timing Chart | 1 | ○ |
| Input Protection | 2 | ○ |
| Output Protection | 2 | ○ |
| Power Supply Current | 2 | ○ |

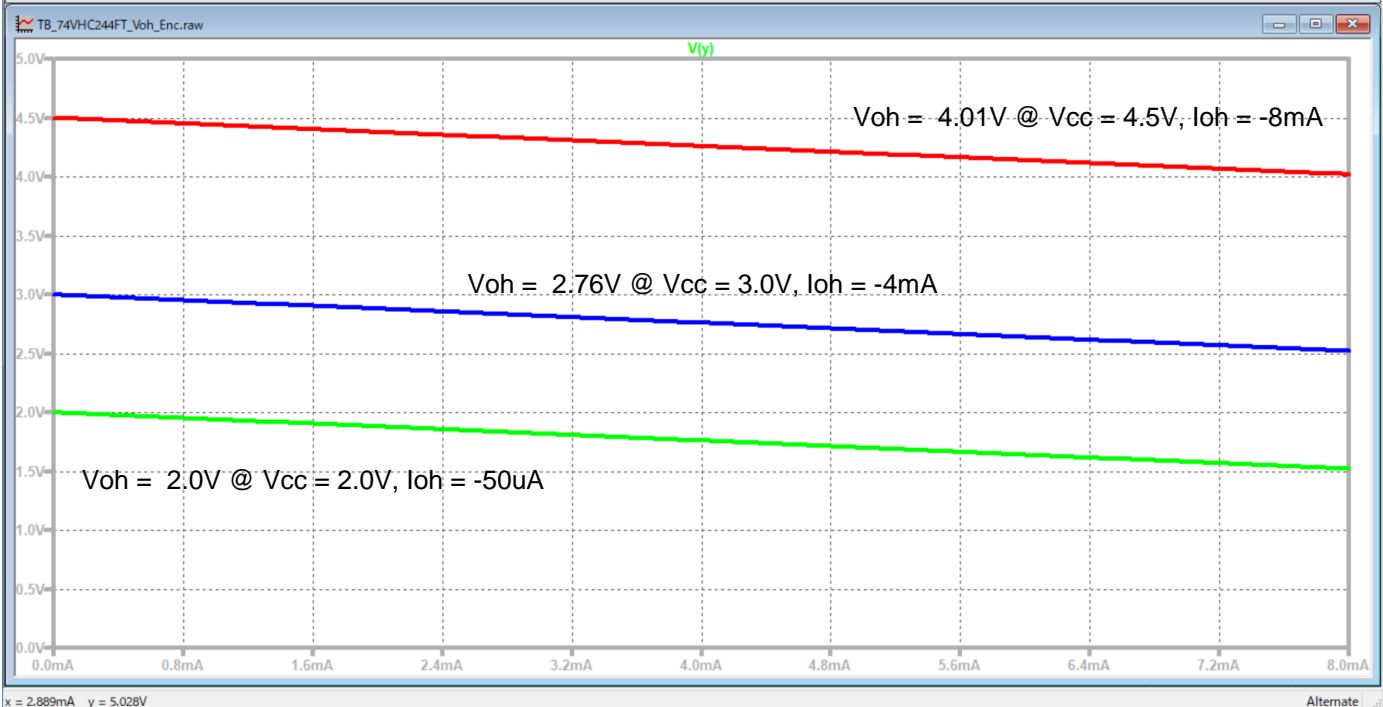
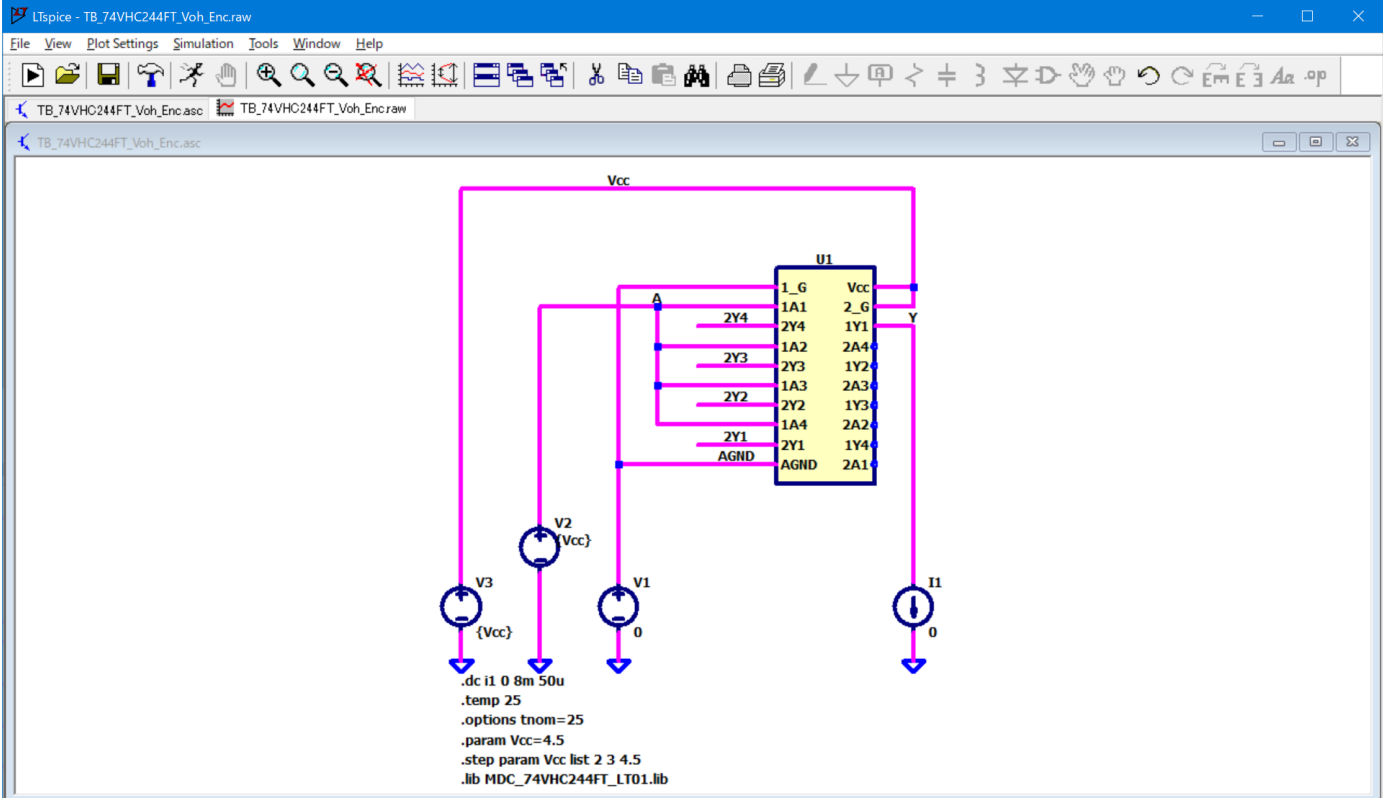
Testbench for truth table function



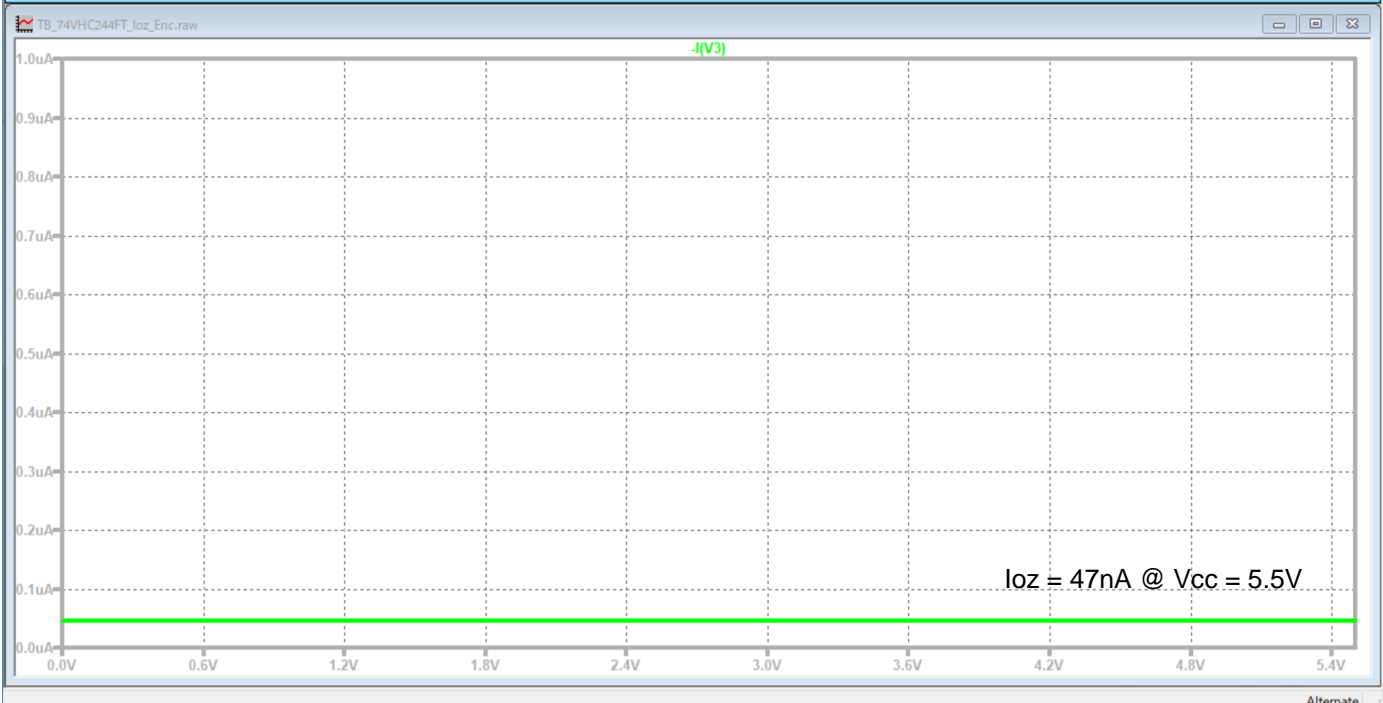
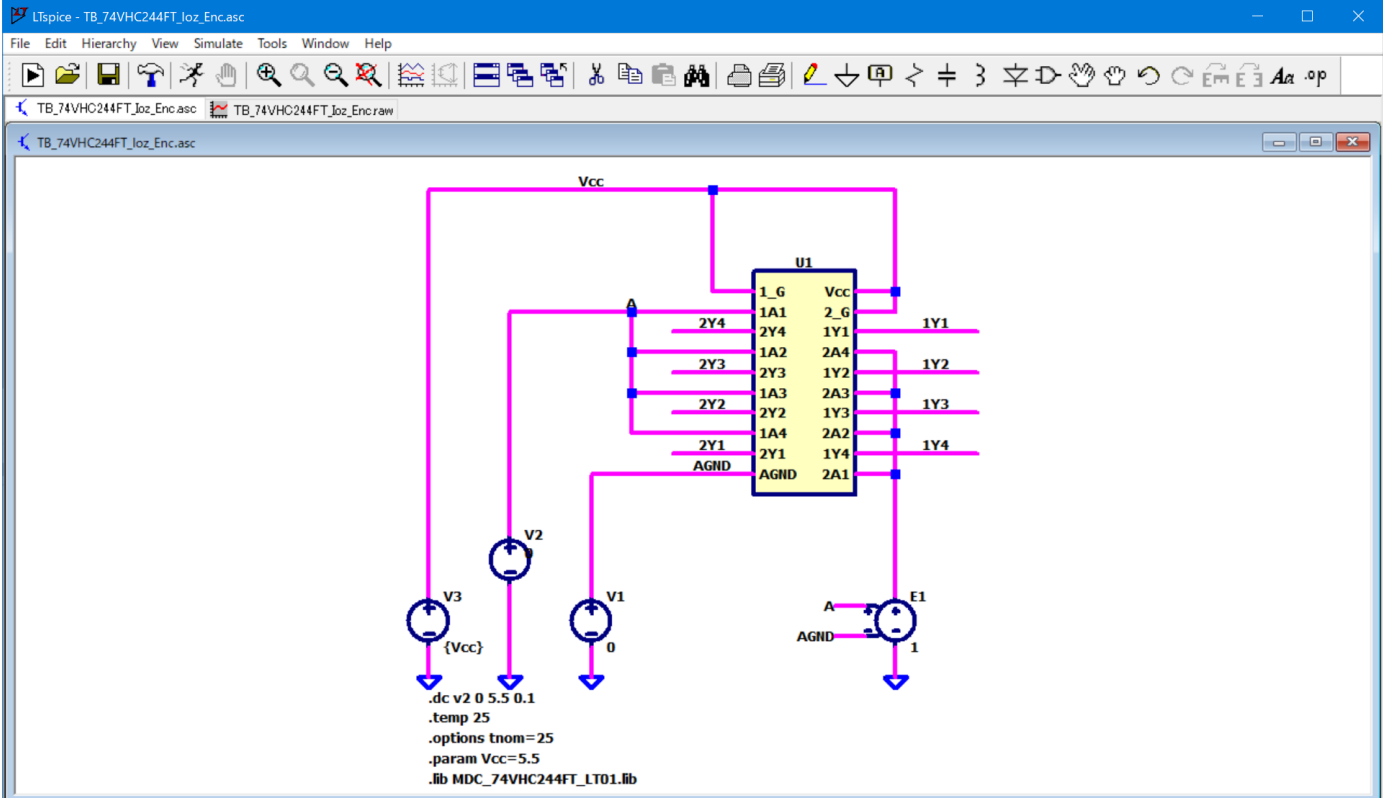
Testbench for Vol



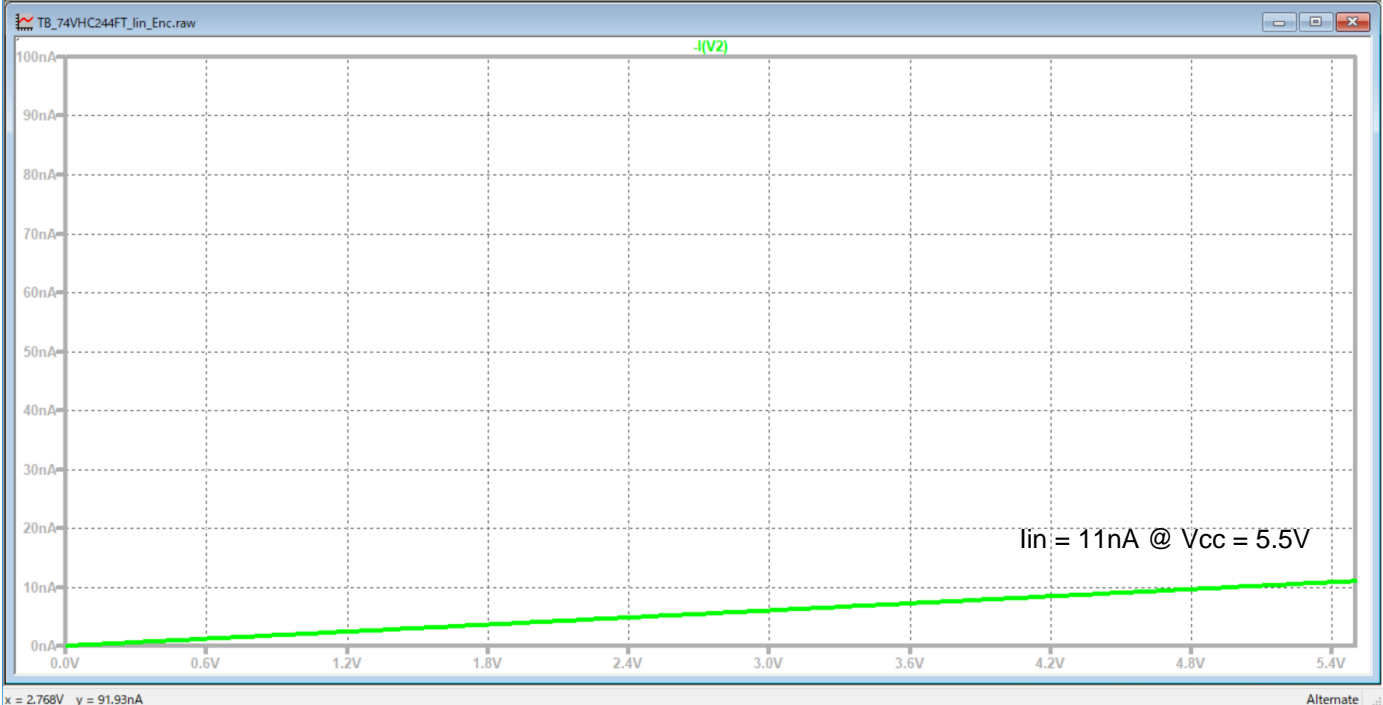
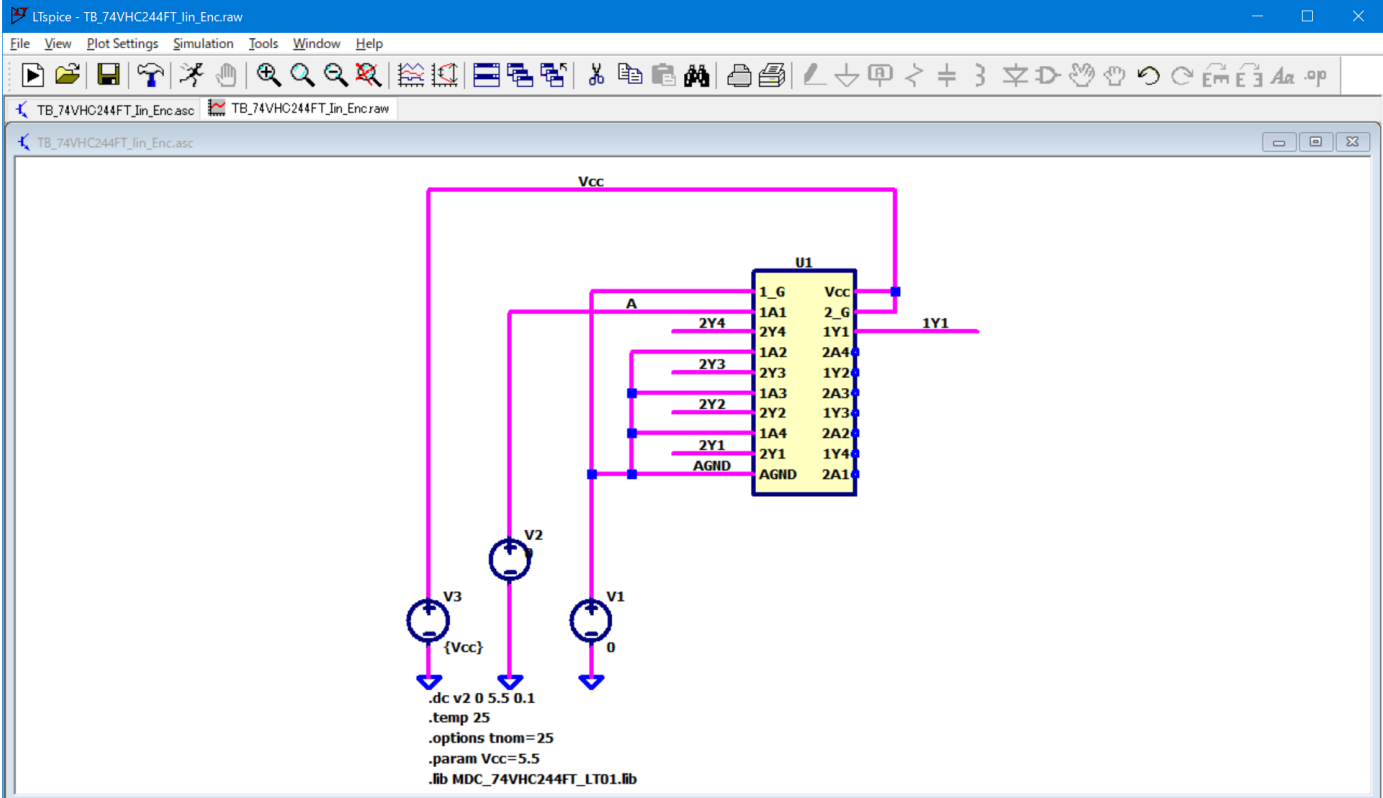
Testbench for Voh



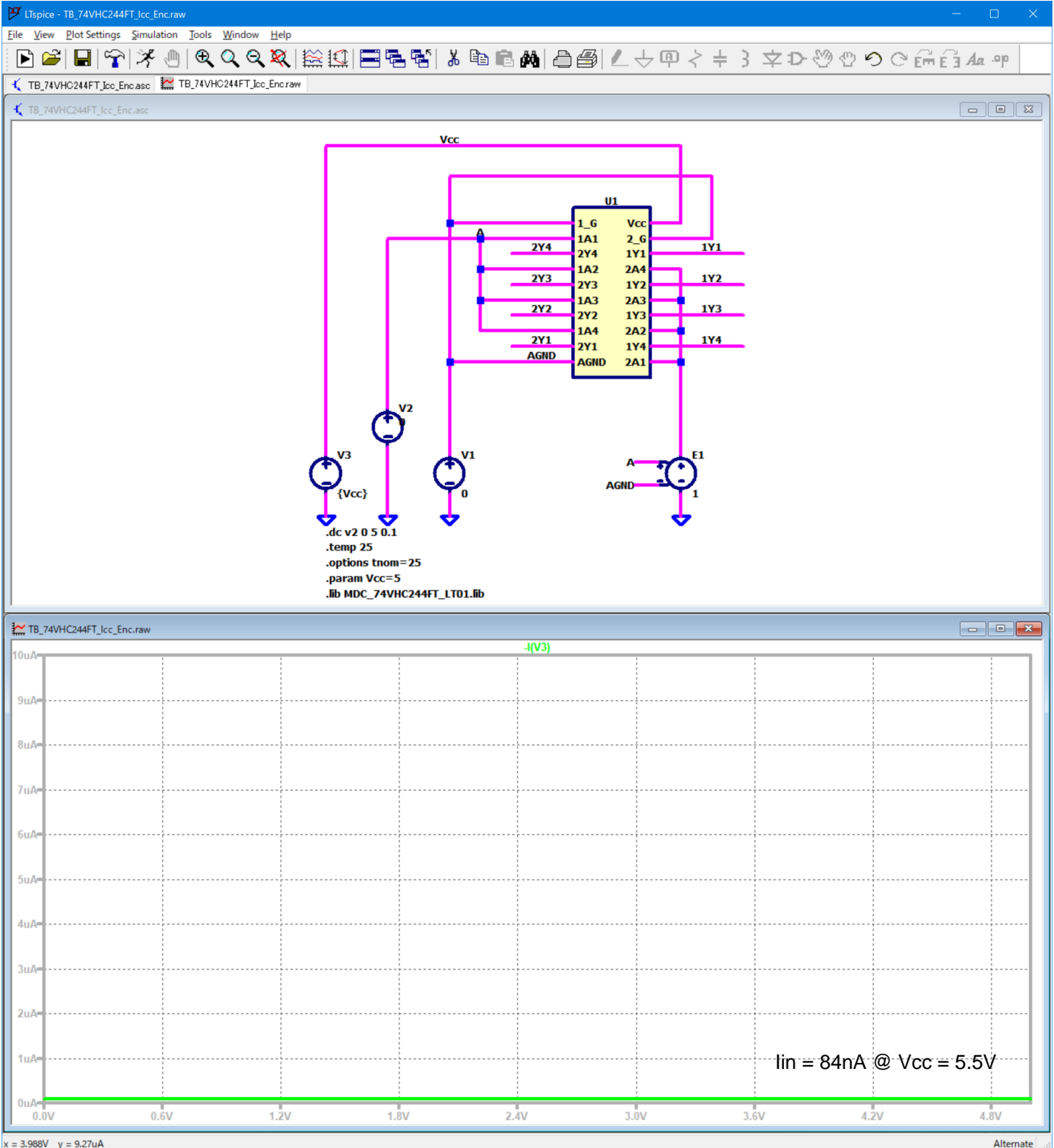
Testbench for loz



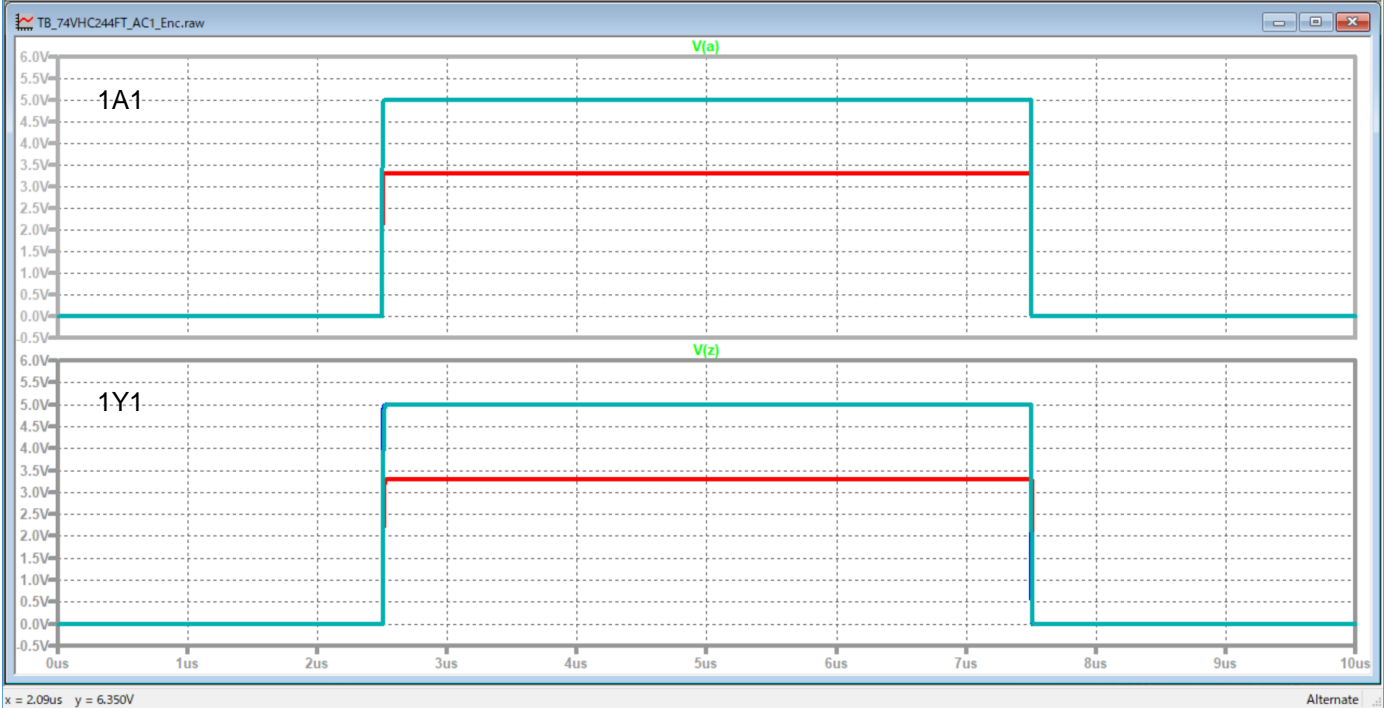
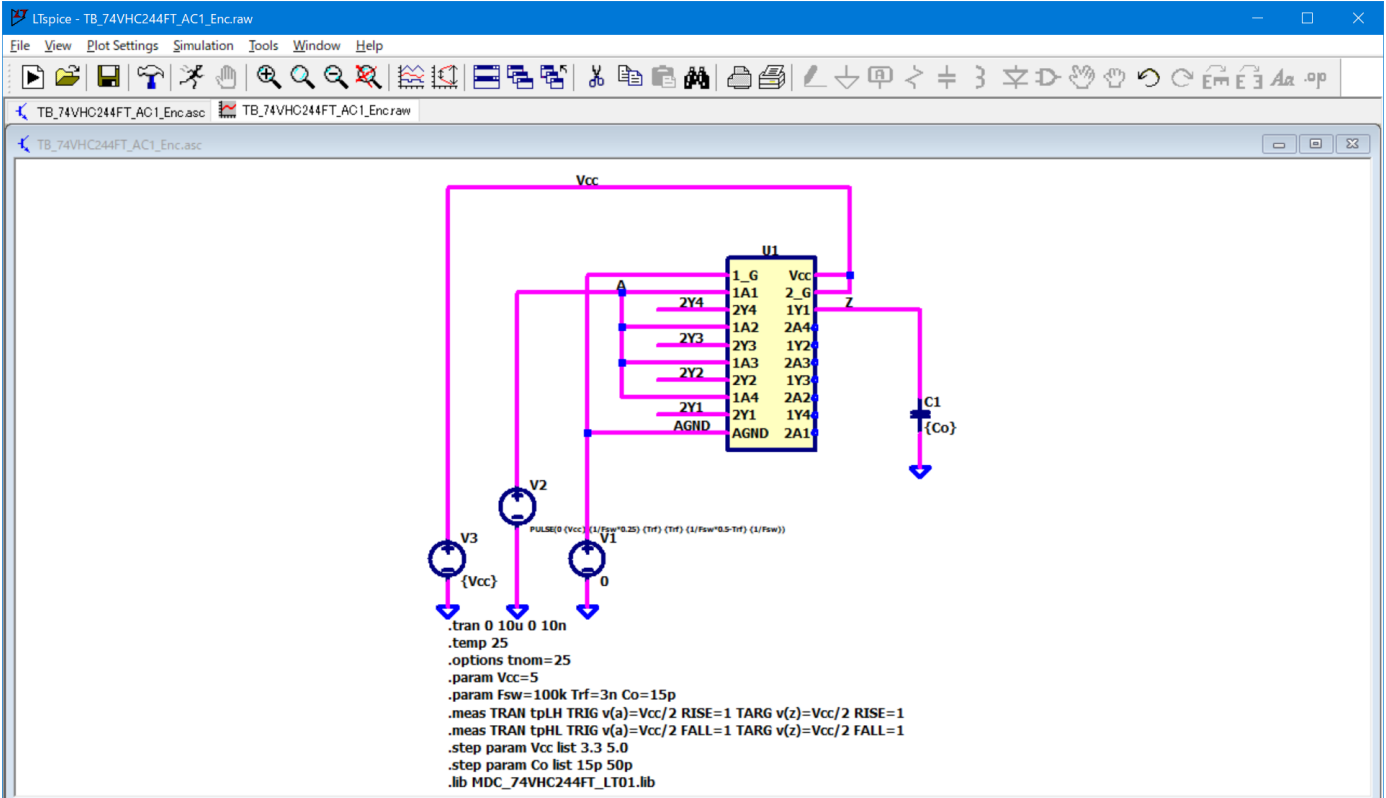
Testbench for lin



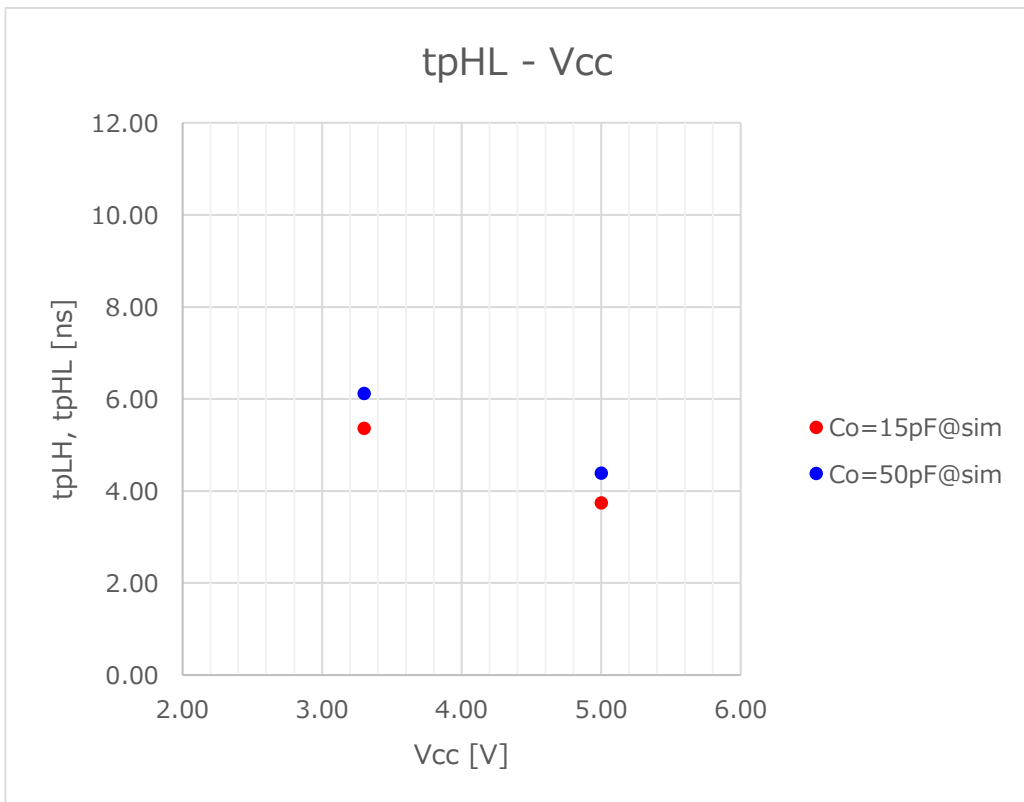
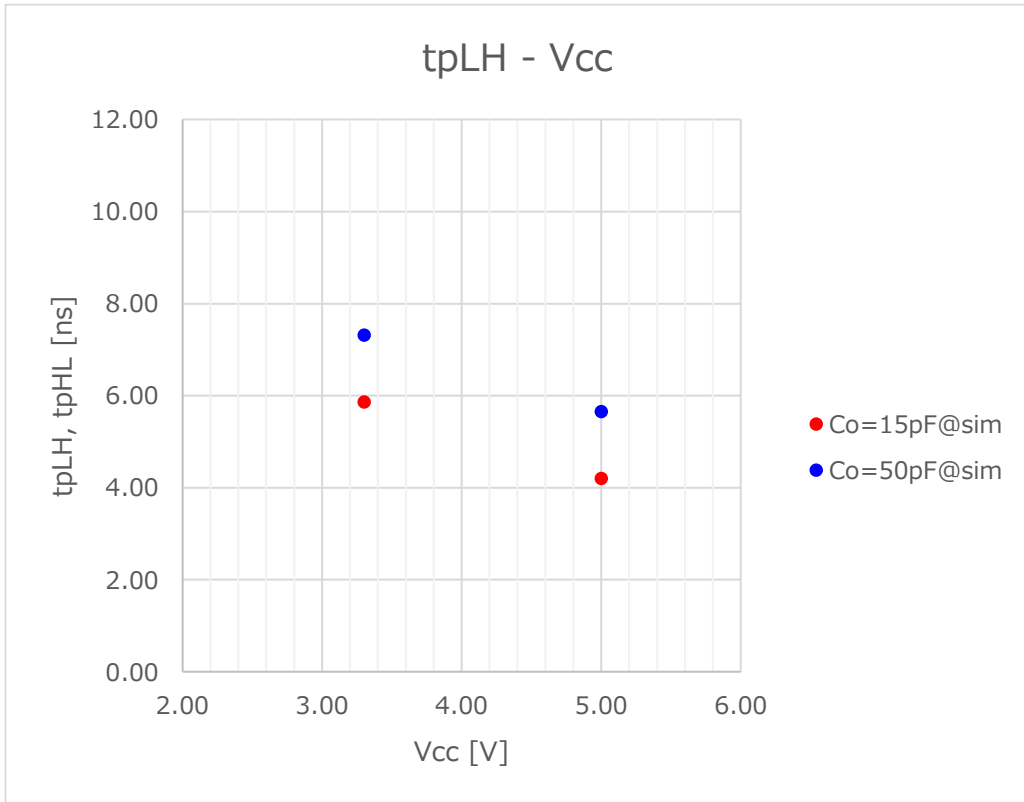
Testbench for Icc



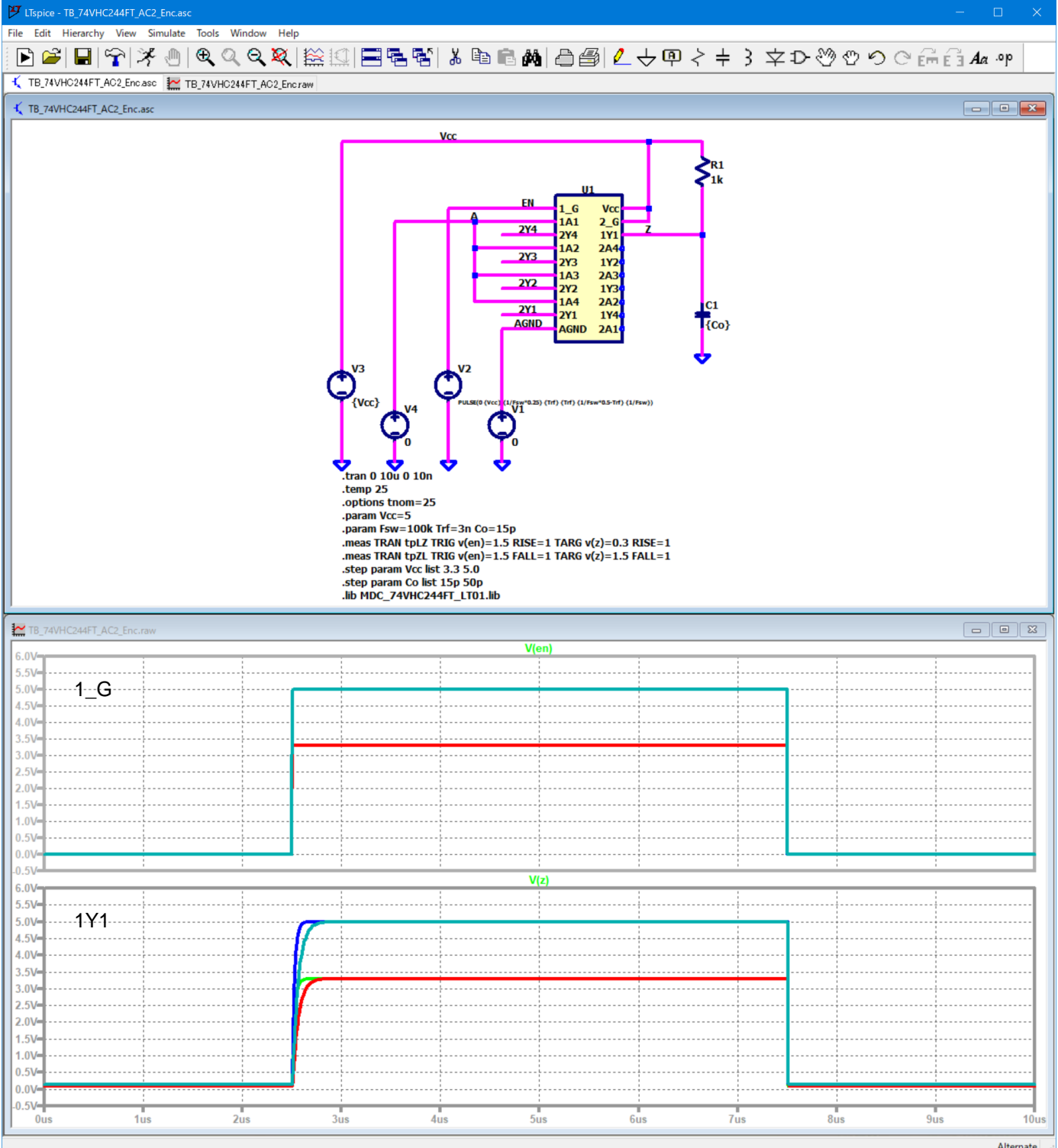
Testbench for tpLH, tpHL



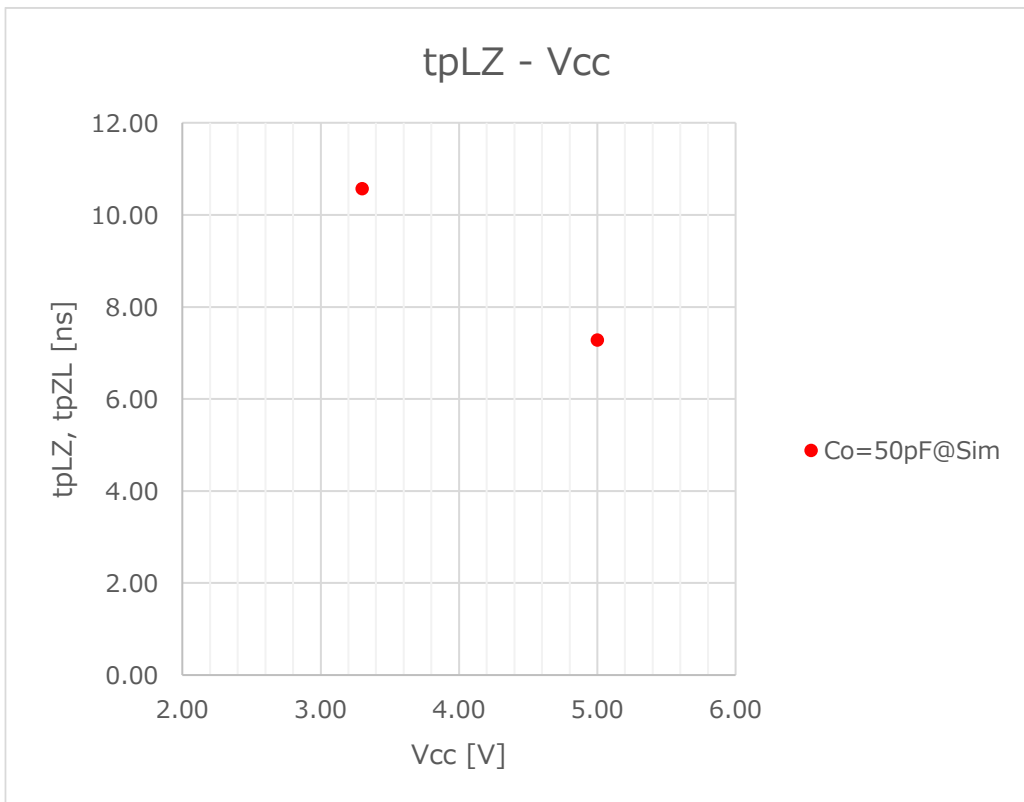
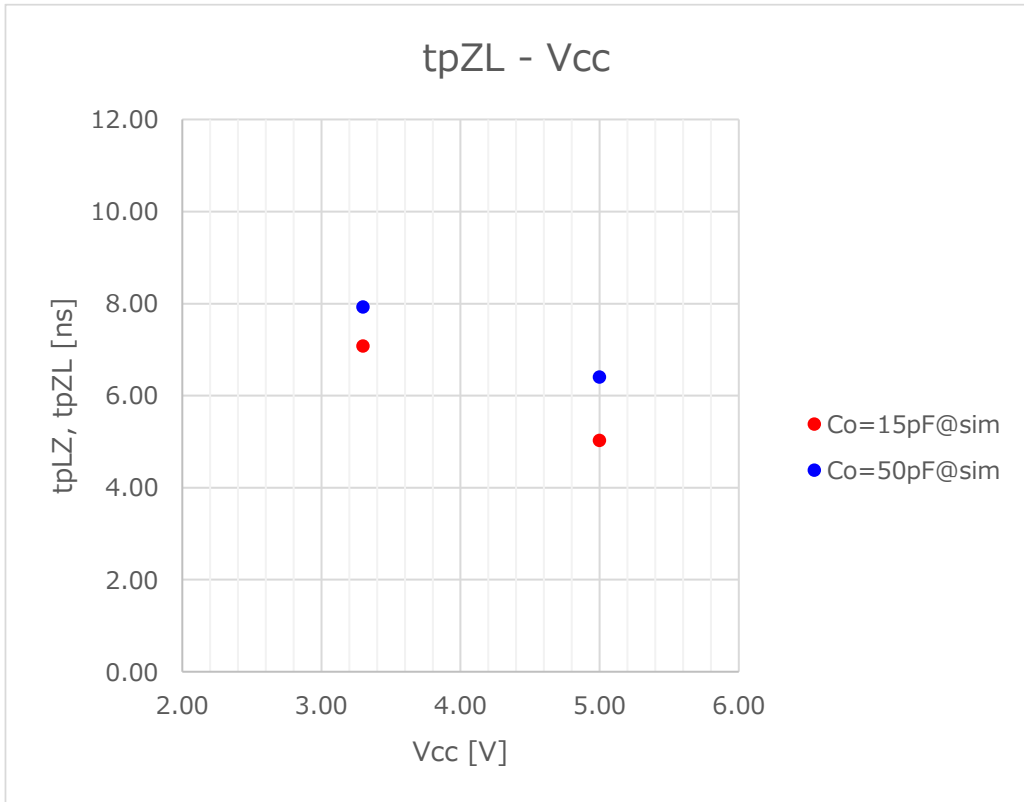
Testbench for tpLH, tpHL



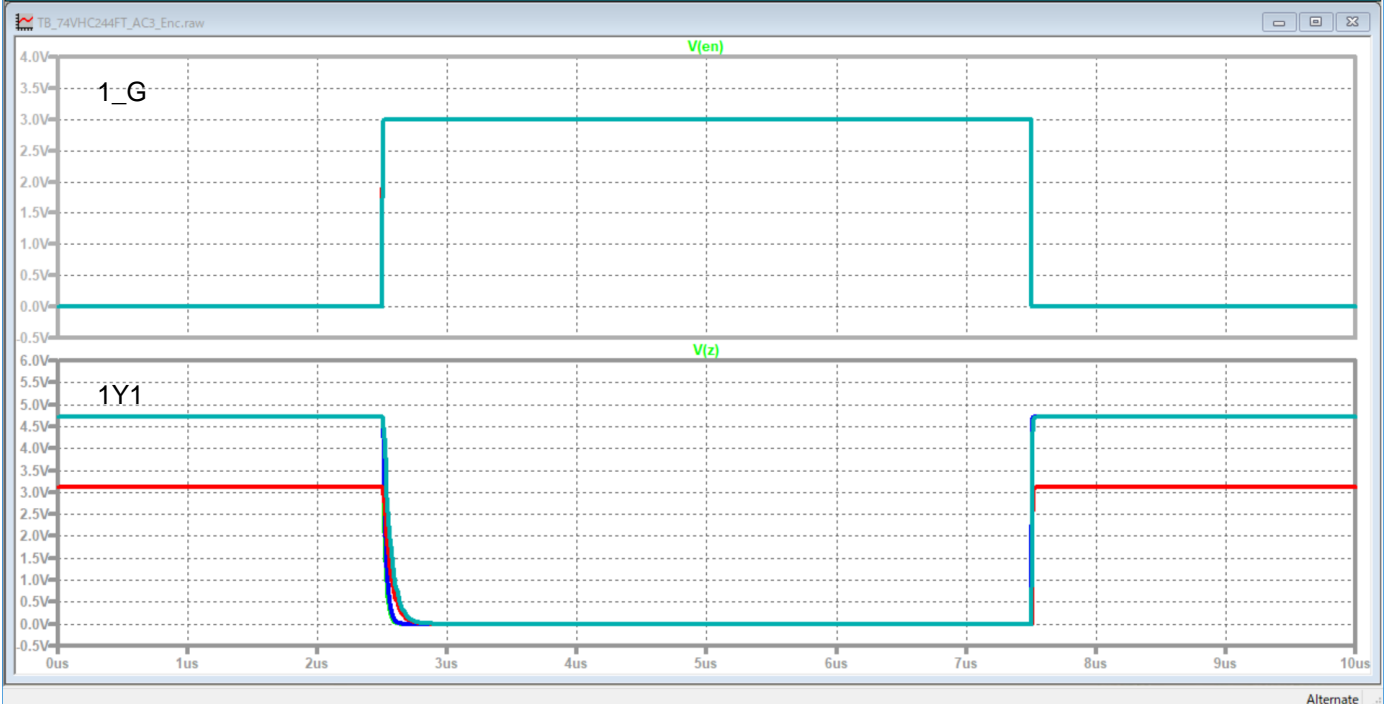
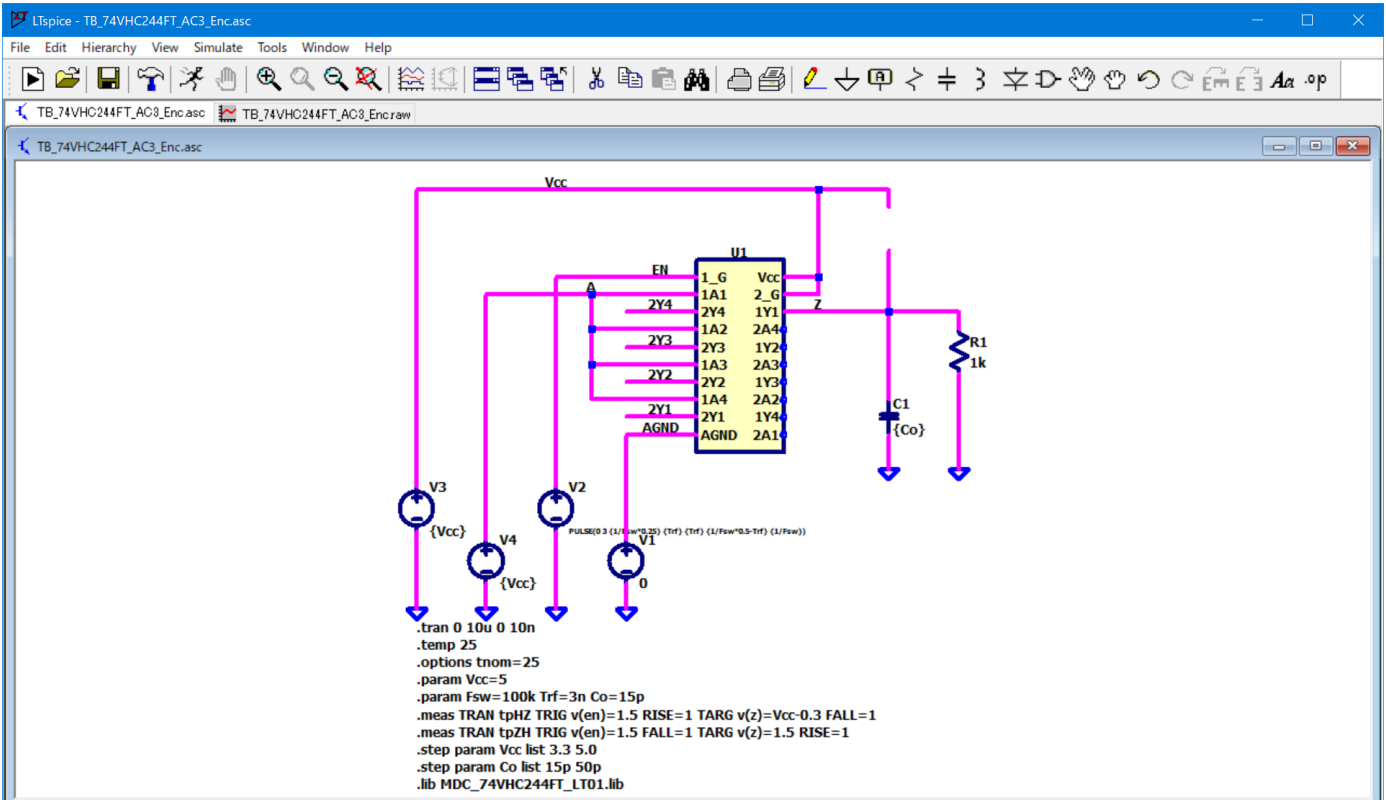
Testbench for tpZL, tpLZ



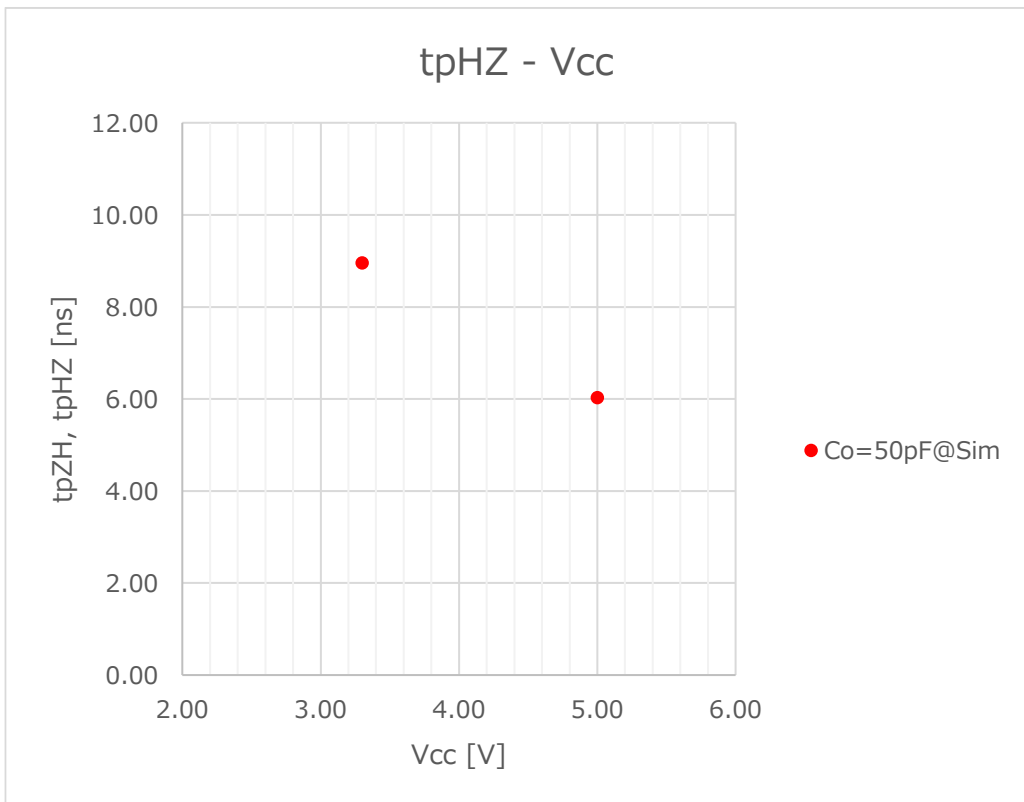
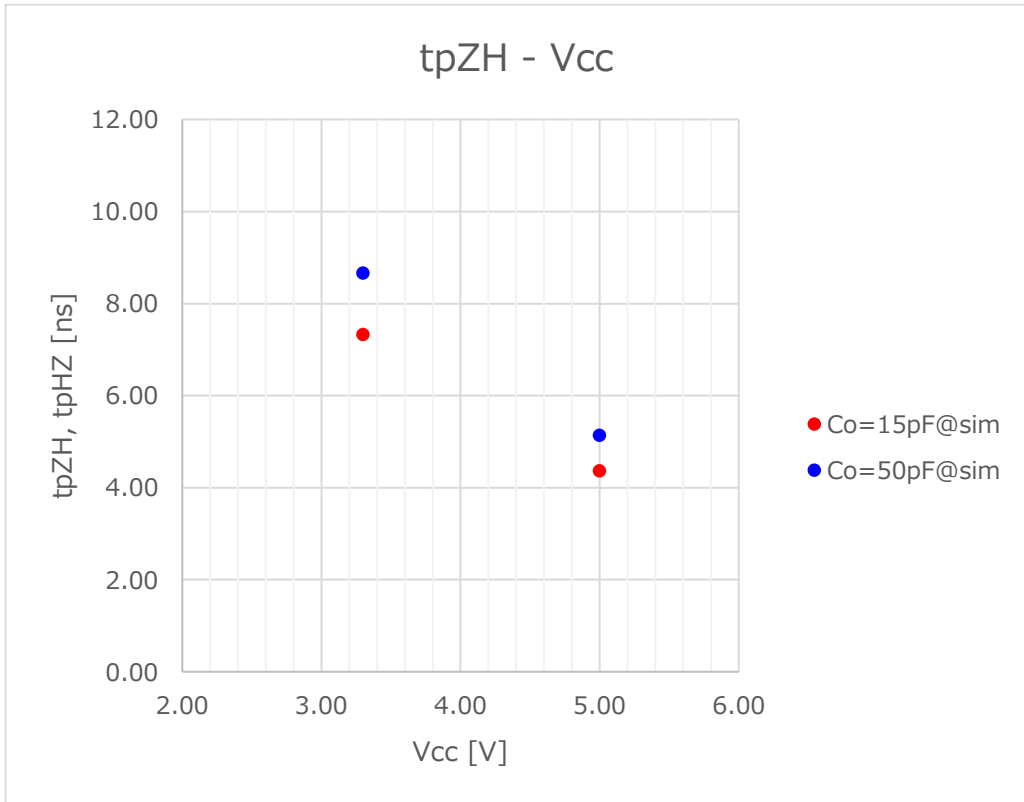
Testbench for tpLZ, tpZL



Testbench for tpZH, tpHZ



Testbench for tpHZ, tpZH



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