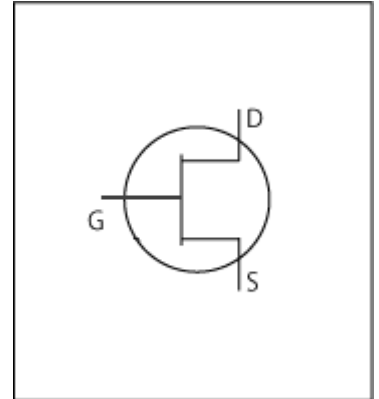


# LTspice Model

## N-Channel JFET

### Isahaya

### 2SK492-T12



### Model Information

**Model** Jfet model  
**Call Name** MDC\_2SK492-T12\_LT  
**Pin Assign** 1:S 2:D 3:G  
**File List** Model Library MDC\_2SK492-T12\_LT01.lib  
 Model Report MDC\_2SK492-T12\_LT.pdf (this file)

**Verified Simulator Version** LTspice version XVII  
**Note**

### References

The information which was used for modeling is as follow:

[Data Sheet]

- Date/Version 20180823 - Rev.002
- Product name 2SK492-T12
- Company name Isahaya Electronics Corporation
- Characteristics IdVds[Vgs], IdVds[Vgs]2, IdVds[Vgs]3, IdVgs[Temp]

### Simulation Range

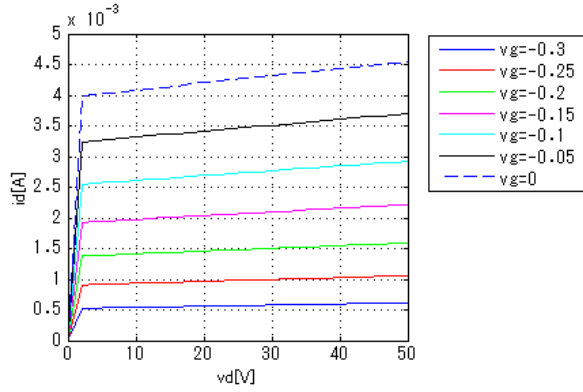
This table shows the range of evaluated simulation range that was not occurs any convergence problems in this area.

| Item                    | Range |    |      | Unit  |
|-------------------------|-------|----|------|-------|
|                         | Min.  |    | Max. |       |
| Gate-drain voltage (DC) | 0     | to | -50  | V     |
| Gate current (DC)       | 0     | to | 10m  | A     |
| Temperature             | -55   | to | 150  | deg C |

Simulation results are following.  
 Explanatory notes — : simulated

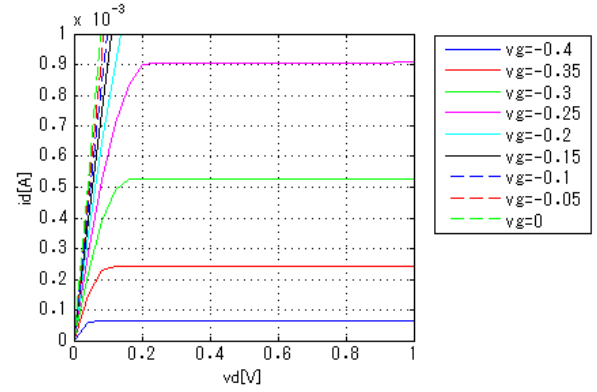
**IdVds[Vgs]**

Temp. = 25deg C



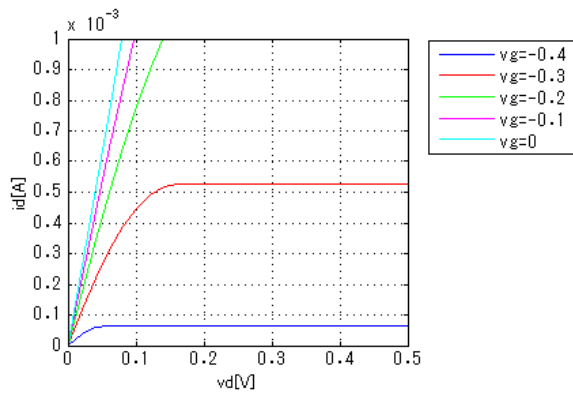
**IdVds[Vgs]2**

Temp. = 25deg C



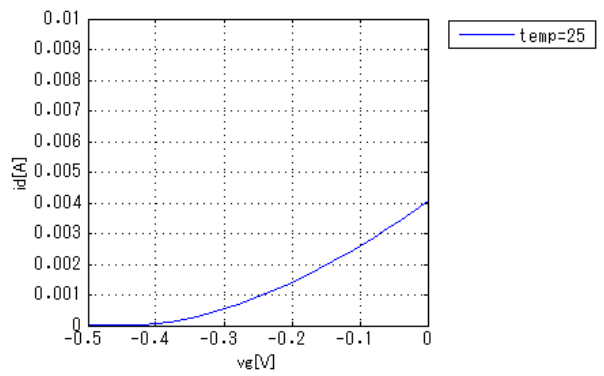
**IdVds[Vgs]3**

Temp. = 25deg C



**IdVgs[Temp]**

Vds = 10V



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