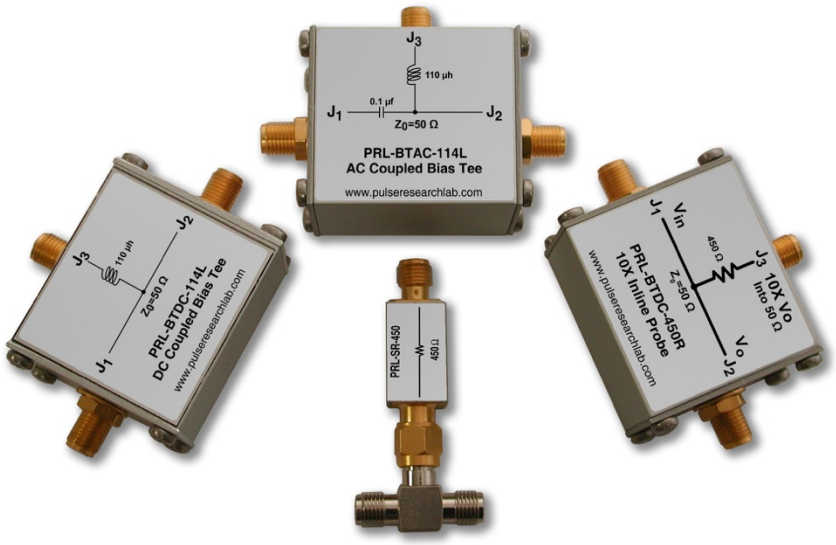
PRL-BTAC and PRL-BTDC, AC/DC COUPLED BIAS TEES

APPLICATIONS

- DC Bias for diode detectors, Laser diodes, FETs, Amplifiers, etc.
- Adding DC offset to Ground-Referenced Signals
- Adding LF signal for jitter simulation
- 10X Inline Signal Pick off (PRL-BTDC-450R)
- An Essential Lab Tool for Working with Microwave and Broadband Digital Circuits

FEATURES

- t_r = 58 ps typical
- Equivalent 3 dB BW > 6 GHz
- Z_0=50 Ω
- Optimized for CW or Pulse Response
- AC or DC Coupling
- SMA I/O Connectors
- 1.0 x 1.3 x 1.5-in. Module



DESCRIPTION

The PRL-BTAC and PRL-BTDC are, respectively, AC-coupled and DC-coupled 50 Ω Bias Tees. These devices enable insertion of a DC or low frequency signal into a broadband 50 Ω coaxial transmission line system, while preserving the integrity of the high frequency characteristics of the 50 Ω I/O ports. Typical applications of Bias Tees include supplying DC bias to semiconductor devices, such as diode detectors, laser diodes, FETs and amplifiers, etc., housed in coaxial structures. In addition, the DC-coupled versions can provide DC offset to ground-referenced signals. Furthermore, the PRL-BTDC-450R is also a wide band Inline 10X signal pick-off device which allows extraction of a small portion of the signal for monitoring, while producing negligible amount of disturbance to the main signal path.

Each model has RF I/O ports, J1 and J2, and a Bias port, J3. The RF I/O path is a 50 Ω transmission line, either AC- or DC-coupled between the I/O connectors J1 and J2. The Bias port J3 is used for connecting a DC voltage, a constant current, or a low-frequency signal source to the 50 Ω transmission line, while inductor L isolates the 50 Ω transmission line from the bias source. In the case of the PRL-BTDC-450R, J3 is connected to the I/O line through a 450 Ω resistor, which must be terminated into a 50 Ω input instrument for monitoring purposes. When so terminated the loading on the I/O line is 500 Ω. Since the I/O line looks like a 25 Ω load to the 450 Ω resistor, the signal loss due to the 500 Ω loading is only 5%.

Traditional Bias Tees are AC coupled, as shown in Model PRL-BTAC-114L, where the RF signal is AC-coupled to the DUT, connected to J2 through coupling capacitor C. In many of today's digital applications, where signals with very long 1's and 0's are common, DC coupling is desirable, because it eliminates DC level shift due to duty cycle variations. Furthermore, when a constant current source is connected to the bias port, the lower 3 dB bandwidth can be extended to DC.

The upper bandwidth of a Bias Tee is limited mostly by the imperfection of the isolation inductor L between the 50 Ω transmission line and the bias source. L is usually made up of different combinations of L's and R's. For the PRL series of Bias Tees, the upper 3 dB bandwidth is typically greater than 6 GHz.

For the AC-coupled Bias Tee, the lower 3 dB bandwidth is determined by the dominant pole made up either by $2Z_0C$ or $2L/Z_0$, assuming that both I/O ports are terminated into Z_0 and that L is connected to a voltage source. For the DC-coupled Bias Tee, however, the lower 3 dB bandwidth is determined by L, and it can be extended to DC by using a constant current instead of a voltage bias source. Standard value for the coupling capacitor C is 0.1 µf and the isolation inductor L is 110 µh. Other values are available by special order.

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When used with the PRL series of Coupling and Termination modules the lower 3 dB bandwidth of the DC-coupled model can be customized by using different DC blocks, from 0.01 µf to 2.2 µf, and/or series-coupled inductors, up to 330 µh. Other components, such as feed-through decoupling capacitors or attenuators, also are available.

*SPECIFICATIONS (0^o C ≤ T_A ≤ 35^oC)

All AC measurements are made with RF input and outputs terminated into 50 Ω

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
Z_0	I/O Line Characteristic Impedance	48.5	50	51.5	Ω	
I_{DC1}	J3 Bias Input Current			300	mA	L Input
I_{DC2}	J3 Bias Input Current			40	mA	450 Ω Input
I_{DC3}	J1-J2 Throughput Current			500	mA	
V_{DC}	J3 Bias Input Voltage	Limited by I_{DC}			V	
C	Coupling Capacitor	0.08	0.10	0.12	µf	BTAC only
L	DC Bias Inductor		110		µh	
R_L	Inductor DC Resistance		6		Ω	BTAC/BTDC
T_{PLH}/ T_{PHL}	Propagation Delay from J1 to J2		250	300	ps	
t_r/t_f	Rise/Fall Times (10%-90%)		58	65	ps	J1-J2
t_r/t_f	Rise/Fall Times (10%-90%)		150	200	ps	J3-450 Ω Output
UBW	Equivalent Upper 3 dB Bandwidth	5.3	6.0		GHz	J1-J2
UBW	Equivalent Upper 3 dB Bandwidth	1.75	2.3*		GHz	J3-450 Ω Output
LBWC	Equivalent Lower 3 dB Bandwidth	15.9*			KHz	BTAC
LBWL	Equivalent Lower 3 dB Bandwidth	39.75**			KHz	BTDC
	Size	1.0 x 1.3 x 1.5			in	
	Weight	3			Oz	

*Limited by C
**Limited by L

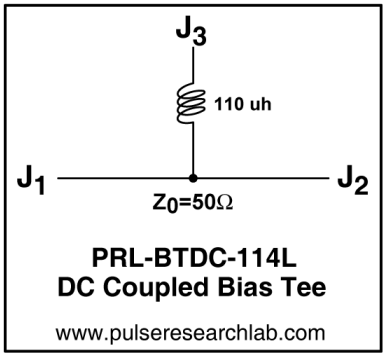

Figure 1: PRL-BTDC-114L Block Diagram

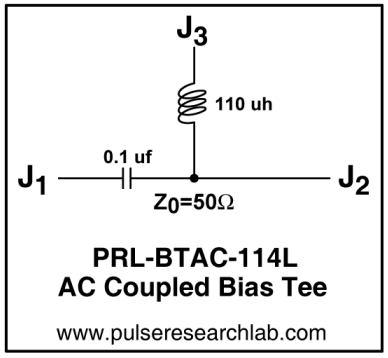

Figure 2: PRL-BTAC-114L Block Diagram

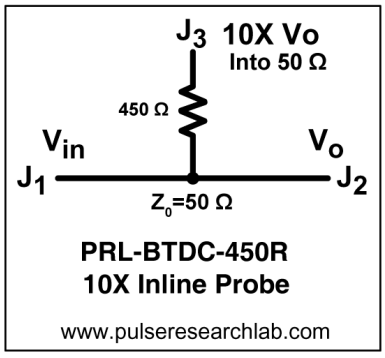

Figure 3: PRL-BTDC-450R Block Diagram

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