

PRL-4509 6-CHANNEL TTL/LVDS LOGIC LEVEL TRANSLATOR SYSTEM

APPLICATIONS

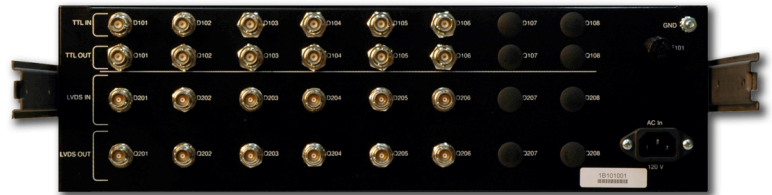
- Converting TTL signals to LVDS Signals
- Converting LVDS signals to TTL Signals
- High Speed Digital Communications System Testing
- Telemetry Translation

FEATURES

- $f_{\max} > 250$ MHz
- 1 ns t_R typical
- 50 Ω TTL Input Termination
- 100 Ω Floating Differential LVDS Input Termination
- 50 Ω TTL Outputs
- LVDS Outputs
- DC Coupled BNC I/O Connectors for TTL
- DC Coupled Triax I/O Connectors for LVDS
- Self-contained 5.25 x 19.0 x 22-in. rack-mountable unit includes internal power supply



PRL-4509 Front View



PRL-4509 Rear View

DESCRIPTION

The PRL-4509 is an 6-channel TTL to LVDS and LVDS to TTL Logic Level Translator system. It contains three PRL-425TTR Dual-Channel LVDS (Triax) to TTL translator modules and three PRL-426TTR-C001 Dual-Channel TTL to LVDS (Triax) translator modules mounted inside a 3U, 5.25 x 19.0 x 22.0-in rack-mountable chassis. All modules are mounted directly to the rear panel through the LVDS (Triax) connectors. The modules' TTL connectors connect internally to BNC bulkhead connectors on the rear panel via equal-length 50 Ω cables. The system contains an internal power supply that operates from a standard 120 VAC input.

Each PRL-425TTR module has two universal differential inputs with floating 100 Ω terminations and 50 Ω TTL outputs. The TTL output logic DC Hi/Lo levels are +2.5 V and 0 V, nominal, when terminated into 50 Ω . The outputs are back-terminated with 50 Ω series resistors and can drive high-impedance loads with minimized reflections.

Each PRL-426TTR-C001 has two TTL inputs with 50 Ω terminations and LVDS outputs. The TTL inputs have an internally-switchable 1.5 V or 1.0 V trigger threshold, factory set for 1.0 V. The LVDS outputs can drive 100 Ω /124 Ω floating loads. Basic block diagrams of these modules are shown in Figs. 1A and 1B.

These Logic Level Translators are designed for use in testing and interfacing of high speed digital communications circuits, where conversion between LVDS and TTL logic signals is often required. The PRL-4509 is part of the Mini Modular Instruments family that find increasing applications in high speed digital data recording instruments, transient recording instruments and other high speed measurement equipment where LVDS and TTL signals are often specified.



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PRELIMINARY SPECIFICATIONS ($0^{\circ} \text{ C} \leq T_A \leq 35^{\circ} \text{ C}$)

Unless otherwise specified, all logic level and dynamic measurements are made with all outputs terminated into 50Ω .

SYMBOL	PARAMETER	PRL-425TTR			PRL-426TTR-C001 ¹			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{IN}	Input Resistance				49.5	50.0	50.5	Ω
R_{IND}	Differential Input Resistance	95	100	105				Ω
R_{INC}	Common Mode Input Resistance		5					$k\Omega$
V_{CMI}	Input Common Mode Voltage	-2.4		+4.0				V
R_{OUT}	Output Resistance	49.5	50.0	50.5	49.5	50.0	50.5	Ω
V_{OL}	Output Low Level	-0.05	0.00	0.20		0.90		V
V_{OH}	Output High Level	2.0	2.3	2.5		1.5		V
V_{CMO}	Output Common mode voltage ²					1.2		V
I_{DC+}	DC Input Current, +8.5 V		175	185		100	115	mA
I_{DC-}	DC Input Current, -8.5 V		-365	-385		-245	-265	mA
V_{DC}	DC Input Voltage	± 7.5	± 8.5	± 12	± 7.5	± 8.5	± 12	V
t_{PROPI}	Propagation Delay, internal units		2.2			2.0		ns
t_{PROP2}	Propagation Delay, external I/Os		3.7			3.5		ns
t_R/t_F	Rise/Fall Times (10%-90%) ³		1.0	1.3		1.0	1.25	ns
t_{SKEW}	Skew between any 2 outputs ³		500	1200		200	500	ps
f_{MAX}	Max Clock Frequency ³	250	300		250	350		MHz

SYMBOL	PARAMETER	PRL-4509			UNIT
		Min	Typ	Max	
V_{AC}	AC Input Voltage	103	115	127	
V_{VA}	AC Input Power		50		VA
	Size	5.25H x 19.0W x 16.5D (excluding rail slides)			in
	Weight	16.0			lb

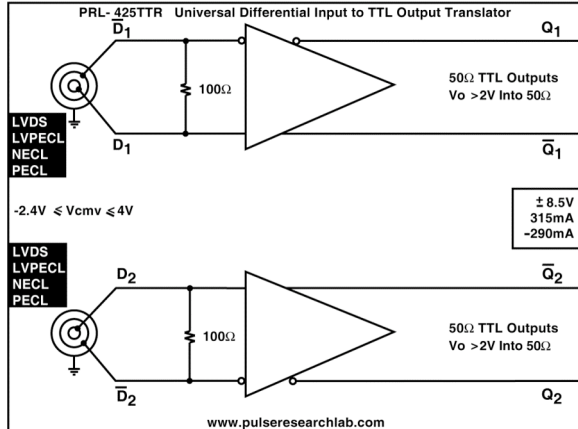


Fig. 1A PRL-425TTR Block Diagram

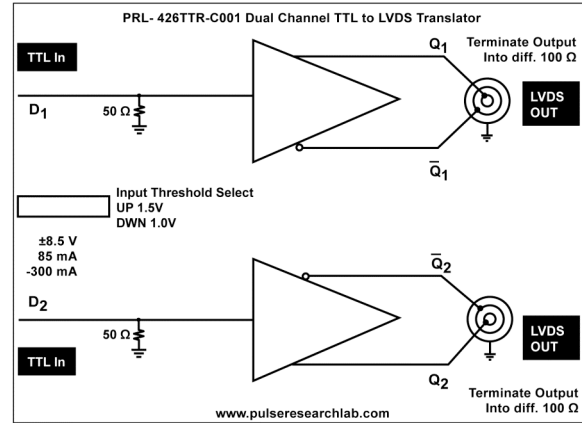


Fig. 1B PRL-426TTR-C001 Block Diagram

(1) The PRL-426TTR-C001 is functionally equivalent to a standard PRL-426TTR module, except that the DC power cable is hard-wired to the unit and routed out through the input side.

(2) $V_{CMO} = (V_{OH} - V_{OL})/2$

(3) t_R/t_F , t_{SKEW} , and f_{MAX} for the PRL-426TTR are determined by driving a PRL-425TTR and monitoring the output on a 50Ω sampling oscilloscope.