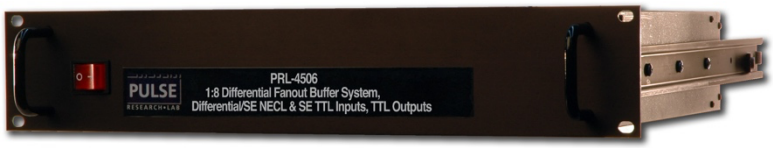
PRL-4506 1:8 DIFFERENTIAL FANOUT BUFFER SYSTEM, NECL AND TTL INPUTS, 50 Ω BACK-TERMINATED TTL OUTPUTS

APPLICATIONS

- Long Line Driver/Level Translator
- Reference Clock Distribution/Translation
- 1 PPS/IRIG-B Signal Distribution
- Test and System Integration



PRL-4506 Front View

PRL-4506 Rear View

FEATURES

- 1:8 Fanout with Complementary TTL Outputs
- Channel-to-channel Skew < 200 ps
- Unit-to-unit Skew < 300 ps[3]
- t_R= 1.4 ns Typ. @ 2.5 V Output into 50 Ω
- Back-terminated 50 Ω Outputs Drive Long Lines into 50 Ω or Unterminated Loads
- TTL and NECL Inputs (logically ORed)
- NECL Input can be driven differentially, single-ended, or AC-coupled for sinewave conversion
- Standard 19-in. Rack-Mount Chassis with optional slide rails

GENERAL DESCRIPTION

The PRL-4506 is a low-skew, 1:8 differential fanout buffer system with 8 complementary 50 Ω back-terminated TTL outputs and two inputs. The single-ended TTL input has a selectable 50 Ω or 1 KΩ to ground termination. The NECL input can be driven by single-ended NECL, differential NECL or AC-coupled sinewave signals. The TTL and NECL inputs are logically ORed; therefore a Hi level applied to either input can be used as a gate signal.

For the NECL input a toggle switch selects either single-ended or differential inputs. In the differential input mode both the NECL and $\overline{\text{NECL}}$ inputs and are terminated internally into 50 Ω/-2 V, and, therefore, either one or both inputs can accept AC-coupled signals as well.

In the single input mode, signal should be connected to the NECL input only. The $\overline{\text{NECL}}$ input is switched internally to V_{BB}, nominally -1.3 V, and termination resistor R_T for the $\overline{\text{NECL}}$ input channel is changed to a Hi Z value. In the single-input mode, therefore, the $\overline{\text{NECL}}$ input should not be used for receiving signals. If the NECL inputs are not connected to an active signal, the switch should be in the down position.

The input resistance of the TTL input can be selected to be either 50 Ω or 1 KΩ by a toggle switch. The 1 KΩ input is desirable when interfacing with low power circuits. The TTL input threshold voltage is 1.0 V minimum. When over-driven, the input voltage to the internal circuit is limited to 3.5 V through a current limiting 25 Ω series resistor. The output swing is typically 0-2.5 V into 50 Ω or 0-5.0 V into high impedance.

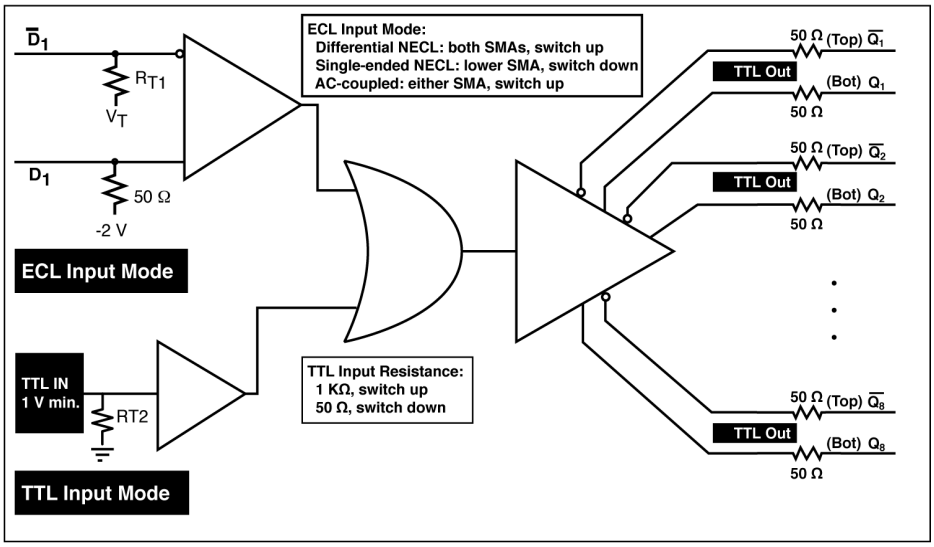
All I/Os are DC coupled and have SMA connectors at the rear panel of the unit. The PRL-4506 is housed in a standard 19-in. rack-mountable enclosure with optional slide rails, powered by an internal power supply switchable for 120/240 VAC, 50-60 Hz operation.

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com

*SPECIFICATIONS (0 °C ≤ T_A ≤ 35 °C)

Unless otherwise specified, dynamic measurements are made with all rear-panel outputs terminated into 50 Ω, using precision-trimmed 18.0", phase-stable 50 Ω RF cables.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comment
R_{T1-1}	Input Resistance, NECL	49.5	50.0	50.5	Ω	Differential Input mode
R_{T2-1}	Input Resistance, TTL 50 Ω	49	50	51	Ω	
R_{T2-2}	Input Resistance, TTL 1 KΩ	0.95	1.00	1.05	KΩ	
V_{TT}	D Input Termination Voltage	-2.2	-2.0	-1.8	V	NECL input
V_{T1}	Input Termination Voltage	-1.25	-1.30	-1.35	V	Single-ended mode
V_{T2}	Input Termination Voltage	-2.20	-2.00	-1.80	V	Differential mode
V_{IH1}	TTL Input Hi Level	1.0		5.0	V	Internally limited to 3.5 V
V_{IL1}	TTL Input Lo Level	-0.5		0.5	V	
V_{IH2}	NECL Input Hi Level	-1.13	-0.90	-0.81	V	
V_{IL2}	NECL Input Lo Level	-1.95	-1.60	-1.48	V	
R_{OUT}	Output Resistance	49.5	50.0	50.5	Ω	
V_{OH1}	Output High Level	2.2	2.5	2.6	V	R_{LOAD} = 50 Ω
V_{OH2}	Output High Level	4.4	5.0	5.2	V	R_{LOAD} = 1 MΩ
V_{OL}	Output Low Level	-0.25	0.00	0.25	V	
V_{AC1}	AC Input Voltage, 120	108	115	127	V	
V_{AC2}	AC Input Voltage, 220	216	230	254	V	
V_{VA}	AC Input Power		40	45	VA	
T_{PROP1}	Prop. Delay to Output ↑, Diff. NECL Input	5.88	6.03	6.18	ns	See Notes 1, 2
T_{PROP2}	Prop. Delay to Output ↑, TTL Input, 50 Ω	6.30	6.45	6.60	ns	See Notes 1, 2
T_R	Rise Time (10%-90%)		1.4	2.0	ns	
T_F	Fall Time (10%-90%)		1.4	2.0	ns	
T_{SKEW1}	Ch./Ch. skew between any 2 True Outputs		125	200	ps	See Notes 1, 2
T_{SKEW2}	Unit/Unit skew between any 2 True Outputs		200	300	ps	See Notes 1, 2, 3
F_{MAX}	Max Clock Frequency	150	175		MHz	
	Size	19.0"W x 3.5"H x 16.5"D			in	Excluding slide rails
	Weight	13			lbs	



PRL-4506 Block Diagram (simplified)

Notes:

1. Skew measurements valid when using same input logic level. TTL-input measurements made with TTL input set to 50 Ω. ECL-input measurements made with ECL input set for differential mode.
2. T_{PROP} and T_{SKEW} measurements made via PRL-8506 Test Mux, which provides 50 MHz input clocks in ECL and TTL logic as well as delay-matched ECL and TTL reference timing paths.
3. Unit-to-unit skew specification valid only for units within a single lot, purchased on a single PO.

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com