PRL-4501 8-CHANNEL NECL/NCML LOGIC LEVEL TRANSLATOR SYSTEM

APPLICATIONS

- Converting Differential NECL signals to Differential NCML Signals
- Converting Differential NCML signals to Differential NECL Signals
- Differential NCML Inputs also accept Sinewave or Differential TTL Signals
- High Speed Digital Communications System Testing
- High Speed SONET Clock Level Translation

PRL-4501 Front View

PRL-4501 Rear View

FEATURES

- f_{max} > 1.5 GHz
- 650 ps t_r
- 50 Ω/-2 V NECL Input Termination
- 50 Ω to Ground NCML Input Termination
- Complementary NECL Outputs
- Complementary NCML Outputs
- DC Coupled SMA I/O Connectors
- Self-contained 5.25 x 19 x 22-in. rack-mountable unit includes internal power supply

DESCRIPTION

The PRL-4501 is an 8-channel differential NECL to differential NCML and differential NCML to differential NECL Logic Level Translator system. It contains four PRL-427-C001 dual-channel NECL to NCML translator modules and four PRL-360ECL-C002 dual-channel NCML to NECL translator modules mounted inside a 5.25 x 19 x 22-in rack-mountable chassis. All modules are mounted directly to the rear panel through the SMA input connectors. The module output connectors are connected to the rear panel-mount SMA connectors with equal-length 50 Ω cables. The system contains an internal power supply that operates from standard 120 VAC input.

Each PRL-427-C001 has dual-channel differential NECL inputs terminated to 50 Ω/-2 V and ground-referenced differential 35 Ω NCML outputs. The NCML DC output logic Hi/Lo levels are 0 V and -350 mV, respectively, when terminated to ground-referenced 50 Ω loads.

Each PRL-350ECL-C002 has dual-channel comparator inputs with ground-referenced 50 Ω terminations and differential NECL outputs. The comparator inputs accept differential NCML, differential TTL or single-ended sinewave inputs. They will also accept nearly any differential input signals within the common mode range from -2.4 V to +3 V with a minimum peak-to-peak input signal of 20 mV. The standard NECL outputs can drive 50 Ω loads terminated to -2 V, AC-coupled 50 Ω loads or floating 100 Ω loads. Basic block diagrams of these modules are shown in Figs. 1A and 1B.

These Logic Level Translators are designed specifically for use in testing and interfacing of high speed digital communications circuits, where conversion between NECL and NCML logic signals is often required. The PRL-4501 is part of the **B**asic **L**aboratory **T**ools family that find increasing applications in high speed digital data recording instruments, transient recording instruments and other high speed measurement equipment where NECL and NCML signals are often specified.

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PRELIMINARY SPECIFICATIONS (0° C ≤ T_A ≤ 35° C)

Unless otherwise specified, all logic level and dynamic measurements are made with all outputs terminated into 50 Ω/V_{TT}, where V_{TT} = -2 V for NECL outputs and 0 V for NCML outputs.

SYMBOL	PARAMETER	PRL-350ECL-C002			PRL-427-C001			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{in}	Input Resistance	49.5	50	50.5	49.5	50	50.5	Ω
R_{out}	Output Resistance		NPN emitter			35		Ω
V_{TH0}	Preset threshold voltage(1)		4.5			4.5		mV
V_{OL}	DC Output Low Level	-2	-1.6	-1.5		-0.35		V
V_{OH}	DC Output High Level	-1	-0.8	-0.6		0		V
Vop-p	Output Logic Swing from DC-500MHz Output Logic Swing from 500MHz-1GHz Output Logic Swing from 1GHz -1.5GHz-		800		300 275 225	350 300 260		mV
VoCM	Output Common Mode Voltage		NA			-200		mV
I_{DC}	DC Input Current		36/ -136	45/ -145		138/ -315	145/ -325	mA
I_{DCS}	System DC Input Current		700/-1800 (nominal)					mA
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	±7.5	±8.5	±12	V
V_{AC}	AC/DC Adapter Input Voltage	108	120	132	108	120	132	V
t_{PLH}	Propagation Delay to output ↑		1.5			1.5		ns
t_{PHL}	Propagation Delay to output ↓		1.5			1.5		ns
t_r/t_f	Rise/Fall Times(2)		650	750		650	750	ps
t_{SKEW}	Skew between any 2 outputs		40	75		40	75	ps
V_{IN} I	Minimum Input Voltage @ 150MHz	20	10		20	10		mVp-p
V_{IN} II	Minimum Input Voltage @ 250MHz	20	10		20	10		mVp-p
V_{IN} III	Minimum Input Voltage @ 1GHz	250	100		250	100		mVp-p
V_{CM}	Input Common Mode Range		+3 /-2.5			N/A		V
f_{MAX}	Max Clock Frequency(4)	1250	1500		1250	1500		MHz
	Size		1.3H x 2.9W x 3.9D			1.3H x 2.9W x 3.9D		in.
	System Size		5.25H x 19.0W x 16.5D (excluding rail slides)					in.
	Weight		7			7		Oz
	System Weight		16.0					lb

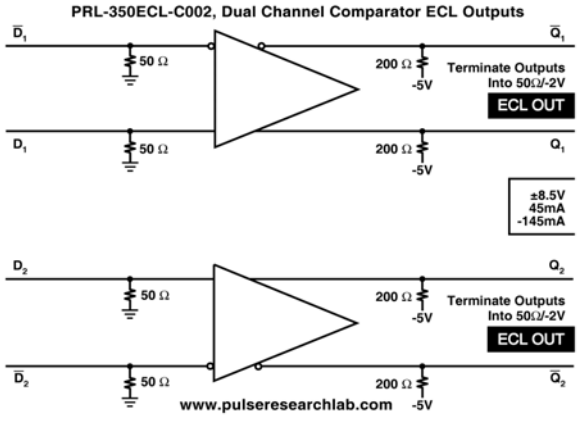

Fig. 1A PRL-350ECL-C002 Block Diagram

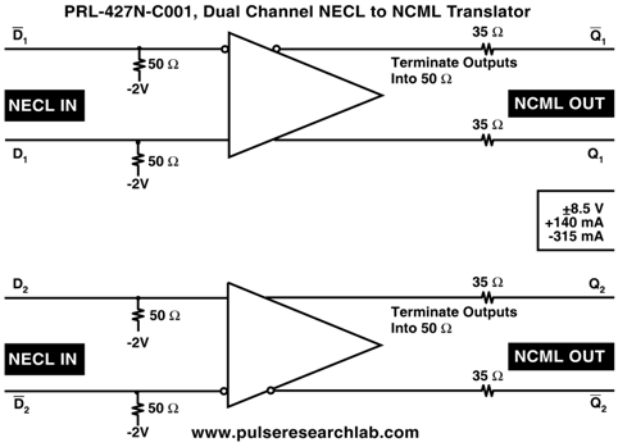

Fig. 1B PRL-427N-C001 Block Diagram

(1) The preset threshold voltage of 4.5 mV will prevent the modules from oscillating when the inputs are open.

(2) 20%-80% for NECL outputs, 10%-90% for NCML outputs. For the PRL-350ECL, an unused complementary output must be either terminated into 50 Ω /V_{TT} or AC coupled into a 50 Ω load; otherwise, output waveform distortion and rise time degradation will occur. Use the PRL-ACT-50 Dual Channel AC-Coupled 50 Ω Termination for terminating unused complementary outputs. Use the PRL-550NQ/PQ4X, four channel NECL/PECL Terminators, respectively, for the 50 Ω/V_{TT} termination and for connection of NECL/PECL signals to 50 Ω input oscilloscopes. If preservation of DC levels is not required, then the PRL-SC-104, 0.1 uf DC block, or the PRL-ACX-12dB, AC-coupled attenuator, may be used to connect the NECL/PECL outputs to 50 Ω input instruments.

For the PRL-427, very slight output waveform distortion and rise time degradation will occur when an unused complementary output is not terminated. For optimum performance, however, all outputs should be terminated.

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