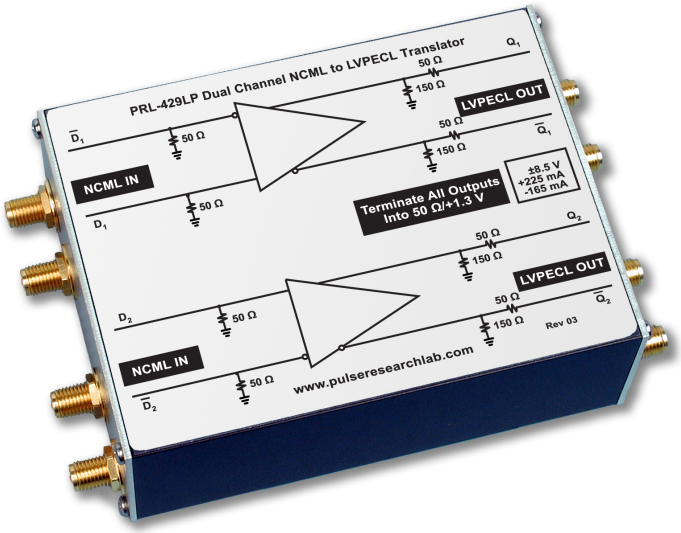
PRL-429LP, 2 Channel NCML to LVPECL Logic Level Translator

APPLICATIONS

- Converting Differential NCML Inputs to Differential LVPECL Outputs
- Accepts AC-coupled Differential or Singled-Ended Sinewave Inputs
- High Speed Digital Communications System Testing
- Satellite/Radar/Telecommunications System Integration

FEATURES

- f_{max} > 1.5 GHz
- 250 ps t_r/t_f typical
- 50 Ω Input Terminations
- Complementary LVPECL Outputs
- DC Coupled SMA I/O Connectors
- Self-contained 1.3" x 2.9" x 3.9" unit includes AC/DC adapter



PRL-429LP

DESCRIPTION

The PRL-429LP is a dual-channel NCML to LVPECL Logic Level Translator module. Each channel has differential ground referenced 50Ω inputs and complementary LVPECL outputs.

Each differential NCML input has a preset 10 mV offset which prevents the input circuit from oscillation when it is not driven or left open. Minimum peak-to-peak differential input swing required is 200 mV typical. When driven single-ended, such as with a sinewave, the input signal needs to swing above and below ground, ±100 mV typical. Either one or both inputs can also accept AC-coupled signals.

The complementary LVPECL outputs are 50 Ω back terminated and are designed for driving 50 Ω loads terminated into 1.3 V. When terminated into 1.3 V, the output Hi/Lo levels are typically 2.20 V and 1.75 V, respectively. Both outputs can also drive AC coupled 50 Ω loads.

The PRL-429LP Level translator is designed specifically for use in testing and interfacing of high speed digital communications circuits, where conversion between NCML and LVPECL logic signals is often required. The PRL-429LP is part of the Mini Modular Instrument (MMI) family that find increasing applications in high speed digital data recording instruments, transient recording instruments and other high speed measurement equipment where LVPECL and NCML signals are often specified.

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SPECIFICATIONS (0° C ≤ T_A ≤ 35° C)

Unless otherwise specified, all logic level and dynamic measurements are made with all outputs terminated into 50 Ω/V_{TT}, where V_{TT} = 1.3 V for LVPECL devices.

SYMBOL	PARAMETER	PRL-429LP			UNIT
		Min	Typ	Max	
R_{IN}	Input Resistance	49.5	50.0	50.5	Ω
R_{OUT}	Output Resistance		50		Ω
V_{IPP}	Differential peak-to-peak Input	250		3000	mV
V_{ICM}	V_{IN} Common Mode Range	-2.4		3.0	V
V_{OL}	Output Low Level, f ≤ 800 MHz		1.75		V
V_{OH}	Output High Level, f ≤ 800 MHz	2.10	2.25		V
V_{OP-P}	Output Logic Swing, f ≤ 800 MHz	400	450		mV
V_{OCM}	Output Common Mode Voltage				mV
I_{DC1}	DC Input Current, +8.5 V		225	245	mA
I_{DC1}	DC Input Current, - 8.5 V	-185	-165		mA
V_{DC}	DC Input Voltage	±7.5	±8.5	±12.0	V
V_{AC}	AC/DC Adapter Input Voltage	108	120	132	V
t_{PLH}	Propagation Delay to output ↑		2.0	2.5	ns
t_{PHL}	Propagation Delay to output ↓		2.0	2.5	ns
t_R/t_F	Rise/Fall Times (10-90%)		200	275	ps
T_{SKEW}	Skew between any 2 outputs, f ≤ 800 MHz		50	100	ps
f_{MAX}	Max Clock Frequency[4]	1500	1750		MHz
	Size	1.3H x 2.9W x 3.9D			in.
	Weight, excluding AC adapter	7			Oz
	Shipping Weight, including AC adapter	4			lb

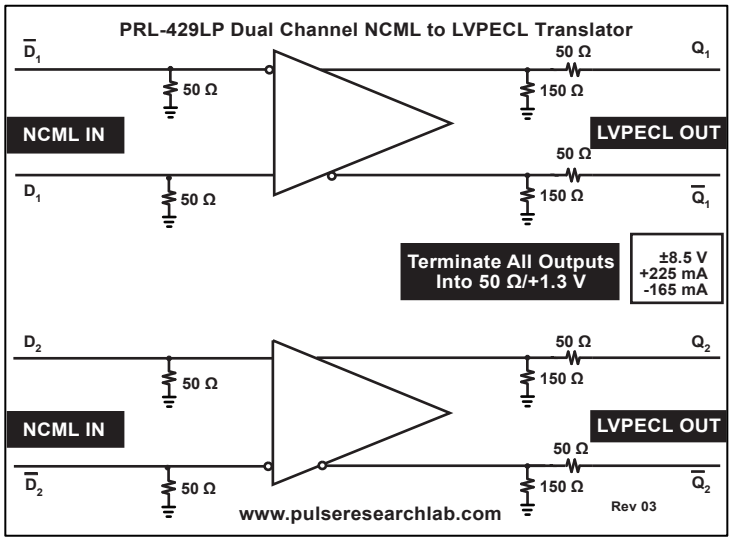

Fig. 1 PRL-429LP Block Diagram

For the PRL-429LP, output waveform distortion and rise time degradation will occur when an unused complementary output is not terminated. For optimum performance, all outputs should be terminated into 50 Ω/1.3 V, or AC coupled into 50 Ω terminations.

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