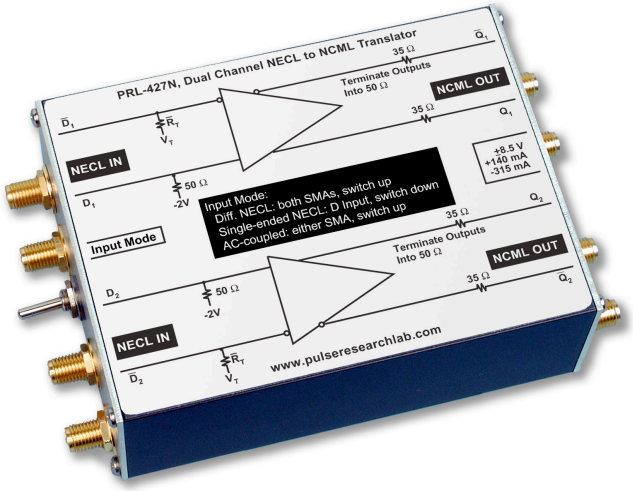
# PRL-427N, 2 CHANNEL NECL to NMCL LOGIC LEVEL TRANSLATOR

## APPLICATIONS

- Converting Single-ended or Differential NECL Inputs to Differential NCML Outputs
- Differential NECL Inputs also accept Sinewave Signals
- High Speed Digital Communications System Testing
- Satellite/Radar/Telecommunications System Integration

## FEATURES

- $f_{max}$ > 1.5 GHz
- 650 ps $t_r$
- 50 Ω/-2 V NECL Input Termination
- Complementary NCML Outputs
- DC Coupled SMA I/O Connectors
- Self-contained 1.3H x 2.9W x 3.9D unit includes AC/DC adapter




**PRL-427N**

## DESCRIPTION

The PRL-427N is a 2-channel NECL to differential NCML Logic Level Translator module. Each channel has a single-ended or differential NECL input and a ground-referenced differential 35 Ω NCML output. The NCML DC output logic Hi/Lo levels are 0 V and -350 mV, respectively, when terminated to ground-referenced 50 Ω loads.

A switch selects either single-ended or differential inputs, as shown in Fig. 1. In the differential input mode, both inputs D and $\overline{D}$ are terminated internally into 50 Ω/$V_{TT}$, where $V_{TT}$ is equal to –2 V for NECL. In the differential input mode, therefore, either one or both inputs can accept AC coupled signals as well. In the single input mode, signals should be connected to the D inputs only. The $\overline{D}$ inputs are switched internally to $V_{BB}$, nominally -1.3 V for NECL, and termination resistors $\overline{R}_T$'s for the $\overline{D}$ input channels are changed to 62 Ω.

These Logic Level Translators are designed specifically for use in testing and interfacing of high speed digital communications circuits, where conversion between NECL and NCML logic signals is often required. The PRL-427N is part of the Mini Modular Instrument (MMI) family that find increasing applications in high speed digital data recording instruments, transient recording instruments and other high speed measurement equipment where NECL and NCML signals are often specified.


PULSE RESEARCH·LAB

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com

## PRELIMINARY SPECIFICATIONS (0° C ≤ $T_A$ ≤ 35° C)

Unless otherwise specified, all logic level and dynamic measurements are made with all outputs terminated into 50 Ω/$V_{TT}$, where $V_{TT}$ = 0 V for NCML outputs.

| SYMBOL | PARAMETER | PRL-427N | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $R_{IN}$ | Input Resistance | 49.5 | 50 | 50.5 | Ω |
| $R_{OUT}$ | Output Resistance | | 35 | | Ω |
| $V_{OL}$ | DC Output Low Level | | -0.35 | | V |
| $V_{OH}$ | DC Output High Level | | 0 | | V |
| $V_{OP-P}$ | Output Logic Swing from DC-500MHz<br>Output Logic Swing from 500MHz-1GHz<br>Output Logic Swing from 1GHz -1.5GHz | 300<br>275<br>225 | 350<br>300<br>260 | | mV |
| $V_{OCM}$ | Output Common Mode Voltage | | -200 | | mV |
| $I_{DC}$ | DC Input Current | | 138/<br>-315 | 145/<br>-325 | mA |
| $V_{DC}$ | DC Input Voltage | ±7.5 | ±8.5 | ±12.0 | V |
| $V_{AC}$ | AC/DC Adapter Input Voltage | 108 | 120 | 132 | V |
| $t_{PLH}$ | Propagation Delay to output ↑ | | 1.5 | | ns |
| $t_{PHL}$ | Propagation Delay to output ↓ | | 1.5 | | ns |
| $t_R/t_F$ | Rise/Fall Times (10-90%) | | 650 | 750 | ps |
| $T_{SKEW}$ | Skew between any 2 outputs | | 40 | 75 | ps |
| $V_{IN}$I | Minimum Input Voltage @ 150 MHz | 20 | 10 | | $mV_{PP}$ |
| $V_{IN}$II | Minimum Input Voltage @ 250 MHz | 20 | 10 | | $mV_{PP}$ |
| $V_{IN}$III | Minimum Input Voltage @ 1 GHz | 250 | 100 | | $mV_{PP}$ |
| $V_{CM}$ | Input Common Mode Range | | N/A | | V |
| $f_{MAX}$ | Max Clock Frequency(4) | 1250 | 1500 | | MHz |
| | Size | 1.3H x 2.9W x 3.9D | | | in. |
| | Weight | 7 | | | Oz |

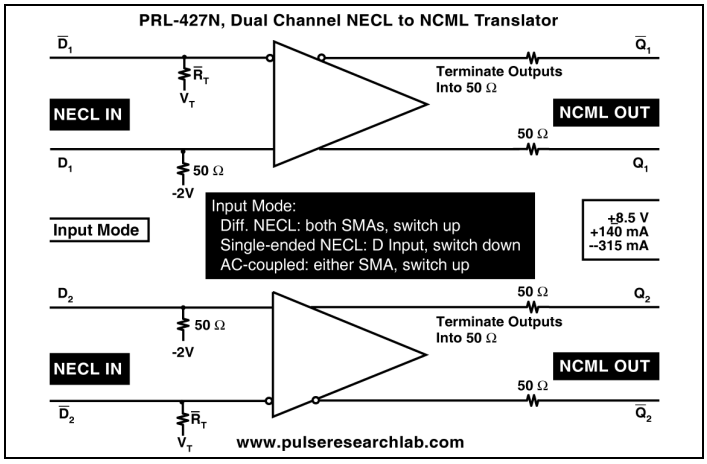



**Fig. 1 PRL-427N Block Diagram**

For the PRL-427, very slight output waveform distortion and rise time degradation will occur when an unused complementary output is not terminated. For optimum performance, however, all outputs should be terminated.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