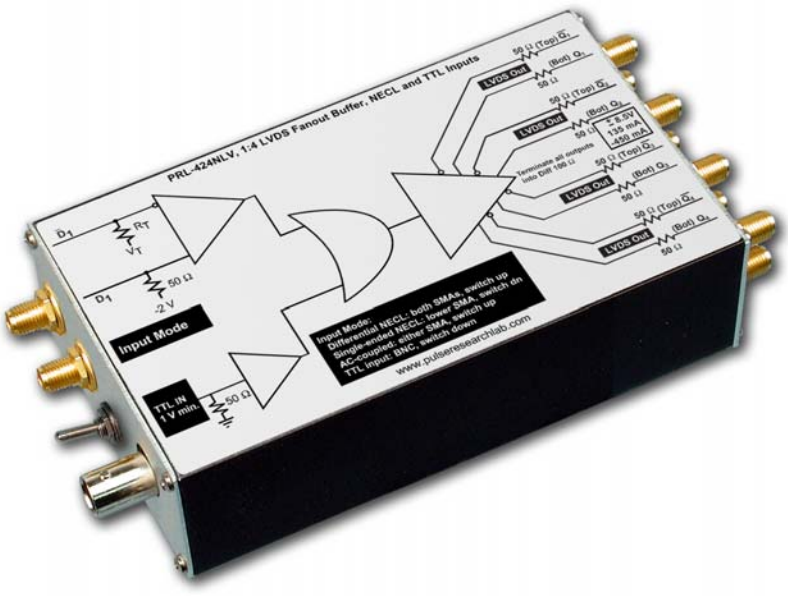
PRL-424NLV 1:4 LVDS FANOUT BUFFER, NECL AND TTL INPUTS

APPLICATIONS

- LVDS Fanout Buffer
- Converting NECL or Sinewave Signals to LVDS
- Converting TTL Signals to LVDS
- High Speed Digital Communications Systems Testing
- Satellite Telemetry/Ground Station System Integration

FEATURES

- f_{max} > 1.25GHz for NECL, > 300 MHz for TTL input
- Single-ended or Differential NECL Input with Internal 50 Ω/V_{TT} Input Termination also accepts Sinewave or AC-coupled Signals
- Separate TTL input (1 V minimum) Logically ORed with NECL Inputs
- 4 Pairs of Complementary 50 Ω LVDS Outputs
- 500 ps Typical Output Rise & Fall Times
- SMA Connectors for NECL Inputs
- BNC Connector for TTL Input
- SMA Output Connectors
- Self-contained 1.3 x 2.9 x 5-in. unit includes ±8.5V/1.4A AC/DC Adapter



PRL-424NLV

DESCRIPTION

The PRL-424NLV is a 1:4 fanout, complementary output, LVDS line driver. It is intended for converting NECL signals, AC-coupled sine waves, or TTL signals into multiple LVDS signals for driving long lines. The PRL-424 high speed fanout line driver facilitates testing of high speed digital communications circuits and distribution of satellite signals.

The PRL-424NLV has two logically ORed input circuits:

- For the NECL input a switch selects either single-ended or differential inputs, as shown in Fig. 1. In the differential input mode, both inputs D and $\overline{D}$ are terminated internally into 50 Ω/V_{TT}, where V_{TT} is –2 V for NECL. In the differential input mode, therefore, either one or both inputs can accept AC coupled signals as well. In the single-ended input mode, signals should be connected to the D input only. The $\overline{D}$ input is switched internally to V_{BB}, nominally -1.3 V for NECL, and termination resistor $\overline{R}_T$ for the $\overline{D}$ input channel is changed to 62 Ω. The connectors for the NECL input are SMA.

- The TTL input has a 50 Ω input termination with a minimum 1 V triggering threshold. The TTL input connector is BNC. When using the TTL input the NECL input selector switch should be in the Down position to prevent spurious triggering.

The four pairs of complementary outputs are 50 Ω back-terminated and are designed for driving floating 100 Ω loads, normally the configuration used in LVDS input circuits. The output swing is typically 600 mV with a common mode voltage of 1.2 V. All output connectors are SMA.

The PRL-424NLV is supplied with a ±8.5 V/1.4 A AC/DC adapter and housed in a 1.3 x 2.9 x 5-in. extruded aluminum enclosure. Available accessories include voltage distribution modules and brackets for mounting multiple units.

PULSE RESEARCH·LAB

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com

*SPECIFICATIONS (0^0 C ≤ T_A ≤ 35^0C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into floating 100 Ω loads.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comment
R_{in}	Input Resistance	49.5	50	50.5	Ω	
V_{TT}	D Input Termination Voltage (fixed)	-2.2	-2	-1.8	V	
V_T	$\overline{D}$ Input Termination Voltage (variable)	-1.17/ -2.2	-1.3/ -2	-1.43/ -1.8	V	
V_{IL}	Input Lo Voltage	-1.95	-1.6	-1.48	V	
V_{IH}	Input Hi Voltage	-1.13	-0.9	-0.81	V	
VoL	Output Low Level		0.9		V	
VoH	Output High Level		1.5		V	
V_{IL}	Input Lo Voltage	-1.95	-1.6	-1.48	V	
I_{DC}	DC Input Current		130 -470	140 -480	mA	
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	V	
V_{AC}	AC/DC Adapter Input Voltage, 120 AC/DC Adapter Input Voltage, 220	103 206	115 220	127 254	V	
t_{PLH}	Propagation Delay to output ↑		2.7		ns	
t_{PHL}	Propagation Delay to output ↓		2.7		ns	
t_r/t_f1	Rise/Fall Times (10%-90%)[1]		500	650	ps	@200 MHz
t_r/t_f2	Rise/Fall Times (10%-90%)[1]		250		ps	@1.25 GHz
t_{SKEW}	Skew between any 2 outputs		200	550	ps	
f_{max}	Max Clock Frequency, SMA Input[2] Max Clock Frequency, TTL Input	1.25	1.35 300		GHz MHz	
	Size		1.3 x 2.9 x 5.0		in.	
	Weight		8		Oz	

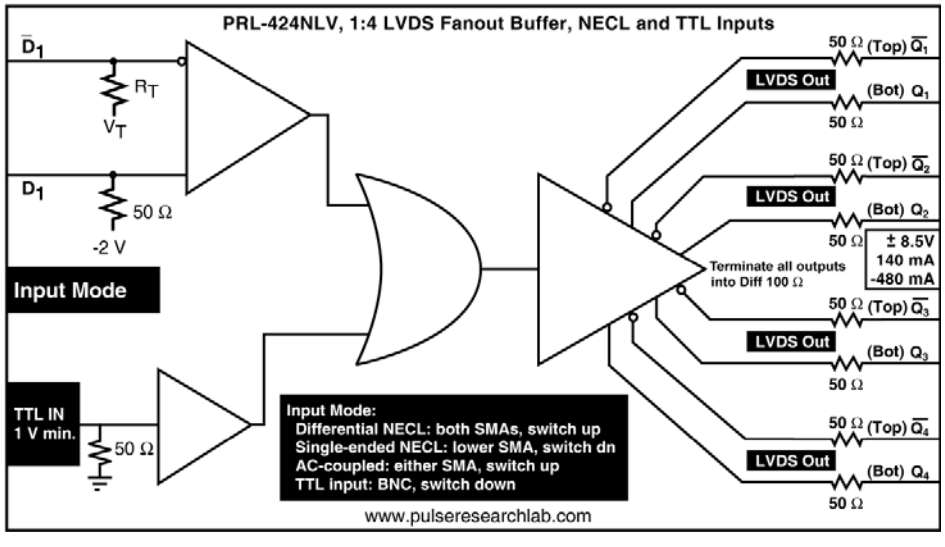


Fig. 1 PRL-424NLV Block Diagram

Notes:
(1) Rise and Fall times are measured with ground-referenced 50 Ω loads.
(2) f_{max} is measured using the PRL-174ANT Clock Driver outputs as the driver and the PRL-425N with SMA input connectors as the receiver. The outputs of the PRL-425N are then measured. f_{max} for the TTL input is currently limited by the lack of TTL drivers faster than 300 MHz.

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