PRL-4216UL-TR 2 x 1:8 DIFFERENTIAL FANOUT BUFFER, UNIVERSAL DIFFERENTAL AND TTL INPUTS, LVDS OUTPUTS

APPLICATIONS

- Long Line Driver/Level Translator
- Reference Clock Distribution/Translation
- 1 PPS/IRIG-B Signal Distribution
- Telemetry and Avionics Distribution
- Test and System Integration

FEATURES

- 2 x 1:8 Fanout with LVDS Outputs
- Two independent sets of fanout for CLK/DATA distribution
- Channel-to-channel Skew < 500 ps
- t_R= 1.6 ns Typ. @ 1.6 V Output into 50 Ω
- Floating 100 Ω Triax Input Compatible with RS-422, LVDS, NECL, or LVPECL
- BNC TTL Input has selectable 50 Ω or 1 kΩ Impedance
- Both TTL and Floating 100 Ω Inputs are Logically ORed
- Back-terminated Differential 50 Ω Triax Outputs Drive Long Lines into Floating 100 Ω Loads
- AC/DC Adapter Included

PRL-4216UL-TR Front View

PRL-4216UL-TR Rear View

GENERAL DESCRIPTION

The PRL-4216UL-TR is a 2 x 1:8 differential fanout buffer system, consisting of two independent 1:8 fanout PCBs, each with eight LVDS outputs and two inputs. The single-ended TTL inputs have selectable 50 Ω or 1 kΩ terminations to ground. The Universal Differential inputs can be driven by differential RS-422, LVDS, NECL, or LVPECL signals (ECL signals must be source-biased). The TTL and Differential inputs on each PCB are logically ORed; therefore a Hi level applied to either input can be used as a gate signal.

The input resistance of the TTL inputs can be selected to be either 50 Ω or 1 kΩ by toggle switches. The 1 kΩ inputs are desirable when interfacing with low power circuits. The TTL input threshold voltages are 1.0 V minimum.

The output swing is typically 600mV_{PP} with a 1.2 V_{CMV} into a 100 Ω floating load.

All I/Os are DC coupled and have Triax connectors, except for the TTL inputs, which are BNC. The PRL-4216UL-TR is housed in a 6.8” x 6.0” x 3.0” extruded aluminum enclosure and is powered by an included AC/DC adapter.

The PRL-4216UL-TR is part of the PRL-4108 series of differential fanout buffers, available with variety of options for input logic, output logic, and connector types.

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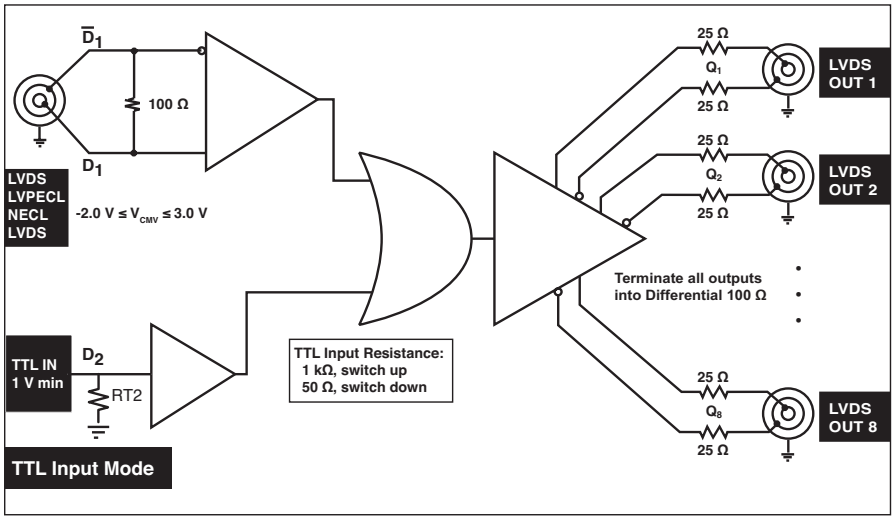
*SPECIFICATIONS (0 °C ≤ T_A ≤ 35 °C)

Unless otherwise specified, dynamic measurements are made with all rear-panel outputs terminated into floating 100 Ω, using 124 Ω shielded twisted pair Triax cables (Trompeter P/N PCGOW10PCG-36 or equivalent). Channel to channel skew and propagation delay measurements are made using a PRL-425NTR Differential Receiver with NECL outputs. Rise and fall time measurements are made using a Triax to SMA adapter and connecting the SMA outputs to a 50 Ω input scope.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comment
R_{T1-1}	Differential Input Resistance	95	100	105	Ω	
R_{INC}	Common Mode Input Resistance		5		kΩ	
R_{T2-1}	Input Resistance, TTL 50 Ω	49	50	51	Ω	
R_{T2-2}	Input Resistance, TTL 1 kΩ	0.95	1.00	1.05	kΩ	
V_{CMR}	Input Common Mode Voltage	-2.0		3.0	V	
V_{IH1}	TTL Input Hi Level	1.0		5.0	V	Internally limited to 3.5V
V_{IL1}	TTL Input Lo Level	-0.5		0.5	V	
R_{OUT1}	Output Resistance	24.75	25	25.25	Ω	Single-ended
R_{OUT2}	Output Resistance	49.5	50	50.5	Ω	Differential
V_{OH1}	Output High Level		1.8		V	No Load
V_{OH2}	Output High Level		1.65		V	Terminated to 100 Ω
V_{OL1}	Output Low Level		0.78		V	No Load
V_{OL2}	Output Low Level		0.95		V	Terminated to 100 Ω
V_{OD}	Output Differential Voltage (V_{OH2}-V_{OL2})		0.7			Terminated to 100 Ω
V_{OCM}	Output Common Mode Voltage*		1.3			Terminated to 100 Ω
V_{AC1}	AC Adapter Input Voltage, 120	108	115	127	V	
V_{AC2}	AC Adapter Input Voltage, 220	216	230	254	V	
I_{DC1}	DC Input Current, +8.5 V Supply		770		mA	
I_{DC2}	DC Input Current, -8.5 V Supply		-1400		mA	
T_{PROP1}	Prop. Delay to Output ↑, Diff. Input		2.5		ns	
T_{PROP2}	Prop. Delay to Output ↑, TTL Input, 50 Ω		3		ns	
T_R	Rise Time (10%-90%)		1.2	1.8	ns	See Note 1
T_F	Fall Time (10%-90%)		1.2	1.8	ns	See Note 1
T_{SKEW1}	Ch./Ch. skew ↔ any 2 ↑ or 2 ↓Vo in each bank		200	350	ps	
T_{SKEW2}	Ch./Ch. skew ↔ any ↑ and ↓Vo in each bank		700	1200	ps	
T_{SKEW3}	Ch./Ch. skew ↔ any 2 ↑ or 2 ↓Vo		400	550	ps	
T_{SKEW4}	Ch./Ch. skew ↔ any ↑ and ↓Vo		1000	1250	ps	
F_{MAX1}	Max Clock Frequency, Diff. Input	150	175		MHz	
F_{MAX2}	Max Clock Frequency, TTL Input	100	125		MHz	
	Size	3.0"H x 6.8"W x 7.3"L			in	Including connectors
	Weight	2			lbs	Excluding AC adapter
	Shipping weight	6			lbs	Including AC adapter

*V_{OCM} by definition is equal to (V_{OH2} + V_{OL2})/2



PRL-4216UL-TR Block Diagram (simplified; unit contains two sets)

Notes:

1. Due to lack of suitable equipment with floating differential 100 Ω input termination, T_R and T_F are measured using a 50 Ω input scope.

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