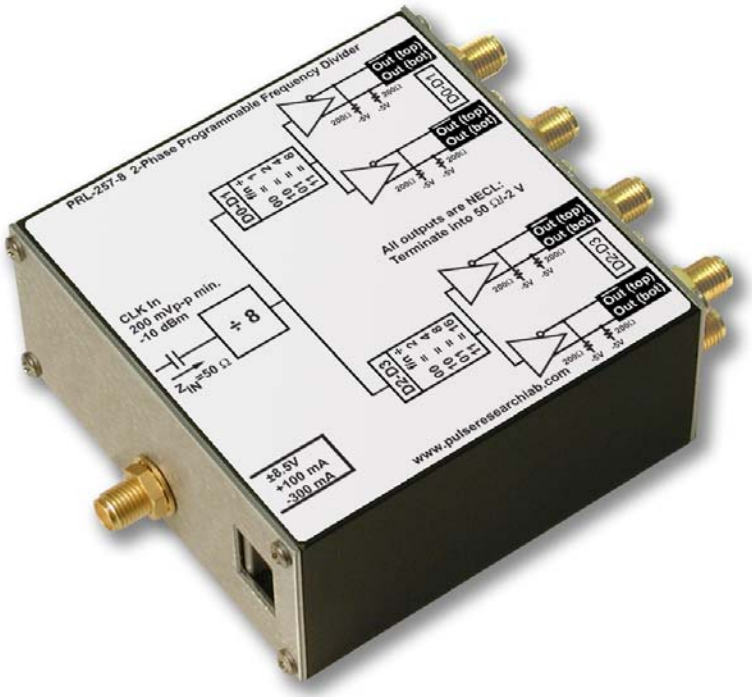
PRL-257-8, 12 GHz PROGRAMMABLE 2Φ FREQUENCY DIVIDER

APPLICATIONS

- Systems Clock Simulation
- Low Jitter NECL Clock Source
- SONET Clock Generator
- Laser Pump Synchronization
- Scope triggering
- PRBS/BERT synchronization
- Optimizing outputs from frequency synthesizers
- Testing high-speed serial/SERDES links (10 GB Ethernet, eSATA, PCIe, HT, etc)
- An Essential Lab Tool for Working with ECL Circuits



FEATURES

- 12 GHz typical maximum External Clock Input frequency
- f/8 to f/128 with independent 2Φ outputs
- Common Divide by 8 pre-scalar for both Φ1 and Φ2
- Φ1 output=(f/8)/(1, 2, 4 or 8), for max. ratio of 64
- Φ2 output=(f/8)/(2, 4, 8 or 16), for max. ratio of 128
- Both Φ1 and Φ2 have two pairs of complementary NECL square wave outputs
- Single-ended AC Coupled Input with internal 50 Ω terminations
- 5 ps typical Edge Jitter
- 40 ps typical skew between f/n & $\overline{f/n}$ NECL outputs
- Complementary DC coupled NECL Outputs drive 50 Ω loads terminated to -2V, AC-coupled or floating 50 Ω loads
- SMA I/O Connectors
- Ready-to-Use 1.3 x 2.9 x 2.9-in. Module includes a ±8.5V AC/DC Adapter

DESCRIPTION

The PRL-257-8 is an AC-coupled input, manually programmable, two phase frequency divider with two sets of complementary NECL outputs. It is capable of running at input frequencies in excess of 12 GHz.

It has a common divide-by-8 pre-scalar front end followed by two banks of independent manually programmable dividers, Φ1and Φ2. The f/8 pre-scalar output is further divided by 1, 2, 4, or 8 for the Φ1 bank via D0 and D1 of a two-bit DIP switch, providing a maximum ratio of 64. It is divided by 2, 4, 8 or 16 for the Φ2 bank via D2 and D3 of a second two-bit DIP switch, providing a maximum ratio of 128. All outputs are synchronous with the input frequency and are square waves (50% duty cycle) suitable for driving long lines terminated into 50 Ω/-2 V or AC-coupled 50 Ω loads.

The PRL-257 is ideal for applications where a high frequency divider or pre-scalar is needed for triggering or down-sampling. The two phases of output enable applications requiring two different ratios from a common reference frequency, and the 1:2 fanout feature enables system synchronization and monitoring/triggering applications from a single reference clock source. Applications for the PRL-257 include data acquisition, test, measurement, R&D, and system integration.

The unit includes an AC adapter for ready-to-use convenience on the bench or in a system. All I/O connectors are SMA. The extruded aluminum housing is suitable for mounting with the optional brackets.

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*SPECIFICATIONS (0^o C ≤ T_A ≤ 35^oC)

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R_{in}	External Clock Input Resistance		50		Ω	AC Coupled
Cc	Input Coupling Capacitor	0.08	0.10	0.12	µf	Input TC=50 µs
V_{INmin}	Minimum p-p Input Amplitude	500 350 100	400 250 50		mV	Sine Wave@ f_{min} In I Square Wave, tr <2ns Square Wave, tr <500ps
V_{INmax}	Maximum p-p Input Amplitude		2	1.25	V	Sine or Square Wave
V_{OL}	Output Lo Level @ 100MHz	-1.95	-1.6	-1.48	V	Output terminated to 50 Ω/-2V
V_{OH}	Output Hi Level @ 100MHz	-1.13	-0.9	-0.81	V	Output terminated to 50 Ω/-2V
I_{DC}	DC Input Current		+80/ -285	+100/ -300	mA	
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	V	
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V	PRL-760 series Adapter
t_{PLH1}	Propagation Delay from Input to Φ1 output ↑		2500		ps	
t_{PLH2}	Propagation Delay from Input to Φ2 output ↓		2500		ps	
t_r/t_fl	Rise/Fall Times (20%-80%), NECL outputs		200	250	ps	Note (1)
t_{SKEW1}	Skew↔ Φ1 or Φ2 outputs		40	120	ps	
t_{SKEW2}	Skew↔ Φ1 and Φ2 outputs		40	120	ps	D0/D1=10, D2/D3=00
	Jitter, p-p		5	10	ps	
$f_{min\ In\ I}$	Minimum Input frequency	120	100		MHz	Sine Wave Input
$f_{min\ In\ II}$	Minimum Input frequency	150	100		KHz	Square Wave Input, tr <2ns
$f_{max\ In}$	Max Input clock frequency	10	12	12.5	GHz	
$f_{max\ Out}$	Max Output frequency	1.25 0.625	1.5 0.75	1.56 0.78	GHz	Φ1 Outputs Φ2 Outputs
	Size	1.3 x 2.9 x 2.9			in.	
	Weight	10			Oz	

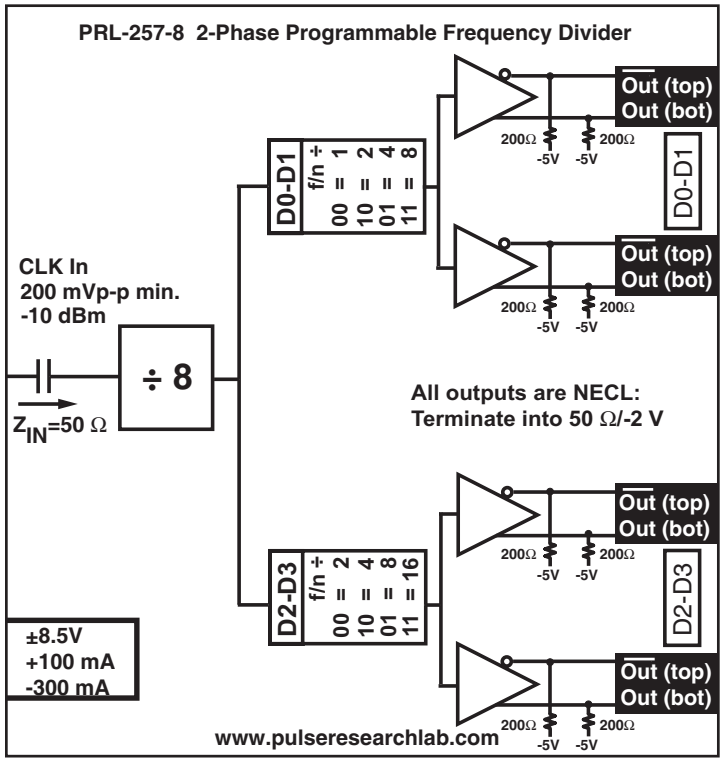

Fig. 1 PRL-257-8 Functional Block Diagram

*All dynamic NECL measurements are made with outputs terminated into 50 Ω/-2 V, using the PRL-550NQ4X, four-channel NECL Terminator, connected to a 50 Ω input sampling oscilloscope.

Notes:
(1) The output rise and fall times of each NECL channel are measured with its complementary output terminated into 50 Ω/-2 V. An unused complementary 50 Ω output must be either terminated into 50 Ω/-2 V or AC coupled into a 50 Ω load; otherwise, output waveform distortion and rise time degradation will occur. Use the PRL-ACT-50, Dual Ch. AC-Coupled 50 Ω Termination, for the AC coupled termination. Use the PRL-SC-104 or PRL-ACX-12dB (0.1 µf DC block and 12 dB AC-coupled attenuator, respectively) for connection of NECL signals to 50 Ω input oscilloscopes.

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