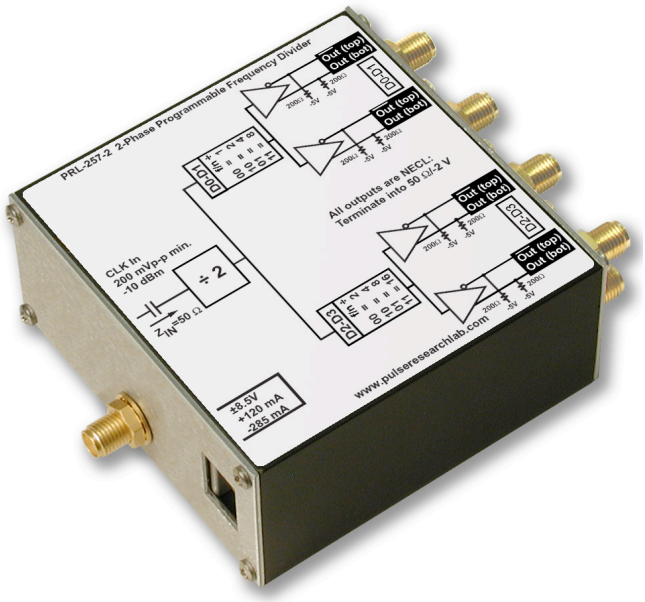
PRL-257-2 6 GHz PROGRAMMABLE 2φ FREQUENCY DIVIDER

APPLICATIONS

- Systems Clock Simulation
- Low Jitter NECL Clock Source
- SONET Clock Generator
- Scope triggering
- PRBS/BERT synchronization
- Optimizing outputs from frequency synthesizers
- Testing high-speed serial/SERDES links
- An Essential Lab Tool for Working with ECL Circuits



FEATURES

- 6.6 GHz maximum External Clock Input frequency
- f/2 to f/32 with independent 2φ outputs
- Common Divide by 2 pre-scalar for both φ1 and φ2
- φ1 output=(f/2)/(1, 2, 4 or 8), for max. ratio of 16
- φ2 output=(f/2)/(2, 4, 8 or 16), for max. ratio of 32
- Both φ1 and φ2 have two pairs of complementary NECL square wave outputs
- Single-ended AC Coupled Input with internal 50 Ω terminations
- 5 ps typical Edge Jitter
- 40 ps typical skew between f/n & $\overline{f/n}$ NECL outputs
- Complementary DC coupled NECL Outputs drive 50 Ω loads terminated to -2 V, AC coupled or floating 50 Ω loads
- SMA I/O Connectors
- Ready-to-Use 1.3 x 2.9 x 2.9-in. Module includes a ±8.5V AC/DC Adapter

DESCRIPTION

The PRL-257-2 is an AC-coupled input, manually programmable, two phase frequency divider with two sets of complementary NECL outputs. It is capable of running at input frequencies in excess of 6.6 GHz.

It has a common divide-by-2 pre-scalar front end followed by two banks of independent manually programmable dividers, φ1and φ2. The f/2 pre-scalar output is further divided by 1, 2, 4, or 8 for the φ1 bank via D0 and D1 of a two-bit DIP switch, providing a maximum ratio of 16. It is divided by 2, 4, 8 or 16 for the φ2 bank via D2 and D3 of a second two-bit DIP switch, providing a maximum ratio of 32. All outputs are synchronous with the input frequency and are square waves (50% duty cycle) suitable for driving long lines terminated into 50 Ω/-2 V or AC-coupled 50 Ω loads.

The PRL-257-2 is ideal for applications where a high frequency divider or pre-scalar is needed for triggering or down-sampling. The two phases of output enable applications requiring two different ratios from a common reference frequency. Applications for the PRL-257-2 include data acquisition, test, measurement, R&D, and system integration.

The unit includes an AC adapter for ready-to-use convenience on the bench or in a system. All I/O connectors are SMA. The extruded aluminum housing is suitable for mounting with the optional brackets.

PULSE RESEARCH•LAB

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com

*SPECIFICATIONS (0^o C ≤ T_A ≤ 35^oC)

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R_{in}	External Clock Input Resistance		50		Ω	AC Coupled
Cc	Input Coupling Capacitor	0.08	0.10	0.12	uf	Input TC=50 µs
I_{DC}	DC Input Current		+120/ -285	+135/ -300	mA	
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	V	
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V	
V_{INmin}	Minimum p-p Input Amplitude	500 350 100	400 250 50		mV	Sine Wave@ f_{min} In I Square Wave, t_r <2 ns Square Wave, t_r <500 ps
V_{INmax}	Maximum p-p Input Amplitude		2.0	1.25	V	Sine or Square Wave
V_{OH}	Output Hi Level @ 100MHz	-1.13	-0.9	-0.81	V	Output terminated to 50 Ω/-2 V
V_{OL}	Output Lo Level @ 100MHz	-1.95	-1.6	-1.48	V	Output terminated to 50 Ω/-2 V
t_{PLH1}	Propagation Delay from Input to φ1 output ↑		2500		ps	
t_{PLH2}	Propagation Delay from Input to φ2 output ↑		2500		ps	
t_r/t_fl	Rise/Fall Times (20%-80%), NECL outputs		200	250	ps	Note (1)
t_{SKEW1}	Skew ↔ φ1 or φ2 outputs		40	120	ps	
t_{SKEW2}	Skew ↔ φ1 and φ2 outputs		40	120	ps	D0/D1=10, D2/D3=00
	Peak to peak Jitter		5	10	ps	
f_{min} In I	Minimum Input frequency	120	100		MHz	Sine Wave Input
f_{min} In II	Minimum Input frequency	150	100		KHz	Square Wave Input, t_r < 2 ns
f_{max} In	Max Input clock frequency	6	6.6		GHz	
f_{max} Out	Max Output frequency	3 1.5	3.3 1.65		GHz	φ1 Outputs φ2 Outputs
	Size	1.3 x 2.9x 2.9			in.	
	Weight	10			Oz	

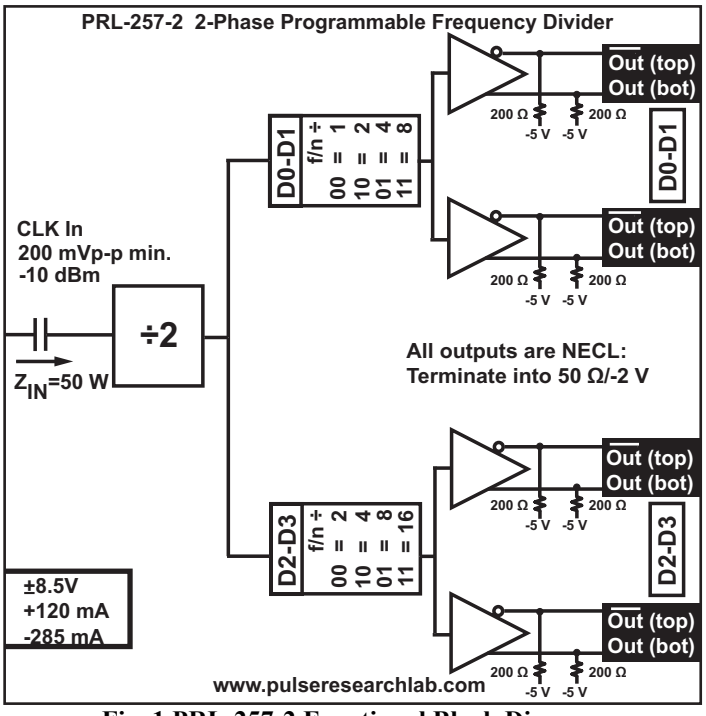


Fig. 1 PRL-257-2 Functional Block Diagram

*All dynamic NECL measurements are made with outputs terminated into 50 Ω/-2 V, using the PRL-550NQ4X, four-channel NECL Terminator, connected to a 50 Ω input sampling oscilloscope.

Notes:
(1) The output rise and fall times of each NECL channel are measured with its complementary output terminated into 50 Ω/-2 V. An unused complementary 50 Ω output must be either terminated into 50 Ω/-2 V or AC coupled into a 50 Ω load; otherwise, output waveform distortion and rise time degradation will occur. Use the PRL-ACT-50, Dual Ch. AC-Coupled 50 Ω Termination, for the AC coupled termination. Use the PRL-SC-104 or PRL-ACX-12dB (0.1 µf DC block and 12 dB AC-coupled attenuator, respectively) for connection of NECL signals to 50 Ω input oscilloscopes.

PULSE RESEARCH•LAB

1234 Francisco Street, Torrance, CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com