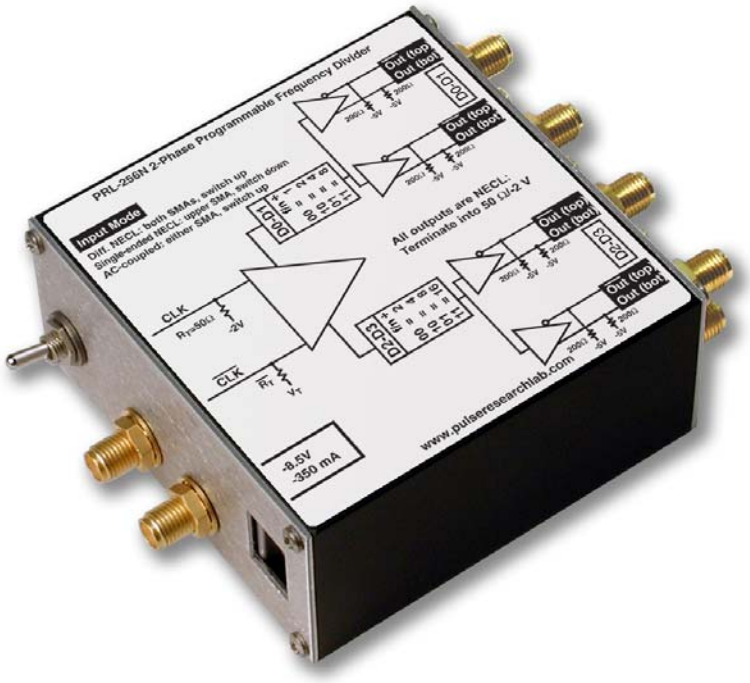
PRL-256N, 2+ GHz PROGRAMMABLE 2Φ NECL FREQUENCY DIVIDER

APPLICATIONS

- System Clock Simulation
- Low Jitter NECL Clock Source
- SONET Clock Generator
- Laser Pump Synchronization
- Scope triggering
- PRBS/BERT synchronization
- Optimizing outputs from frequency synthesizers
- Testing high-speed serial/SERDES links (GB Ethernet, eSATA, PCIe, HT, etc)



FEATURES

- 2+ GHz typical maximum External Clock Input frequency
- f/1 - f/16 outputs with independent 2Φ outputs
- Φ1 output=f/1, 2, 4 or 8
- Φ2 output=f/2, 4, 8 or 16
- Both Φ1 and Φ2 have two pairs of complementary NECL outputs
- Square wave (50% duty cycle) outputs (except f/1)
- Internal 50 Ω/-2V Input Terminations also accept AC-coupled PECL or sinewave signals
- 10 ps typical Edge Jitter
- 40 ps typical skew between f/n & $\overline{f/n}$ NECL outputs (each phase)
- Complementary DC coupled NECL Outputs drive 50 Ω loads terminated to -2V, AC coupled or floating 50 Ω loads
- SMA I/O Connectors
- Ready-to-Use 1.3 x 2.9 x 2.9-in. Module includes a ±8.5V AC/DC Adapter

DESCRIPTION

The PRL-256N is an ECL input, manually programmable, two-phase frequency divider with four pairs of complementary NECL outputs, capable of running at input frequencies in excess of 2 GHz. The input selector switch selects either single-ended or differential inputs. In the differential input mode, both inputs CLK and $\overline{CLK}$ are terminated internally into 50 Ω/V_{TT}, where V_{TT} is equal to -2V for NECL, and therefore, either one or both inputs can accept AC coupled signals as well. In the single input mode, input signals should be connected to the CLK input only. The $\overline{CLK}$ input is internally switched to V_{BB}, nominally -1.3 V for NECL, and the input resistor $\overline{R}_T$ for the $\overline{CLK}$ input channel is changed to 62 Ω.

The input buffer is followed by two banks of independent manually programmable dividers, Φ1 and Φ2. The input is divided by 1, 2, 4, or 8 for the Φ1 bank via D0 and D1 of a two-bit DIP switch. It is divided by 2, 4, 8 or 16 for the Φ2 bank via D2 and D3 of a second two-bit DIP switch. Each bank has two pairs of complementary outputs. All outputs are synchronous with the input frequency and are square waves (50% duty cycle) except for the f/1 outputs, which follow the input. The outputs are suitable for driving long lines terminated into 50 Ω/-2 V or AC-coupled 50 Ω loads.

The PRL-256N is ideal for applications where a high-frequency divider or pre-scalar is needed for triggering or down-sampling. The two phases of output enable applications requiring two different ratios from a common reference frequency, and the 1:2 fanout feature enables system synchronization and monitoring/triggering applications from a single reference clock source. Applications for the PRL-256N include data acquisition, test, measurement, R&D, and system integration.

The unit includes an AC adapter for ready-to-use convenience on the bench or in a system. All I/O connectors are SMA. The extruded aluminum housing is suitable for mounting with the optional brackets.

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*SPECIFICATIONS (0^{o} C ≤ T_A ≤ 35^{o}C)

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R_{in}	Input Resistance	49.5	50	50.5	Ω	
V_{TT}	D Input Termination Voltage	-2.2	-2	-1.8	V	CLK input
V_T	$\overline{D}$ Input Termination Voltage	-1.17/-2.2	-1.3/-2	-1.43/-1.8	V	$\overline{CLK}$ input
V_{IL}	Input Lo Voltage	-1.95	-1.6	-1.48	V	
V_{IH}	Input Hi Voltage	-1.13	-0.9	-0.81	V	
SW Vin	Sinewave Input p-p	30	50	500	mV	
V_{OL}	Output Lo Voltage	-1.95	-1.6	-1.48	V	
V_{OH}	Output Hi Voltage	-1.13	-0.9	-0.81	V	
I_{DC}	DC Input Current		-350	-375	mA	
V_{DC}	DC Input Voltage	-7.5	-8.5	-12	V	
V_{AC}	AC/DC Adapter Input Voltage	103	115	127	V	
T_{PLH}	Propagation Delay to output ↑		2500		ps	
T_{PHL}	Propagation Delay to output ↓		2500		ps	
t_r/t_f	Rise/Fall Times (20%-80%)		200	300	ps	Note (1)
t_{SKEW1}	Skew↔ Φ1 or Φ2 outputs		40	120	ps	
t_{SKEW2}	Skew↔ Φ1 and Φ2 outputs		40	120	ps	D0/D1=10, D2/D3=00
T_{SKEW}	Skew between any 2 outputs		40		ps	
F_{MAX}	Max clock frequency	2.0	2.5		GHz	
	Size	1.3 x 2.9 x 2.9			in.	
	Weight	5			Oz	
	Shipping weight including AC adapter	3			lb	

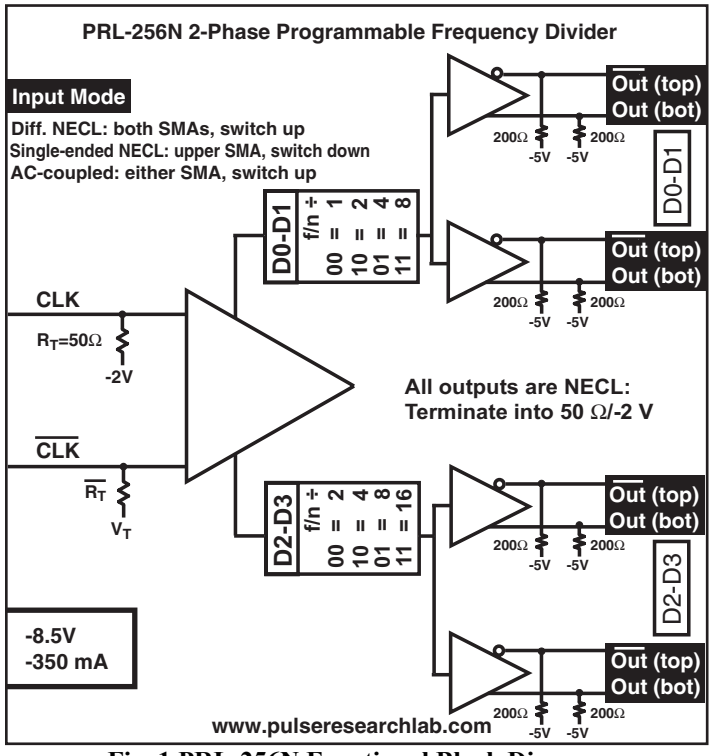

Fig. 1 PRL-256N Functional Block Diagram

*All dynamic NECL measurements are made with outputs terminated into 50 Ω/-2 V, using the PRL-550NQ4X, four-channel NECL Terminator, connected to a 50 Ω input sampling oscilloscope.

Notes:
(1) The output rise and fall times of each NECL channel are measured with its complementary output terminated into 50 Ω/-2 V. An unused complementary 50 Ω output must be either terminated into 50 Ω/-2 V or AC coupled into a 50 Ω load; otherwise, output waveform distortion and rise time degradation will occur. Use the PRL-ACT-50, Dual Ch. AC-Coupled 50 Ω Termination, for the AC coupled termination. Use the PRL-SC-104 or PRL-ACX-12dB (0.1 µf DC block and 12 dB AC-coupled attenuator, respectively) for connection of NECL signals to 50 Ω input oscilloscopes.

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