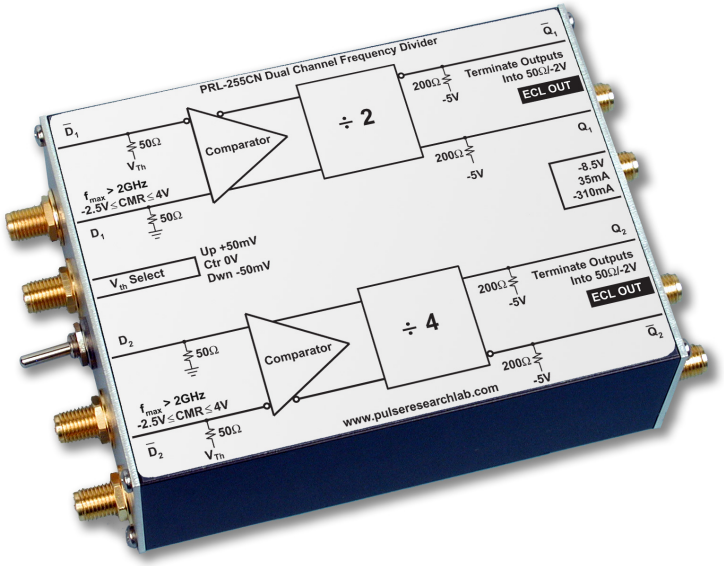
PRL-255CN ÷2 and ÷4 SMALL SIGNAL FREQUENCY DIVIDER

APPLICATIONS

- GHz Frequency Division in Device Test and Systems Integration
- Small Signal Sine wave/Square wave Frequency Division
- High speed Clock signal Generation for SONET applications
- An Essential Lab Tool for Engineering and Production Test



PRL-255CN

FEATURES

- 2.4 GHz Typical Maximum Toggle Frequency
- Comparator Inputs with ±50 mV or 0 V Preset Threshold
- -2.5 V to +4 V Input Common Mode Range
- Complementary ECL Outputs drive 50 Ω Loads terminated to -2V, AC Coupled or floating 50Ω Loads
- 10mV p-p Minimum Input @ 300MHz
- DC Coupled I/O's
- SMA I/O Connectors
- Ready-to-Use 1.3 x 2.9 x 3.9-in. Module includes a ±8.5V AC/DC Adapter

DESCRIPTION

The PRL-255CN is a dual-channel ÷2 and ÷4 frequency divider with DC-coupled, 50 Ω comparator inputs, and complementary NECL outputs. The maximum frequency of operation is greater than 2 GHz, and the minimum input signal required is 10 mV p-p at 300 MHz. It is ideally suited for dividing mV sine wave signals. The module can also provide a ÷8 function by cascading the two channels using AC coupling. The NECL outputs are designed for driving 50 Ω loads terminated to –2 V, AC coupled or floating 50 Ω loads. The PRL-255CN is an Mini-Modular Instrument™ for device test and for system integration in wireless and digital communications applications.

The comparator input threshold voltage can be set to +50 mV, 0 V or –50 mV using the common three-position switch provided. It can also be varied independently in each channel by applying a DC bias voltage to one of the two inputs. In this case, a feed through decoupling capacitor of 0.1 µf, such as the PRL-FTC-104, is recommended for preventing false triggering or oscillation, if the bias voltage contains varying components, such as noise. The Input Common Mode Range is -2.5 V to +4 V. To prevent oscillation in a non-driven channel when the preset threshold is set to 0 V, connect an output to an input so that the two inputs are not at the same voltage.

The PRL-255CN is housed in a 1.3 x 2.9 x 3.9-in. extruded aluminum enclosure and is supplied with a ±8.5 V/±1.8 A AC/DC Adapter. A block diagram of the PRL-255CN is shown in Fig. 1.

If mounting is desired, a pair of 35001420 mounting brackets can accommodate two PRL modules of the same length. A number of PRL modules can also share a single ±8.5V AC/DC adaptor using the PRL-730 voltage distribution module. Please see the Accessories Section for more detail.

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SPECIFICATIONS* (0^{o} C ≤ T_A ≤ 35^{o}C)

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R_{in}	Input Resistance	49.5	50.0	50.5	Ω	
V_{th+}	Preset Positive threshold voltage	+40	+50	+60	mV	
V_{th-}	Preset negative threshold voltage	-60	-50	-40	mV	
$V_{th\ 0}$	Preset zero threshold voltage	-5	0	+5	mV	
Vin Min 1	Minimum input voltage p-p	10	5		mV	0 < f < 300 MHz
Vin Min 2	Minimum input voltage p-p	400	200		mV	300 MHz < f < 2.5 GHz
V_{OL}	Output Lo Voltage	-1.95	-1.70	-1.48	V	Into 50 Ω/-2 V
V_{OH}	Output Hi Voltage	-1.13	-0.90	-0.81	V	Into 50 Ω/-2 V
I_{DC1}	DC Input Current, +8.5 VDC		+35	+55	mA	
I_{DC2}	DC Input Current, -8.5 VDC		-310	-350	mA	
V_{DC}	DC Input Voltage	±7.5	±8.5	±12	V	
V_{AC}	AC/DC Adaptor Input Voltage	103	115	127	V	
t_{PLH} (÷2)	Propagation Delay to output ↑		1.8	2.2	ns	
t_{PHL} (÷2)	Propagation Delay to output ↓		1.8	2.2	ns	
t_{PLH} (÷4)	Propagation Delay to output ↑		2.0	2.5	ns	
t_{PHL} (÷4)	Propagation Delay to output ↓		2.0	2.5	ns	
t_r/t_f	Rise/Fall Times (20%-80%)		400	600	ps	Note (1)
t_{SKEW}	Skew between Q & $\overline{Q}$ outputs		50	150	ps	
f_{MAX}	Max clock frequency	2.0	2.5		GHz	Note (2)
V_{CMR}	Common Mode Range	-2.5		+4.0	V	
	Size	1.3 x 2.9 x 3.9			in.	
	Weight	5			Oz	

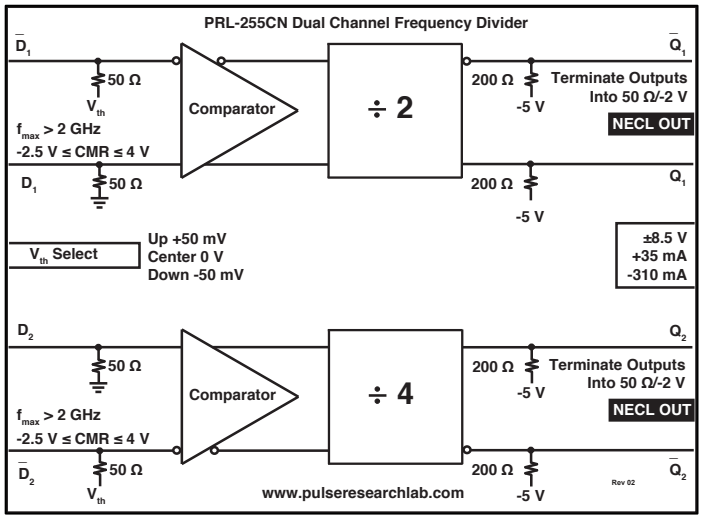

Fig. 1: PRL-255CN Block Diagram

*All measurements are made with outputs terminated into 50 Ω/-2 V, using the PRL-550NQ4X, four channel ECL Terminators, connected to a 50 Ω input sampling oscilloscope.

Notes:

(1). The output rise and fall times are measured with both the Q and $\overline{Q}$ outputs terminated into 50 Ω/-2 V. An unused complementary output should be either terminated into 50 Ω/-2 V or AC coupled into a 50 Ω load. Otherwise, output waveform distortion and rise time degradation will occur. Use the PRL-550ND4X and PRL-550NQ4X, two and four channel ECL Terminators, respectively, for the 50 Ω/-2 V termination and for connection of ECL signals to 50 Ω input oscilloscopes when DC level information is required. Otherwise, use the PRL-ACT-50, dual AC coupled 50 Ω Termination module, for the unused outputs and the PRL-SC-104 DC Block for connection to a 50Ω input oscilloscope.

A -12dB, AC coupled attenuator, can also be used for either terminating unused output or connection to a 50 Ω input oscilloscope.

(2) f_{MAX} is measured by AC coupling an ECL signal > 200 mV to the ÷2 CLK input, with the input threshold voltage set to zero. The ÷2 and ÷4 channels are cascaded using AC coupling and the ÷8 outputs are then measured. The f_{MAX} measurement is then repeated by clocking the ÷4 CLK input.

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