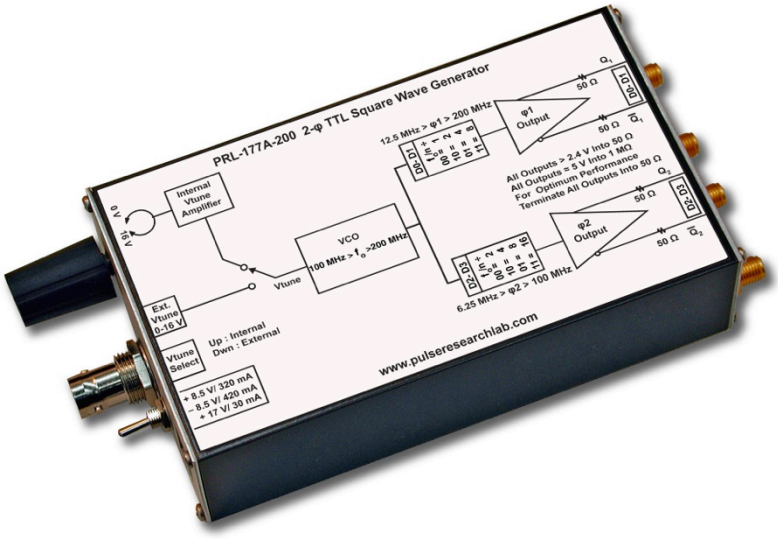
PRL-177A-200, TTL SQUARE WAVE GENERATOR with 2φ COMPLEMENTARY OUTPUTS



APPLICATIONS

- System Clock Simulation
- Split-Cycle Timing
- Low Jitter TTL Clock Sources
- Large Signal Amplifier Response Testing
- Filter Testing
- Two-Phase Clock Simulation
- Square Wave and Sine Wave Generation
- Essential Lab Tool for Working with TTL Circuits

FEATURES

- V_O typically = 5 V into 1 MΩ or 2.5 V into 50 Ω
- 750 ps output t_R/t_F typical
- 2φ complementary TTL square wave outputs
- φ1 output variable from < 12.5 MHz to > 200 MHz,
- φ2 output variable from < 6.25 MHz to > 100 MHz
- 50 Ω back-terminated outputs suitable for driving long lines without load terminations for $\mathbf{f_O}$ < 70 MHz
- Frequency jitter < 20 ps, and short term Δf < 0.1% and < 0.05% when controlled by an external precision DC source
- Four DC-coupled outputs with SMA Connectors
- BNC input connector for external voltage tuning
- Ready-to-Use 1.3 x 2.9 x 5.1-in. module includes a 8.5 V/±1.4 A, 17 V/150 mA AC/DC Adapter

DESCRIPTION

The PRL-177A-200 is a 200 MHz, 2φ, TTL square wave generator with two pairs of complementary 50 Ω back-terminated outputs. The internal VCO clock frequency $\mathbf{f_O}$ is continuously variable over one octave, from less than 100 MHz to greater than 200 MHz, controlled by a 10-turn pot. The VCO frequency can also be controlled over the same range using an external 0-16 V voltage source. The buffered VCO output $\mathbf{f_O}$ is connected to two independent 2-bit dividers for generating the 2φ outputs. φ1 divides $\mathbf{f_O}$ by 1, 2, 4 or 8, and provides output frequencies from less than 12.5 MHz to greater than 200 MHz. φ2 divides $\mathbf{f_O}$ by 2, 4, 8 or 16, and provides output frequencies from less than 6.25 MHz to greater than 100 MHz. Except for the $\mathbf{f_O}$/1 outputs from φ1 (D0 = D1 = 00), all outputs are nearly perfect square waves, as they are derived from outputs of binary dividers. The duty cycle of the $\mathbf{f_O}$/1 output is typically better than 55%/45%.

The PRL-177A-200 is a **M**ini **M**odular **I**nstrument (**MMI**) designed for everyday lab use. It is also a stable, low-jitter frequency source, covering the frequency range from less than 6.25 MHz to greater than 200 MHz. Its outputs (5 V/open circuit or 2.5 V/50 Ω) are ideally suited for testing CMOS/TTL circuits, amplifiers, discrete semiconductor devices, filters and other passive components, etc. The two sets of independent, complementary outputs are useful for split-cycle timing applications, sequential address simulation and for scope triggering or frequency monitoring using a counter. The PRL-177A-200 can also generate sine waves when used with a 7-pole low-pass Chebyshev filter built from a PRL Signal Conditioning Kit. The output waveforms are shown in Figs. 6 and 7, where a 10 MHz and 5.2 MHz square waves are converted into sine waves (2.4 V_{P-P}) using the same filter. More information and links to filter calculators are available on our web site.

With its clean, sub-ns rise-time and precision 50 Ω back-terminated outputs, the PRL-177A-200 is also an ideal TDR signal generator when used with the PRL-812-TDR passive splitter. This type of simple TDR generator is very affordable, and is well suited for testing cable impedance and for measuring biased input terminations that cannot be measured using a DVM. It can also replace expensive and cumbersome pulse generators, occupying less than 20 square inches of bench space, in applications where simple clock signals are needed. With the addition of a DC block, the PRL-177A-200 outputs can be converted into a ±1.25 V bipolar output for testing amplifiers.

The PRL-177A-200 is housed in a 1.3 x 2.9 x 5.1-in. extruded aluminum enclosure and is supplied with a ±8.5 V, +17 V AC/DC Adapter.

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*SPECIFICATIONS: PRL-177A-200 (0° C ≤ T_A ≤ 35°C)

Unless otherwise specified, tests performed with all outputs terminated into 50 Ω.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
I_{DC1}	DC Input Current, +8.5 V*		+320	+335	mA	
I_{DC2}	DC Input Current, -8.5 V*		-410	-430	mA	
I_{DC3}	DC Input Current +17 V*		30	35	mA	
V_{DC1}	External DC Input Voltage 1	+7.5	+8.5	+12	V	
V_{DC2}	External DC Input Voltage 2	-12.0	-8.5	-7.5	V	
V_{DC3}	External DC Input Voltage 3	+19.0	+20.0	+22.0	V	
V_{AC}	AC Adapter Input Voltage	103	115	127	V	
V_{OH1}	Output Hi Level f ≤ 25 MHz		5		V	R_L = 1 MΩ
V_{OH2}	Output Hi Level 6.25 MHz ≤ f ≤ 200 MHz	2.4	2.5		V	R_L = 50 Ω
V_{OL1}	Output Lo Level f ≤ 25 MHz	-0.2	0	0.2	V	R_L = 1 MΩ
V_{OL2}	Output Lo Level 6.25 MHz ≤ f ≤ 200 MHz	-0.15	0	0.15	V	R_L = 50 Ω
t_R/t_F	Rise/Fall Times (10%-90%), all outputs		750	850	ps	@ 100 MHz
DC1	Q1 Duty Cycle @ 100 MHz		55	60	%	D0 = D1 = 00
DC2	Duty Cycle, All Outputs, (D0 ≠ 0 || D1 ≠ 00)		50		%	All settings
VCO f_{MAX}	Internal VCO maximum frequency	200	214		MHz	D0 = D1 = 00
VCO f_{MIN}	Internal VCO minimum frequency	100	86		MHz	D0 = D1 = 00
$f_{MAX}\varphi1$	φ1 Output maximum frequency	200	214		MHz	D0 = D1 = 00
$f_{MIN}\ \varphi1$	φ1 Output minimum frequency	12.50	10.75		MHz	D0 = D1 = 11
$f_{MAX}\varphi2$	φ2 Output maximum frequency	100	107		MHz	D2 = D3 = 00
$f_{MIN}\ \varphi2$	φ2 Output minimum frequency	6.250	5.375		MHz	D2 = D3 = 11
t_{SKEW1}	Skew ↔ Q1 and $\overline{Q1}$		< 100	< 250	ps	f = 100 MHz
t_{SKEW2}	Skew ↔ Q2 and $\overline{Q2}$		< 100	< 250	ps	f = 100 MHz
t_{SKEW3}	Skew ↔ Q1 and Q2		< 200	< 300	ps	f = 100 MHz
Δf	1 Hr. Frequency Stability, 23 °C ≤ T_A ≤ 25 °C		< 0.1		%	1 hr warm up
JPPKPK	Period Jitter peak to peak		20	40	ps	
	Enclosure Size		1.3 x 2.9 x 5.1		in.	
	Weight		8		Oz	

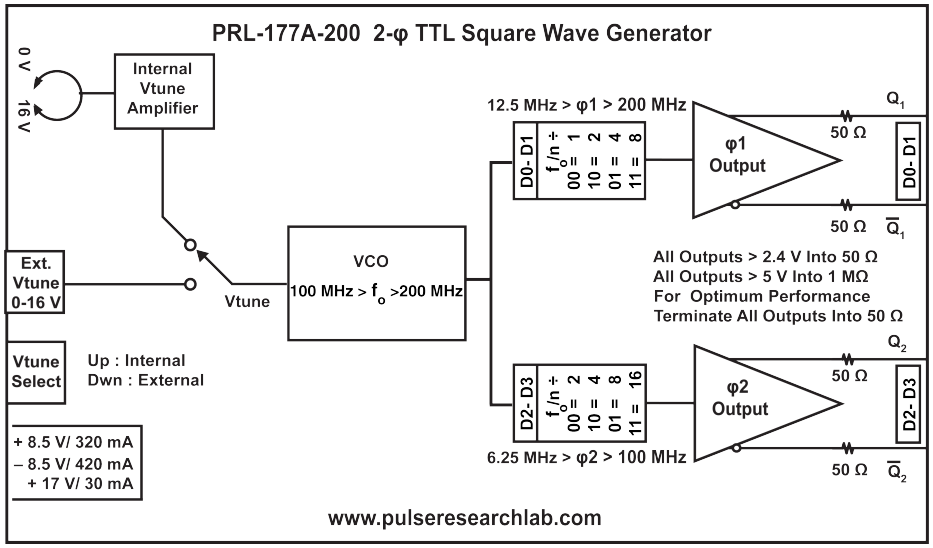

Fig. 1: PRL-177A-200 Functional Block Diagram

*These are the specified, fully loaded, unregulated output voltages from the PRL-760B or PRL-760C AC adapters. For non-fully loaded conditions, these voltages may be ±10 V and +20 V.

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PRL-177A-200 Output Waveforms

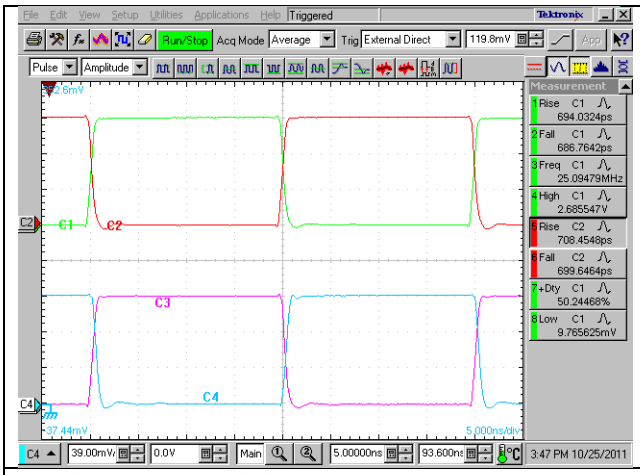

Fig. 2: All outputs @ 25 MHz

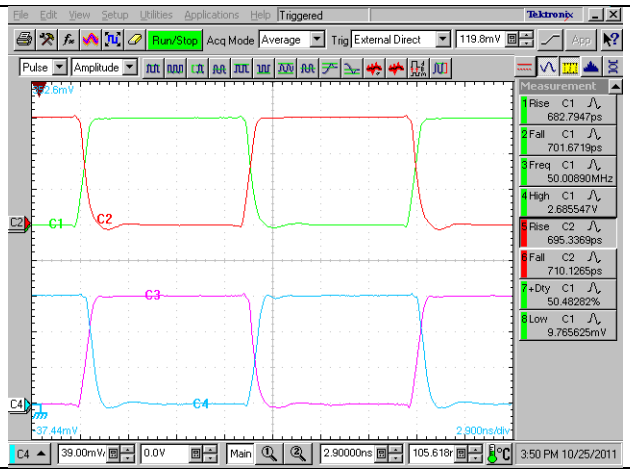

Fig. 3: All Outputs @ 50 MHz

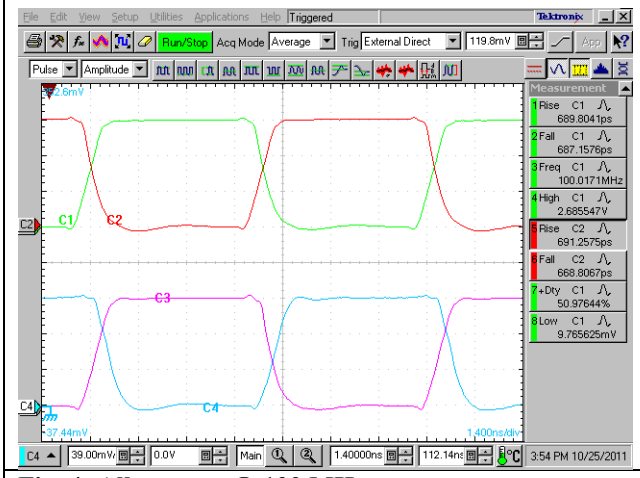

Fig. 4: All outputs @ 100 MHz

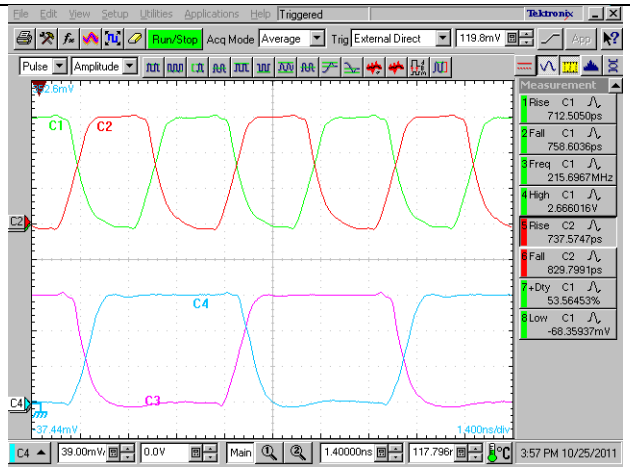

Fig. 5: Q1/ $\overline{Q1}$ @ 215 MHz, Q2/ $\overline{Q2}$ @ 107.5 MHz

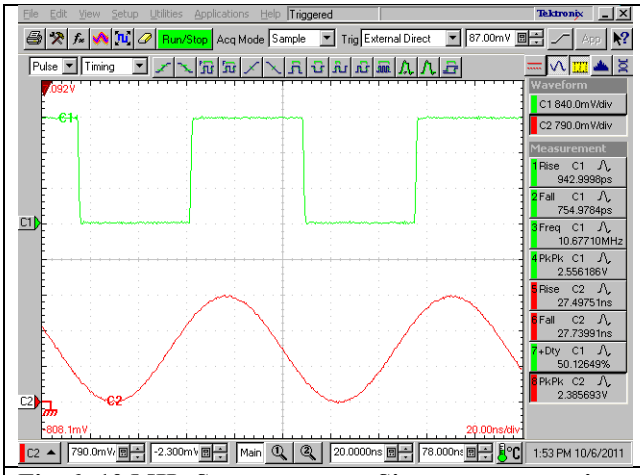

Fig. 6: 10 MHz Square wave to Sine wave conversion

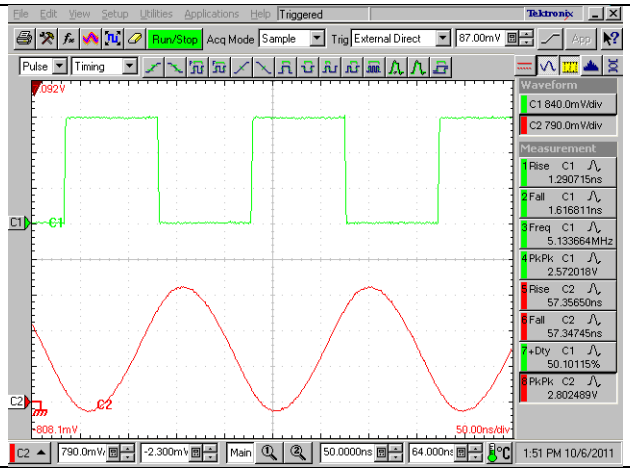

Fig. 7: The same filter is usable down to 5.14 MHz

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TDR Wave Forms obtained using the PRL-177A-200 and the PRL-812-TDR Splitter. More information regarding the PRL-177A-200/PRL-812-TDR set up will be available from the web site (see ***An Affordable TDR Generator*** app note).

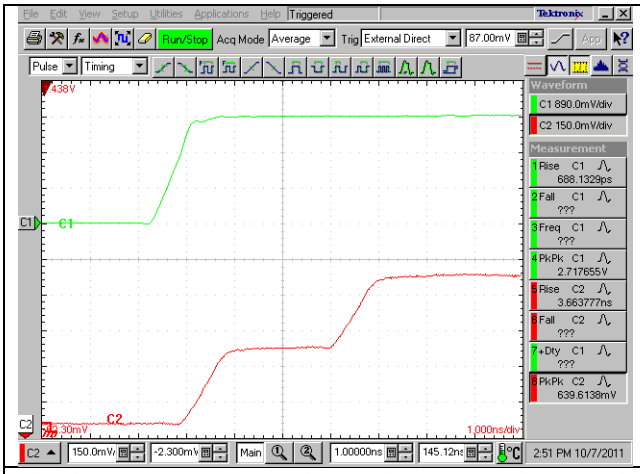

Fig. 8: TDR output waveform with an open line termination

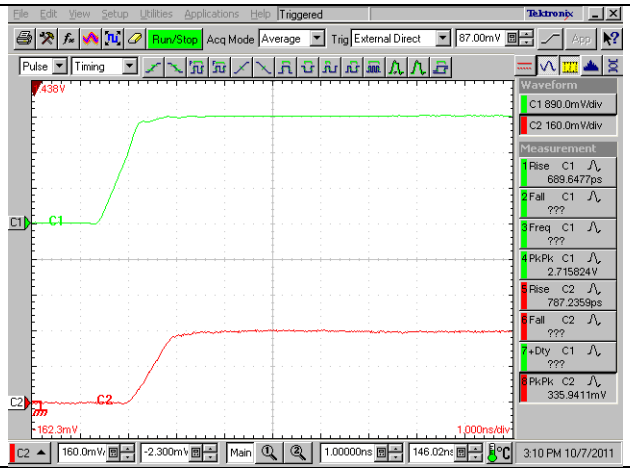

Fig. 9: TDR output waveform with a high quality, wideband 50 Ω termination

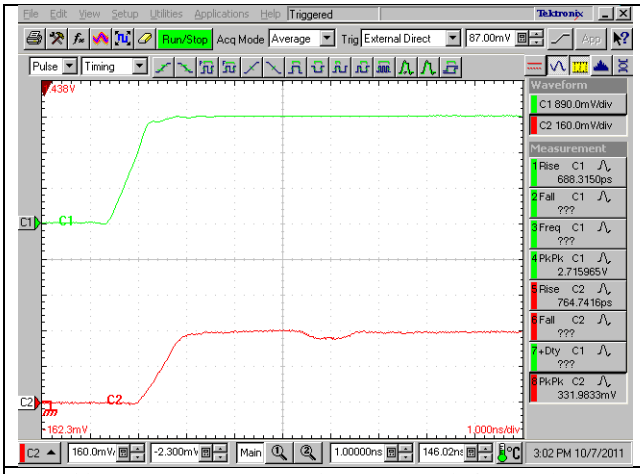

Fig. 10: TDR output waveform with 50 Ω termination having a small // capacitive component

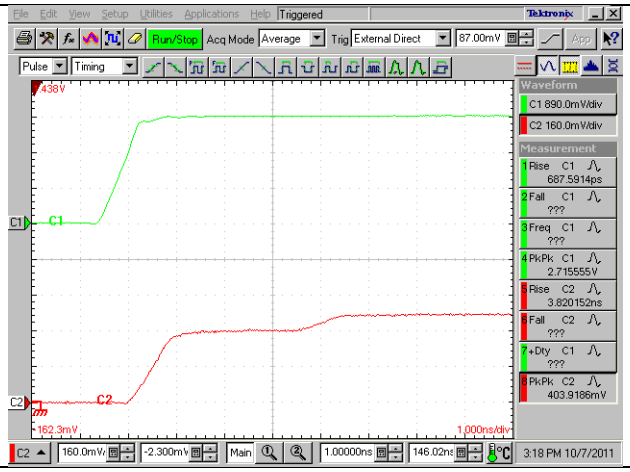

Fig. 11: TDR output waveform with an open ended 6 dB attenuator (83.3 Ω)

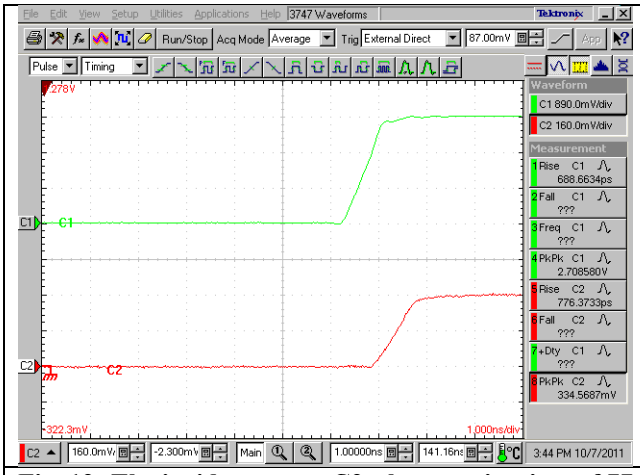

Fig. 12: The incident wave, C2, shows a rise time of 776 ps

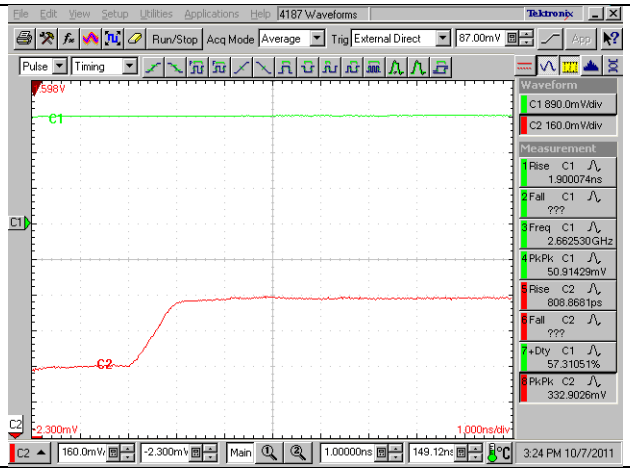

Fig. 13: The reflected wave, C2, shows a rise time of 809 ps

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