PRL-420ND-S20 TWENTY CHANNEL TTL TO DIFFERENTIAL NECL LOGIC LEVEL TRANSLATOR SYSTEM

APPLICATIONS

- Converting TTL/CMOS signals to Differential NECL Signals
- High Speed Digital Communications system Testing
- High Speed SONET Clock Level Translation
- Converting TTL/CMOS Clocks to NECL Clocks for connection to Transient Recorders

PRL-420ND-S20 Front View

FEATURES

- f_{max} > 300 MHz
- 900ps tr
- 50Ω TTL/CMOS Input, 1V Input Threshold
- Complementary NECL/Outputs
- DC Coupled BNC I/O Connectors
- Self-contained 5.25 x 19 x 22-in. rack-mountable unit including internal power supply

PRL-420ND-S20 Rear View

DESCRIPTION

The PRL420ND-S20 is a twenty channel TTL/CMOS to differential NECL Logic Level Translator system. It contains ten PRL-420ND dual channel TTL to NECL translator modules mounted inside a 5.25 x 19 x 22-in rack-mountable chassis. All I/O's from the modules are connected to the rear panel BNC connectors with equal length 50Ω coaxial cables. It contains an internal power supply that operates from standard 120V AC input.

Each channel has a 50Ω CMOS/TTL compatible input that can be triggered with less than 1.5V of signal. The complementary NECL outputs can drive 50Ω loads terminated to -2V, AC coupled or floating 50Ω loads. The basic block diagram of the individual module is shown in Fig. 1.

These Logic Level Translators are designed specifically for use in testing and interfacing of high speed digital communications circuits, where conversion from TTL/CMOS level signals to NECL level signals is often required. The PRL420ND-S20 is part of the **B**asic **L**aboratory **T**ools family that find increasing applications in high speed digital data recording instruments, Transient recording instruments and other high speed measurement equipment where NECL inputs are often specified.

PULSE RESEARCH LAB
1234 Francisco Street Torrance CA 90502
Tel: 310-515-5330 Fax: 310-515-0068
Email: sales@pulseresearchlab.com
www.pulseresearchlab.com

*SPECIFICATIONS (0^{o} C ≤ T_A ≤ 35^{o}C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50Ω/-2V

SYMBOL	PARAMETER	Min	Typ	Max	UNIT
R_{in}	Input Resistance	49.5	50	50.5	Ω
R_{out}	Output Resistance		NPN emitter		Ω
V_{TosL}	Input Threshold Voltage (Low)	0.9	1.0	1.1	V
V_{OL}	Output Low Level	-1.85	-1.7	-1.55	V
V_{OH}	Output High Level	-1.0	-0.8	-0.7	V
I_{DC}	DC Input Current		400 -1400		mA
V_{DC}	DC Input Voltage	±8	±8.5	±11	V
V_{AC}	AC/DC Adaptor Input Voltage	103	115	127	V
I_{AC}	AC Input current		0.5		A
t_{PLH}	Propagation Delay to output ↑		9	12	ns
t_{PHL}	Propagation Delay to output ↓		9	12	ns
t_r/t_f (1)	Rise/Fall Times (20%-80%)		850	1200	ps
t_{SKEW}	Skew: Vo↑↔ Vo↓		500	750	ps
t_{SKEW}	Skew: Vo1↑↔ Von↑		750	1000	ps
f_{max} (2)	Max Clock Frequency	250	300		MHz
	Size		5.25 x 19 x 22		in.
	Weight		12		lb

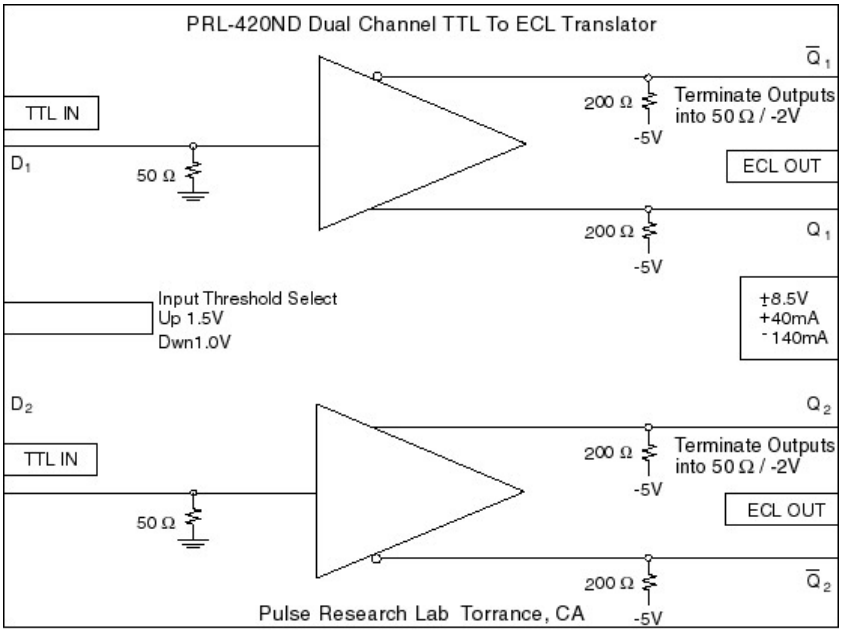

Fig. 1 PRL420ND Block Diagram

Notes:

(1). The output rise and fall times are measured with both the Q and $\overline{Q}$ outputs terminated into 50Ω/V_{TT}, using the PRL550NQ4X/ four channel ECL Terminators, connected to a 50Ω input sampling oscilloscope. V_{TT} =-2V for ECL and +3V for PECL. If either output is left unterminated, both the rise and fall times will increase by approximately 15%, due to slight degradation of the pulse corners.

(2). f_{MAX} is measured by connecting its inputs to the PRL450ND, ECL to TTL Logic Level Translator, and its outputs to the ÷2 differential inputs of the PRL-255N ECL frequency divider. The outputs of the PRL 255N are then measured using the PRL-550NQ4X, four channel ECL Terminators, connected to a 50Ω input sampling 'scope.