LGT900 Series TCXOs

1PPS-Disciplined, Software Compensated, Ultra-Low-G

Key Features

- As good as 0.01 ppb/g per axis
- +/- 0.5 ppb accuracy under lock
- As low as ±0.50 ppb over temp.
- Aging as low as +/- 100 ppb over 20 years
- Frequency Output to nearest 1 Hz

Common Applications

- GPS/GNSS
- Naval Vessels
- Commercial and Military Aircraft
- Smart Munitions
- Ground Vehicles
- Test Instruments
- Front-haul switches

Functional Description

The LGT900 Ultra-Low-G product family, is a 1 PPS-disciplined TCXO incorporating Esterline Research and Design's patented MSAC compensation architecture. This platform achieves frequency stability performance of less than ±2.00 ppb over the temperature range of -40°C to +85°C. The LGT900 design platform can deliver acceleration sensitivity performance of less than 0.01 ppb/g, translating into minimal phase noise degradation under vibration.

The LGT900 also offers other unique and performance-enhancing features such as vastly superior turn-on characteristics as compared to OCXO product offerings. A turn-on stability within +/-150 ppb of final frequency after 1 second of runtime is achieved before signal lock to nominal frequency. Superior aging options as low as +/-100 ppb over 20 years can be selected.

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Standard Specifications:

Parameter	Minimum	Typical	Maximum	Units	Notes
Operating Frequency	1		60	MHz	
Operational Temperature Range					See ordering Options
Frequency vs. Temperature					See ordering info for other options.
Calibration Tolerance			±50.0	ppb	At time of shipment: Free running
Frequency vs. Supply			±0.1	ppb	5% Change (CMOS Output)
Frequency vs Load			±0.25	ppb	5% Change (CMOS Output)
Frequency Accuracy in lock	-0.5	nominal	+0.5	ppb	At room temperature
Aging					
Supply Voltage	4.75	5.00	5.25	Volts	
Input Power			0.5	Watts	Steady State at +25 °C
CMOS Output Characteristics					Load = LVCMOS (15 pF)
Output Level High (Voh)		3.3		Volts	
Output Low (Vol)		0.1		Volts	
Duty Cycle	45	50	55	%	
Rise/Fall Time			6	ns	Measured between 10% and 90%
Sinewave Output Characteristics					Load = 50 Ω
Ourput Power	7	9	11	dBm	
Harmonics			-27	dBc	
Allan Deviation [4]		1.5E-11	TBD		Tau = 10 seconds (See Note 4, Page 3)
1pps Output		1		Hz	
Output Amplitude		3.3V			LVCMOS
Duty Cycle	45%	50%	55%		Firmware upgrade scheduled to make duty cycle programmable.
Rise/Fall Time		TBD			
Load		10MΩ || 10 pF			
1pps Input		1Hz			
Timing Edge		Rising Edge			
Input Amplitude		3.3V			LVCMOS
Input Impedance		10MΩ || 10 pF			
1pps Lock Pin Indicator					Can be locked up to 94 seconds before indicator goes HIGH
Oscillator Locked	2.85			Volts	LOAD = High Impedance; I_{OUT} < 5 mA
Oscillator NOT Locked			0.4	Volts	LOAD = High Impedance; I_{OUT} < 5 mA
Phase Noise Characteristics					Displayed phase noise at 10MHz.
1 Hz Offset		-80	-74	dBc/Hz	
10 Hz Offset		-108	-102	dBc/Hz	
100 Hz Offset		-127	-123	dBc/Hz	
1 KHz Offset		-148	-145	dBc/Hz	
10 KHz Offset		-154	-151	dBc/Hz	
100 KHz Offset		-154	-150	dBc/Hz	

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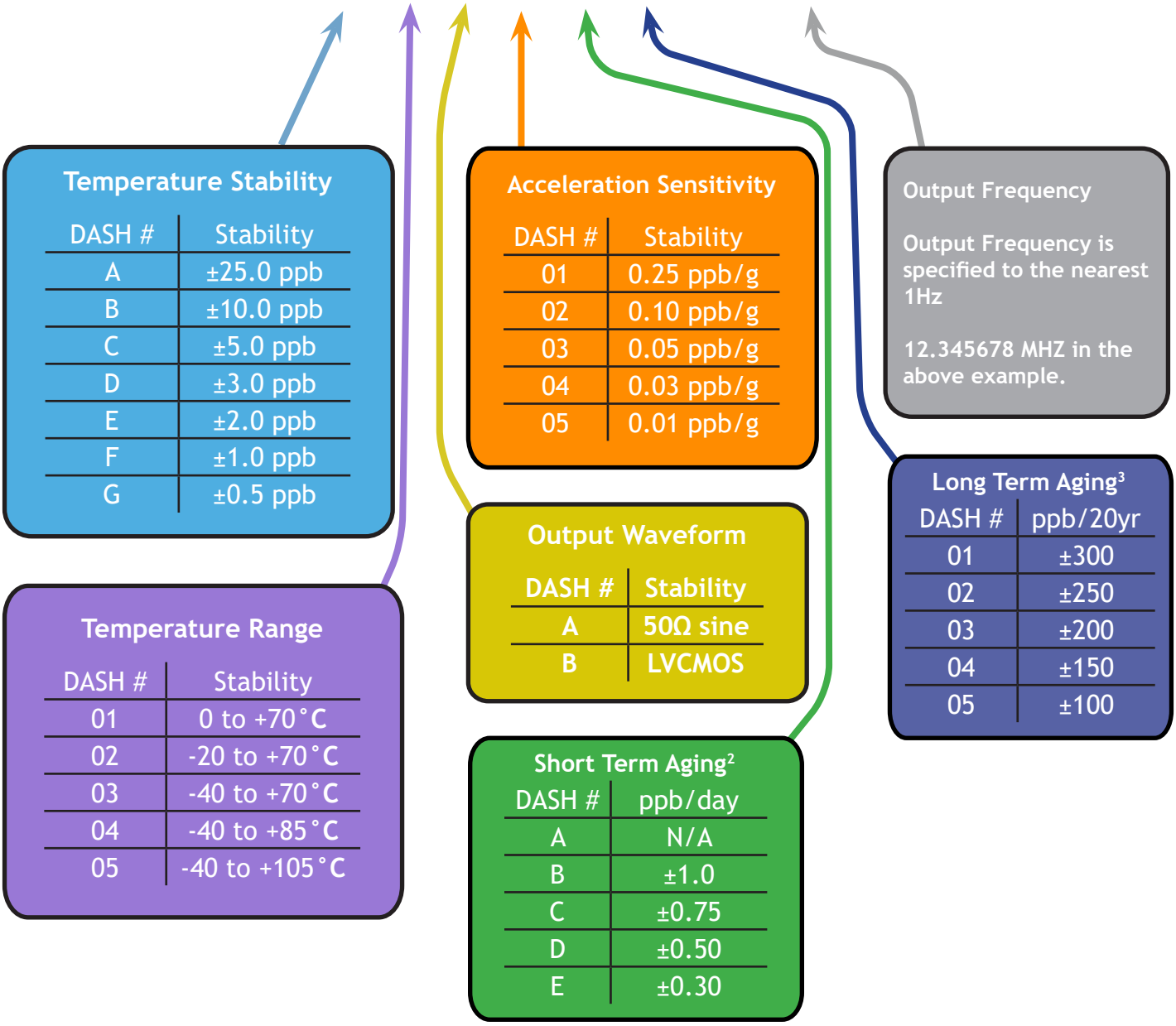
Ordering Information:

LGT900-A-01-A-01-A-01-12M345678



Temperature Stability

DASH #	Stability
A	±25.0 ppb
B	±10.0 ppb
C	±5.0 ppb
D	±3.0 ppb
E	±2.0 ppb
F	±1.0 ppb
G	±0.5 ppb

Acceleration Sensitivity

DASH #	Stability
01	0.25 ppb/g
02	0.10 ppb/g
03	0.05 ppb/g
04	0.03 ppb/g
05	0.01 ppb/g

Output Frequency

Output Frequency is specified to the nearest 1Hz

12.345678 MHZ in the above example.

Long Term Aging[3]

DASH #	ppb/20yr
01	±300
02	±250
03	±200
04	±150
05	±100

Output Waveform

DASH #	Stability
A	50Ω sine
B	LVCMOS

Temperature Range

DASH #	Stability
01	0 to +70°C
02	-20 to +70°C
03	-40 to +70°C
04	-40 to +85°C
05	-40 to +105°C

Short Term Aging[2]

DASH #	ppb/day
A	N/A
B	±1.0
C	±0.75
D	±0.50
E	±0.30

Notes:
1.) Not all combinations of options are available. Consult factory for additional guidance.
2.) Daily rate is measured after 30 days of continuous operation at 85°C.
3.) Long term aging is measured after 7 days of continuous operation at 85°C.
4.) ADEV measured after 2 hours of continuous operation at a constant temperature in still air.

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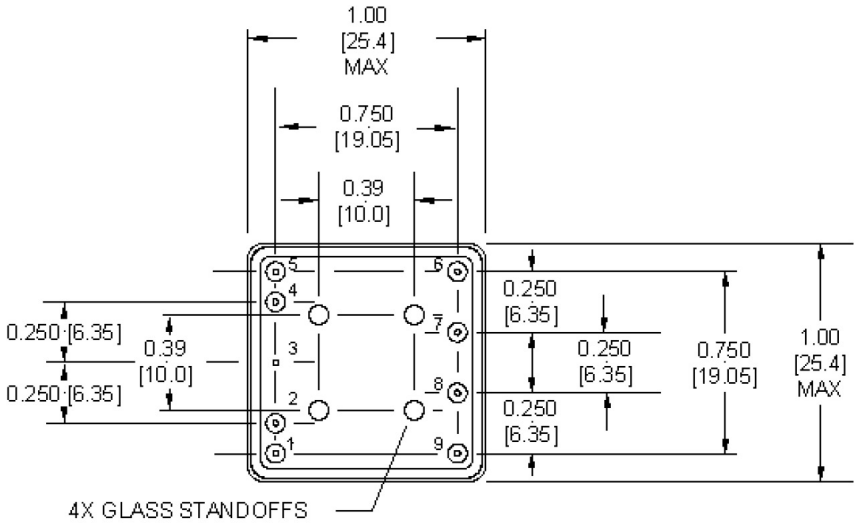
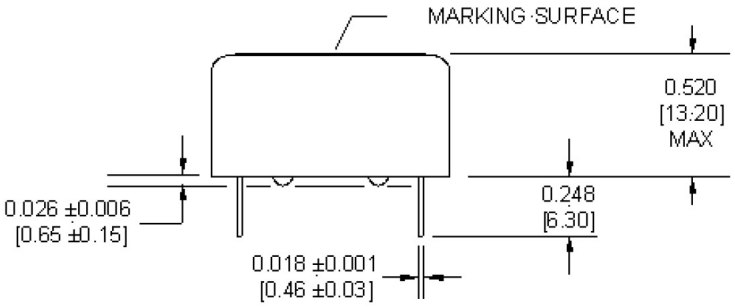
Mechanical Dimensions:

Bottom View:



Side View:



Notes:

1.) Dimensional Units: in [mm]
2.) Tolerance: ±0.004 in [±0.1 mm]
3.) Pin markings do not appear on the surfafce.
4.) Pins labeled "N/C" should be left floating.

Environmental Specifications		
Shock per MIL-STD-202	Survive	Method 213, Condition C
Vibration per MIL-STD-202	Survive	Method 204, Condition A

PIN FUNCTIONS	
Pin #	Function
1	RF Output
2	Serial Out
3	GROUND
4	Serial In
5	1PPS In
6	Lock Indicator
7	NC
8	1PPS Out
9	Supply Voltage

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