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FH3D12

SOFTWARE DEFINED DUAL 3D HALL SENSOR

DATASHEET

DATE	20.11.2023
EDITION	1
REVISION	1.03

CHANGELOG

Date / Edition / Revision	Changes
13.10.2023, Edition 1, Revision 1.00	Initial version
24.10.2023, Edition 1, Revision 1.01	Cosmetic Changes
17.11.2023, Edition 1, Revision 1.02	Magnetic specification updated
20.11.2023, Edition 1, Revision 1.03	Content revised

0 Content

1
FH3D12 Overview

1.1
General Description

The FH3D12 is a dual 3D Hall sensor based on Fraunhofer HallinOne® technology. This versatile magnetic field sensor uses pure Hall effect principle without magnetizable materials.
FH3D12 offers high dynamic magnetic range and accurate 3D magnetic field measurement at two positions 2 mm apart with a planar IC in a punched MLF-16 5x5x0.9 mm, 0.8 mm pitch.
It can be used as a position sensor for linear (axial/orthogonal and axial/parallel) or angular (on-axis and off-axis) movement of permanent magnets, as a current sensor or as a magnetic field probe. By use of both 3D Hall sensors stray field robust applications can be implemented.

Sensor placement: Two 3D Hall sensors (also called pixel cells) with a distance of 2.0 mm between each other.
Temperature sensor for system-level drift tracking

Measurements: Magnetic field value (X-, Y- or Z-direction) of the activated sensor or temperature signal. Measurement range full scale from ~10 mT up to ~1.5 T.
Measurement rate up to 20 kHz at 12 Bit or 1.8 kHz at 16 Bit resolution.

Software defined sensor: Each sensor element can be independently configured concerning measurement range and rate. The measurement flow (active sensor elements and measurement order) is software defined, too.

Integrated excitation coil: Enables magnetic calibration without need for magnetic setup and magnetic self-test during operation.

Communication interface: The ASSP offers a register based four wire SPI interface with the pins MISO, MOSI, SCK, CS_N and an optional READY signal. The maximum interface clock frequency is 16 MHz.

Digital state machine: The digital state machine consists of

- an automatic decimation of the sigma-delta based ADC values
- shadow registers as memory for the output values for continuous operation
- control for automatic spinning current measurement and offset centring
- diagnostic flags

During normal operation minimum the following functionality has to be implemented for example in an external microcontroller:

- initialization of the ASIC
- sequential control of the measurements (measure x, y, z and temperature)
- signal processing
    - sensitivity compensation over temperature
    - offset compensation over temperature

1.2 Block Diagram

The chip consists of two 3D Hall sensors, an excitation coil and its high voltage current source, the analogue signal computation channel with programmable gain amplifier plus offset centering, ΣΔ-Modulator and a decimation register. The state machine controls the decimation, offset centering and the 4-phase measurement cycle. The system clock has to be fed in by a dedicated CLK pad.

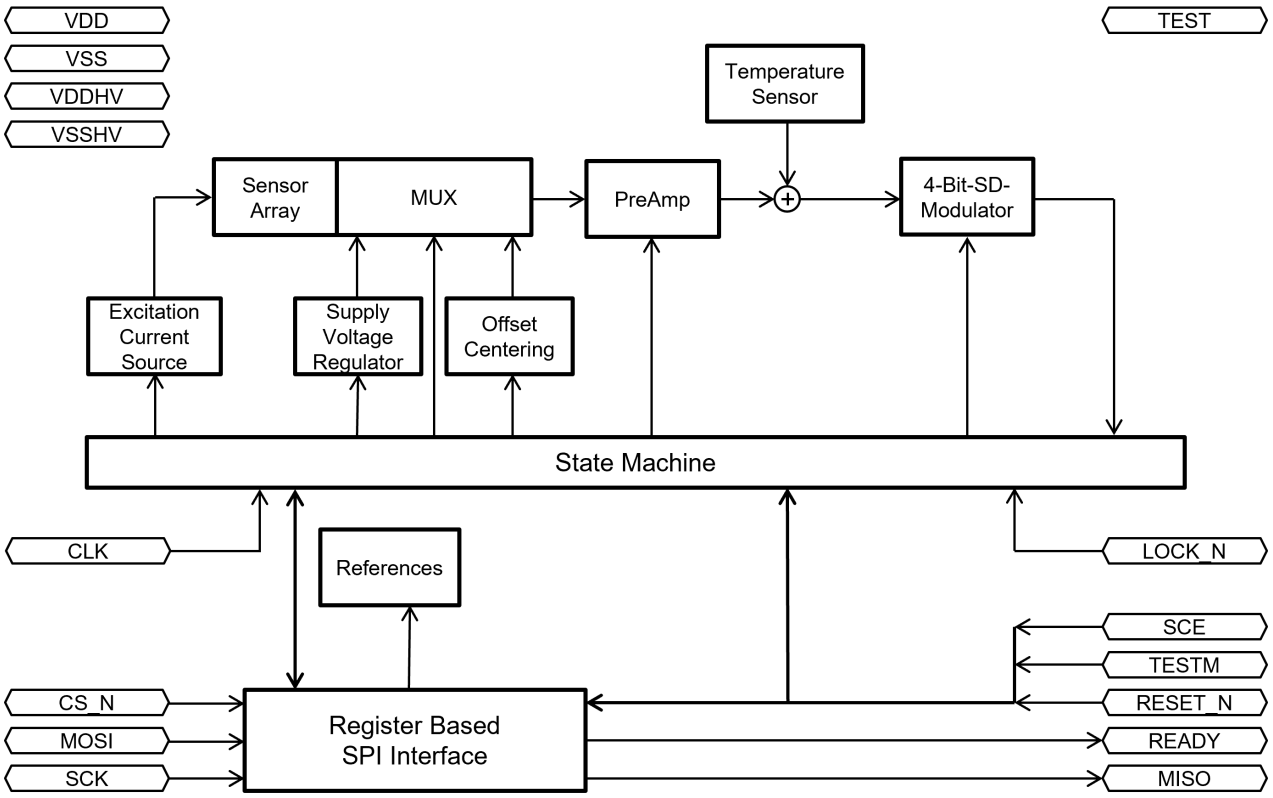

Figure 1: Block diagram

1.3 Customer Support

For questions and troubleshooting please contact the customer support:

Email: contact@lze-innovation.de

2
Characteristics

2.1
Operating Conditions

Table 1: Operating conditions

Parameter	**Min.**	**Typ.**	**Max.**	Unit
Ambient temperature	-40	25	125	°C
VDD	3.0	3.3	3.6	V
VDDHV during routine test		20		V
VDDHV during normal operation	3.0	3.3	3.6	V

2.2
Absolute Maximum Ratings (Non-Operating)

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (eq. hot carrier degradation).

Table 2: Absolute Maximum Ratings

Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Note**
DC supply voltage	VDD	-0.3	7.0	V	
DC supply voltage	VDDHV	-0.3	22	V	
Input pin voltage	V_in	-0.3	VDD+0.3	V	
Input current on any pin	I_in	-100	100	mA	Norm: JEDEC78
Storage Temperature	T_strg	-55	125	°C	
Humidity		5	85	%	Non-condensing
Electrostatic discharge	ESD	+/-2		kV	Norm: MIL 883 E method 3015
Soldering Conditions	T_lead				Norm: IEC 61760-1

2.3
Magnetic Specifications

As the chip has no memory it can't be trimmed during the final test, so the raw measurements have huge tolerances.

As described in chapter 6.6 the integrated test circuits can be used to measure the magnetic trim values on module level. With this information and the signal processing described in chapter 6.4 accurate measurements can be done.

Both magnetic specifications for raw values and for on chip calibrated and postprocessed values are given in the following tables.

The min. typ. and max. values are based on a small number of samples from two engineering lots, measured with 3.3 V supply. Unless otherwise noted 25°C. Drift values are with respect to 25°C. 1σ values are measured while 5σ values are calculated.

Table 3: Magnetic Specifications: Basic configuration with signal processing on microcontroller and on chip trimming; unless otherwise noted 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Magnetic field range XY	BmaxXY	-88		88	mT	-40°C … 125°C 5σ value
		-131		131	mT	5σ value
Magnetic field range Z	BmaxZ	-131		131	mT	-40°C … 125°C 5σ value
		-172		172	mT	5σ value
Magnetic sensitivity XY	SXY	99.7	100.0	100.5	LSB/mT	1σ = 0.198
Magnetic sensitivity Z	SZ	99.7	100.0	100.3	LSB/mT	1σ = 0.156
Magnetic resolution XY			10.0		µT/LSB	
Magnetic resolution Z			10.0		µT/LSB	
Sensitivity drift X, Y		-0.7	0.0	0.7	%	-40°C … 125°C 1σ = 0.39
Sensitivity drift Z		-1.6	0.0	1.7	%	-40°C … 125°C 1σ = 0.58
Sensitivity matching X/Y		99.8	100	100.3	%	-40°C … 125°C 1σ = 0.13
Sensitivity matching XorY/Z		99.6	100	100.3	%	1σ = 0.1
Sensitivity matching drift XorY/Z		-1.5		1.1		-40°C … 125°C
Orthogonality X/Y		88.8	89.8	90.5	°	1σ = 0.42
Orthogonality Z2X or Z2Y		89.7	90.0	90.2	°	1σ = 0.15
Magnetic offset XY	BoffsXY	0.0	0.0	0.0	mT	(1)
Magnetic offset Z	BoffsZ	0.0	0.0	0.0	mT	(1)
Magnetic offset drift XY		-0.32	0.0	0.31	mT	-40°C … 125°C 1σ = 0.16
Magnetic offset drift Z		-0.09	-0.02	0.01	mT	-40°C … 125°C 1σ = 0.02
1σ Noise XY			12.9		µT	
1σ Noise Z			10.6		µT	

Basic configuration: GainXY =128, GainZ = 64, UD = 2.6 V.
(1) After offset adjustment. Take care of the geomagnetic field!

Table 4: Magnetic Specifications: Raw Values with basic configuration

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Magnetic field range XY	BmaxXY	-88		88	mT	-40°C … 125°C 5σ value
		-131		131	mT	5σ value
Magnetic field range Z	BmaxZ	-131		131	mT	-40°C … 125°C 5σ value
		-172		172	mT	5σ value
Magnetic sensitivity XY	SXY	89.9	94.4	100.2	LSB/mT	1σ = 2.8
Magnetic sensitivity Z	SZ	79.0	82.4	88.9	LSB/mT	1σ = 2.9
Magnetic resolution XY			10.59		µT/LSB	
Magnetic resolution Z			12.13		µT/LSB	
Sensitivity drift XY		-39.8		42.9	%	-40°C … 125°C
Sensitivity drift Z		-34.1		30.4	%	-40°C … 125°C
Sensitivity matching X/Y		99.87	100.04	100.23	%	-40°C … 125°C 1σ = 0.08
Sensitivity matching XorY/Z		55.4	57.0	59.1	%	1σ = 1.0
Sensitivity matching drift XorY/Z		-10.7		8.7	%	
Orthogonality X/Y		88.8	89.8	90.5	°	1σ = 0.42
Orthogonality Z/X Z/Y		88.9	91.2	94.4	%	1σ = 1.83
Magnetic offset XY	BoffsXY	-5.1	-1.88	3.5	mT	1σ = 2.27
Magnetic offset Z	BoffsZ	-0.12	-0.05	0.02	mT	1σ = 0.04
Magnetic offset drift XY		-1.24	0.05	1.21	mT	-40°C … 125°C 1σ = 0.7
Magnetic offset drift Z		-0.13	0	0.10	mT	-40°C … 125°C 1σ = 0.04
1σ Noise XY			12.9		µT	
1σ Noise Z			10.6		µT	

Table 5: Magnetic Specifications: Small measurement range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Magnetic field range XY	BmaxXY	-9.1		9.1	mT	-40°C … 125°C 5σ value
		-17.7		17.7	mT	5σ value
Magnetic field range Z	BmaxZ	-11.2		11.2	mT	-40°C … 125°C 5σ value
		-14.7		14.7	mT	5σ value
Magnetic sensitivity XY	SXY	193.2		620	LSB/mT	-40°C … 125°C 5σ value
		321.0	377.8	434.5	LSB/mT	5σ value
Magnetic sensitivity Z	SZ	358.2		1011.5	LSB/mT	-40°C … 125°C 5σ value
		543.5	659.5	775.5	LSB/mT	5σ value

Small measurement range configuration: GainXY = 512, Gain Z = 512, UD = 2.6 V

Table 6: Magnetic Specifications: High measurement range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Magnetic field range XY	BmaxXY	-1.76		1.76	T	-40°C … 125°C 5σ value
		-2.50		2.50	T	5σ value
Magnetic field range Z	BmaxZ	-2.19		2.19	T	--40°C … 125°C 5σ value
		-2.87		2.87	T	5σ value
Magnetic sensitivity XY	SXY	3.02		9.79	LSB/mT	-40°C … 125°C 5σ value
		5.02	5.90	6.79	LSB/mT	5σ value
Magnetic sensitivity Z	SZ	2.80		7.90	LSB/mT	-40°C … 125°C 5σ value
		4.24	5.15	6.06	LSB/mT	5σ value

High measurement range configuration: GainXY = 64, GainZ = 32, UD = 0.325 V

2.4
Current Consumption

Table 7: Current Consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
IDD during measurements	IDD_{meas}		11.0	15.0	mA	(1, 2)
IDD all analog blocks PD	IDD_{reset}		0.25	0.5	mA	(1, 2)
IDD analog PD, clk off	IDD_{PD}		1	20	µA	(1, 2)

(1) Output currents in I/O pins are not included.
(2) Values are DC mean currents.

3
Package and Circuit Connection

3.1
Package and Dimension

Punched MLF 5x5x0.9 mm; lead pitch 0.8 mm package, with lead frame material C7025. The exposed pad should be connected to GND.

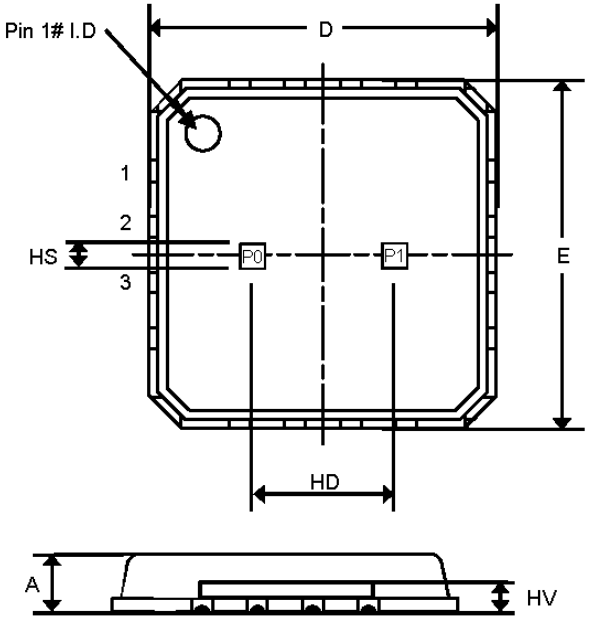

Figure 2: Package Drawing

Table 8: Package Dimensions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Hall Sensor Size	HS		0.1		mm
Hall Sensor Distance	HD		2		mm
Package Length	D		5		mm
Package Width	E		5		mm
Package Thickness	A		0.9		mm
Hall Sensor Vertical Position	HV		0.45		mm

3.2 Pins

Table 9: Pin description

Pin QFN16	Name	Pad	Description
1	TEST	Analogue IO	Test pin
2	RESET_N	Digital In	Reset
3	LOCK_N	Digital In	Lock, must be connected to VSS
4	READY	Digital Out	Measurement ready signal
5	VSS	Supply	Ground (0V)
6	VDD	Supply	Supply voltage (3.0V … 3.6V)
7	MISO	Digital Out	Master in / Slave out (SPI output)
8	MOSI	Digital In	Master out Slave in (SPI input)
9	SCK	Digital In	SPI Interface clock
10	CLK	Digital In	System clock (max. 8 MHz)
11	VSSHV	Supply	Ground (0V)
12	CS_N	Digital In	Chip Select (low-active)
13	-	-	-
14	VDDHV	Supply	Supply voltage (3.0V … 3.6V or 20V for routine tests)
15	TESTM	Digital In	Test Mode, must be connected to VSS.
16	SCE	Digital In	Scan test enable, must be connected to VSS

The digital input pins have Schmitt-trigger functionality. The outputs are slew rate controlled CMOS drivers. The corresponding levels are shown in this table and are valid for a junction temperature range of –40 …125°C.

Table 10: Pin input and output levels

Name	Min.	Max.	Unit	Comment
Input negative going threshold	1.12	1.27	V	VDD=3.0V
Input negative going threshold	1.42	1.52	V	VDD=3.6V
Input positive going threshold	1.77	1.87	V	VDD=3.0V
Input positive going threshold	2.07	2.23	V	VDD=3.6V
Output low level	0	0.4	V	8mA load
Output high level	2.5	VDD	V	8mA load

CS_N as low active chip select signal activates receiving and sending of interface data. If only a single chip is used, CS_N can remain ‘low’. All interface data is synchronized internally and transferred after 16 SCK cycles.

The system clock CLK only toggles the state machine and ADC. It can be run at a maximum frequency of 8 MHz.

3.3
Electrical Connection

The sensor chip must be connected to a supply of 3.3 V via its VDD and VSS pins.

The integrated coils may be connected to 3.3 V or up to 20 V depending on the application. If the integrated coils should be used to measure the sensitivity during the final module test in a short time, VDDHV should be connected to 20 V. If the integrated coils should be used to monitor the sensors functionality the integrated coils can be connected to 3.3 V. All unused input pins should be connected to VSS to guarantee proper function. Decoupling capacitors between VDD and VSS as well as between VHHDV and VSSHV close to the sensor chip are strongly recommended. For communication of a single sensor with a microcontroller, all four SPI signals CS_N, SCK, MOSI and MISO have to be connected. After power up, a proper reset cycle of the sensor chip has to be executed. Pin READY can be used to detect a finished measurement. To trim reference voltage, reference current and sensor supply test pin TEST has to be connected during the final module test.

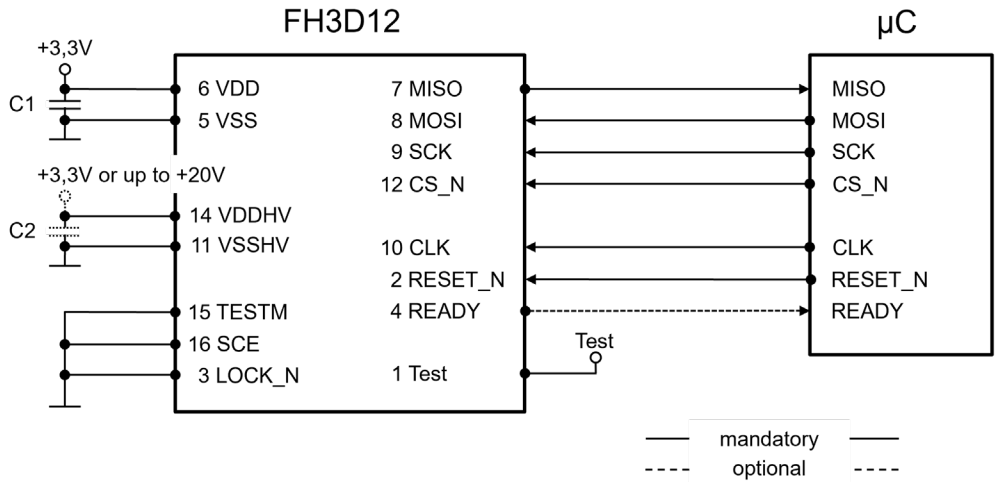

Figure 3: Typical electrical connection

Recommended additional components:
C1 : Non-magnetic capacitor near pins (100 nF)
Optional components:
C2: Non-magnetic capacitor near pins (100 nF)

Please note:
It is strongly recommended to use a PCB with wide bandwidth, low impedance supply layer system and impedance controlled digital signal lines with matching series resistors to the hardware setup. A stable supply and clean signals are mandatory for low sensor noise and faultless communication at high SPI frequency.

4
SPI Communication

4.1
Communication Interface

The serial interface samples the information at MOSI with the rising edge of SCK.
The output bits at MISO are updated with every falling SCK edge. MISO is only activated if CS_N is low. Otherwise the output is hi-Z. This allows for parallel operation of multiple ICs.
Two different access modes are possible. A 16 bit word can be written to a certain address or a 16 bit word can be read. The MSB of the address word (A<15>) decides about reading or writing the data.

A<15> = 0 (read measurement data / RAM)
A<15> = 1 (write parameter / RAM)

Writing:
For writing a word into a register the appropriate address and the write/read bit must be written to the interface. The interface counter counts the SCK cycles and detects the end of the address word and the beginning and end of the data word. Therefore the chip select (CS_N) can be set to 'low' and does not need to be controlled.
During the write access the current data in the addressed register is written to MISO. Using this, the interface register behaves like a 32-bit shift register. The chip select does not affect the register but controls the transfer of data only.

Reading:
For reading a register the address with A<15> = 0 is written to the interface. After 16 SCK cycles the actual reading starts.
During clocking out the data from a register at MISO, the bits at MOSI are interpreted as new R/W command and address.

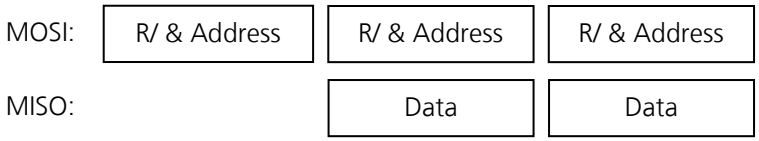

Figure 4: Reading mode

Failure detection:
For detection of communication errors, the current value of a register can be read back at the same time as new data is written to it.

During a write access first the address is transmitted. After the address is written, the interface can read the content of this register and prepare for read back. During writing the new data and finalizing the transmission, the old register content is available at the MISO pin. The controller can verify the old register content.

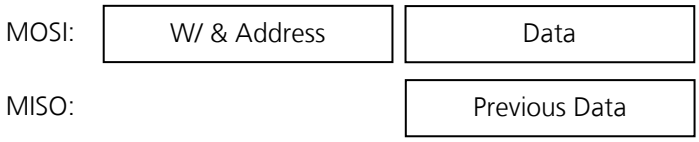

Figure 5: Writing mode

With this function it is possible to check the connection between ASIC and controller as well as the content of the concerning register.
After a write command transfer is complete, the complete transfer data is present at MISO during the next transfer phase. The correct communication can be verified here.

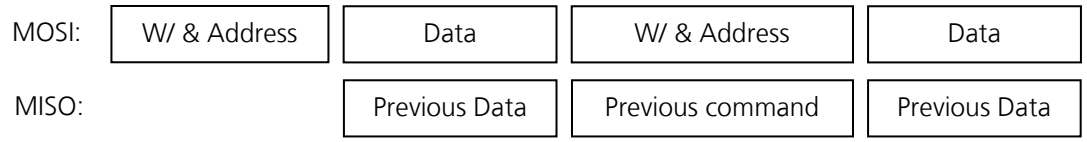

Figure 6: Command verification

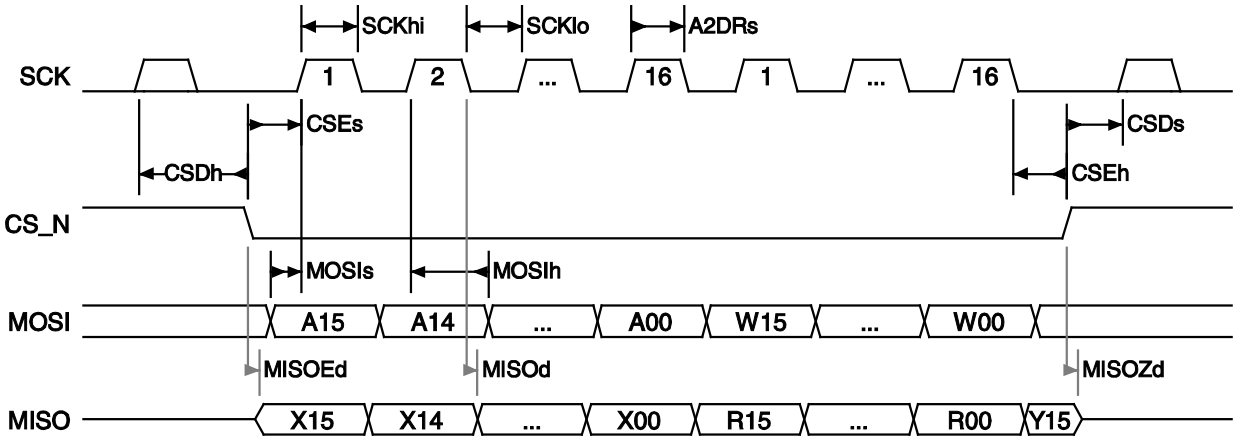

Figure 7: SPI timing

Table 11: SPI timing values

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
External CLK frequency	f_{CLK}	7.95	8	8.05	MHz	
External CLK pulswidth HI	t_{CLKhi}	62	62.5	63	ns	
External CLK pulswidth LO	t_{CLKlo}	62	62.5	63	ns	
External CLK duty cycle	D_{CLK}	49	50	51	%	
SCK frequency Standard registers	f_{SCK}	0		16	MHz	(1)
SCK pulswidth HI	t_{SCKhi}	30	31.25		ns	
SCK pulswidth LO	t_{SCKlo}	30			ns	
CS_N enable setup time before SCK	t_{CSEs}	10			ns	
CS_N enable hold time after SCK	t_{CSEh}	10			ns	
CS_N disable setup time before SCK	t_{CSDs}	10			ns	
CS_N disable hold time after SCK	t_{CSDh}	10			ns	
MOSI setup time before SCK	t_{MOSIs}	10			ns	
MOSI hold time after SCK	t_{MOSIh}	10			ns	
MISO delay after SCK	t_{MISOd}			10	ns	
MISO enable delay after CS_N	t_{MISOEd}			20	ns	
MISO high Z delay after CS_N	t_{MISOZd}			20	ns	
Output edge rise time	t_{Or}		3	8	ns	
Output edge fall time	t_{Of}		3	8	ns	

Typical values are given for 25°C. Output load 25 pF.
(1) must not exceed $8 \cdot f_{CLK}$

5
Register Map

Following tables show all available registers for communication with the sensor via SIP.
After a reset the configuration registers 0x002 to 0x027 have to be written once. Measurements can be started using register 0x001. The measured values can be read from register 0x100, while 0x102 contains status bits. A read operation from register 0x100 deletes the ready bit.

Table 12: Register 0x001 content

Bitpos.	Signal	Width	Meaning
15-13	AmpGain<2:0>	3	Amplifier Gain 0=32, 1=64, 2=128, 3=256, 4=512, 5=1024, 6 and 7 is not allowed
12	TempSel	1	Temperature Select
11	PixelSel	1	Pixel Select 0: left 3D Hall sensor, 1: right 3D Hall sensor
10-9	SensSel<1:0>	2	Sensor Select <1:0>: Sensor: 0 = X, 1 = Y, 2 = Z, 3 = all sensors off
8-1	DecLen<11:4>	8	Decimation Length <3:0> is always 0 If DecLen<11:4> is 0 DecLen = 1
0	DecEn	1	Decimation Enable

To start a measurement with basic configuration using register 0x001 write via SPI transfer:
8001h – ??41h Pixel ?, Sensor ?, Gain ?, DecLen 512

Table 13: Register 0x002 content

Bitpos.	Signal	Width	Meaning
15-13	SRegDVal<2:0>	3	Sensor Regulator Difference Value 0 = 0.325V, 1 = 0.65V, 2 = 1.3V 3 = 2.0V, 5 = 2.6V, 6 = 2.8V
12-10	SRegNVal<2:0>	3	Sensor Regulator Negative Value 0 = 0.2V, 2 = 0.5V, 3 = 0.65V 5 = 0.95V, 6 = 1.1V
9-7	ECCSel<2:0>	3	Excitation Current Coil Select 0 = all off, 1 = QP1, 2 = XYP1, 3 = ZP1+HP0, 4 = ZP0+HP1, 5 = XYP0, 6 = QP0
6-4	ECVal<2:0>	3	Excitation Current Value
3	ECSign	1	Excitation Current Sign
2	ECEnHV	1	Excitation Current Enable High Voltage 0: 0.2mA per Digit (EC_Val+1) 1: 1.4mA per Digit (EC_Val+1)
1-0	Phase<1:0>	2	Phase

For basic configuration of register 0x002 write via SPI transfer:
8002h – A000h SRegNVal:0 = 0.2 V; SRegDVal:5 = 2.6 V

Table 14: Register 0x003 content

Bitpos.	Signal	Width	Meaning
15-12	Reserved	4	Reserved set to zero
11-8	Auto4P<3:0>	4	Auto4P
7	SMUXChopInv	1	Sensor MUX Chopper Invert
6	SMUXChopFast	1	Sensor MUX Chopper Fast
5	SMUXDisComp	1	Sensor MUX Disable Compensation
4-0	DecWait<7:3>	5	Decimation Wait <2:0> is always 0; DecWait has to be at least 8, so DecWait<7:3> has to be at least 1b

For basic configuration of register 0x003 write via SPI transfer:
8003h – 090Ah Auto4P:1001b; DecWait<7:3>: 01010b (DecWait 01010000b=80)

Table 15: Register 0x004 content

Bitpos.	Signal	Width	Meaning
15-11	Reserved	5	Reserved set to zero
10	OC_PO	1	Offset Centering PO
9	ModRefBuf_PO	1	Modulator Reference Buffer Power On
8	Buf_PO	1	Buffer Power On
7	EC_PO	1	Excitation Current Power On
6	Bias_PO	1	Bias Power On
5	Mod_PO	1	Modulator Power On
4	Amp_PO	1	Amplifier Power On
3	SRegN_PO	1	Sensor Regulator N Power On
2	SRegD_PO	1	Sensor Regulator D Power On
1	SMUXPowerEn	1	Sensor Modulator Power Enable
0	SMUXSigEn	1	Sensor Mux Signal Enable

For basic configuration of register 0x004 write via SPI transfer:
8004h – 077Fh All PO except EC_PO; SMUXPowEn; SMUXSigEn

Table 16: Register 0x007 content

Bitpos.	Signal	Width	Meaning
15-11	Reserved	5	Reserved set to zero
10	HistEn	1	Histogram Enable
9-0	Reserved	10	Reserved set to zero

For basic configuration of register 0x007 no action is needed.

Table 17: Register 0x008 content

Bitpos.	Signal	Width	Meaning
15-14	Reserved	2	Reserved set to zero
13	ICTUP	1	In-Circuit-Test UP Switch positive sensor supply voltage to *TEST*
12	ICTUN	1	In-Circuit-Test UN Switch negative sensor supply voltage to *TEST*
11	ICTIb	1	In-Circuit-Test Ib Switch 10uA reference current to *TEST*
10	ICTURef	1	In-Circuit-Test URef Switch bandgap reference voltage to *TEST*
9	OCRInt	1	Offset Centering R Internal 0: Dummy Sensor 1: Internal Resistor
8	OCIRefR	1	Offset Centering Current Reference Resistor
7-6	OCMode<1:0>	2	Offset Centering Mode Typical: 0b10
5	OCAuto	1	Auto Centering
4	OCSign	1	Offset Centering Sign
3	OCToggle	1	Offset Centering Toggle
2-0	OCGain	3	Offset Centering Gain

For basic configuration of register 0x008 write via SPI transfer:
8008h – 00A9h OCMode:10b; OCAuto; OCToggle; OCGain: 001b

Table 18: Register 0x010 content

Bitpos.	Signal	Width	Meaning
15-8	OCVal1<7:0>	8	Offset Centering Value 1
7-0	OCVal0<7:0>	8	Offset Centering Value 0

For basic configuration of register 0x010 no action is needed.

Table 19: Register 0x027 content

Bitpos.	Signal	Width	Meaning
15-14	Reserved	2	Reserved set to zero
13-10	SReg_or_IBias_Trim<3:0>	4	Trim bits for sensor regulator and IBias generation
9-4	BGTrim<5:0>	6	Bandgap Trim
3-2	RM<1:0>	2	Ready Mode
1	RVR1	1	Read Value Register 1
0	ModOpM	1	Modulator Operating Mode

For basic configuration of register 0x027 several write transfers via SPI are necessary. Please look at chapter 6.1.1 for details.

Table 20: Register 0x100 content

Bitpos.	Signal	Width	Meaning
15-0	DecVal<15:0>	16	Decimation Value

Table 21: Register 0x102 content

Bitpos.	Signal	Width	Meaning
15	Ready	1	Ready
14	HistWarn	1	Histogram Warning
13	RngWarn	1	Range Warning
12-8	Reserved	5	Reserved set to zero
7-4	FC<3:0>	4	Field Component <3>: Temperature <2>: Pixel <1:0> : Sensor: 0 = X, 1 = Y, 2 = Z,
3-2	Reserved	2	Reserved set to zero
1-0	DecVal<17-16>	2	Decimation Value

Table 22: Register 0x103 content

Bitpos.	Signal	Width	Meaning
15-0	Reserved<7:0>, OCVal<7:0>} or HistVal<15:0>	16	Offset Centering value if one of the Auto4P Bits is set otherwise Histogram in single phase measurements

6
Application Notes

In this chapter a step-by-step instruction is given to use the sensor in a proper way.
With the basic configuration (Chap. 6.1) first measurements can be done for bring-up.
Using the described signal postprocessing (Chap. 6.4), the described determination of electrical trim values (Chap. 6.5) and the determination of magnetic trim values (Chap. 6.6) measurements over temperature with a high accuracy can be realized.

6.1
First raw measurements with the basic configuration

The wait length should be equal for all sensors. The typical wait length is 80.
A decimation length of 512 leads to a resolution of 15 bit.
The sensor supply regulator has to be set to 2.6 V.
The gain is different for XY and Z sensors. XY sensors use gain 128, Z sensors use gain 64.

6.1.1
Basic configuration

The basic configuration has to be written once after a sensor reset.
The default trim values for the bandgap reference and sensor supply regulator are:

- ICT_VREF_TRIM: 6'b100000
- ICT_IBIAS_TRIM: 4'b1000
- ICT_SREG_TRIM: 4'b1000

These values can be used for the initial operation. For final applications the trim values have to be measured as described in Determination of the trim values (Chap. 6.3).
For a basic configuration please send the following commands:

- **8002h – A000h**
  - SRegNVal:0 = 0.2V; SRegDVal:5 = 2.6V
- **8003h – 090Ah**
  - Auto4P:1001b; DecWait<7:3>: 01010b (DecWait 01010000b=80)
- **8004h – 077Fh**
  - all PO except EC_PO; SMUXPowEn; SMUXSigEn
- **8008h – 0800h**
  - ICTIb
- **8027h – (2'b00, ICT_IBIAS_TRIM, VREF_TRIM, 4'b0100)**
  - SReg_or_IBias_Trim value; BGTrim value; RM:01b
- **8008h – 00A9h**
  - OCMode:10b; OCAuto; OCToggle; OCGain: 001b
- **8027h – (2'b00, ICT_SREG_TRIM, VREF_TRIM, 4'b0100)**
  - SReg_or_IBias_Trim value ; BGTrim value; RM:01b

6.1.2
Measurement of Pixel 0, Sensor X, Gain 128, DecLen 512

- Gain 128 = 2-> 010b
- PixelSel = 0b
- SensSel = X = 00b
- DecLen = 512 = 200h -> bit 3 to 0 are allways 0 -> 100000b
- DecEn = 1b start measurement

Send the following command to start the measurement:

- **8001h – 4041h** Pixel 0, Sensor X, Gain 128, DecLen 512

Read out measurement by sending the following commands as described in chapter 4.1.

- **0102h – 0100h – 0000h**

6.1.3
Measurement of Pixel 1, Sensor Z, Gain 64, DecLen 512

- Gain 64 = 1-> 001b
- PixelSel = 1b
- SensSel = Z = 10b
- DecLen = 512 = 200h -> bit 3 to 0 are allways 0 -> 100000b
- DecEn = 1b start measurement

Send the following command to start the measurement:

- **8001h – 2C41h** Pixel 1, Sensor Z, Gain 64, DecLen 512

Read out measurement by sending the following commands as described in chapter 4.1.

- **0102h – 0100h – 0000h**

6.1.4
Measurement of the Temperature, with preheating of the next Sensor Pixel 0, Sensor X, Gain 128, DecLen 512

For a constant power consumption and a stable sensor temperature the next Hall sensor can be activated during the temperature measurement. The gain setting for the next Hall sensor has to be used.

- Gain 128 = 2-> 010b
- TempSel = 1b
- PixelSel = 0b
- SensSel = X = 00b
- DecLen = 512 = 200h -> bit 3 to 0 are allways 0 -> 100000b
- DecEn = 1b start measurement

Send the following command to start the measurement:

- **8001h – 5041h** Pixel 0, Sensor X, Gain 128, DecLen 512

Read out measurement by sending the following commands as described in chapter 4.1.

- **0102h – 0100h – 0000h**

6.2 Magnetic resolution

The basic configuration is working in four-phase spinning current scheme with a decimation length of 512. As the ∑Δ-ADC has a resolution of 4 bit and is symmetrical around 0. The maximum ADC value is 7.5. The measurement values are in the range of ±15360 which is a resolution of 14.9 bit.

The following picture shows the signal path and its typical parameters.

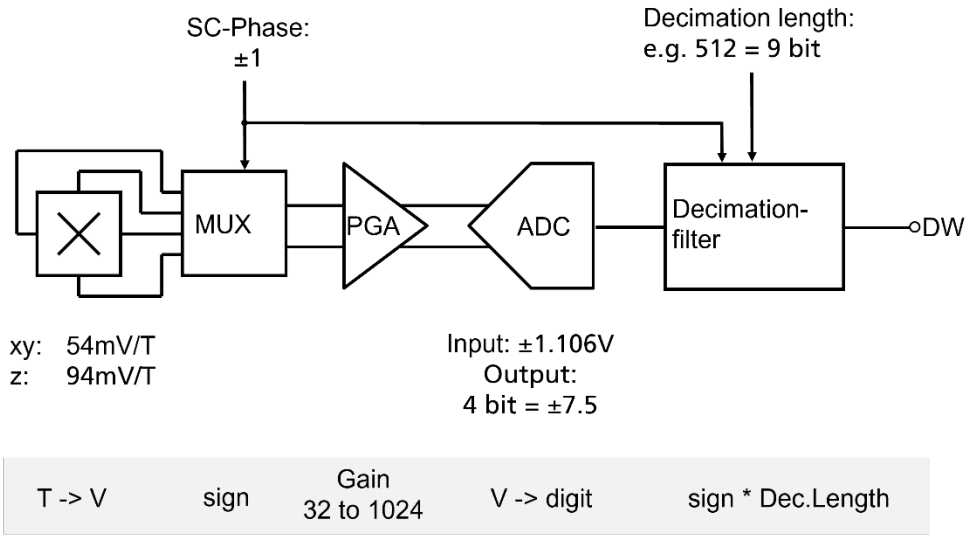

Figure 8: Signal Path

With a differential input of the ADC of ±1.106 V, a 4-bit resolution, a decimation length of 512 a gain of 128 and a 4 phase spinning current scheme the resolution of the ADC can be calculated to:

(2*1.06 V) / 128 / (512 * 15 * 4) = 539.1 nV

With a sensitivity of 54 mV/T for the X and Y sensors the magnetic resolution can be calculated to:

539.1 nV / 54 mV/T = 9.98 µT.

With a gain of 64 and a sensitivity of 94 mV/T the magnetic resolution of the Z sensors is:

(2*1.06 V) / 64 / (512 * 15 * 4) = 1078.3 nV

1078.3 nV / 94 mV/T = 11.47 µT

6.3 Measurement time

The Hall sensors are operated in a four-phase spinning current scheme while the temperature sensor is operated in a two phase chopper principle.
The pure measurement time can be calculated by:

- (DecLen + DecWait + 6) * **4** * (nr. of Hall sensors) + (DecLen+ DecWait + 6) * **2**
- (512 + 80 + 6) * 4 * 3 + (512 + 80 + 6) *2 = 8372
- MHz = 125 ns
- 8372 * 125ns = 1046.5 µs

If the SPI runs at 16MHz the time for communication can be calculated by:

- 16 bit address + 16 bit data = 32 bit
- 16MHz = 62.5 ns
- Per sensor (magnet or temperature) 1 x start + 2 x read
- 32 * 4 * 3 * 62.5 ns = 24 µs

The complete measurement time for all tree Hall sensors and the temperature sensor is about 1070.5 µs.

6.4 Signal postprocessing

In many applications, the raw senor values can be used without any postprocessing. In this case the parameters described in Table 4 can be used. If the performance described in Table 3 is needed the raw measured digital values have to be converted into magnetic flux density values by using the following signal postprocessing. The necessary parameters can be generated on chip by using the integrated excitation wires as described in chapter 6.6. If higher accuracies are needed the sensitivities and offsets have to be measured by using 3D Helmholtz coils.

6.4.1 Temperature postprocessing

As the sensitivity of the Hall sensors is temperature dependent the temperature has to be measured. The necessary temperature postprocessing is shown in Figure 9.

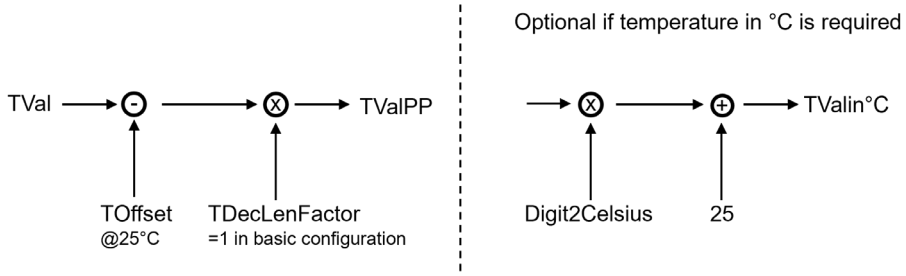

Figure 9: Temperature postprocessing

Using the basic configuration, the temperature value $TVal$ has only to be compensated with the device specific temperature offset $TOffset$ which has to be measured at 25°C.

$$TOffset = TVal(at\ 25°C)$$

This postprocessed temperature value $TValPP$ can then be used for the magnetic postprocessing.

$$TValPP = TVal - TOffset$$

If a different configuration is used the measured temperature value $TVal$ hast to be scaled by the factor $TDecLenFactor$ which can be calculated by:

$$TDecLenFactor = \frac{512}{DecLen}$$

If the temperature in °C is needed $TValPP$ can be converted in °C by the factor $Digit2Celsius$.

$$Digit2Celsius = 0.072484471 \frac{°C}{Digit}$$

The temperature in °C can be calculated by:

$$TValin°C = TValPP * Digit2Celsius + 25°C$$

6.4.2
Magnetic postprocessing

The necessary magnetic postprocessing is shown in Figure 10.

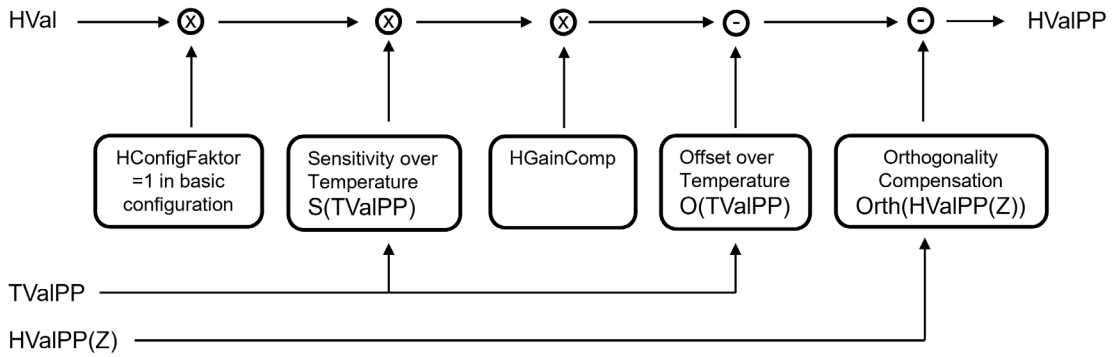

Figure 10: Magnetic postprocessing

Using the basic configuration, the digital Hall signal $HVal$ can be converted from Digit to Tesla over temperature using the direction specific typical functions $S_{XY}(\,TValPP)$ or $S_Z(TValPP)$.

$$S_{Typ,XY}(\,TValPP) = 1.0276 \times 10^{-14} \times TValPP^3 + 5.4044 \times 10^{-10} \times TValPP^2 + 4.0808 \times 10^{-6} \times TValPP + 0.010583$$

$$S_{Typ,Z}(TValPP) = 1.0057 \times 10^{-13} \times TValPP^3 + 3.2504 \times 10^{-10} \times TValPP^2 + 3.5704 \times 10^{-6} \times TValPP + 0.012118$$

If different configurations than the basic configurations are used the measured Hall values $HVal$ have to be scaled to the basic configuration parameters (decimation length of 512; gain 128 for XY, gain 64 for Z; sensor supply) by the factor $HConfigFactor$ which can be calculated by:

$$HConfigFactor = \frac{1}{\left(\frac{UsedGain}{BasicGain}\right) \times \left(\frac{UsedDecLen}{BasicDecLen}\right) \times \left(\frac{UsedSupply}{BasicSupply}\right)}$$

For high accuracies as described in Table 3, the device specific production deviations concerning nominal sensitivity, amplifier gains and sensor supply regulator voltages has to be compensated using the factor $HGainComp$ which needs to be calculated for each sensor. Chapter 6.6 describes how this value can be measured.

The magnetic values in Tesla have to be compensated with the device and sensor specific magnetic offsets over temperature $O(TValPP)$. The minimum offset compensation should be done at 25°C as described in chapter 6.6. For higher accuracies the offset temperature coefficient has to be used as described in chapter 6.6.

As the orthogonality errors Z/X and Z/Y can be in the range of several degrees. Depending on accuracy needed in application these orthogonality errors have to be compensated by the coefficient $Orth_{XY}(\mathrm{HV}alPP(Z))$. Chapter 6.6 describes how these factors can be measured on chip.

Using the basic configuration, the postprocessed magnetic field values can be calculated by:

$$HValPP_Z = HVal_Z \times HGainComp \times S_Z(TValPP) - O_Z(TValPP)$$

$$HValPP_{XY} = HVal_{XY} \times HGainComp \times S_{XY}(TValPP) - O_{XY}(TValPP) - Orth_{XY}(HValPP_Z(TValPP))$$

6.5 Determination of electrical trim values

6.5.1 Bandgap trimming

Initialize the devices (Reset, CLK, …).

Configure setup for voltage measurement on pin TEST.

- Send **8004h – 0040h** to enable bias
- Send **8008h – 0400h** to set In-Circuit-Test for Vref
- Repeat the following routine for values for m from 0h, 1h, 2h to 3Fh:
- Send **8027h – (m*10h)** to set the bias trimming
- Measure the voltage at pin TEST (ICT_V_REF_m)
- Send **8008h – 0000h** to disable In-Circuit-Test for Vref

Select lowest value of m that gives ICT_V_REF_m = 1.18 V to get ICT_VREF_TRIM = m.

6.5.2 IBias trimming

Assumption:

Bias trimming is performed directly after bandgap trimming. Otherwise initialize the devices and configure setup for voltage measurement on pin TEST.

TestDefault = ICT_VREF_TRIM * 10h

- Send **8027h – TestDefault** BGTrim value
- Send **8004h – 0040h** to enable bias
- Send **8008h – 0800h** to set In-Circuit-Test for IBias (Ib)
- Repeat the following routine for values for m from 0h, 1h, 2h to Fh:
  - Send **8027h – [TestDefault + (m*400h)]** to set the supply regulator trimming
  - Measure the current at pin TEST (ICT_I_BIAS_m)
- Send **8008h – 0000h** to disable In-Circuit-Test for IBias

Select lowest value of m that gives ICT_I_BIAS_m = 10 µA to get ICT_IBIAS_TRIM = m.

6.5.3
Supply Regulator trimming

Assumption:

Bias trimming is performed directly after bandgap trimming. Otherwise initialize the devices and configure setup for voltage measurement on pin TEST.

TestDefault = ICT_VREF_TRIM * 10h

- Send **8008h – 0800h** to set In-Circuit-Test for IBias (Ib)
- Send **8027h – [TestDefault + (ICT_IBIAS_TRIM*400h)]** to set the bandgap and bias trimming
- Send **8002h – A000h** to set supply regulator
- Send **8004h – 004Eh** to enable bias and supply regulator
- Send **8008h – 2000h** to set In-Circuit-Test for Vref
- Repeat the following routine for values for m from 0h, 1h, 2h to Fh:
    - Send **8027h – [TestDefault + (m*400h)]** to set the supply regulator trimming
    - Measure the voltage at pin TEST (ICT_V_SREG_UP_m)
- Send **8008h – 0000h** to disable In-Circuit-Test for Vref

Select lowest value of m that gives ICT_V_SREG_UP_m = 2.8 V to get ICT_SREG_TRIM = m.

6.6 Determination of magnetic trim values using the integrated excitation coils

The integrated excitation coils can be used to measure the sensors sensitivities, offsets and offset temperature coefficients due to self-heating. If possible choose the maximum excitation current and supply voltage to get low noise measurements and high self-heating effects. Perform this test at room temperature (25°C).

At first the magnetic trimming measurement sequence has to be implemented.
Ensure Excitation Current Power On is set (EC_PO), measure Coil Current (pin VDD_HV) in parallel to measurements.

- Loop over Sensitivity (and CrossSensititivity) coils
  - Loop over used pixels (PixelSel)
    - Loop over used sensor directions (SensSel)
      - Perform measurement on temperature sensor (TempSel=1) and preheat (activate) desired next sensor (PixelSel and SensSel), read decimation value.
      - Set appropriate coil (ECCSel) according to Table 24, current value (ECVal) and ECEnHV according to Table 23 and set ECSign to 1
      - Perform measurement on magnetic field sensor, read decimation value and store it with correct sign according to Table **54**, postfix P
      - Change ECSign to 0.
      - Perform measurement on magnetic field sensor, read decimation value and store it with correct sign according to Table **54** postfix N

Table 23: Excitation coil configuration depending on the available supply voltage.

Supply Voltage	Excitation Current	Mode	Configuration
3.3 V	1.0 mA	LV	ECEnHV = 0; ECVal<2:0> = 100
5 V	1.6 mA	LV	ECEnHV = 0; ECVal<2:0> = 111
9 V	4.2 mA	HV	ECEnHV = 1; ECVal<2:0> = 010
12 V	4.2 mA	HV	ECEnHV = 1; ECVal<2:0> = 010
20 V	4.2 mA	HV	ECEnHV = 1; ECVal<2:0> = 010

Table 24: Coil configuration for on-chip calibration

Pixel	SensSel	Coil Setup	ECCSel
0	Z	Sensitivity	ZP0+HP1
0	Y	Sensitivity	XYP0
0	X	Sensitivity	XYP0
1	Z	Sensitivity	ZP1+HP0
1	Y	Sensitivity	XYP1
1	X	Sensitivity	XYP1
0	Z	CrossSensitivity	QP0
0	Y	CrossSensitivity	QP0
0	X	CrossSensitivity	QP0
1	Z	CrossSensitivity	QP1
1	Y	CrossSensitivity	QP1
1	X	CrossSensitivity	QP1

With this magnetic trimming measurement sequence, the following routine has to be implemented:

- Perform several loops with deactivated excitation coils (EC_PO = 0) to get measured values at 25°C.
    - If the measured temperature sensor has a stable value store all values
    - Use the temperature value T0 (at 25°C) for the temperature postprocessing
        - $TOffset = TVal_{T0}$
        - $TValPP_{T0} = TVal_{T0} - TOffset$ should be 0.
- Perform several loops with activated excitation coils (EC_PO = 1) to get measurements at a higher temperature due to self heating
    - Measure the current $ICoil$ at pin VDDHV while operating the excitation coils.
    - Calculate the excitation fields for each coil by
        - $BCoil_{XY} = 191\frac{\mu T}{mA} \times ICoil \times 2$
        - $BCoil_{Z} = 182\frac{\mu T}{mA} \times ICoil \times 2$
    - If the measured temperature sensor has a stable value store the measured values
    - Calculate the postprocessed temperature measurement at T1
        - $TValPP_{T1} = TVal_{T1} - TOffset$

- Calculate all sensitivity related values
    - Calculate the sensor sensitivities at temperature T1

- $S(TValPP_{T1}) = \frac{BCoil}{HValP - HVal_N}$

- Calculate all $HGainComp$ factors to fit the typical sensitivity functions
  - $HGainComp = \frac{S(TValPP_{T1})}{S_{Typ}(TValPP_{T1})}$

- Calculate all offset related values with postprocessed Hall Measurements HValPP
  - Calculate the sensor offsets at temperature T1 and T0
    - $O_{TValPP_{T1}} = \frac{HValP,T1 + HVal_{N,T1}}{2} \times HConfigFactor \times S_{Typ}(TValPP_{T1}) \times HGainComp$
    - $O_{TValPP_{T0}} = \frac{HValP,T0 + HVal_{N,T0}}{2} \times HConfigFactor \times S_{Typ}(TValPP_{T0}) \times HGainComp$
  - Define all offset over temperature functions
    - $O(TValPP) = O_{TValPP_{T0}} + \frac{O_{TValPP_{T1}} - O_{TValPP_{T0}}}{TValPP_{T1} - TValPP_{T0}} \times TValPP$

- Calculate all orthogonality values
  - Calculate the orthogonality coils fields in Z direction
    - $HValPP_Z = (HValPP_{Z,QP,P} - HValPP_{Z,QP,N})$
  - Calculate the orthogonality coils fields in X any Y direction
    - $HValPP_{XY} = (HValPP_{XY,QP,P} - HValPP_{XY,QP,N})$
  - Calculate the orthogonality compensation factors
    - $Orth_{XY} = \frac{HValPP_{XY}}{HValPP_Z}$

Now the postprocessed Hall value can be calculated according to chapter 6.4.2.

As an example please take a look in the Excel file “Calculation of magnetic trimm values with FH3D12.xlsx”.

7
Digital Building Block

The digital part of the ASIC is separated into two main sub blocks:

- the communication interface with register set
- the state machine for measurement and decimation

The **communication interface** is asynchronous to the state machine. This allows for a fast communication up to 16 MHz.
It reads the serial data via the SPI and provides it as parallel data for the state machine. The measurement output values are written to the SPI so they can be read by the user.
It is important to note that during the communication the SPI clock must not exceed a frequency of 8 times the system clock frequency. Nevertheless both clock domains are fully static and the clocks can be reduced to 0 Hz.

The **state machine** uses the register content to control the analogue components. It adds up the ΣΔ modulator output values to a decimation value and provides the register set with this data.

7.1
Communication Interface

The communication interface is already described in chapter 4.1.

7.2
Control State Machine

The digital state machine is a complex building block which controls the analogue components according to the configuration set via the interface, performs measurement cycles and calculates output values from these measurements. The functions are described ‘bottom up’ here. The basic functions are explained first and the complex top level functions in the later chapters. Additional functions not directly involved in the measurement or signal processing algorithms are described last.

7.2.1
Sensor selection and analogue configuration

The state machine uses the parameters for measurement control present in the configuration registers. The sensor is selected according to the setting and the analogue blocks configured. The switching of the Hall phase is organized in a non-overlapping way.

Table 25: Decimation enable bit position, register 0x001

Bitpos.	Signal	Meaning
0	DecEn	"Decimation Enable" Setting this bit starts a new measurement. Deleting this bit cancels a running decimation.

7.2.2 Single phase measurement

During a measurement cycle the modulator is controlled according to the number of void cycles and measurement clock periods. The void cycles are necessary to let the analogue front end settle after the change of the Hall phase.
The decimation filter computes the output signals of the modulator to a single value. The result from this decimation represents a single phase measurement and can be read via the interface.

Table 26: Decimation length bit position, register 0x001

Bitpos.	Signal	Meaning
8-1	DecLen<11:4>	"Decimation Length"

DecLen<3:0> is always 0.
If DecLen<11:4> = 0, decimation length 1 will be used for test modes.

Table 27: Decimation wait state bit position, register 0x003

Bitpos.	Signal	Meaning
4-0	DecWait<7:3>	"Decimation Wait states" Number of void clock cycles before the decimation starts. DecWait<2:0> is always 0; DecWait has to be at least 8, so DecWait<7:3> has to be at least 1b.

After the measurement is finished, pin READY goes to high state and the measured value can be read from the result register. The ready flag can also be polled from register 0x102.

Table 28: Ready flag bit position, register 0x102

Bitpos.	Signal	Meaning
15	Ready	"Decimation Ready" Allows for a polling operation if the READY pin is not connected.

Reading from register 0100h indicates that the measurement result has been read completely and that the internal buffer can be used for the next measurement. If more than one register should be read, the address 0100h must be read last, as it resets the ready signal.

Table 29: Measurement value LSB bit position, register 0x100

Bitpos.	Signal	Meaning
15-0	DecVal<15:0>	"Decimation Value" Measurement value, LSBs

Table 30: Measurement value MSB bit position, register 0x102

Bitpos.	Signal	Meaning
1-0	DecVal<17:16>	"Decimation Value" Measurement value, MSBs

Pin READY can be configured with RM<1:0>. This is necessary if several chips use one ready wire. If only one chip is used ready mode should be set to RM<1:0> = 0x1.

Table 31: READY mode bit position, register 0x027

Bitpos.	Signal	Meaning
3	RM<1>	"Ready Mode" Ready Open Drain 0: pin: push – pull 1: pin: open drain
2	RM<0>	"Ready Mode" Ready Permanent 0: pin high-impedance is CS_N = 1 1: pin always active

7.2.3 Automatic 4-phase measurement

A 4-phase spinning current is needed to reduce the Hall sensors high single phase offsets. The digital state machine switches through the sensor phases and calculates the spinning current value automatically. The digital values from four single phase measurements are added in a configurable way. Together with the

single phase offsets, also the offset of the preamplifier is compensated. Such an automatic measurement will result in a value reaching at most four times the maximum of a single phase reading and consume four times the time.
The automatic 4-phase measurement is activated if at least one bit in “Auto4P” is set to 1. The bits Auto4P set the summation scheme. For example for the scheme -++- : 1001.

Table 32: 4-phase summation scheme, register 0x003

Bitpos.	Signal	Meaning
11-8	Auto4P<3:0>	“Automatic 4-Phase spinning signs” Sign order for automatic 4-phase measurement and calibration (standard: 1001).

It is important to note that with activated automatic 4-phase measurement the resulting value can be greater than the decimation length times ±7.5 times 4. Therefore, the MSBs must be read if a large decimation length value is set.

In contrast to the Hall sensor measurement the temperature measurement uses only a 2-phase measurement.

7.2.4
Read Value Register 1

If bit RVR1 is set it is possible to read the measurement value from register 0x001 while the new configuration is written to register 0x001. If the measurement is a magnetic four phase measurement the read value is DecVal[16:1]. If the measurement is a two phase temperature measurement the read value is DecVal[15:0]. If RngWarn is set during the measurement the read value will be 0x7FFF.

Writing to register 0x001 sets ready to zero if RVR1 is set.

Table 33: RVR1, register 0x027

Bitpos.	Signal	Meaning
1	RVR1	“Read Value Resister 1” Read the decimation value from register 0x001

7.3
Example of a Measuring Process

After the initial reset all registers are set to zero. Now the chip has to be configured. This configuration has to be done only once after the reset.

Now it's possible to start a measurement by choosing the sensor and setting the bit DecEn. Both can be done in register 0x001.
The chip does an automatic 4-phase measurement. If the measurement is done the measurement result is transferred into the measurement register and pin READY is set to high. Now the measurement value can be read. By reading the measurement value from register 0x100 the pin READY is set to low.
Now it's possible to start the next measurement.

7.3.1 Continuous measurement

Instead of waiting for a measurement completion and reading the output data before starting a new measurement also a continuous measurement procedure can be used. To enable this, the relevant registers have shadow registers. This way a new configuration can be written without effecting the configuration of the running measurement. The new configuration is taken over as soon as the running measurement is finished.
Continuous measurement procedure:
If a measurement is started externally before READY indicates the completion of a previous one, the IC triggers the next measurement not before READY goes high. Now the measurement is started internally, and the previous measurement data can be read from the interface. During the decimation the output data can be read, and the next measurement set up, which is again started after the current one is finished.
If a measurement is finished before the previous result is read from register 0100h, the next measurement is not started. It starts after the result is read from 0100h. Directly after that the actual result is available at the output registers.

7.3.2 Offset Centering

For every Hall sensor there is a dedicated register to store the offset centering values. During operation these values are regulated towards a minimum single-phase offset. The bit "OCAuto" in register 0x008 enables this function.
The registers are not directly accessible via the interface. Still register 0103h allows for transparent access to the offset centering register of the currently selected sensor. After every automatic 4-phase measurement the offset centering register of the measured sensor is updated with a new value minimizing the single-phase offset.

Table 34: Bit assignment, register 0x008

Bitpos.	Signal	Meaning
7-6	OCMode<1:0>	"Offset Centering Mode" Assignment of the offset centering values to the phases (standard setting: 10b). AmpOsCM: 10b; Phase 0: AmpOS0_1; Phase 1: AmpOS0_1; Phase 2: AmpOS0_0; Phase 3: AmpOS0_0
5	OCAuto	"Offset Centering Automatic" Enables the offset regulation.
4	OCSign	"Offset Centering Sign" Set the regulation direction.
3	OCToggle	"Offset Centering Toggle" Forces the offset centering to toggle between two settings.
2-0	OCGain<2:0>	"Offset Centering Gain" Set the regulation gain for offset centering.

Auto centering is only possible during the automatic 4-phase measurement as all phases are needed for calculation of the offset centering values. The regulated offset centering values can be read from register 0103h during operation.

Table 35: Bit assignment, register 0x010

Bitpos.	Signal	Meaning
15-8	OCVal1<7:0>	„ Offset Centering value 1" The offset centering value of the currently selected sensor.
7-0	OCVal0<7:0>	„ Offset Centering value 0" The offset centering value of the currently selected sensor.

The regulation works proportionally. Two times the first 16 summation cycles of the Sigma Delta decimation are used to calculate the difference between two corresponding spinning current phases. An adjustable number of digits of the difference is shifted to the edge and added to the offset centering value.

7.3.3
Control Flags

The FH3D12 has two diagnostic flags which allow for a basic self-monitoring.

RangeWarn indicates that the ADC input value is at the upper or lower limit. The bit is set if during a decimation eight sequenced ADC values are at the upper or lower limit.

HistWarn indicates that there might be an issue with the signal path. The bit is set if:

- More than three different ADC values are detected
- Missing ADC value between two ADC values.

Table 36: Diagnostic flag bit positions, register 0x102

Bitpos.	Signal	Meaning
14	HistWarn	"**Hist**ogram **Warn**ing" Indicates an improper distribution of ADC output values inside the possible range.
13	RngWarn	"Range Warning" Indicates that the ADC input signal exceeds the input range.

8 Detailed Building Block Description

8.1 Block Enable / Disable

The main building blocks in the design can be enabled separately. Thus the IC can be set to inactive modes to reduce power consumption during operation.
All power on bits are located in register 0x004.

8.2 Reset_N

During or at least after rise of the supply voltage (power on), pin RESET_N has to be set to 0 V to reset the chip. The reset affects the interface and the state machine. It is fed through directly to all registers and is released synchronized to a system clock edge.

8.3 References

An internal bandgap reference generates a constant voltage from which bias currents, excitation coil current, and the ADC references emerge. The bias current is generated with an integrated shunt and has to be trimmed.
Additionally, a temperature dependent signal is generated.

Table 37: References

Parameter	Min.	Typ.	Max.	Unit	Note
Positive Reference Voltage		2.1		V	
Negative Reference Voltage		0.9		V	
Bandgap Reference Voltage		1.2		V	Need to be trimmed
Bias current (trimmed)		10.0		µA	Need to be trimmed

The references block can be controlled by the following bits.

Table 38: References setting bit position, register 0x004

Bitpos.	Signal	Meaning
6	Bias_PO	"Bias Power On" Switch on the internal bandgap reference.

Table 39: References setting bit position, register 0x027

Bitpos.	Signal	Meaning
9-4	BGTrim<5:0>	"Bandgap Voltage Trimming"

Table 40: References setting bit position, register 0x027

Bitpos.	Signal	Meaning
13-10	SReg_or_IBias_Trim<3:0>	"Trim bits for sensor regulator and IBias generation" These bits can only be changed when TestIbURef or ICTIb is set to high. If TestIbURef or ICTIb is set to low the trim value for the reference current will be stored. The default value 1000b will be loaded automatically with setting BiasPO to high.

The bits SReg_or_IBias_Trim<3:0> are used to trim the reference current and the sensor regulator. To realize this dual use the trim value for the bias generation can only be changed when TestIbURef or ICTIb is set to high. If TestIbURef or ICTIb is set to low the trim value for the reference current will be stored.

8.4 Sensors

Two 3D Hall sensors, each with an X-/Y-/Z-Sensor, are arranged in a line parallel to the chip edge, 2.0 mm distant from each other.

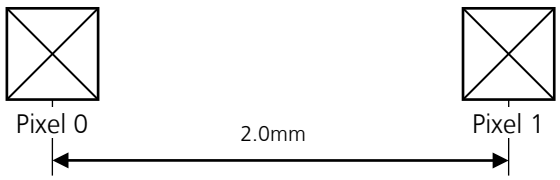

Figure 11: 3D Hall sensor arrangement

The sensor sensitivity, current consumption and offsets vary from chip to chip and over temperature.
The sensor parameters are normalized to the sensor supply voltage of 2.6 V.

Table 41: Hall sensor sensitivity and resistance

Parameter	Min.	Typ.	Max.	Unit	Note
Sensitivity X-/Y-sensor		54		mV/T	at 2.6 V sensor supply voltage, 25°C
Sensitivity Z-sensor		95		mV/T	
Resistance X-/Y-sensor		850		Ω	
Resistance Z-sensor		1135		Ω	

The position of the 3D Hall sensors is shown in the following bond diagram.

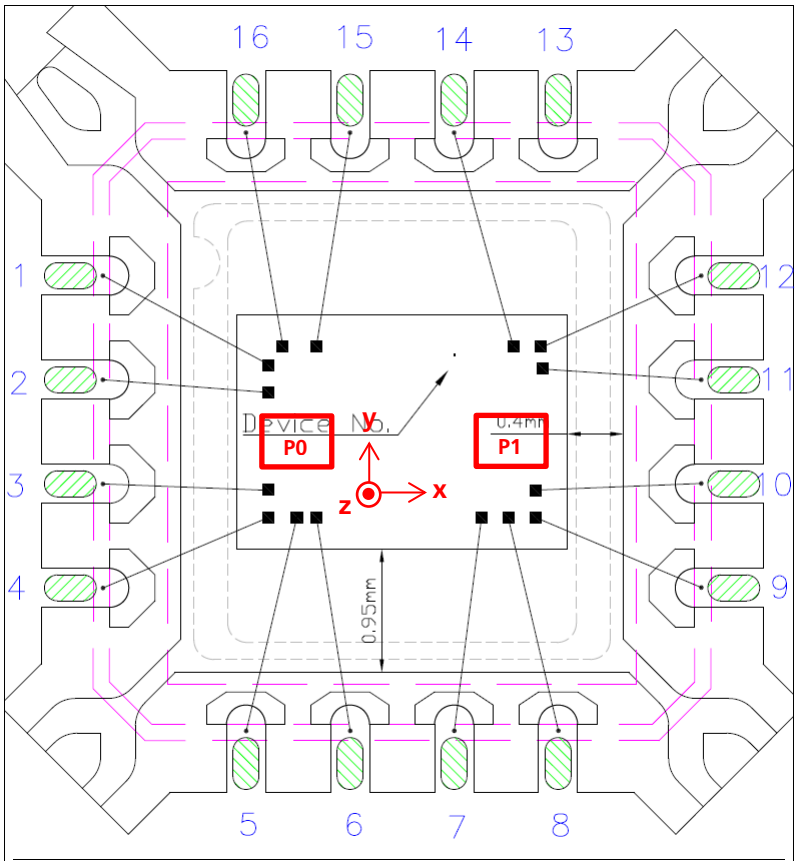

Figure 12: Bond diagram

The exact position on silicon chip according to design database is:

P0: 232 µm / 762 µm P1: 2232 µm / 762 µm

8.5 Sensor multiplexer

The sensor multiplexer activates the desired 3D Hall sensor, sensor type and phase.

The configuration bits are present in register 0x001, 0x002 and 0x004.

Table 42: Sensor setting bit position, register 0x001

Bitpos.	Signal	Meaning
11	PixelSel	“Pixel Select” Pixel 0 [0], Pixel 1 [1]
10-9	SensSel<1:0>	“Sensor Select” X [00], Y [01], Z [10]

Table 43: Sensor setting bit position, register 0x002

Bitpos.	Signal	Meaning
1-0	Phase<1:0>	“Phase setting” Sets the spinning current phase for all sensors.

The sensors need to be enabled to output a signal. The supply and sensor output can be enabled separately. Without the sensor output enable the preamplifiers input is floating and an external signal can be fed to it.

Table 44: Sensor enable bit position, register 0x004

Bitpos.	Signal	Meaning
1	SMUXPowEn	“Sensor-Multiplexer Power Enable“ Enable of the sensor supply transistors.
0	SMUXSigEn	“Sensor-Multiplexer Signal Enable“ Enable the transmission gates between sensor output and preamplifier.

Three additional bits allow the configuration of the sensor multiplexer.

Table 45: Sensor enable bit position, register 0x003

Bitpos.	Signal	Meaning
7	SMUXChopInv	“Sensor-Multiplexer Chopper Invert“ Inverts the Hall signal for offset compensation.
6	SMUXChopFast	“Sensor-Multiplexer Chopper Fast“ Enables the fast chopper mode.
5	SMUXDisComp	“Sensor-Multiplexer Disable Compensation“ Disables a compensation signal.

8.6 Sensor Supply Voltage Regulator

The sensor supply voltage can be controlled by an integrated supply regulator. The voltage of the negative supply node UN and the differential sensor supply voltage UD can be set, both present in register 0x002. Additionally, the sensor supply voltage can be trimmed SRegTrim<3:0> in register 0x027.
If the signals SRegN_PO and SRegD_PO (register 0x004) are deactivated, the sensors are directly connected to VDD and VSS.

Table 46: Sensor supply regulator settings

SMPowEN	SRegNPO	SRegDPn	Sensor supply	
			Low supply	High supply
0	X	X	off	off
1	0	0	VSS	VDD
1	0	1	VSS	regulated
1	1	0	regulated	VDD
1	1	1	regulated	regulated

The voltages at the supply nodes affect all sensors identically.
With sensor supply voltage regulator enabled six modes of operation can be selected.

Table 47: Sensor Supply modes

Mode	UN	SRegNVal	UD	SRegDVal
Standard (Default)	0.2 V	0	2.6 V	5
Low offset	0.5 V	2	2.0 V	3
High sensitivity (VDD > 3.2 V)	0.2 V	0	2.8 V	6
Half sensitivity	0.65 V	3	1.3 V	2
Quarter sensitivity	0.95 V	5	0.65 V	1
Eighth sensitivity	1.1 V	6	0.325 V	0

UN: negative sensor supply node

UD: differential sensor supply voltage

The sensor supply voltages must be set to a reasonable value matching to the input range of the pre-amplifier. Note that the differential supply voltage is critical for the sensors sensitivity.

Table 48: Sensor supply bit position, register 0x004

Bitpos.	Signal	Meaning
3	SRegN_PO	"Sensor supply voltage Regulator Negative Power On" 1: lower supply voltage is regulated, 0: power off for lower supply voltage => if SMPowEN = [1], then the sensor connected directly to VSS
2	SRegD_PO	"Sensor supply voltage Regulator Differential Power On" Activates the regulator for the sensor supply voltage. 1: differential supply voltage is regulated, 0: power off for differential supply voltage regulator => if SMPowEN = [1], then the sensor is connected directly to VDD

Table 49: Sensor supply bit position, register 0x002

Bitpos.	Signal	Meaning
15-13	SRegDVal<2:0>	"Sensory supply voltage Regulator Differential Value"
12-10	SRegNVal<2:0>	"Sensor supply voltage Regulator Negative Value"

Table 50: Sensor supply bit position, register 0x027

Bitpos.	Signal	Meaning	Note
13-10	SReg_or_IBias_Trim<3:0>	"Trim bits for sensor regulator and IBias generation"	Need to be trimmed

The supply voltage regulator is separated into two sub blocks:
SupRegSetPoint generates the analogue set point for the regulators
SupReg contains the opamps which regulate the voltage at the negative and positive supply to the defined voltages

The set point DAC translates the digital input to analogue reference output values for the sensor supply regulator.
Depending on the 1.2 V reference voltage and the operational amplifier offset the sensor supply voltages have limited accuracy. To increase the accuracy, it is possible to trim the set point DAC.

8.7 Excitation Coil and Current DAC

Every sensor is magnetically coupled to an excitation coil which can apply a magnetic field to the sensors. The current through this coil is generated by a 3-bit current DAC, whose digit converts into a current I0, typically 100 µA. The output stage can work in a low voltage and high voltage mode, where the output current is multiplied by 2 or 14. This results in a current range from typically 0.2 to 1.6 mA in the low voltage mode and from 1.4 to 11.2 mA in the high voltage mode.

EnHV=0: current=0.2 mA x (ECVal<2:0> + 1)

EnHV=1: current=1.4 mA x (ECVal<2:0> + 1)

Due to the orientation of the sensors two different coils are necessary to apply magnetic fields to the vertical and horizontal sensors.

Two additional coils are placed to enable distance measurements between coil and sensor and cross sensitivity measurements between X- and Y- to Z- sensors.
The physical width of the coil metal wires is only 0.95 µm at the narrowest point. According to the design rules the maximum allowed dc current is 0.63 mA at 125°C. Because the coils are used in AC mode, higher currents can be applied during the routine test of the chip.

Table 51: Excitation coil parameters, measured on a small number of samples from eng. and prod lot

Parameter	Min.	Typ.	Max.	Unit
Coil factor X- and Y-sensor		191		µT/mA
Coil factor Z-sensor		182		µT/mA
Calibration coil factor X- and Y-sensor	115		160	µT/mA
Cross sensitivity X- and Y-sensor		0		µT/mA
Current per digit; ENHV = 0		0.2		mA
Current per digit; ENHV = 1		1.4		mA

Table 52: Current source power on bit position, register 0x004

Bitpos.	Signal	Meaning
7	EC_PO	„Excitation Current Power On“ Switch on the excitation current source.

Table 53: Excitation current setting bit position, register 0x002

Bitpos.	Signal	Meaning
9-7	ECCSel<2:0>	„Excitation Current Coil Select“ Activates the calibration coil. 0: coils off 1: -> QP1; 2: XYP1; 3: ZP1 + HP0 4: -> ZP0 + HP1; 5: XYP0; 6: QP0
6-4	ECVal<2:0>	„Excitation Curent Value“
3	ECSign	“Excitation Current Sign“ Direction of the excitation current.
2	ECEnHV	“Excitation Current Enable High Voltage“ Enables the high voltage mode

Due to the rotations of the pixels the excitation coils have the following signs

Table 54: Excitation of the single sensors

Pixel 0		Pixel 1	
XY	X: - Y: -	XY	X: - Y: +
Z	Z: +	Z	Z: -
Q	Z: +	Q	Z: -
H	X: - Y: -	H	X: - Y: +

8.8 Temperature Measurement

The chip contains a linear temperature sensor. A separate buffer provides the ADC with the appropriate signal strength. The intrinsic buffer offset is eliminated by chopping the input signal.
The measurement is treated like a normal signal reading where the temperature sensor represents a special sensor. It can be activated by selecting bit TempSel.
Please note, that even with inverted input signals the temperature output signal is not inverted but only shifted by the intrinsic offset. This allows for a quasi-calibration measurement on the temperature sensor with an offset free result.

Table 55: Temperature sensor select bit position, register 0x001

Bitpos.	Signal	Meaning
12	TempSel	"Temperature Select" Select the temperature sensor.

8.9 Programmable Gain Amplifier

Single stage analogue low-noise instrument amplifier with gain steps of 32, 64, 128, 256, 512 and 1024. For very large magnetic fields, the sensor supply and hence the sensor sensitivity can be reduced.

Table 56: Amplifier power on bit position, register 0x004

Bitpos.	Signal	Meaning
4	Amp_PO	"Amplifier Power On" Switch on the preamplifier.

Table 57: Amplifier gain, register 0x001

Bitpos.	Signal	Meaning
15-13	AmpGain<2:0>	"Amplifier Gain" Set the Gain.

Table 58: PGA parameters

Parameter	Min.	Typ.	Max.	Unit
Gain in setting 000		32		V/V
Gain in setting 001		64		V/V
Gain in setting 010		128		V/V
Gain in setting 011		256		V/V
Gain in setting 100		512		V/V
Gain in setting 101		1024		V/V

8.10 Offset-Centering

This mechanism allows for the use of a large input range of the ADC even if the single phase offset of the Hall sensors is large. An additional offset is applied to the sensor output compensating for a better part of it. Every sensor needs two different offset values for compensation. They are regulated automatically or can be set manually.

The offset centering is realized as a current source which is connected to the sensor. Depending on the sign its effect is positive or negative.

The control word is 8 bit signed integer.

If the centering current is derived from the sensor current, the step size is independent of the sensors resistance.

Table 59: Offset centering parameters

Parameter	Min.	Typ.	Max.	Unit
Generated offset voltage per digit		200		µV

The offset centering can be operated manually or in an automatic mode. The automatic mode is described in chapter 7.3.2.

Table 60: Offset Centering power on bit position, register 0x004

Bitpos.	Signal	Meaning
10	OC_PO	"Offset Centering Power On " Switch on the offset centering.

Table 61: Offset Centering values, register 0x010

Bitpos.	Signal	Meaning
15-8	OCVal1<7:0>	"Offset Centering Value 1" The values are used for offset centering.
7-0	OCVal0<7:0>	"Offset Centering Value 0" The values are used for offset centering.

Due to the internal wiring this register is not applied directly after writing but only if a measurement is started (bit 0 in register 0001h). Additionally, the configuration must not be written a second time before starting the measurement. Otherwise it would not be applied. There are two further ways to generate the centering current which can be configured in register 0x008.

Table 62: Register 0x008 content

Bitpos.	Signal	Meaning
9	OCRInt	Offset Centering R Internal 0: Use external sensor matched resistor 1: Use internal reference resistor
8	OCIRefR	Offset Centering Current Reference Resistor 0: Use external sensor voltage control current 1: Use reference / replica resistor generated current

8.11 Buffer

As the PGA itself cannot drive the switched capacitor circuitry of the ADC, additional buffers are needed between the two blocks. The buffer gain is typically 1.
The buffer works as multiplexer to switch between magnetic signal and temperature signal. As the temperature signal has a much lower voltage the input type is PMOS in, whereas the magnetic signal input type is NMOS. The input is switched automatically depending on the activated sensor.

Table 63: Buffer power on bit position, register 0x004

Bitpos.	Signal	Meaning
8	Buf_PO	"Buffer Power On" Enables the ADC buffers between PGA and ADC.

The input selection is automatically done by choosing the temperature sensor.

Table 64: Choosing the temperature Sensor 0x001

Bitpos.	Signal	Meaning
12	TempSel	"Temperature Select" Select the temperature sensor.

8.12 Sigma-Delta Modulator

The Sigma-Delta-Modulator converts the analogue values into digital data. It can be clocked with a maximum frequency of 8 MHz at the most. With the 4-bit topology and the decimation length register width of 12 bit the maximum possible resolution is 16 bit. The modulator input is fully differential. Positive and negative signals symmetrical to 0.

Table 65: Modulator power on bit position, register 0x004

Bitpos.	Signal	Meaning
9	ModRefBuf_PO	"Modulator Reference Buffer Power On" Switch on the reference buffer
5	Mod_PO	"Modulator Power On" Switch on the ADC.

At the beginning of a measurement the input signal has to settle so that the first ADC codes are correct. A void cycle counter allows the analogue signal to settle after a new measurement cycle is triggered. See setting DecWait register 003h.

8.13 Module End of Line Test

FH3D12 has no nonvolatile memory, so it has to be trimmed during the module end of life test. The following values have to be measured.

- Bandgap voltage: The bandgap voltage has to be measured and trimmed to 1.18 V with an accuracy of 0.5 mV, using a high impedance input DMM. The trim value has to be stored in the µC and has to be written to the ASIC during the configuration phase.
- Reference current: The reference current has to be measured and trimmed to 10 µA with an accuracy of 0.1 µA. The trim value has to be stored in the µC and has to be written to the ASIC during the configuration phase.

- Sensor supply voltage regulator: If necessary the positive sensor supply node has to be trimmed to 2.8 V. The trim value has to be stored in the µC and has to be written to the ASIC during the configuration phase.

Table 66: Module Test access bit position, register 0x008

Bitpos.	**Signal**	Meaning
13	ICTUP	In-Circuit-Test UP Switch positive sensor supply voltage to *TEST*
12	ICTUN	In-Circuit-Test UN Switch negative sensor supply voltage to *TEST*
11	ICTIb	In-Circuit-Test Ib Switch 10uA reference current to *TEST*
10	ICTURef	In-Circuit-Test URef Switch bandgap reference voltage to *TEST*

8.14 System Clock

The system clock has to be fed in via the dedicated CLK pad. The typical clock frequency is 8 MHz. Any floating state of CLK has to be prevented.

The SPI interface is independent from the system clock and can be controlled asynchronously.

Table 67: CLK parameters

Parameter	**Min.**	**Typ.**	**Max.**	**Unit**	Note
Typical CLK frequency	7.95	8.0	8.05	MHz	The characterization of the chip was done with a frequency 8 MHz.
Maximum frequency range	1.0	8.0	8.05	MHz	
Duty Cycle	49	50	51	%	

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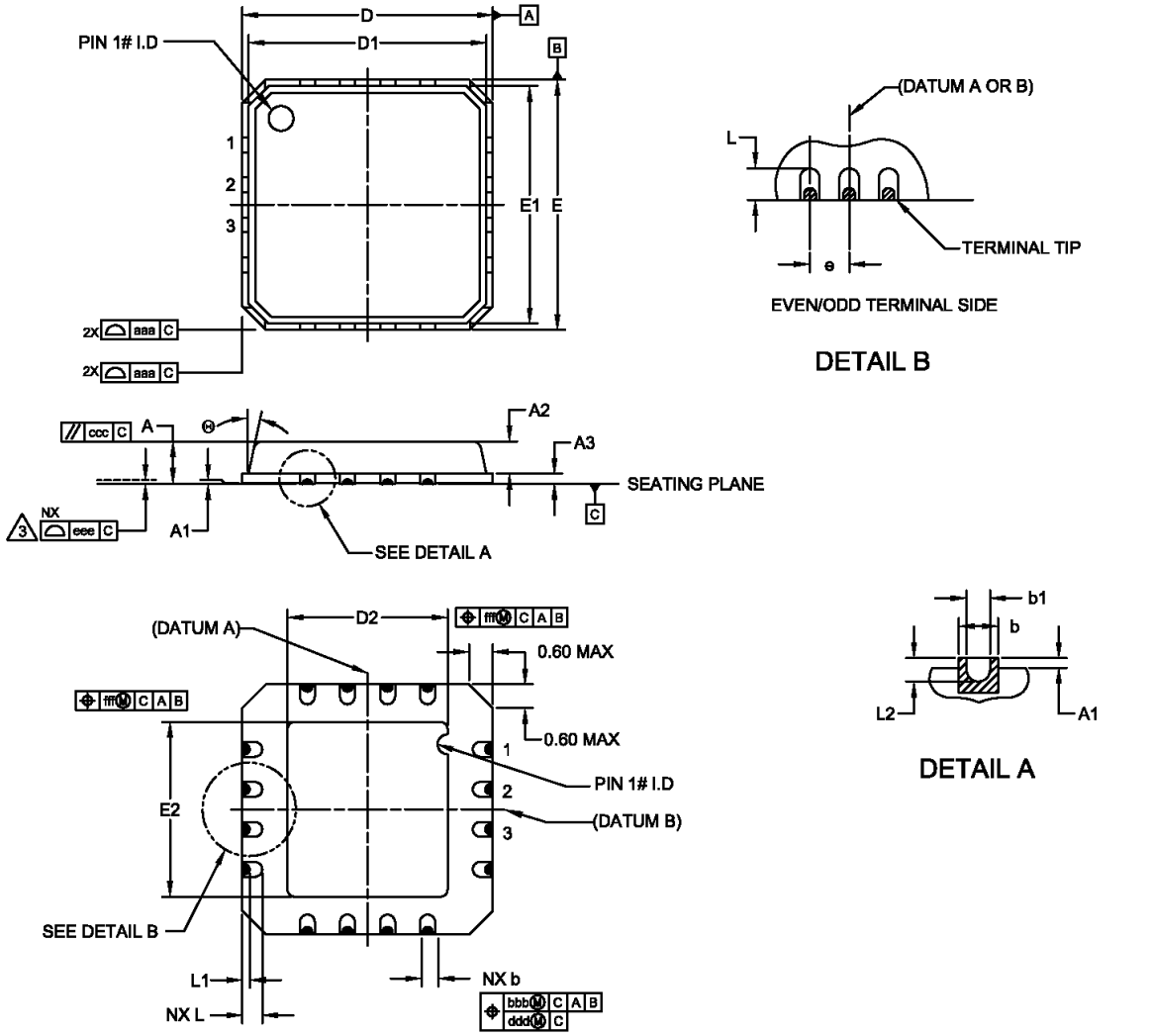
Package Information



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.01	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.30	0.40	0.50
L1	0.05	0.15	0.25
L2	0.05	0.10	0.15
Θ	0°	-	14°
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
e		0.80 BSC	
D1		4.75 BSC	
E1		4.75 BSC	
D2	3.10	3.20	3.30
E2	3.40	3.50	3.60
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		16	

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINAL.
4. RADIUS ON TERMINAL IS OPTIONAL.
5. N IS THE TOTAL NUMBER OF TERMINALS.

Figure 13: Block description

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