TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
'LS95B	36 MHz	65 mW

description

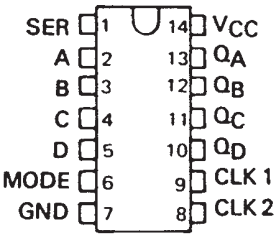
These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

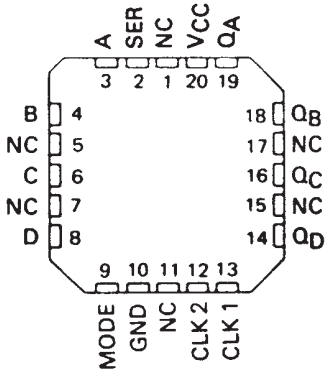
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

SN5495A, SN54LS95B . . . J OR W PACKAGE
SN7495A . . . N PACKAGE
SN74LS95B . . . D OR N PACKAGE
(TOP VIEW)



SN54LS95B . . . FK PACKAGE
(TOP VIEW)



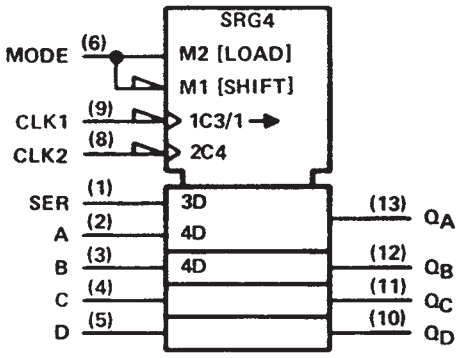
NC - No internal connection

FUNCTION TABLE

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

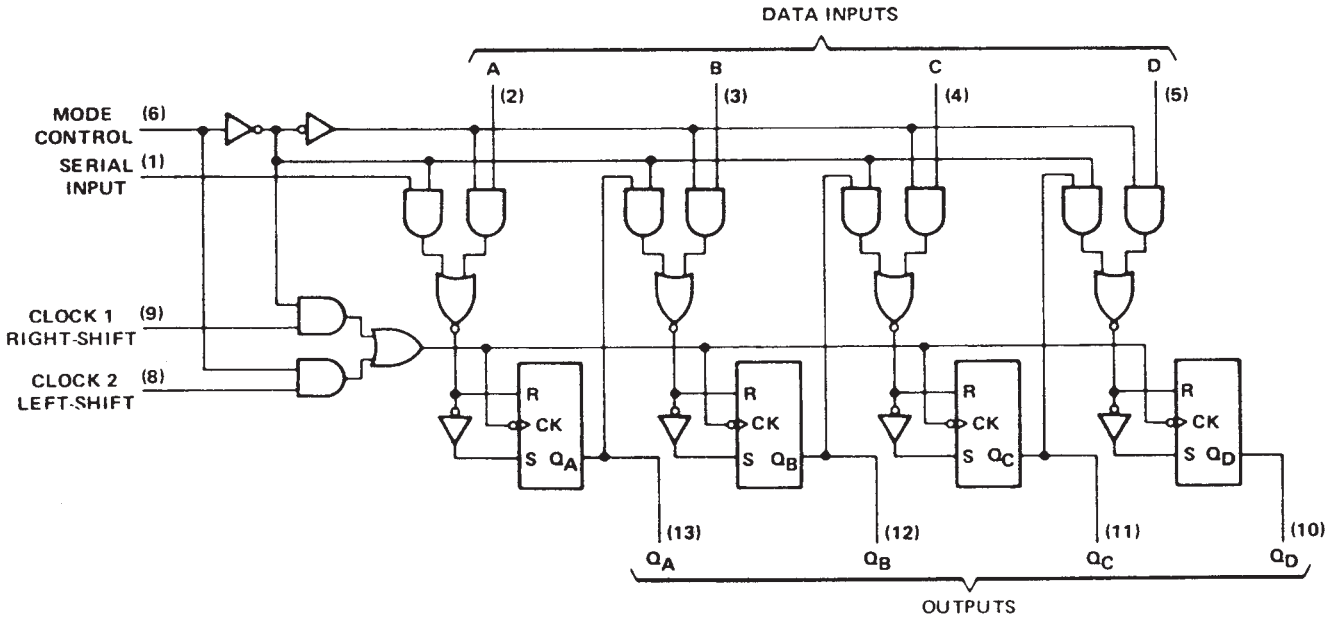
†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

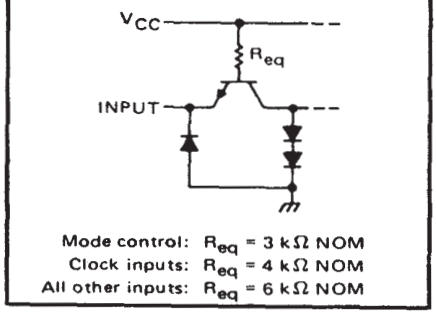
logic diagram (positive logic)



schematics of inputs and outputs

'95A

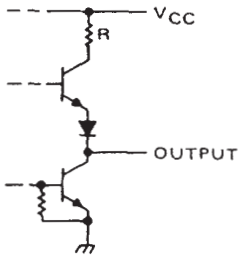
EQUIVALENT OF EACH INPUT



Mode control: R_{eq} = 3 kΩ NOM
Clock inputs: R_{eq} = 4 kΩ NOM
All other inputs: R_{eq} = 6 kΩ NOM

'95A

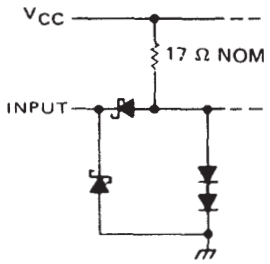
TYPICAL OF ALL OUTPUTS



'95A: R = 100 Ω
'L95: R = 500 Ω

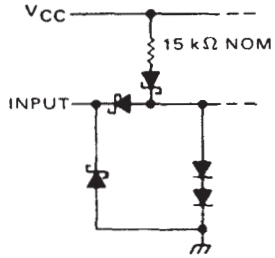
'LS95B

EQUIVALENT OF CLOCK AND MODE CONTROL INPUTS



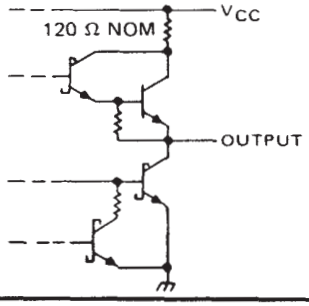
'LS95B

EQUIVALENT OF DATA AND SERIAL INPUTS



'LS95B

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54′	SN54LS′	SN74′	SN74LS′	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Interemitter voltage (see Note 2)	5.5		5.5		V
Operating free-air temperature range	−55 to 125		0 to 70		°C
Storge temperature range	−65 to 150		−65 to 150		°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies between the clock-2 input and the mode control input of the '95A.

recommended operating conditions

	SN5495A			SN7495A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (See Figure 1)	20			20			ns
Setup time, high-level or low-level data, t_{su} (See Figure 1)	15			15			ns
Hold time, high-level or low-level data, t_h (See Figure 1)	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (See Figure 2)	15			15			ns
Time to enable clock 2 (See Figure 2)	15			15			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (See Figure 2)	5			5			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (See Figure 2)	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5495A			SN7495A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Mode control				80			80	
I_{IL}	Low-level input current	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Mode control				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		39	63		39	63	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	32	ns

recommended operating conditions

	SN54LS95B			SN74LS95B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	20			20			ns
Setup time, high-level or low-level data, t_{su} (see Figure 1)	20			20			ns
Hold time, high-level or low-level data, t_h (see Figure 1)	20			10			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2)	20			20			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2)	20			20			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2)	20			20			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 2)	20			20			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

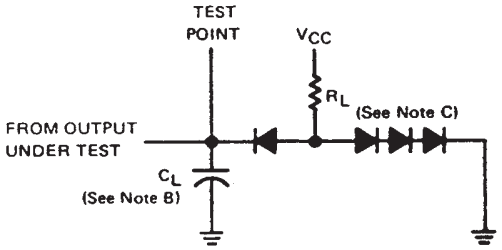
PARAMETER		TEST CONDITIONS†		SN54LS95B			SN74LS95B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		13	21		13	21	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

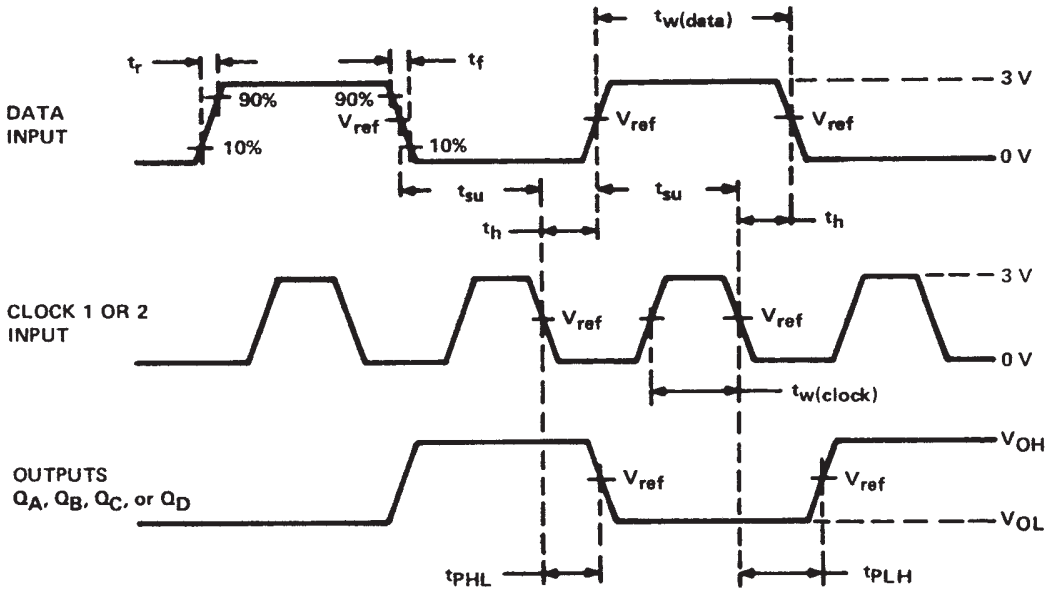
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	32	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and $Z_{out} \approx 50\ \Omega$. For the data pulse generator, PRR = 500 kHz; for the clock pulse generator, PRR = 1 MHz. When testing f_{max}, vary PRR. For '95A, $t_{w(data)} \geq 20$ns, $t_{w(clock)} \geq 15$ ns. For 'LS95B, $t_{w(data)} \geq 20$ ns, $t_{w(clock)} \geq 15$ ns.

B. C_L includes probe and jig capacitance.

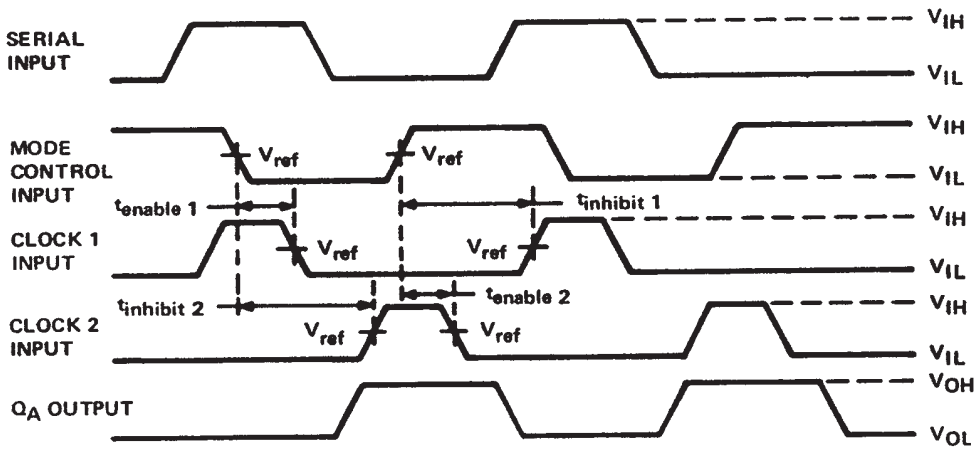
C. All diodes are 1N3064 equivalent.

D. For '95A, $V_{ref} = 1.5$ V; for 'LS95B, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS

FIGURE 1-SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input is at a low level.
B. For '95A, V_{ref} = 1.5 V; for 'LS958, V_{ref} = 1.3 V.

VOLTAGE WAVEFORMS

FIGURE 2-CLOCK ENABLE/INHIBIT TIMES

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN5495AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SN7495AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
SN7495AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	0 to 70		
SN7495AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7495AN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS95BD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74LS95BD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74LS95BDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74LS95BDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70		
SN74LS95BN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN74LS95BN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SNJ5495AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5495AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5495AW	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	-55 to 125		
SNJ5495AW	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF SN5495A, SN7495A :

- Catalog: SN7495A
- Military: SN5495A

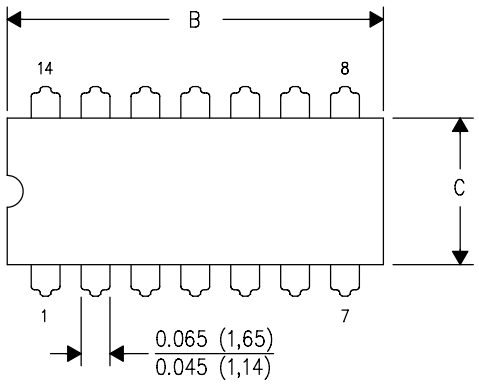
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

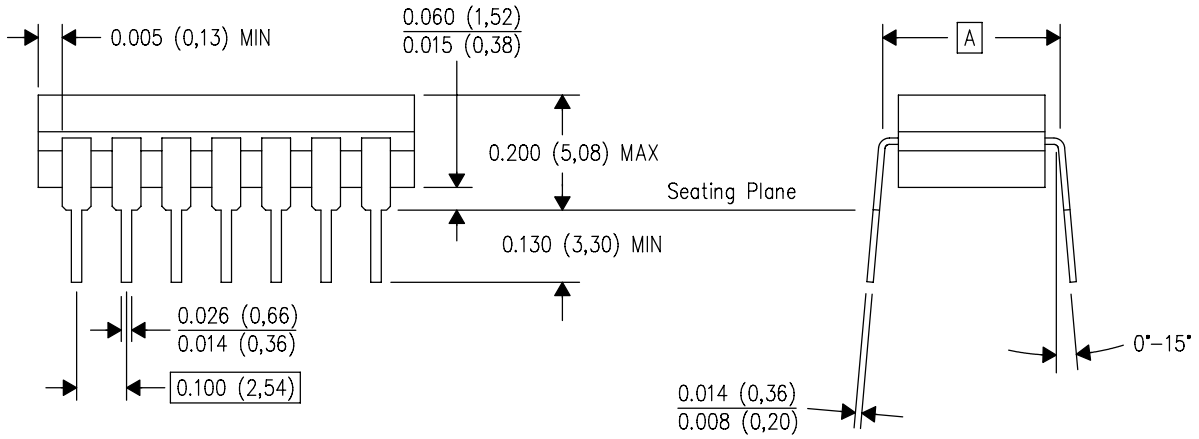
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



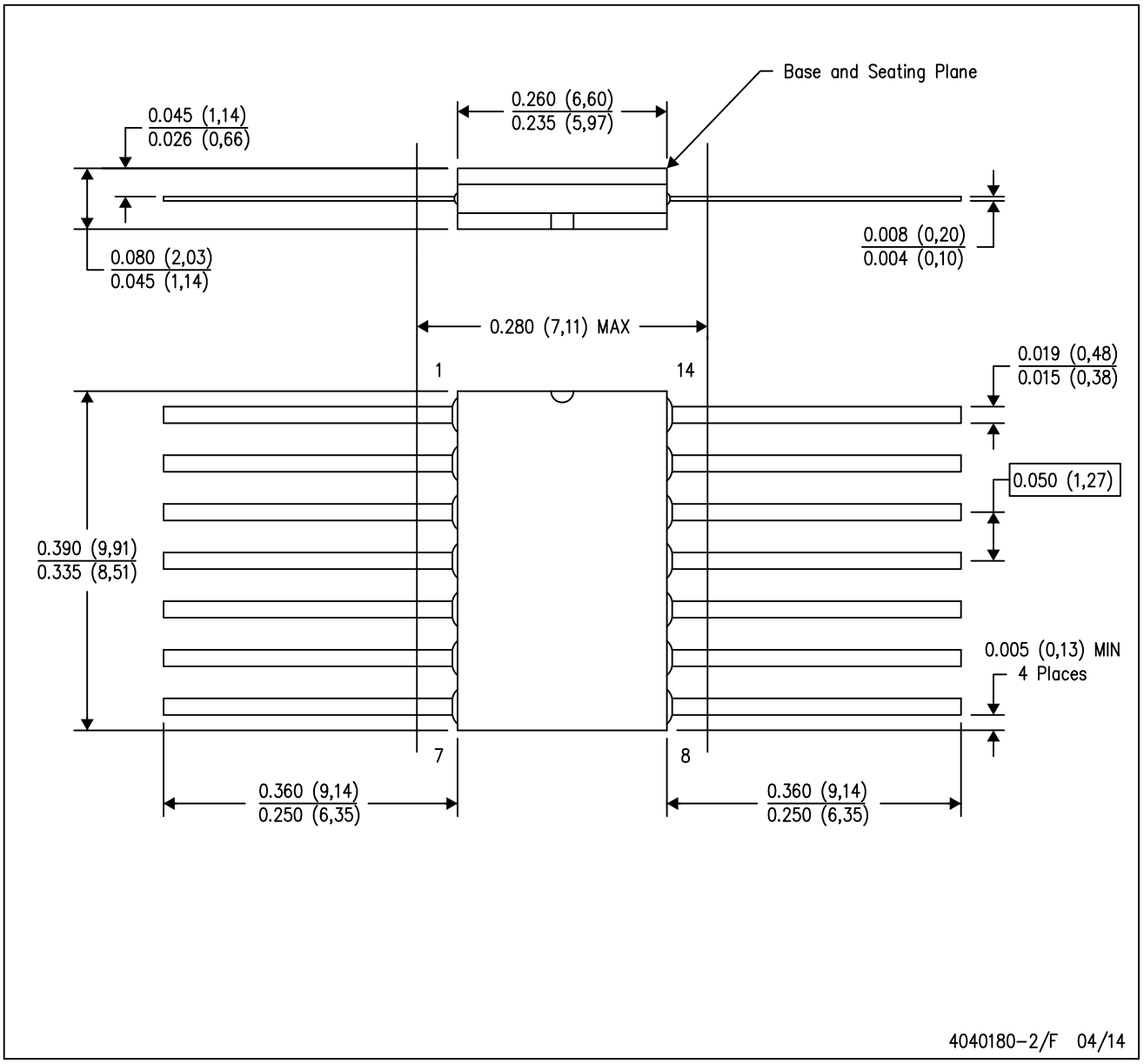
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

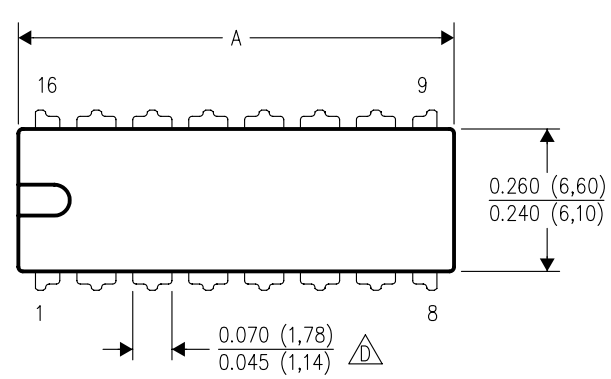


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

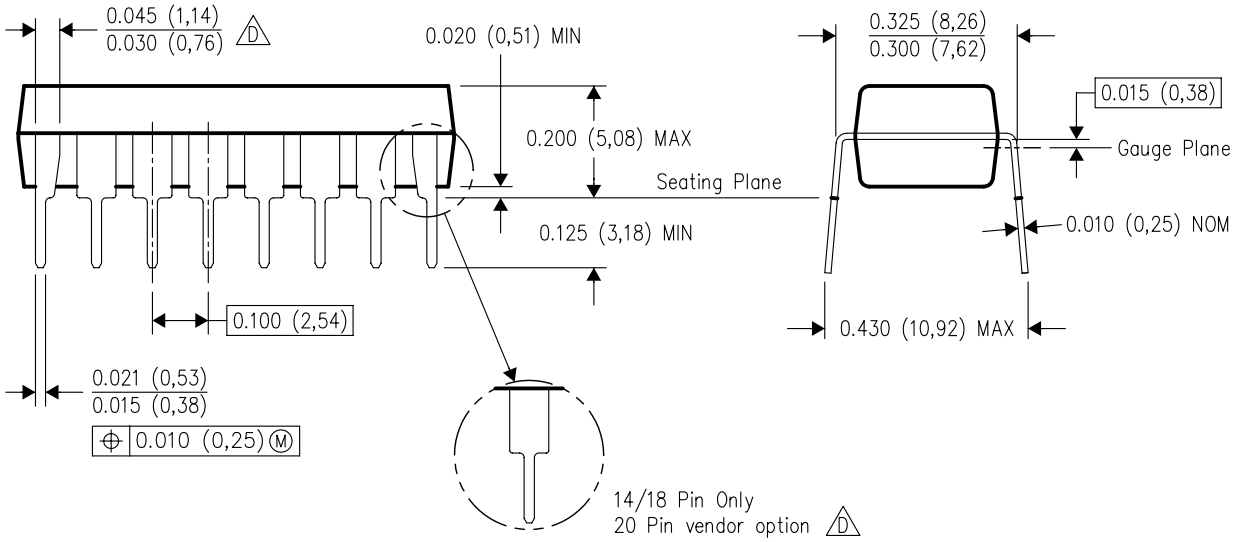
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



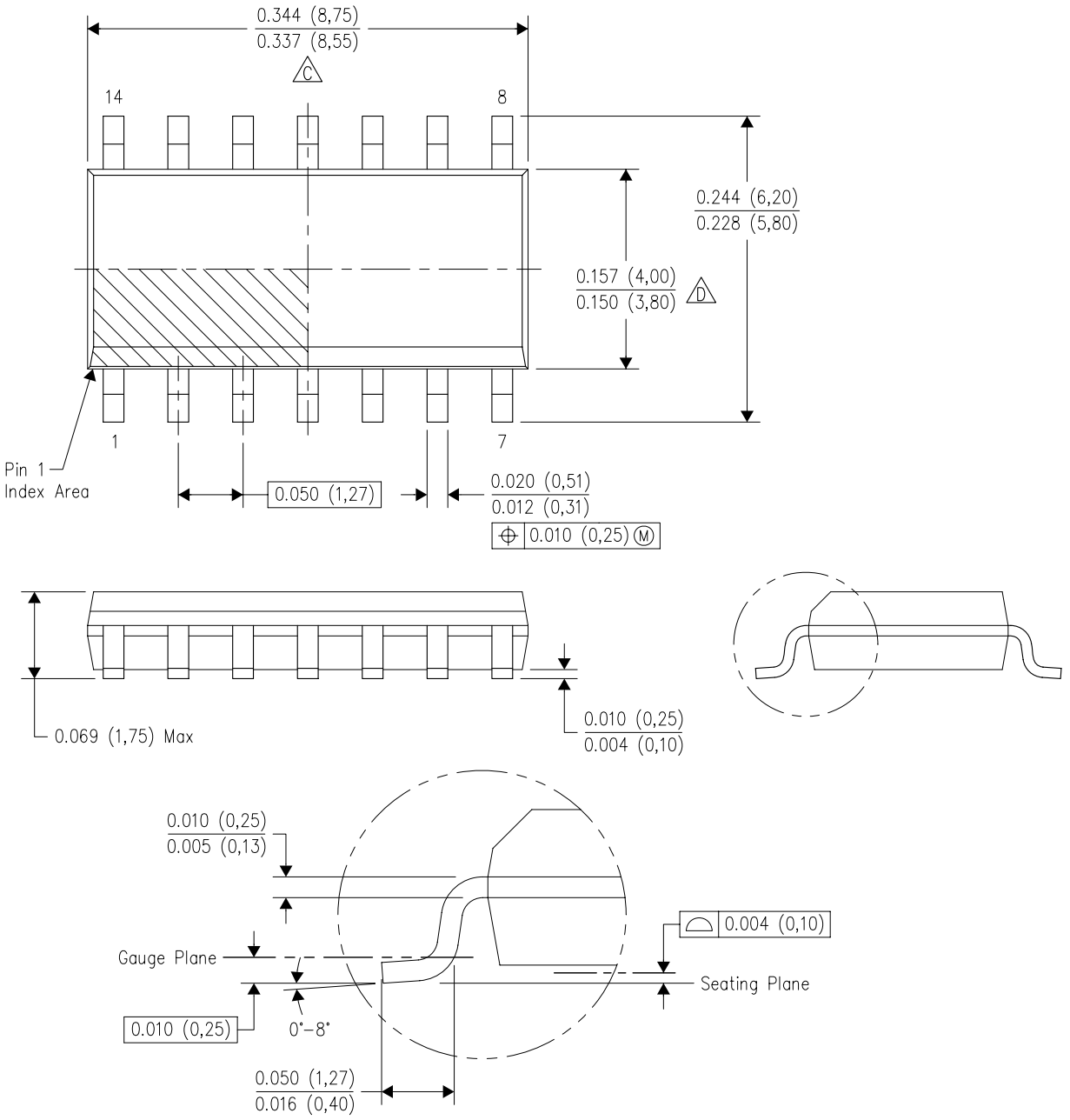
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265