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CD74HCT4052, CD54/74HC4053, CD54/74HC54053 HIGH-SPEED CMOS LOGIC ANALOG MULTIPLEXERS/DEMULTIPLEXERS

Check for Samples: CD/74HC4051, CD54/74HCT4051, CD54/74HC4052,

FEATURES

- Wide Analog Input Voltage Range. . ±5 V Max
- Low ON Resistance
 - 70 Ω Typical ($V_{CC} V_{EE} = 4.5 V$)
 - 40 Ω Typical (V_{CC} V_{EE} = 9 V)
- Low Crosstalk Between Switches
- Fast Switching and Propagation Speeds
- Break-Before-Make Switching
- Wide Operating Temperature Range -55°C to 125°C
- CD54HC/CD74HC Types
 - Operation Control Voltage 2 V to 6 V
 - Switch Voltage 0 V to 10 V
 - «
- CD54HCT/CD74HCT Types
 - Operation Control Voltage . . . 4.5 V to 5.5 V
 - Switch Voltage 0 V to 10
 - V

- Direct LSTTL Input Logic Compatibility $V_{IL} = 0.8 V Max$, $V_{IH} = 2 V Min$
- − CMOS Input Compatibility $I_{I} \le 1 \ \mu A$ at V_{OL} , V_{OH}

DESCRIPTION

These devices are digitally controlled analog switches which utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e., V_{CC} to V_{EE}). They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low ON resistance and low OFF leakages. In addition, all three devices have an enable control which, when high, disables all switches to their OFF state.

v	ORDERING INFORMATION ⁽¹⁾	
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4051F3A	-55 to 125	16 Ld CERDIP
CD54HC4052F3A	-55 to 125	16 Ld CERDIP
CD54HC4053F3A	-55 to 125	16 Ld CERDIP
CD54HCT4051F3A	-55 to 125	16 Ld CERDIP
CD74HC4051E	-55 to 125	16 Ld PDIP
CD74HC4051M	-55 to 125	16 Ld SOIC
CD74HC4051MT	-55 to 125	16 Ld SOIC
CD74HC4051M96G3	-55 to 125	16 Ld SOIC
CD74HC4051NSR	-55 to 125	16 Ld SOP
CD74HC4051PWR	-55 to 125	16 Ld TSSOP
CD74HC4051PWT	-55 to 125	16 Ld TSSOP
CD74HC4052E	-55 to 125	16 Ld PDIP
CD74HC4052M	-55 to 125	16 Ld SOIC
CD74HC4052MT	-55 to 125	16 Ld SOIC
CD74HC4052M96G3	-55 to 125	16 Ld SOIC
CD74HC4052NSR	-55 to 125	16 Ld SOP
CD74HC4052PW	-55 to 125	16 Ld TSSOP
CD74HC4052PWR	-55 to 125	16 Ld TSSOP

(1) When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.



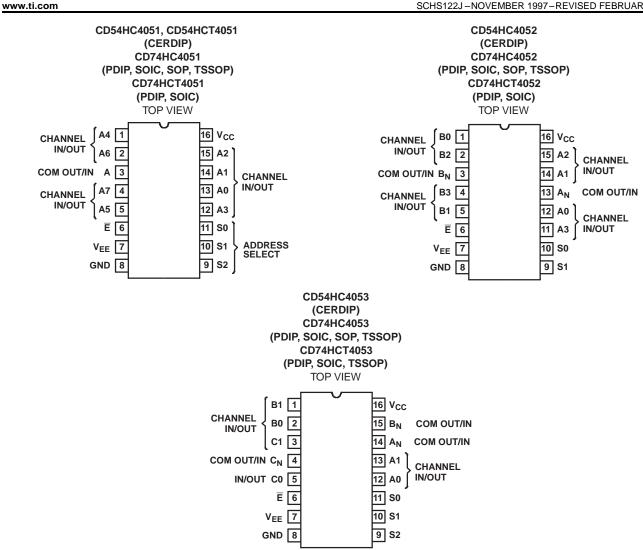
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OR	DERING INFORMATION ⁽¹⁾ (continue	ed)
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC4052PWT	-55 to 125	16 Ld TSSOP
CD74HC4053E	-55 to 125	16 Ld PDIP
CD74HC4053M	-55 to 125	16 Ld SOIC
CD74HC4053MT	-55 to 125	16 Ld SOIC
CD74HC4053M96G3	-55 to 125	16 Ld SOIC
CD74HC4053NSR	-55 to 125	16 Ld SOP
CD74HC4053PW	-55 to 125	16 Ld TSSOP
CD74HC4053PWRG3	-55 to 125	16 Ld TSSOP
CD74HC4053PWT	-55 to 125	16 Ld TSSOP
CD74HCT4051E	-55 to 125	16 Ld PDIP
CD74HCT4051M	-55 to 125	16 Ld SOIC
CD74HCT4051MT	-55 to 125	16 Ld SOIC
CD74HCT4051M96	-55 to 125	16 Ld SOIC
CD74HCT4052E	-55 to 125	16 Ld PDIP
CD74HCT4052M	-55 to 125	16 Ld SOIC
CD74HCT4052MT	-55 to 125	16 Ld SOIC
CD74HCT4052M96	-55 to 125	16 Ld SOIC
CDHCT4053E	-55 to 125	16 Ld PDIP
CDHCT4053M	-55 to 125	16 Ld SOIC
CDHCT4053MT	-55 to 125	16 Ld SOIC
CDHCT4053M96	-55 to 125	16 Ld SOIC
CDHCT4053PWR	-55 to 125	16 Ld TSSOP
CDHCT4053PWT	-55 to 125	16 Ld TSSOP





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TEXAS INSTRUMENTS

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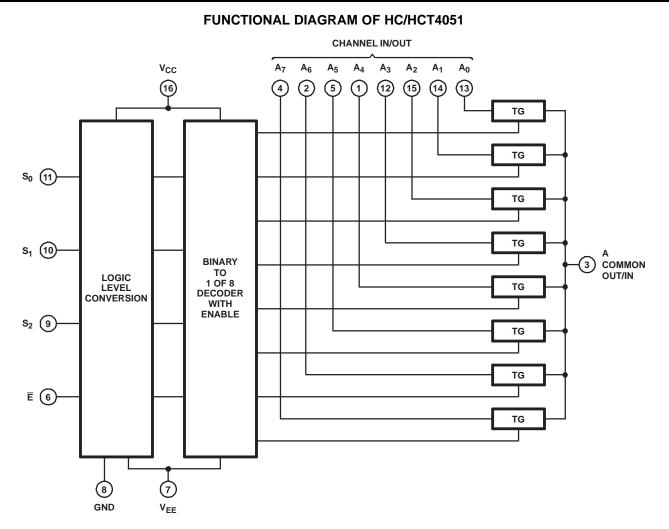


Table 1. TRUTH TABLE 'HC/CD74HCT4051⁽¹⁾

	INPUT	STATES		ON CHANNELS
ENABLE	S ₂	S ₁	S ₀	
L	L	L	L	A0
L	L	L	Н	A1
L	L	Н	L	A2
L	L	Н	Н	A3
L	Н	L	L	A4
L	Н	L	Н	A5
L	Н	Н	L	A6
L	Н	Н	Н	A7
Н	Х	Х	Х	None

(1) X = Don't care

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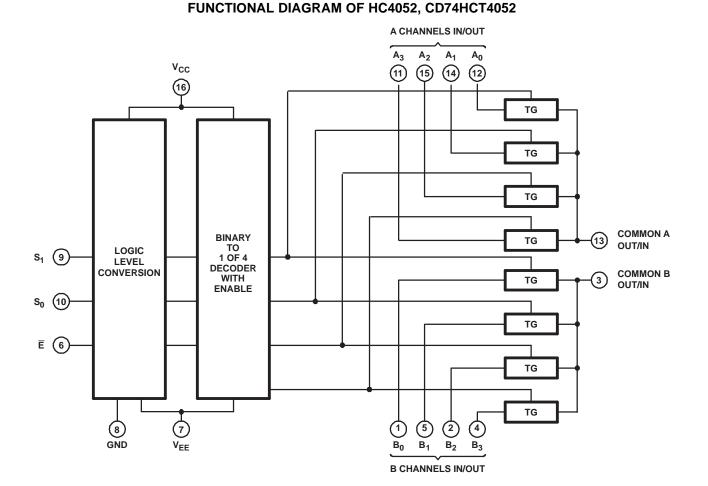


Table 2. FUNCTION TABLE 'HC4052, CD74HCT4052⁽¹⁾

	INPUT STATES		ON CHANNELS
ENABLE	S ₁	S ₀	
L	L	L	A0, B0
L	L	Н	A1, B1
L	Н	L	A2, B2
L	Н	Н	A3, B3
Н	Х	Х	None

(1) X = Don't care

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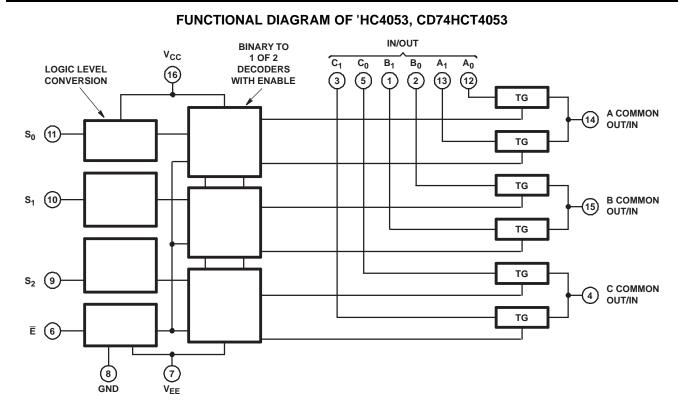


Table 3. FUNCTION TABLE 'HC4053, CD74HCT4053⁽¹⁾

	INPUT STATES							
ENABLE	S ₀	S1	S ₂	ON CHANNELS				
L	L	L	L	C0, B0, A0				
L	Н	L	L	C0, B0, A1				
L	L	Н	L	C0, B1, A0				
L	н	Н	L	C0, B1, A1				
L	L	L	Н	C1, B0, A0				
L	Н	L	Н	C1, B0, A1				
L	L	Н	Н	C1, B1, A0				
L	н	Н	Н	C1, B1, A1				
Н	Х	Х	Х	None				

(1) X = Don't care

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Absolute Maximum Ratings⁽¹⁾ ⁽²⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC} - V_{EE}$	DC supply voltage		-0.5	10.5	V
V _{CC}	DC supply voltage		-0.5	7	V
V _{EE}	DC supply voltage		0.5	-7	V
I _{IK}	DC input diode current	$V_{\rm I} < -0.5$ V or $V_{\rm I} > V_{\rm CC} + 0.5$ V		±20	mA
I _{OK}	DC switch diode current	$V_{I} < V_{EE} - 0.5 V \text{ or } V_{I} > V_{CC} + 0.5 V$		±20	mA
	DC switch current	$V_{I} > V_{EE} - 0.5 V \text{ or } V_{I} < V_{CC} + 0.5 V$		±25	mA
I _{CC}	DC V_{CC} or ground current			±50	mA
I _{EE}	DC V _{EE} current			-20	mA
		E (PDIP) package		67	
0	Declares the second interval (3)	M (SOIC) package		73	°C 44/
θ_{JA}	Package thermal impedance ⁽³⁾	NS (SOP) package		64	°C/W
		PW (TSSOP) package		108	
	Maximum junction temperature			150	°C
	Maximum storage temperature rang	ge	-65	150	°C
	Maximum lead temperature (solder		300	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to GND unless otherwise specified.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

	PARAM	METER	MIN	MAX	UNIT
V (1)	Supply voltage range	CD54/74HC types	2	6	V
V _{CC} ⁽¹⁾	$(T_A = full package temperature range)$	CD54/74HCT types	4.5	5.5	v
$V_{CC} - V_{EE}$	Supply voltage range $(T_A = full package temperature range)$	CD54/74HC types, CD54/74HCT types (see Figure 1)	2	10	V
V _{EE} ⁽²⁾	Supply voltage range (T _A = full package temperature range)	CD54/74HC types, CD54/74HCT types (see Figure 2)	0	-6	V
VI	DC input control voltage		GND	V_{CC}	V
V _{IS}	Analog switch I/O voltage		V _{EE}	V_{CC}	V
T _A	Operating temperature		-55	125	О°
		2 V	0	1000	
t _r , t _f	Input rise and fall times	4.5 V	0	500	ns
		6 V	0	400	

(1) All voltages referenced to GND unless otherwise specified.

(2) In certain applications, the external load resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{ON} values shown in Electrical Specifications table). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the HC/HCT4051; terminals 3 and 13 on the HC/HCT4052; terminals 4, 14, and 15 on the HC/HCT4053.



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Recommended Operating Area as a Function of Supply Voltages

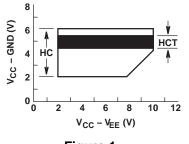


Figure 1.

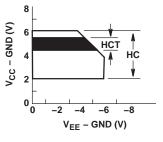


Figure 2.

DC Electrical Specifications

							AMBIENT TEMPERATURE, T _A									
	PARAMETER		TE		ONS		2			–40°C to 85°C		–55°C to 125°C		UNIT		
			V _{IS} (V)	V _I (V)	V _{EE} (V)	V _{cc} (V)	MIN	ТҮР	МАХ	MIN	МАХ	MIN	МАХ			
НС Ту	pes										·					
						2	1.5			1.5		1.5				
V _{IH}	High-level input ve	oltage				4.5	3.15			3.15		3.15	0	V		
						6	4.2			4.2		4.2				
						2			0.5		0.5		0.5			
V _{IL}	Low-level input vo	oltage		-		4.5			1.35		1.35		1.35	V		
						6			1.8		1.8		1.8			
				-	0	4.5		70	160		200		240			
		ON resistance (see Figure 11)	L – 1 m A		V_{CC} or V_{EE}	-	0	6		60	140		175		210	
r _{on}	ON resistance)	V_{IL} or V_{IH}	-4.5	4.5		40	120		150		180	Ω		
0.1					0	4.5		90	180		225		270			
			V_{CC} to V_{EE}	-	0	6		80	160		200		240			
					-4.5	4.5		45	130		162		195			
	Maximum ON res	istance		-	0	4.5		10						0		
∆r _{ON}	between any two				0	6 4.5		8.5 5						Ω		
		1 and 2	For switch OFF:		-4.5 0	4.5 6		Э	±0.1		±1		±1			
		channels	When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$,	-	-											
	Switch ON/OFF	4053	When V _{IS} = V _{EE} ,	-	-5	5			±0.1		±1		±1			
I_{IZ}	leakage current	4 channels 4052	For switch ON:	$V_{\text{IL}} \text{ or } V_{\text{IH}}$	0 5	6 5			±0.1 ±0.2		±1 ±2		±1 ±2	μA		
	current		All applicable combinations of	-	-5 0	5 6					±2 ±2					
		8 channels	V _{IS} and V _{OS}		-	-			±0.2				±2			
		4051	voltage levels		-5	5			±0.4		±4		±4			
I _{IL}	Control input leak	age current		V _{CC} or GND	0	6			±0.1		±1		±1	μA		
	Quiescent device	0	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$	V _{CC} or	0	6			8		80		160	μA		
I _{CC}	current	I _O = 0	When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	ĞŇD	-5	5			16		160		320	μA		

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								AME	BIENT T	EMPER	ATURE,	T _A			
	PARAMETER		TEST	CONDITI	ONS			25°C		-40° 85°		–55°(125		UNIT	
			V _{IS} (V)	V _I (V)	V _{EE} (V)	V _{cc} (V)	MIN	ТҮР	МАХ	MIN	МАХ	MIN	МАХ		
НСТ Ту	pes										÷				
V _{IH}	High-level input v	oltage				4.5 to 5.5	2			2		2		V	
V _{IL}	Low-level input vo	oltage				4.5 to 5.5			0.8		0.8		0.8	V	
					0	4.5		70	160		200		240		
			$V_{\rm CC}$ or $V_{\rm EE}$												
	ON resistance	I _O = 1 mA (see		V _{IL} or	-4.5	4.5		40	120		150		180	Ω	
r _{ON}	ON resistance	(see Figure 15)		Ÿ _{IH}	0	4.5		90	180		225		270	Ω	
				V_{CC} to V_{EE}											
					-4.5	4.5		45	130		162		195		
	M · ON · ·				0	4.5		10							
Δr_{ON}	Maximum ON res between any two													Ω	
					-4.5	4.5		5							
		1 and 2 channels	For switch OFF: When $V_{IS} = V_{CC}$,		0	6			±0.1		±1		±1		
		4053	$V_{OS} = V_{EE},$ When $V_{IS} = V_{EE},$		-5	5			±0.1		±1		±1		
I _{IZ}	Switch ON/OFF	4 channels	$V_{OS} = V_{CC}$	V _{IL} or	0	6			±0.1		±1		±1	μA	
12	leakage current	4052	For switch ON: All applicable	VIH	-5	5			±0.2		±2		±2	r	
		8 channels	combinations of		0	6			±0.2		±2		±2		
		4051	V _{IS} and V _{OS} voltage levels		-5	5			±0.4		±4		±4		
IIL	Control input leak	age current		(1)		5.5			±0.1		±1		±1	μA	
	Quiescent device		When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$	V _{CC} or	0	5.5			8		80		160	μA	
I _{CC}	current	I _O = 0	When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	ĞŇD	-4.5	5.5			16		160		320	μA	
ΔI_{CC} ⁽²⁾	Additional quiesce device current per 1 unit load		ΔI_{CC} ⁽²⁾	V _{CC} – 2.1		4.5 to 5.5		100	360		450		490	μA	

(1) Any voltage between V_{CC} and GND (2) For dual-supply systems, theoretical worst-case (V₁ = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.



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Table 4. HCT INPUT LOADING TABLE

ТҮРЕ	INPUT	UNIT LOADS ⁽¹⁾
4051, 4053	All	0.5
4052	All	0.4

(1) Unit load is ΔI_{CC} limit specified in DC Specifications table, e.g., 360 mA MAX at 25°C.

Switching Specifications

 $V_{CC} = 5 \text{ V}, \text{ } \text{T}_{\text{A}} = 25^{\circ}\text{C}, \text{ input } \text{t}_{\text{r}}, \text{ } \text{t}_{\text{f}} = 6 \text{ ns}$

						TYP	ICAL			
	PARAMETER	TEST CONDITIONS	CL (pF)	40	051	40	52	40	53	UNIT
			(91)	HC	нст	нс	нст	HC	нст	
t _{PHL} , t _{PLH}		Switch IN to OUT	15	4	4	4	4	4	4	
t _{PHZ} , t _{PLZ}	Propagation delay	Switch turn-off (S or E)	15	19	19	21	21	18	18	ns
t _{PZH} , t _{PZL}		Switch turn-on (S or E)	15	19	23	27	29	18	20	
C _{PD} ⁽¹⁾	Power dissipation capacitance			50	52	74	76	38	42	pF

(1) C_{PD} is used to determine the dynamic power consumption, per package. $P_D = C_{PD} V_{CC} {}^2 f_I + \sum (C_L + C_S) V_{CC} {}^2 f_O$ $f_O = output frequency$

 $f_{I} = input frequency$ $C_{L} = output load capacitance$

 $C_{\rm S}$ = switch capacitance

V_{CC} = supply voltage



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Switching Specifications

 C_L = 50 pF, input t_r, t_f = 6 ns

												JRE, T _A					
	PARAMETER		V_{EE}	Vcc		25°C				–40°C t	o 85°C			–55°C to	o 125°C		UNI
			(V)	(V)	нс		но	т	Н	С	н	т	н	С	нс	т	
					MIN MA	٩X	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
			0	2		60				75				90			
t _{PLH} ,	Propagation delay,		0	4.5		12		12		15		15		18		18	ns
t _{PHL}	switch in to out		0	6		10				13				15			- 13
			-4.5	4.5		8		8		10		10		12		12	
			0	2	2	25				280				340			
		4051	0	4.5		45		45		56		56		68		68	
		4051	0	6		38				48				57			
			-4.5	4.5		32		32		40		40		48		48	
			0	2	2	50				315				375			
t _{PHZ} ,	Maximum switch turn	4052	0	4.5	:	50		50		63		63		75		75	
t _{PLZ}	OFF delay from S or \overline{E} to switch output	4052	0	6		43				54				65			n
			-4.5	4.5		38		38		48		48		57		57	1
			0	2	2	10				265				315			
		4050	0	4.5		42		44		53		55		63		66	1
		4053	0	6		36				45				54			
			-4.5	4.5		29		31		36		39		44		47	1
			0	2	2	25				280				340			
		4054	0	4.5		45		55		56		69		68		83	
		4051	0	6		38				48				57			1
			-4.5	4.5		32		39		40		49		48		59	
			0	2	3	25				405				490			1
t _{PZL} ,	Maximum switch turn	4050	0	4.5		65		70		81		68		98		105	
t _{PZH}	ON delay from S or \overline{E} to switch output	4052	0	6		55				69				83			n
	·		-4.5	4.5		46		48		58		60		69		72	
			0	2	2	20				275				330			1
		4050	0	4.5	,	44		48		55		60		66		72	1
		4053	0	6		37				47				56			
			-4.5	4.5		31		34		39		43		47		51	1
Cı	Input (control) capacitance					10		10		10		10		10		10	р

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Analog Channel Specifications

Typical values at $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	HC/HCT TYPES	V _{EE} (V)	V _{CC} (V)	НС/НСТ	UNIT
CI	Switch input capacitance		All			5	pF
			4051			25	
C _{COM}	Common output capacitance		4052			12	pF
			4053			8	
			4051			145	
			4052	-2.25	2.25	165	
4	Minimum switch frequency	See Figure 3 ⁽¹⁾⁽²⁾	4053			200	MHz
f _{MAX}	response at –3 dB (see Figures 12, 14, 16)		4051			180	
			4052	-4.5	4.5	185	
			4053			200	
	Sine-wave distortion	Soo Figuro F	All	-2.25	2.25	0.035	%
	Sille-wave distolation	See Figure 5	All	-4.5	4.5	0.018	70
			4051	-2.25	2.25	-73	
			4052			-65	
	Switch OFF signal feedthrough	$C_{a} = \overline{C}_{a}^{(2)} (3)$	4053			-64	-10
	(see Figures 13, 15, 17)	See Figure 7 ^{(2) (3)}	4051	-4.5	4.5	-75	dB
			4052			-67	-
			4053			-66	-

Adjust input voltage to obtain 0 dBm at V_{OS} for $f_{\rm IN}$ = 1 MHz V_{IS} is centered at (V_{CC} – V_{EE})/2. Adjust input for 0 dBm (1)

(2) (3)

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APPLICATION INFORMATION

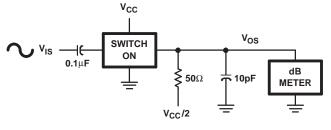
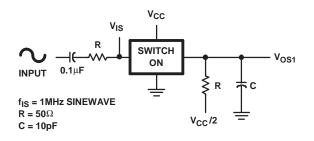
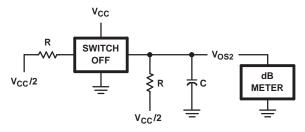
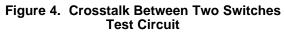


Figure 3. Frequency Response Test Circuit







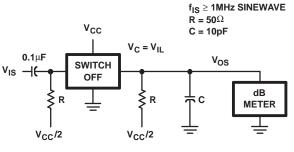


Figure 7. Switch OFF Signal Feedthrough

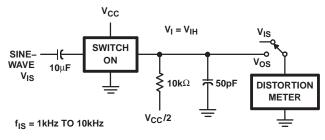


Figure 5. Sine-Wave Distortion Test Circuit

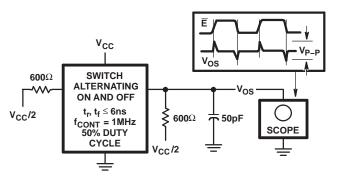
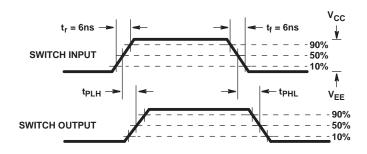


Figure 6. Control to Switch Feedthrough Noise Test Circuit



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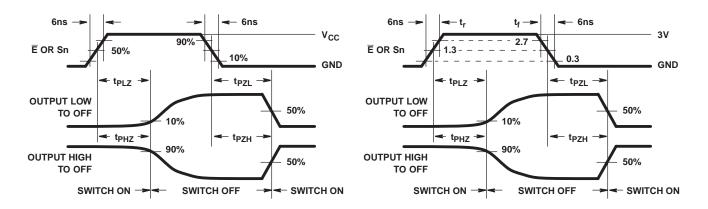
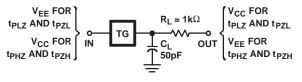


FIGURE 8B. HC TYPES

FIGURE 8C. HCT TYPES

Figure 8. Switch Propagation Delay, Turn-On, Turn-Off Times





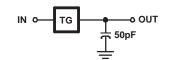


Figure 10. Switch In to Switch Out Propagation Delay Test Circuit

14 Submit Documentation Feedback

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TYPICAL PERFORMANCE CURVES

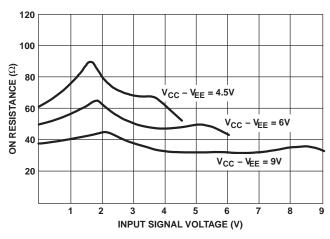
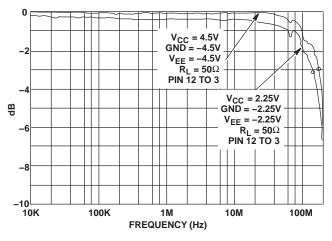
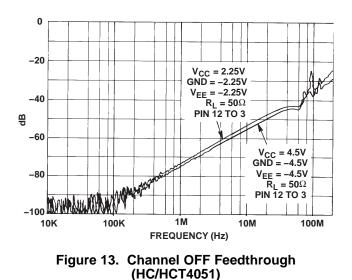


Figure 11. Typical ON Resistance vs Input Signal Voltage







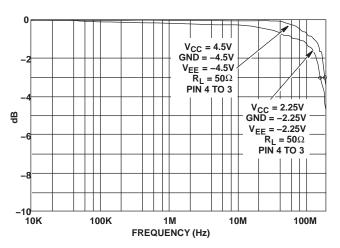


Figure 14. Channel ON Bandwidth (HC/HCT4052)

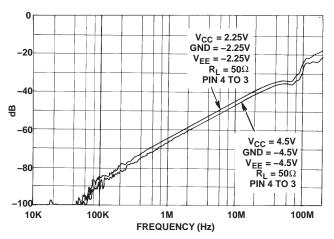
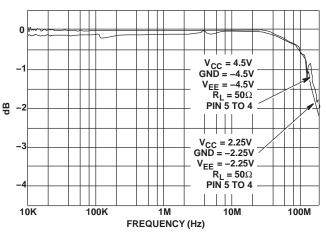


Figure 15. Channel OFF Feedthrough (HC/HCT4052)





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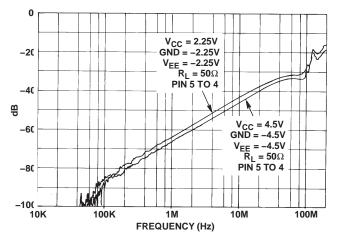


Figure 17. Channel OFF Feedthrough (HC/HCT4053)



10-Jun-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	•	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
5962-8775401EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A	Samples
5962-8855601EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A	Samples
5962-9065401MEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9065401ME A CD54HCT4051F3A	Samples
CD54HC4051F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4051F	Samples
CD54HC4051F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4051F3A	Samples
CD54HC4052F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4052F	Samples
CD54HC4052F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A	Samples
CD54HC4053F	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4053F	Samples
CD54HC4053F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A	Samples
CD54HCT4051F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9065401ME A CD54HCT4051F3A	Samples
CD74HC4051E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4051E	Samples
CD74HC4051EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4051E	Samples
CD74HC4051M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051M96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples
CD74HC4051M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samples



Orderable Device	Status	Package Type		Pins I		Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samp
	(1)		Drawing	_	Qty	(2)	(6)	(3)		(4/5)	
CD74HC4051ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samp
CD74HC4051MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samp
CD74HC4051MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samp
CD74HC4051NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samp
CD74HC4051NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M	Samj
CD74HC4051PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4051	Samj
CD74HC4051PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	Samj
CD74HC4051PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	Sam
CD74HC4051PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051	Sam
CD74HC4052E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4052E	Sam
CD74HC4052EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4052E	Sam
CD74HC4052M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Sam
CD74HC4052M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	HC4052M	Sam
CD74HC4052M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Sam
CD74HC4052M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Sam
CD74HC4052ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Sam
CD74HC4052MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Sam
CD74HC4052MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Sam



Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4052MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M	Samples
CD74HC4052PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4052PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052	Samples
CD74HC4053E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4053E	Samples
CD74HC4053EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4053E	Samples
CD74HC4053M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053M96G3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples
CD74HC4053MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samples



Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samp
CD74HC4053MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samp
CD74HC4053NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M	Samp
CD74HC4053PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samp
CD74HC4053PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samp
CD74HC4053PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samp
CD74HC4053PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samp
CD74HC4053PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053	Samj
CD74HCT4051E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4051E	Sam
CD74HCT4051M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samj
CD74HCT4051M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samj
CD74HCT4051M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samj
CD74HCT4051M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Samj
CD74HCT4051ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Sam
CD74HCT4051MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Sam
CD74HCT4051MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Sam
CD74HCT4051MTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M	Sam
CD74HCT4052E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4052E	Sam
CD74HCT4052EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4052E	Sam



Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4052M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Samples
CD74HCT4052M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Sample
CD74HCT4052M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Sample
CD74HCT4052ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Sample
CD74HCT4052MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Sample
CD74HCT4052MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M	Samples
CD74HCT4053E	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4053E	Sample
CD74HCT4053EE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4053E	Sample
CD74HCT4053M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Sample
CD74HCT4053M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Sample
CD74HCT4053M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Samples
CD74HCT4053ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Sample
CD74HCT4053MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Sample
CD74HCT4053MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M	Sample
CD74HCT4053PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-55 to 125	HK4053	Sample
CD74HCT4053PWRE4	ACTIVE	TSSOP	PW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	Sample
CD74HCT4053PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	Samples



10-Jun-2014

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4053PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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- Catalog: CD74HC4051, CD74HC4052, CD74HC4053, CD74HCT4051
- Automotive: CD74HC4051-Q1, CD74HCT4051-Q1, CD74HC4051-Q1, CD74HCT4051-Q1
- Enhanced Product: CD74HC4051-EP, CD74HC4051-EP
- Military: CD54HC4051, CD54HC4052, CD54HC4053, CD54HCT4051
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 - Enhanced Product Supports Defense, Aerospace and Medical Applications
 - Military QML certified for Military and Defense Applications

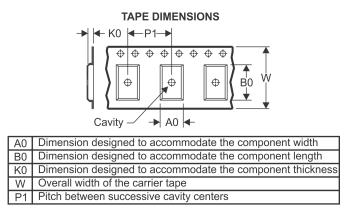
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051M96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4052PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053M96	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

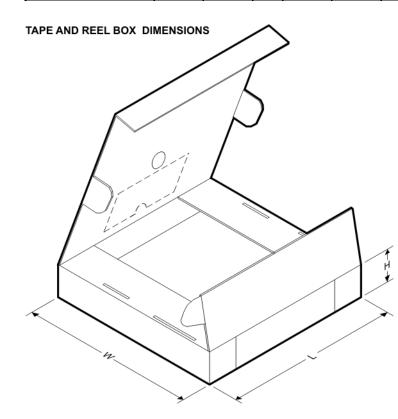
PACKAGE MATERIALS INFORMATION

TEXAS INSTRUMENTS

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29-Apr-2014

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4053M96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4051M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4052M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4053M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4053PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4051M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4051M96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4051M96G4	SOIC	D	16	2500	333.2	345.9	28.6

PACKAGE MATERIALS INFORMATION



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29-Apr-2014

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4051PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4051PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4051PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HC4052M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4052M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4052M96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4052NSR	SO	NS	16	2000	367.0	367.0	38.0
CD74HC4052PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4052PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4052PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4052PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HC4053M96	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4053M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4053M96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4053M96G4	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4053PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HC4053PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4053PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4053PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HCT4051M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4052M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4053M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT4053PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
CD74HCT4053PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HCT4053PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HCT4053PWT	TSSOP	PW	16	250	367.0	367.0	35.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/E 08/12

D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) –16x0,55 -14x1,27 -14x1,27 16x1,50 5,40 5.40 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 .55 Example 1. Solder Mask Opening (See Note E) -0,07 All Around

NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. β . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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