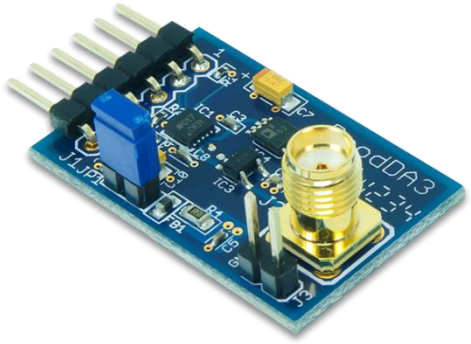
1300 Henley Court
Pullman, WA 99163
509.334.6306
www.digilentinc.com

# PmodDA3™ Reference Manual

Revised April 12, 2016
This manual applies to the PmodDA3 rev. B

## Overview

The PmodDA3 is a 16-bit digital-to-analog converter (DAC) with an SMA connector for high resolution and low noise analog output.



*The PmodDA3.*

Features include:

- High resolution, 16-bit Digital-to-Analog converter
- Low noise analog output
- SMA connector
- 2.5V reference voltage
- Small PCB size for flexible designs 1.2" × 0.8" (3.0 cm × 2.0 cm)
- 6-pin Pmod port with GPIO interface
- Follows Digilent Pmod Interface Specification Type 1

## 1 Functional Description

The PmodDA3 utilizes Analog Devices AD5541A to provide analog output with 16-bit resolution.

## 2 Interfacing with the Pmod

The PmodDA3 communicates with the host board via a SPI-like protocol. This interface is different than the traditional SPI protocol in the fact that the pin normally designated to the host receiving data (MISO), is now used for a Load DAC (LDAC) function so that the output of the DAC can be updated immediately once the module is loaded with the incoming 16 bits of data.

To send data to the Pmod, users must drive the Chip Select (CS) line to a logic level low voltage and then send the 16 clock pulses and 16 bits of data in SPI Mode 0; that is, placing the most significant bit (MSB) of data on the data line right after the Serial Clock line (SCLK) has been brought to a logic level low voltage.

When all of the data has been latched into, i.e. prepared for, the internal serial input register, bringing the CS line back to a logic level high voltage will transfer all of the data from the shift register to the serial input register if

LDAC is at a high voltage state. Pulsing the LDAC pin low and then high will asynchronously transfer all of the data into the DAC register, resulting in the appropriate analog voltage on the SMA connector. Alternatively, users may hold the LDAC pin at a logic level low voltage when bringing the CS pin high to directly transfer the data from the shift register to the DAC register.

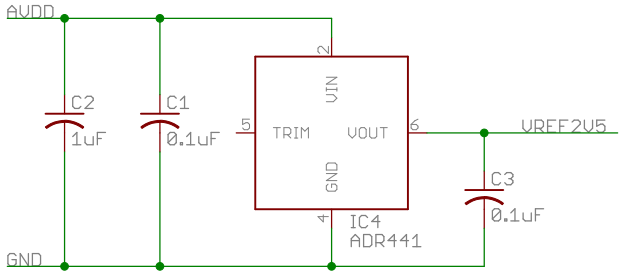
| Pin | Signal | Description |
|---|---|---|
| 1 | ~CS | Chip Select |
| 2 | DIN | Data Input |
| 3 | ~LDAC | LOAD DAC |
| 4 | SCLK | Serial Clock |
| 5 | GND | Power Supply Ground |
| 6 | VCC | Power Supply (3.3V/5V) |

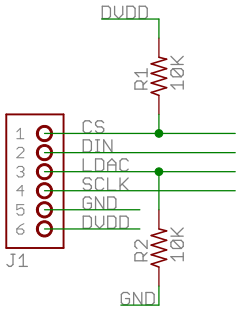
*Table 1. Pinout description table.*

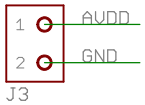
Any external power applied to the PmodDA3 must be within 2.7V and 5.5V; however, it is recommended that the Pmod is operated at 3.3V.

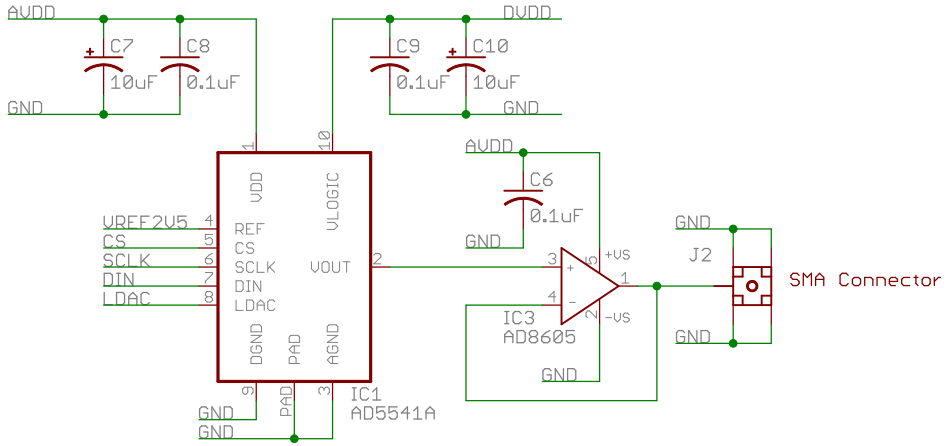
# 3 Physical Dimensions

The pins on the pin header are spaced 100 mil apart. The PCB is 1.2 inches long on the sides parallel to the pins on the pin header and 0.8 inches long on the sides perpendicular to the pin header.


Note: Any external voltage applied to AVDD must be kept between 3.0V and 5.5V in order to avoid damaging the parts used in this circuit.

For more information on the parts used in this design, please refer to:
www.analog.com/AD5541A - 2.7V to 5.5V, Serial-Input, Voltage Output, Unbuffered 16-Bit DAC
www.analog.com/AD8605 - Precision, Low Noise, CMOS, Rail-to-Rail, Input/Output Operational Amplifier
www.analog.com/ADR441 - Ultralow Noise, LDO XFET Voltage Reference with Current Sink and Source

ROHS CHINA WEEE

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| PmodDA3<br>Copyright 2012, Digilent Inc. | | Engineer: MTA |
| SHEET: | | Author: PJA |
| TITLE: PmodDA3 | | Rev: B.0 |
| Doc#: 500-241 | Date: 07/31/2012 | Sheet: 1/1 |