PCI-2602U
Series Card User Manual

Multi-Function Boards Version 1.0, Feb. 2014

SUPPORTS

Board includes PCI-2602U

WARRANTY

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Email: service@icpdas.com, service.icpdas@gmail.com

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Packing List

The shipping package includes the following items:

	One multi-function card as follows: PCI-2602U Series
	One printed Quick Start Guide
	One software utility CD

Note:

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

Related Information

Product Page:

http://www.icpdas.com/root/product/solutions/pc_based_io_board/pci/pci-2602.html

Documentation and Software for UniDAQ SDK:

CD:\NAPDOS\PCI\UniDAQ\

http://ftp.icpdas.com/pub/cd/iocard/pci/napdos/pci/unidaq/

1. Introduction

The PCI-2602U card provides 1MHz 16/16-ch 16-bit Analog Input, 2-ch 16-bit Analog Output with 32-ch programmable Digital Input/Output

1.1. General Description

The PCI-2602U is a powerful multifunction card with 1M/s sampling rate and 16-bit resolution converter to suitable for most industrial application. The PCI-2602U card has a universal PCI interface supporting both 3.3 V and 5V PCI bus. This card features a continuous, 1M Samples/Sec 16-bit high resolution AD converter, 8k samples hardware AD FIFO, 2-ch 16-bit DA converter, 32-ch programmable digital I/O and DO read back. PCI-2602U provides either 16-ch single-ended or 8-ch differential analog inputs which are jumper less. The PCI-2602U is equipped with a high speed PGA featuring programmable gain controls.

Our PCI-2602U provides five Programmable trigger methods: Software Trigger Pos_Trigger ,Mid_Trigger,Pre_Trigger and Delay_Trigger. The AD channel scan function of PCI-2602U is so amazing, we call it MagicScan. The MagicScan controller takes out most works of getting AD value such as select channel, set gain, settling time, trigger ADC and get data. With the built-in MagicScan and interrupt features, it is effectively off-loading your CPU from the job. Even in channel scan mode, it can have different gain code for each channel, and the sampling rate can still reach 1M S/s total.

The PCI-2602U has the Card ID switch. Users can set a card ID for each card so that when more than two PCI-2602U boards is used in a computer at the same moment, users can still instantly recognize them one by one. When the DI channels are unconnected, the DI status will remain in low status without being left floating.

1.2. Features

The following is a list of general features for the PCI-2602U. Check section 1.3 for more details.

Interface

- Universal PCI(3.3 V/5 V) interface.
- 2-CH bus mastering scatter/gather DMA.
- Card ID switch.
- Auto-calibration function.

Analog Input

- One 16-bit AD converter with maximum 1M samples/second.
- 16 single-ended / 8 differential programmable analog inputs.
- Provides multiple AD trigger methods.
- Programmable gain control, programmable offset control.
- On Board 8192 samples AD FIFO.

Analog Output

- One DA converter.
- 2-ch 16-bit voltage output.
- Voltage output range: +/-10 V, +/-5V, 0 ~ 10 V, 0 ~ 5 V.
- On board 512 samples DA FIFO.
- No bus loading in repetitive waveform generation application.

Digital Input/Output

- On board 512 samples DO FIFO.
- 32-ch programmable DIO (4 x 8-ch).
- DO readback function.
- Programmable input digital filter for all digital input signals.
- No bus loading in repetitive 8-bit digital pattern generation application.

1.3. Specifications

Model Name	PCI-2602U
Analog Input	
Channels	16 single-ended/8 differential
A/D Converter	16-bit, 1 µs conversion time
Sampling Rate	1 MS/s
FIFO Size	8192 samples
Over voltage Protection	Continuous +/-35 Vp-p
Input Impedance	10,000 MΩ/4pF
Trigger Modes	Software, Pacer, External
Data Transfer	Polling, Interrupt, DMA
Accuracy	0.05 % of FSR ±1 LSB @ 25 °C, ± 10.24 V
Input Range	Gain: 0.4, 0.8, 1.6 Bipolar Range: ±10.24 V, ±5.12 V, ±2.56 V,
Analog Output	
Channels	2
Resolution	16-bit
Accuracy	± 6 LSB
Output Range	±5 V, ±10 V, 0 ~ 10 V, 0 ~ 5 V, ±EXT_REF, 0~EXT_REF
Output Driving	+/- 5 mA
Slew Rate	8.33 V/µs
Output Impedance	0.1 Ω (Max.)
Operating Mode	Static update, Waveform generation (only for Channel 0)
Output Rate	20 MS/s (Max.)
FIFO Size	512 samples
Programmable I/O	
Channels	32(4 port programmable)
Digital Input	
Compatibility	5 V/TTL
Input Voltage	Logic 0: 0.8 V (Max.)/Logic 1: 2.0 V (Min.)
Response Speed	1.0 MHz (Typical)
Trigger Mode	Software
Data Transfer	Polling

Digital Output	
Compatibility	5 V/CMOS
Output Voltage	Logic 0: 0.4 V (max.)/Logic 1: 2.4 V (min.)
Output Capability	Sink: 6 mA @ 0.33 V/Source: 6 mA @ 4.77 V
DO Readback	Yes
Operation Mode	Static update, Waveform generation
Response Speed	4.0 MHz (Typical)
DO Sample Clock frequency	10 MHz
General	
Bus Type	3.3 V/5 V Universal PCI, 32-bit
Data Bus	16-bit
Card ID	Yes (4-bit)
I/O Connector	SCSI 68-pin
Dimensions (L x W x D)	149 mm x 102 mm x 22 mm
Power Consumption	1 A @ +5 V (Max.)
Operating Temperature	0 ~ 60 °C
Storage Temperature	-20 ~ 70 °C
Humidity	5 ~ 85% RH, non-condensing

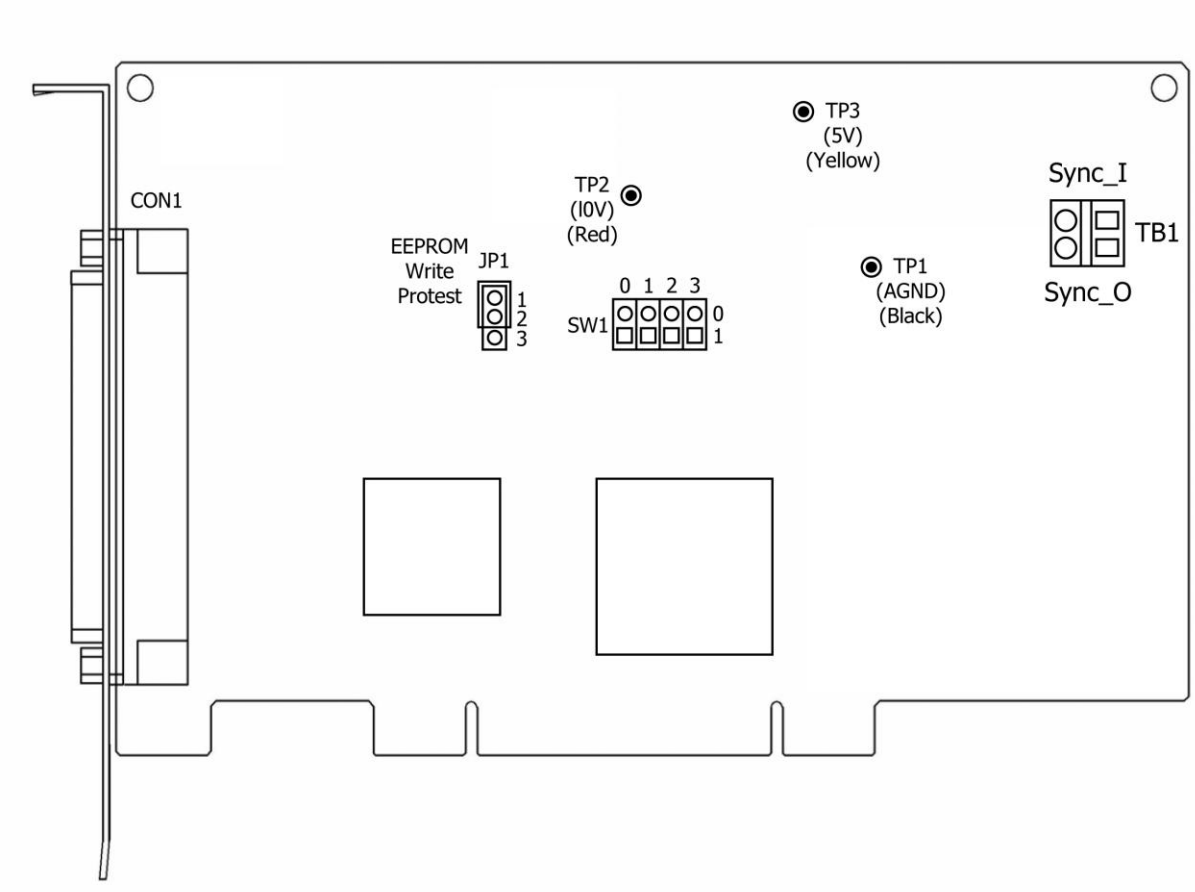
1.4. Applications

- Signal analysis.
- FFT & frequency analysis.
- Transient analysis.
- Temperature monitor.
- Vibration analysis.
- Energy management.
- Other industrial and laboratory measurement and control.

2. Hardware Configuration

2.1. Board Layout

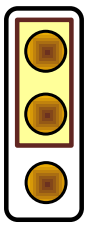
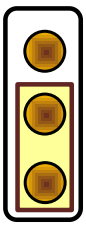
SW1 : Dip Switch for Board ID
TP1 : AGND for AD Calibration, Black
TP2 : 10 V for AD Calibration, Red
TP3 : 5 V for AD Calibration, Yellow
CON1 : I/O Signals
TB1 : (Sync_I, Sync_O) for Board Synchronization
JP1 : EEPROM Write Protection



2.2. Jumper/Programmable Setting

2.2.1. JP1 EEPROM Write Protection

JP1 is used to select the EEPROM Write Protection. To select the LOCK, the EEPROM doesn't write the data, otherwise EEPROM can write the data.

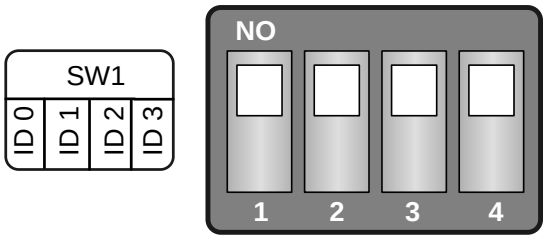
EEPROM Write Protection Selection (JP1)	
JP1 EEPROM WRITE PROTECT 	JP1 EEPROM WRITE PROTECT 
LOCK EEPROM(Default)	UNLOCK EEPROM

2.2.2. Card ID Switch

The PCI-2602U has a Card ID switch (SW1) with which users can recognize the board by the ID via software when using two or more PCI-2602U cards in one computer. The default Card ID is 0x0. For detail SW1 Card ID settings, please refer to Table 2.1.

Table 2.1 (*) Default Settings; OFF → 1; ON → 0

Card ID (Hex)	1 ID0	2 ID1	3 ID2	4 ID3
(*) 0x0	ON	ON	ON	ON
0x1	**OFF**	ON	ON	ON
0x2	ON	**OFF**	ON	ON
0x3	**OFF**	**OFF**	ON	ON
0x4	ON	ON	**OFF**	ON
0x5	**OFF**	ON	**OFF**	ON
0x6	ON	**OFF**	**OFF**	ON
0x7	**OFF**	**OFF**	**OFF**	ON
0x8	ON	ON	ON	**OFF**
0x9	**OFF**	ON	ON	**OFF**
0xA	ON	**OFF**	ON	**OFF**
0xB	**OFF**	**OFF**	ON	**OFF**
0xC	ON	ON	**OFF**	**OFF**
0xD	**OFF**	ON	**OFF**	**OFF**
0xE	ON	**OFF**	**OFF**	**OFF**
0xF	**OFF**	**OFF**	**OFF**	**OFF**



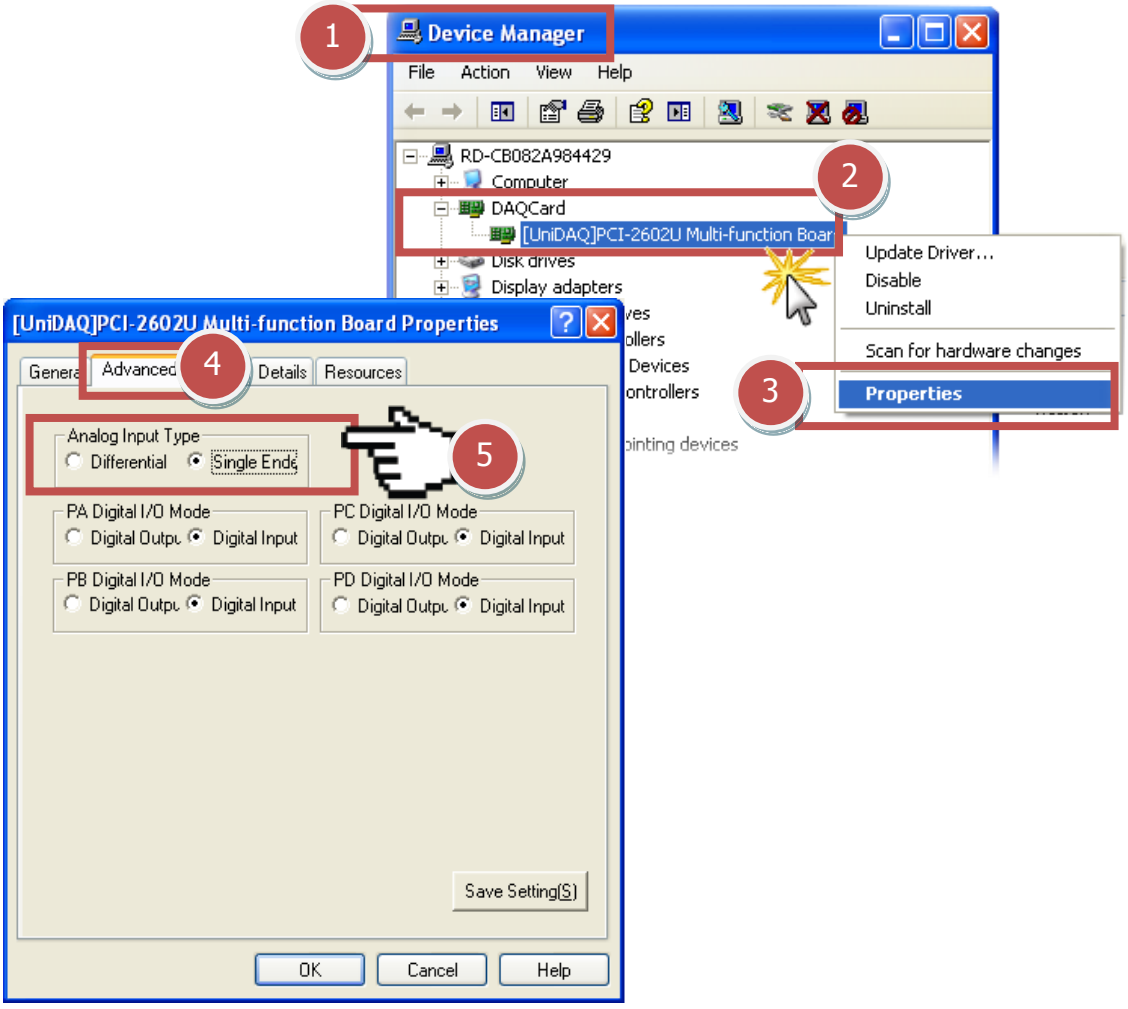
(Default Settings)

2.2.3. Analog Input Type Setting

This option is used to select the Analog Input type. For single-ended inputs, select the Single Ended. For differential inputs, select Differential. How to use the advanced configuration tool in the Windows Device Manager to settings the Analog Input type, the detail configuration is illustrated in the figure below.

Note that before the Analog Input type settings, you must complete the hardware and software installation. Refer to Chapter 4 Hardware Installation and Chapter 5 Software Installation for more detailed information.

Step 1: Open the Windows **Device Manager**.
Step 2: **Right-Click** on the name of the PCI-2602U.
Step 3: Select the **Properties** item from the popup menu.
Step 4: In the **[UniDAQ]PCI-2602U Multi-function Board Properties** dialog box, click the **Advanced** tap.
Step 5: In the **Analog Input Type** area, select the **Differential or Single Ended** for you need.

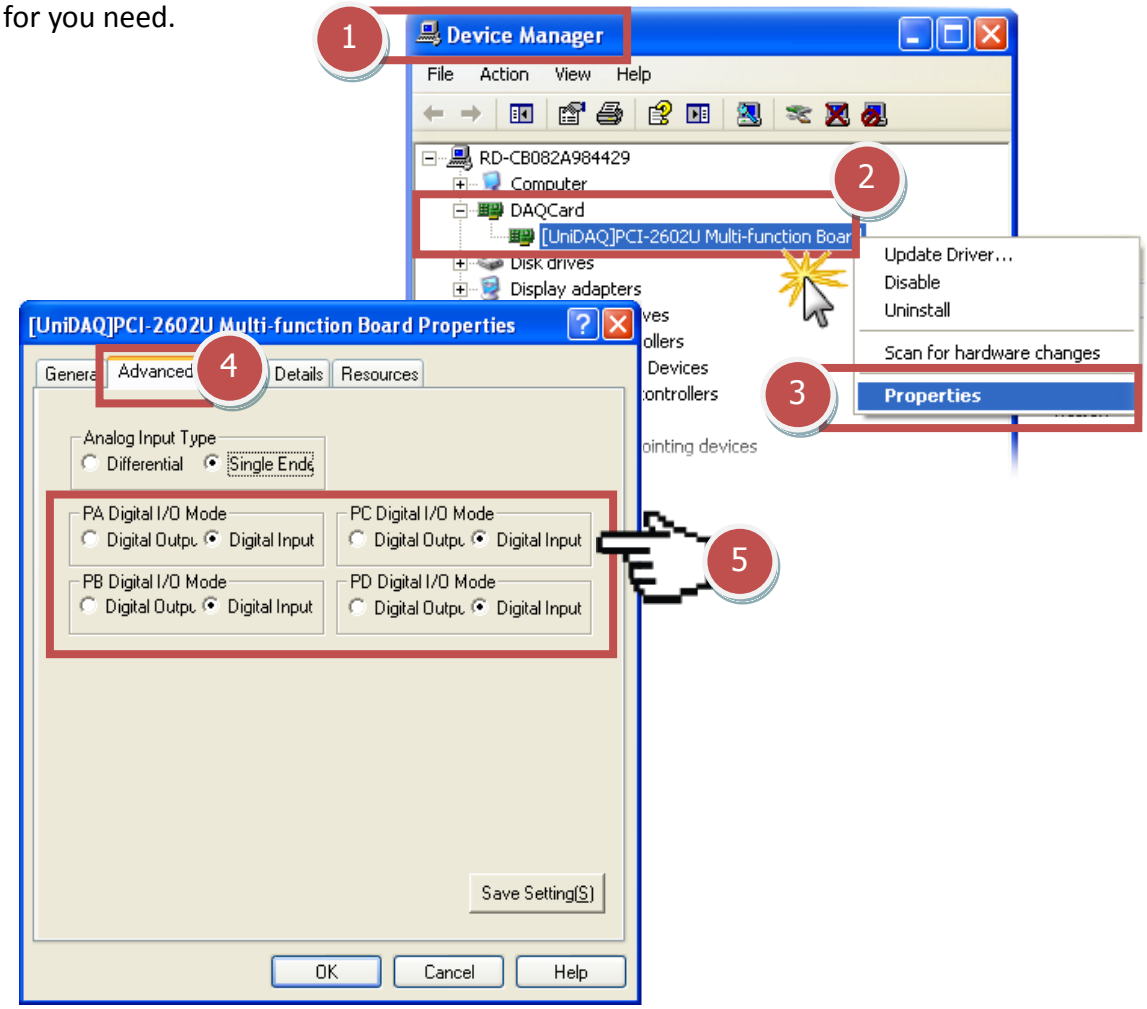


2.2.4. Digital Input/Output Mode Setting

This option is used to select the Digital Input/Output mode for digital output port. For Input mode, select the Digital Input. For output mode, select Digital output. How to use the advanced configuration tool in the Windows Device Manager to settings the Digital I/O Ports, the detail configuration is illustrated in the figure below.

Note that before the Digital Input/Output mode settings, you must complete the hardware and driver installation. Refer to Chapter 4 Hardware Installation and Chapter 5 Software Installation for more detailed information.

Step 1: Open the Windows **Device Manager**.
Step 2: **Right-Click** on the name of the PCI-2602U.
Step 3: Select the **Properties** item from the popup menu.
Step 4: In the **[UniDAQ]PCI-2602U Multi-function Board Properties** dialog box, click the **Advanced** tap.
Step 5: In the **PA/PB/PC/PD Digital I/O Mode** area, select the **Digital Output or Digital Input** for you need.



2.3. System Block Diagram

The block diagram of PCI-2602 is given as follows:

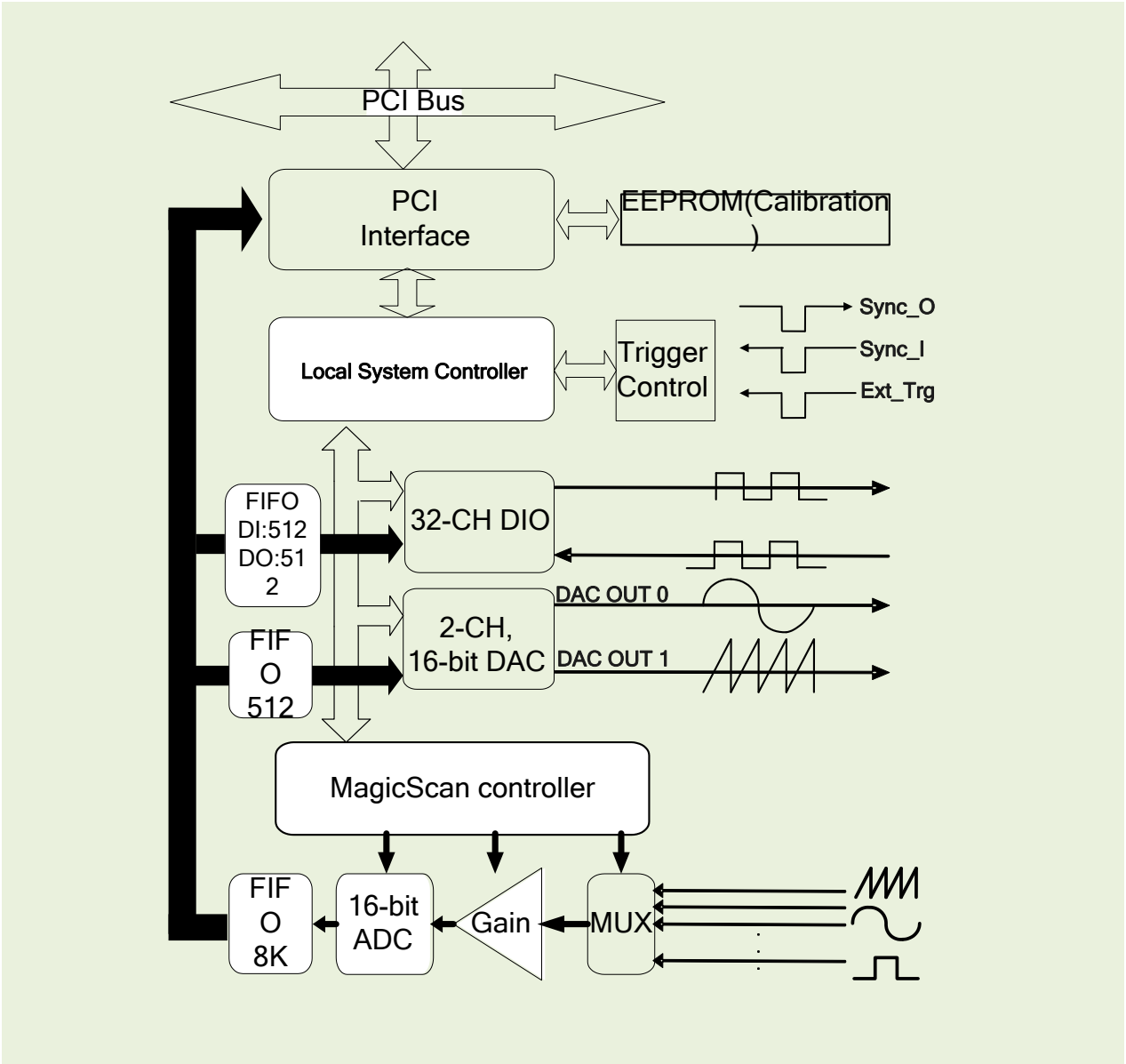


Figure 2.3-1: The block diagram of PCI-2602U

2.4. Analog Input Signal Connections

The PCI-2602U can measure single-ended or differential-type analog inputs signal. Some analog signals can be measured in both modes. However, some analog signals only can be measured in one or the other. The user must decide which mode is suitable for measurement.

In general, there are 4 different analog signal connection methods (shown from **Figure 2.4-1** to **Figure 2.4-5**). The connection in **Figure 2.4-1** is suitable for grounding source analog input signals. The **Figure 2.4-3** connection is used to measure more channels than in **Figure 2.4-1**, but it is only suitable for large analog input signals. The connection in **Figure 2.4-4** is suitable for thermocouple and the re **Figure 2.4-5** connection is suitable for floating source analog input signals. **Note: In Figure 2.4-4 the maximum common mode voltage between the analog input source and the AGND is 70Vp-p, so the user must take care that the input signal is under this specification first. If the common mode voltage is over 70Vp-p, the input multiplexer will be permanently damaged!**

The simple way to select your input signal connection configuration is listed below.

1. **Grounding source input signal → select Figure 2.4-1**
2. **Thermocouple input signal → select Figure 2.4-4**
3. **Figure 2.4-4Floating source input signal → select Figure 2.4-5**
4. **If Vin > 1 V, the gain<=10 and more channels are needed → select Figure 2.4-3**

If you are unsure of the characteristics of your input signal, follow these test step:

1. **Step1 : Try and record the measurement result Figure 2.4-1**
2. **Step2 : Try and record the measurement result Figure 2.4-4**
3. **Step3 : Try and record the measurement result Figure 2.4-5**
4. **Compare the three results and select the best one**

Figure 2.4-1 Connecting to grounding source input (Right way)

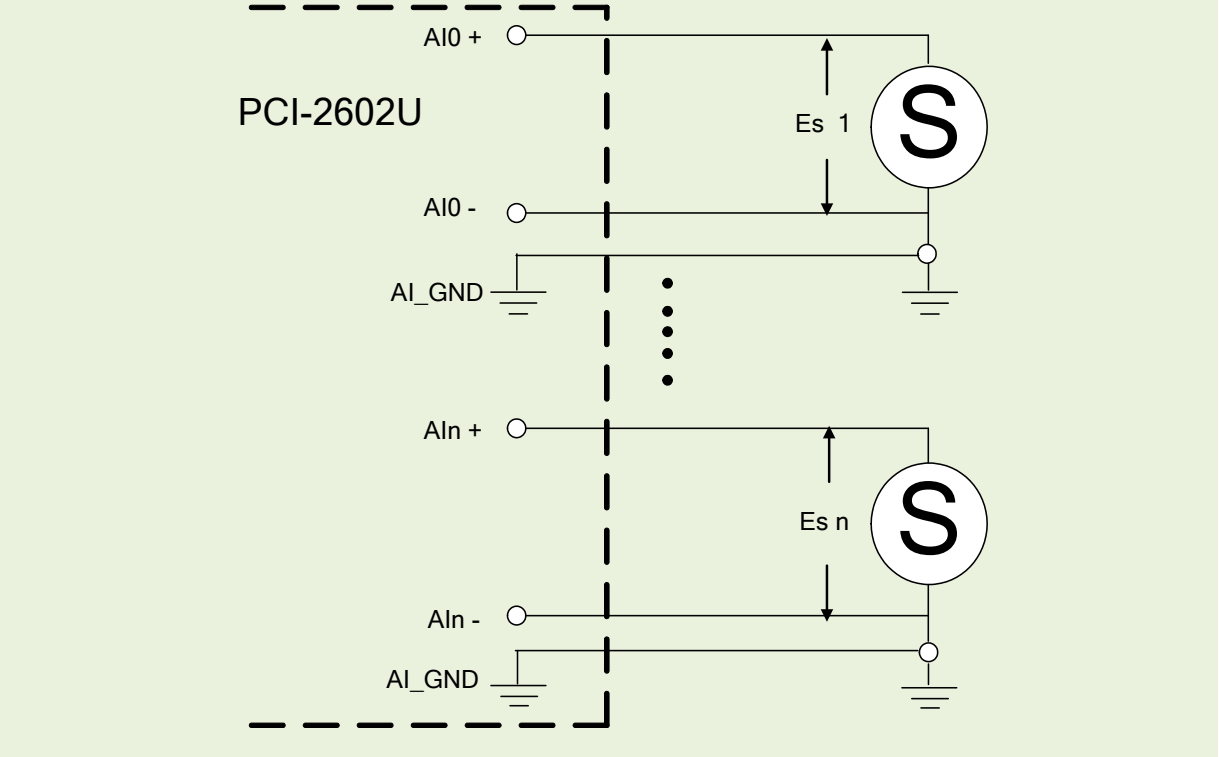


Figure 2.4-2 Ground loop input (Wrong way)

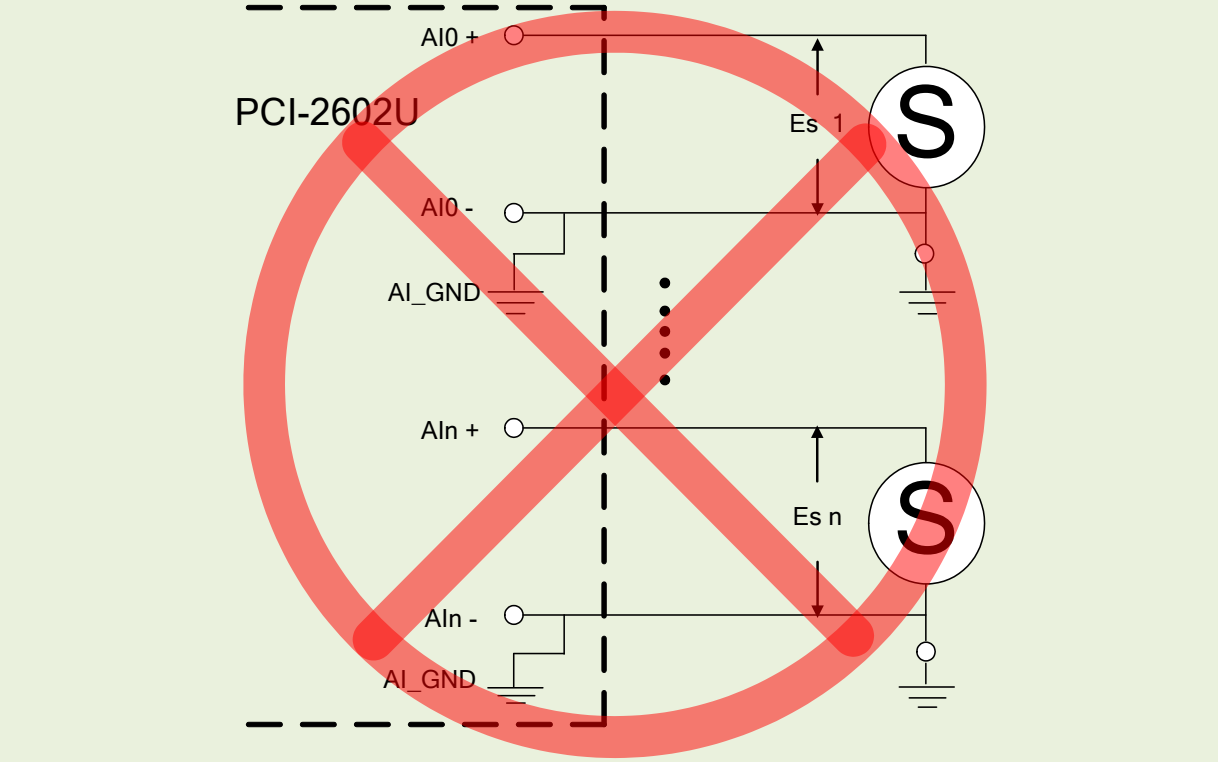


Figure 2.4-3 Connecting to single-ended input configuration

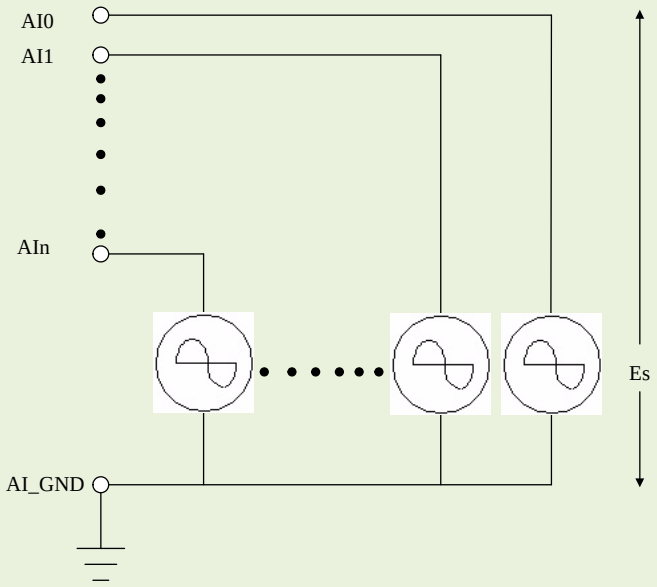
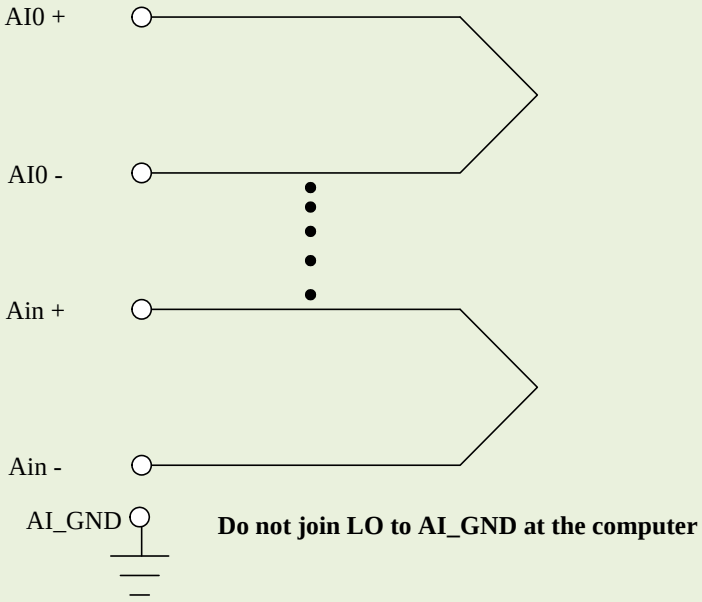


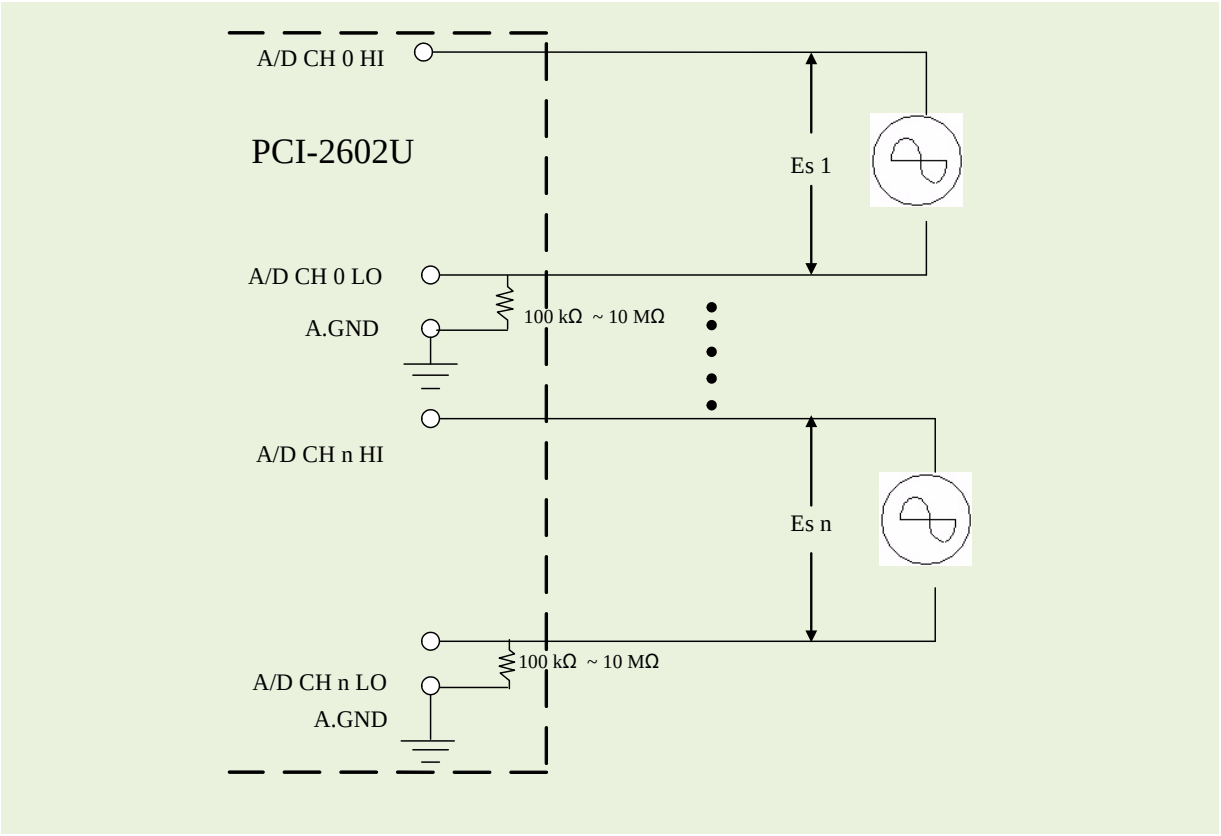
Figure 2.4-4 Connecting to thermocouple configuration



Note: If the input signal is not thermocouple, the user should use an oscilloscope to measure common mode voltage of Vin before connecting to PCI-2602U. Don't use a voltage meter or multimeter.

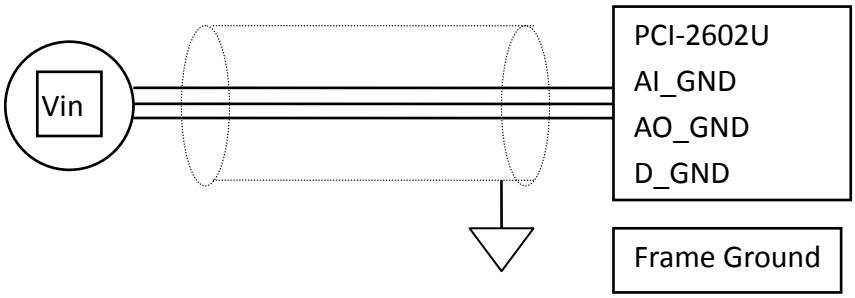
CAUTION: In **Figure 2.4-4**, the maximum common mode voltage between the analog input source and the AGND is 70Vp-p. Make sure that the input signal is under specification first! If the common mode voltage is over 70Vp-p, the input multiplexer will be permanently damaged.

Figure 2.4-5 Connecting to floating source configuration



Signal Shielding

- Signal shielding connections in **Figure 2.4-1to Figure 2.4-5** are all the same
- Use a single-point connection to **frame ground (not AI_GND, AO_GND or D_GND)**



2.5. Analog Output Signal Connections

PCI-2602U provides two DA output channels, AO0 and AO1. You may use the PCI-2602U internally-provided precision -5 V (-10 V) reference to generate 0 V to +5 V (+10 V) DA output range. You may also create a DA output range through the external reference, AOx_REF. The external reference input range is +/-10 V. For example, connecting with an external reference of +8 V will generate 0 ~ +8 V DA output.

Figure 2.5-1 Connecting to analog output for internal reference(Recommended)

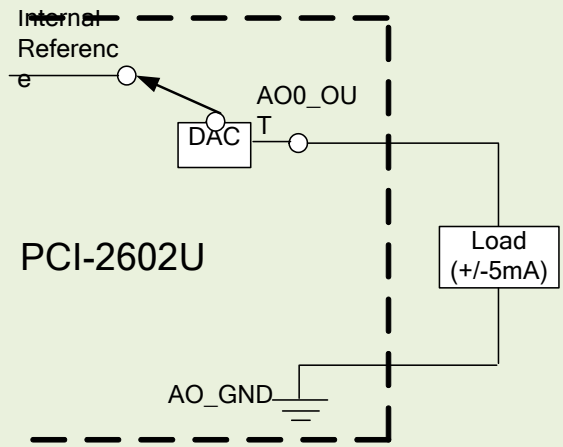
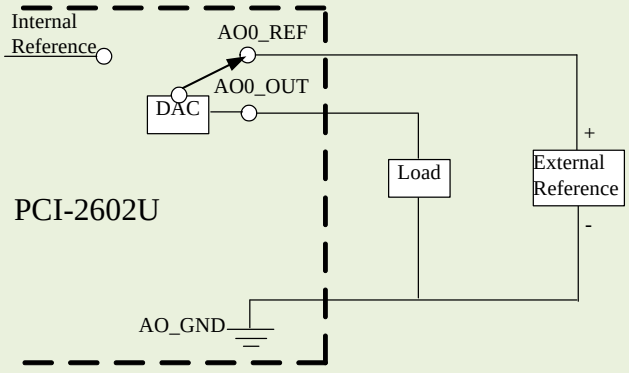


Figure 2.5-2 Connecting to analog output for external reference



2.6. Pin Assignments

Pin Assign-ment		Terminal No.		Pin Assign-ment	
+5V (Output)		01	35	+12V (Output)	
Ext_TRG		02	36	Cnt0_GATE	
Trg_GATE		03	37	Cnt0_OUT	
Pacer_OUT		04	38	Cnt0_CLK	
D_GND		05	39	D_GND	
PD7		06	40	PD6	
PD5		07	41	PD4	
PD3		08	42	PD2	
PD1		09	43	PD0	
PC7		10	44	PC6	
PC5		11	45	PC4	
PC3		12	46	PC2	
PC1		13	47	PC0	
D_GND		14	48	D_GND	
PB7		15	49	PB6	
PB5		16	50	PB4	
PB3		17	51	PB2	
PB1		18	52	PB0	
PA7		19	53	PA6	
PA5		20	54	PA4	
PA3		21	55	PA2	
PA1		22	56	PA0	
AO_GND		23	57	AO_GND	
AO1_OUT		24	58	AO0_OUT	
AO1_REF		25	59	AO0_REF	
AI_GND		26	60	AI_GND	
AI15	AI7-	27	61	AI14	AI7+
AI13	AI6-	28	62	AI12	AI6+
AI11	AI5-	29	63	AI10	AI5+
AI9	AI4-	30	64	AI8	AI4+
AI7	AI3-	31	65	AI6	AI3+
AI5	AI2-	32	66	AI4	AI2+
AI3	AI1-	33	67	AI2	AI1+
AI1	AI0-	34	68	AI0	AI0+
S.E.	Diff.			S.E.	Diff.

Female SCSI 68-pin (CON1)

Note:

AI0 ~ AI15 : single-ended

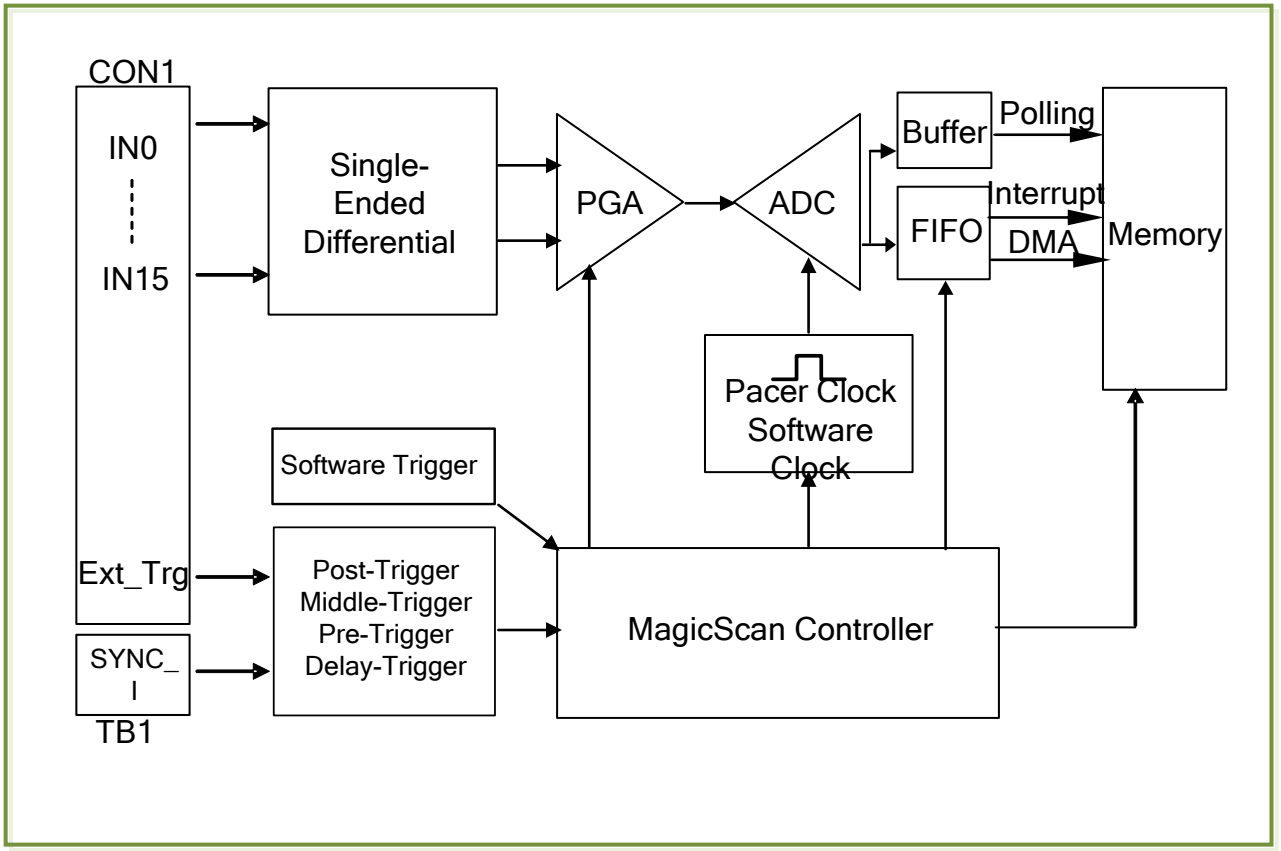
(AI0+,AI0-) ~ (AI7+,AI7-) : differential

I/O Connector Signal Description			
AI0 ~ AI15 **AI0+ ~ AI7+** **AI0- ~ AI7-**	AI_GND	Input	Analog Input Channels 0 through 15. Each channel pair, AIx+, AIx-(x = 0 to 7), can be configured as either two single-ended inputs or one differential input.
AI_GND	-	-	Analog Input Ground.
AO0_OUT **AO1_OUT**	AO_GND	Input	Analog Output Channels 0 and 1.
AO0_REF **AO1_REF**	AO_GND	Output	Analog Output Channel 0 and 1 External Reference.
AO_GND	-	-	Analog Output Ground.
PA0 ~ PA7 **PB0 ~ PB7** **PC0 ~ PC7** **PD0 ~ PD7**	D_GND	Input Output	Digital Input/Output Channels.
D_GND	-	-	Digital Ground
Cnt0_CLK	D_GND	Input	Counter 0 Clock Input. The clock input of counter 0 can be either external or internal, as set by software.
Cnt0_OUT	D_GND	Output	Counter 0 Output.
Cnt0_GATE	D_GND	Input	Counter 0 Gate Control.
Pacer_OUT	D_GND	Output	Pacer Clock Output. This pin pulses once for each pacer clock when turned on. If AD conversion is in the pacer trigger mode, users can use this signal as a synchronous signal for other applications.
Trg_GATE	D_GND	Input	AD External Trigger Gate. When Trg_GATE is connected to DGND, it will disable the external trigger signal to input.
Ext_TRG	D_GND	Input	AD External Trigger.
+12 V	D_GND	Output	+12 VDC Source.
+5 V	D_GND	Output	+5 VDC Source

3. Operation

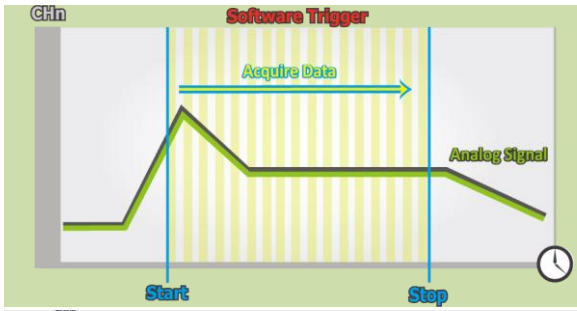
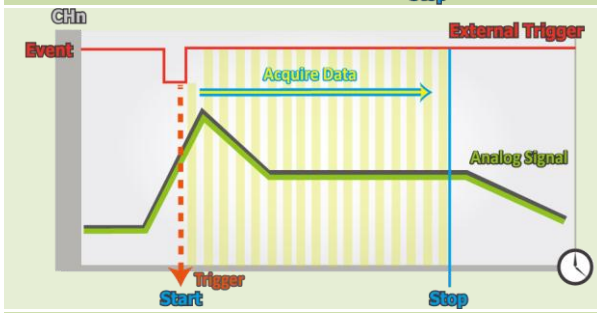
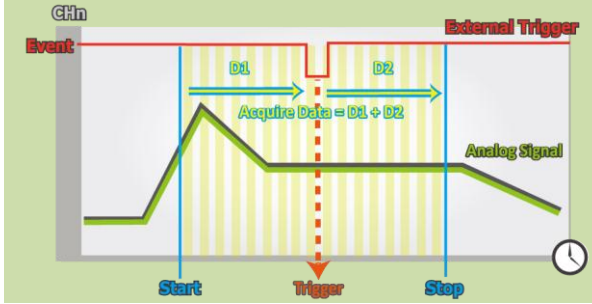
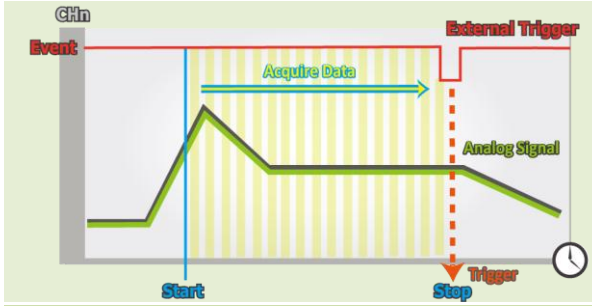
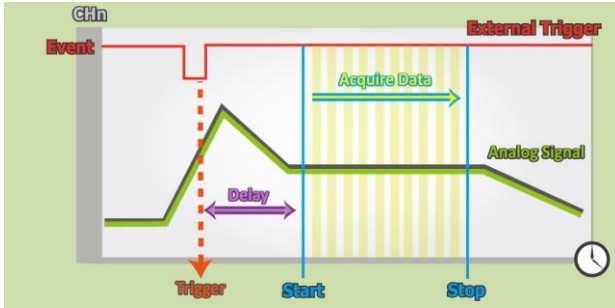
3.1. AD Operation

The block diagram of AD system is given as follows:



The trigger signal, Ext_Trg or Sync_I, is used to start a sequence of AD operations. If the Software Trigger is used, the AD operations will be started without Ext_Trg or Sync_I.

There are 5 trigger modes are given as follows:

Trigger Mode		Description
Software Trigger		There is no trigger signal. The AD operations are started by software program.
Post Trigger		The trigger signal, Ext_Trg or Sync_I, is used to start the AD operations.
Middle Trigger		The trigger signal, Ext_Trg or Sync_I, is used to indicate the middle of these AD operations.
Pre Trigger		The trigger signal, Ext_Trg or Sync_I, is used to indicate the end of these AD operations.
Delay Trigger		The trigger signal, Ext_Trg or Sync_I, is used to start the delay timer. The delay timer is used to start the AD operations. The only difference between Post-Trigger and Delay-Trigger is the delay timer.

The clock signal is generated to get one AD data. This data is saved to the buffer or FIFO. There are 2 clock sources, software clock and pacer clock, are provided.

The saved data can be transferred to PC's memory by software polling, Interrupt transfer or DMA transfer.

The combinations of trigger mode, clock signal and data transfer are provided for differential AD applications. There are 4 types of AD applications are given as follows:

Trigger Mode	Clock Mode	Transfer Mode	FIFO	Trigger Source
Software Trigger	Software	Polling	N/A	N/A
Software Trigger Post-Trigger Middle-Trigger Pre-Trigger Delay-Trigger	Pacer Clock	Polling	8K	Ext_Trg Sync_I
Software Trigger Post-Trigger Delay-Trigger	Pacer Clock	Interrupt	8K	Ext_Trg Sync_I
Software-Trigger Post-Trigger Delay-Trigger	Pacer Clock	DMA	8K	Ext_Trg Sync_I

Note:

Ext_Trg is Pin2 of CON1, Refer to Sec. 2.6.1

Sync_I is pin1 of TB1, Refer to Sec. 2.1

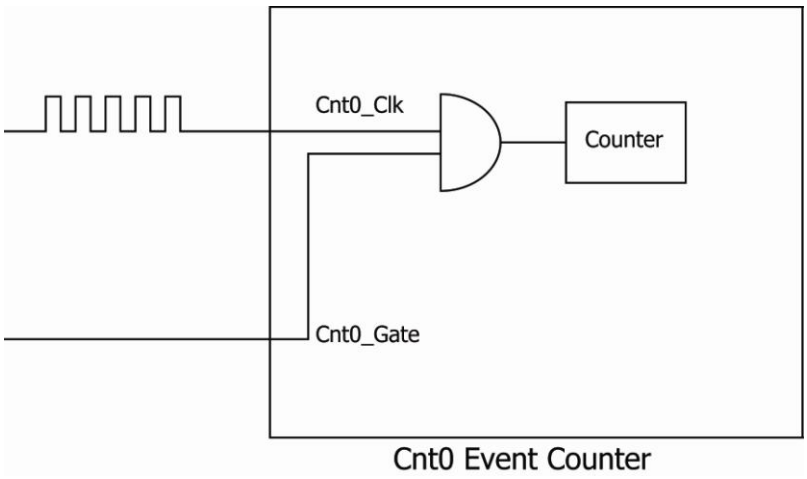
3.2. DIO Operation

There are 4 groups, PA, PB, PC and PD, provided in this board. There are 8 channels provided in every group. All groups are configured to DI when the PC is first on. The user's program can re-configure all 4 groups to DI or DO independently. The read operation from DO group will get the DO value. The write operation to DI group will not do anything. There is a digital filter provided for all DI ports.

When PA set to output mode, it can continuously output digital pattern on DO port by using user-defined data pattern and rate that bases on 100 ns high-resolution timing.

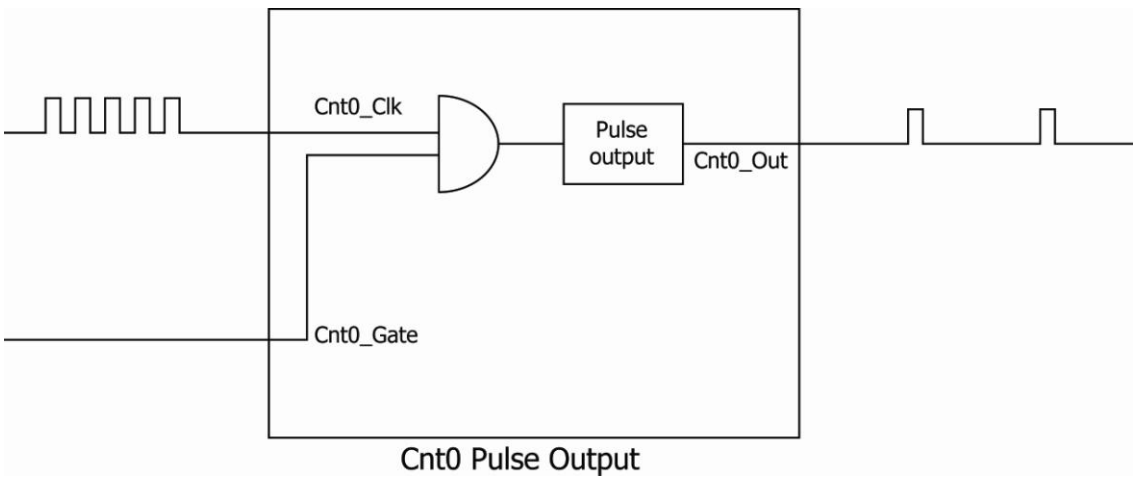
3.3. CON1 I/O Operation

The CK0 at CON1 can be used as a event counter or a pulse output. The designed as a Board Synchronization Interface. The block diagram of CK0 event Counter is given as follows:



Cnt0 Event Counter

The block diagram of CK0 pulse output is given as follows:



Cnt0 Pulse Output

4. Hardware Installation

Note:

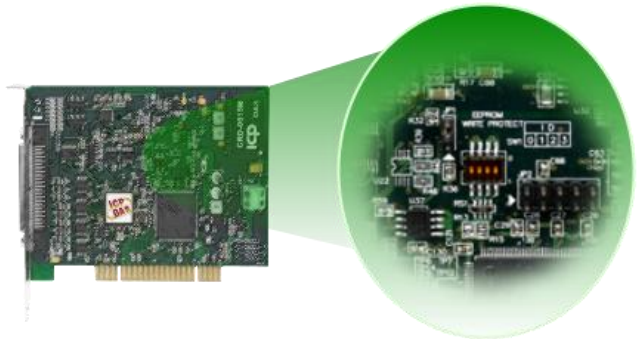
As certain operating systems, such as Windows 2000/XP may require the computer to be restarted after a new driver is installed, it is recommended that the driver is installed first, which will reduce the installation time.

Follow the process described below to install your PCI-2602U card:

Step 1: Install the PCI-2602U card driver on your computer.

For detailed information about the driver installation, please refer to Chapter 4 Software Installation.

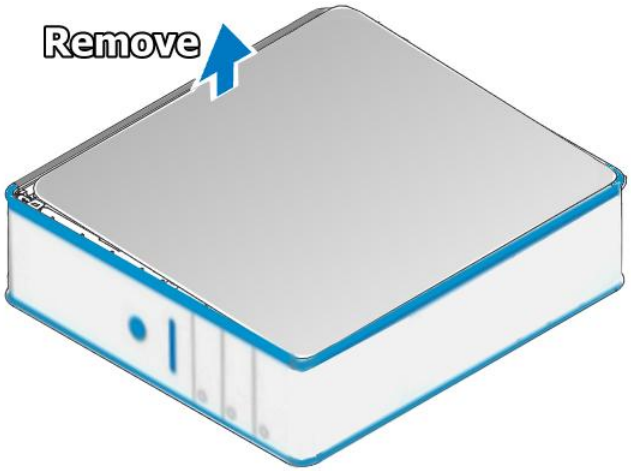
Step 2: Configuring the Card ID by the SW1 DIP-Switch.



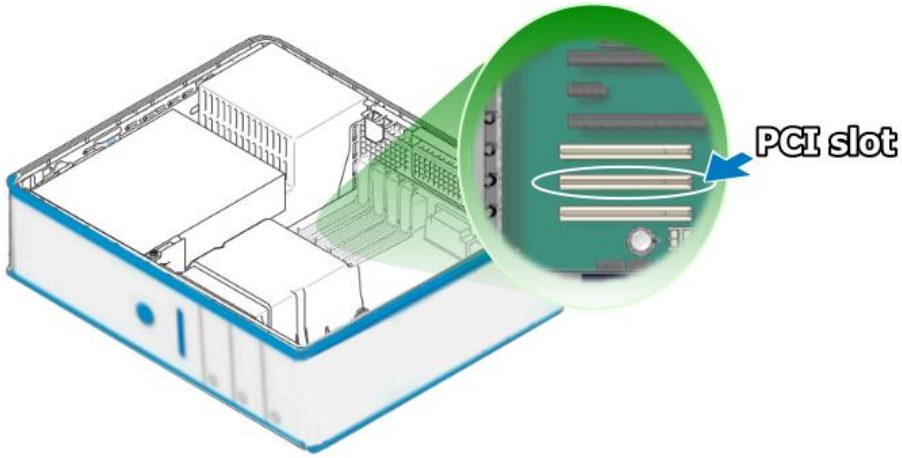
For detailed information about the card ID (SW1), please refer to Sec. 2.2.2 Card ID Switch .

Step 3: Correctly shut down and power off your computer, and then disconnect the power supply.

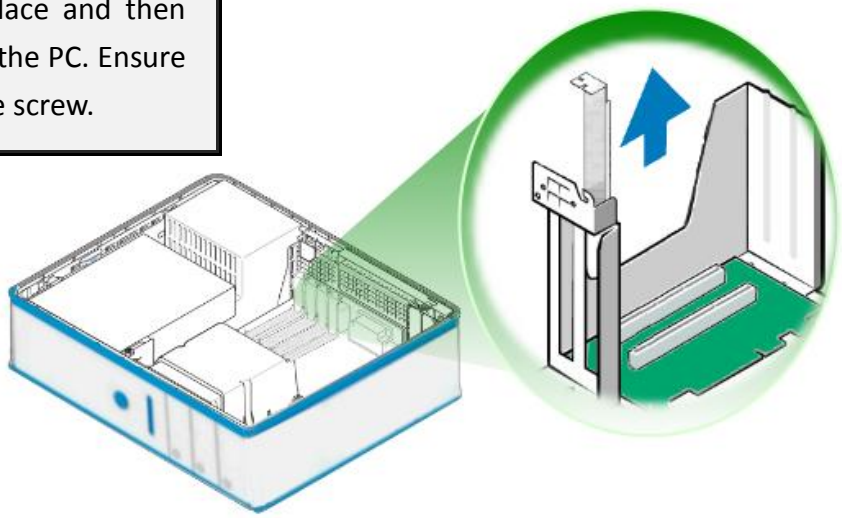
Step 4: Remove the cover from the computer.

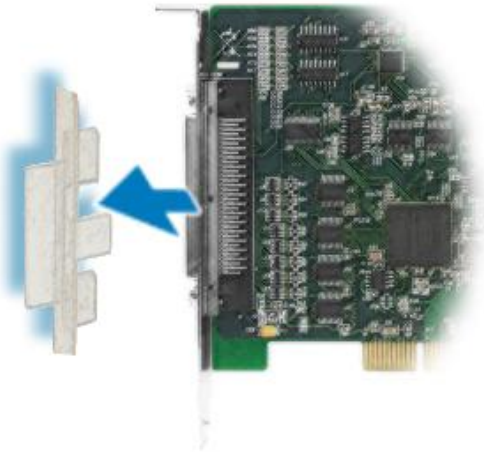


Step 5: Select an empty PCI slot.



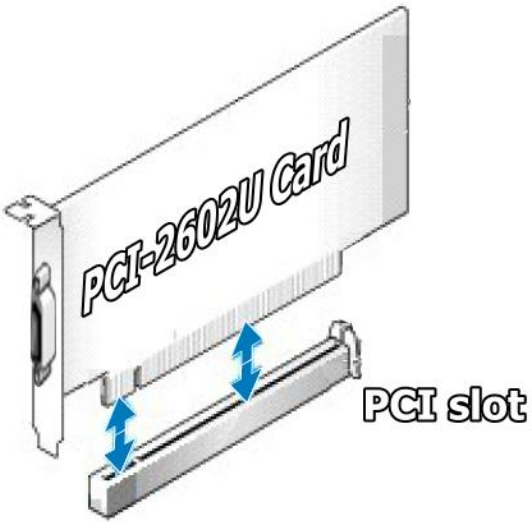
Step 6: Remove the screw holding the cover for the PCI slot in place and then remove the slot cover from the PC. Ensure that you do not misplace the screw.

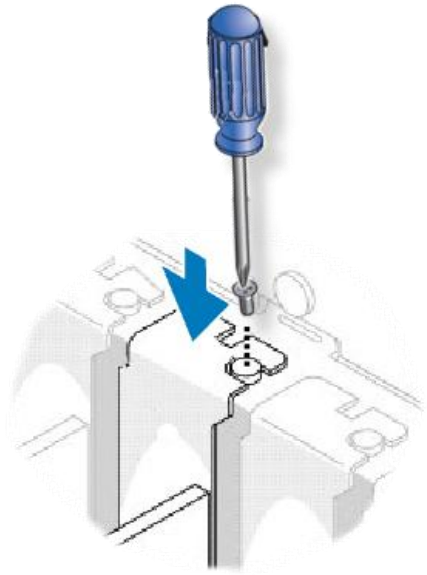




Step 7: Remove the connector cover form the PCI-2602U card.

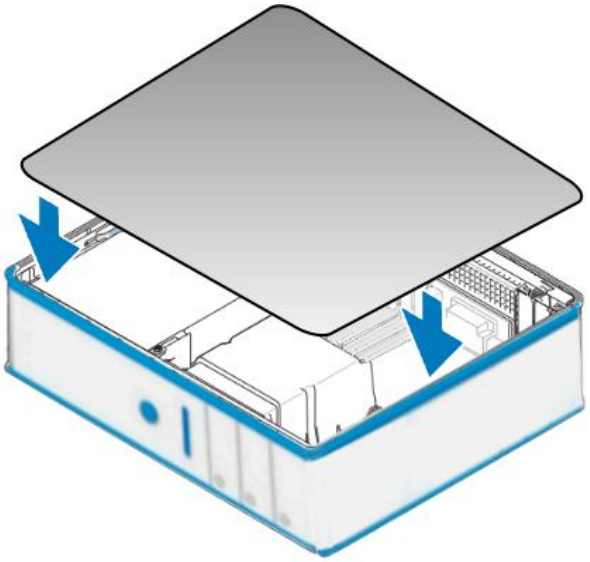
Step 8: Align the contacts of the PCI card with the open slot on your motherboard and carefully insert your PCI-2602U card into the PCI slot.





Step 9: Screw the mounting bracket screw removed in step 5 into the new PCI card bracket to secure the card in place.

Confirm that the PCI-2602U card is correctly mounted on the motherboard.



Step 10: Re-attach cover for the computer and reconnect the power supply.

Step 11: Power on the computer.

Follow the prompt message to finish the Plug&Play steps, please refer to Chapter 4 Software Installation.

5. Software Installation

This chapter provides a detailed description of the process for installing the PCI-2602U driver and how to verify whether the PCI-2602U was properly installed. PCI-2602U card can be used on Windows 2000 and 32-/64-bit XP/2003/2008/Vista/7/8 based systems, and the drivers are fully Plug &Play (PnP) compliant for easy installation.

5.1 Obtaining/Installing the Driver Installer Package

The driver installer package for the PCI-2602U card can be found on the supplied CD-ROM, or can be obtained from the ICP DAS FTP web site. Install the appropriate driver for your operating system. The location and addresses are indicated in the Table5.1-1 below.

Table 5.1-1: UniDAQ Driver/SDK

OS	Windows 2000、32/64-bit Windows XP、32/64-bit Windows 2003、32/64-bit Windows 2008、32/64-bit Windows Vista、32/64-bit Windows 7、32/64-bit Windows 2008、32/64-bit Windows 8
Driver Name	**UniDAQ Driver/SDK (unidaq_win_setup_xxxx.exe)**
CD-ROM	CD:\\ NAPDOS\PCI\UniDAQ\DLL\Driver\
Web Site	http://ftp.icpdas.com/pub/cd/iocard/pci/napdos/pci/unidaq/dll/driver/
Installing Procedure	For detailed information about the UniDAQ driver installation, please refer to UniDAQ DLL Software Manual. The user manual is contained in: CD:\NAPDOS\PCI\UniDAQ\Manual\ http://ftp.icpdas.com/pub/cd/iocard/pci/napdos/pci/unidaq/manual/

5.2 PnP Driver Installation

Power off the computer and install the PCI-2602U card. Turn on the computer and Windows 2000 and 32-/64-bit Windows XP/2003/2008/Vista/7/8 should automatically defect the new PCI device(s) and then ask for the location of the driver files for the hardware.

5.3 Verifying the Installation

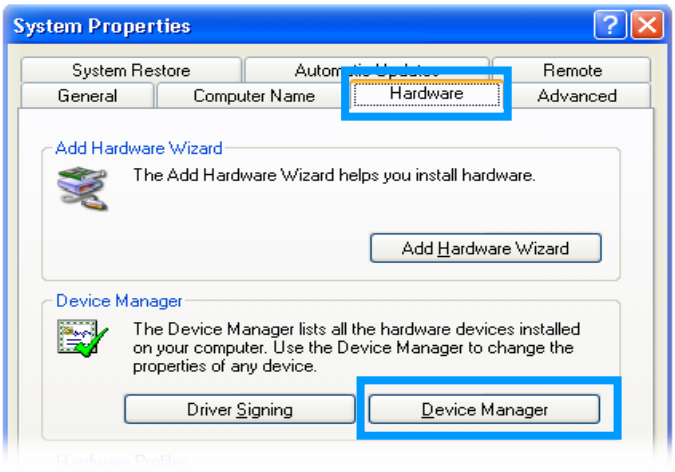
To verify the installation, use the Windows **Device Manager** to view and update the device drivers installed on your computer, and check to ensure that hardware is operating correctly. The following is a description of how access the Device Manager in each of the major versions of Windows. Refer to the appropriate description for your specific operating system to verify the installation.

5.3.1 How do I get into Windows Device Manager?

■ Microsoft Windows 2000/XP

Step 1: Click **"Start"** → then point to **"Settings"** → **"Control Panel"**.
Double-click the **"System"** icon to open the **"System Properties"** dialog box.

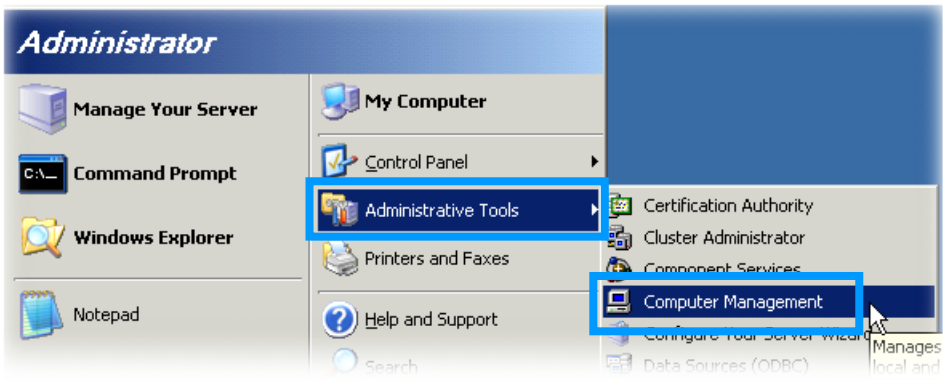
Step 2: Click the "**Hardware**" tab and then click the "**Device Manager**" button.



■ Microsoft Windows 2003/2008

Step 1: Click **"Start"** → point to **"Administrative Tools"**, and then click **"Computer Management"**.

Step 2: From **"System Tools"** in the console tree, click **"Device Manager"**.



■ Microsoft Windows Vista/7

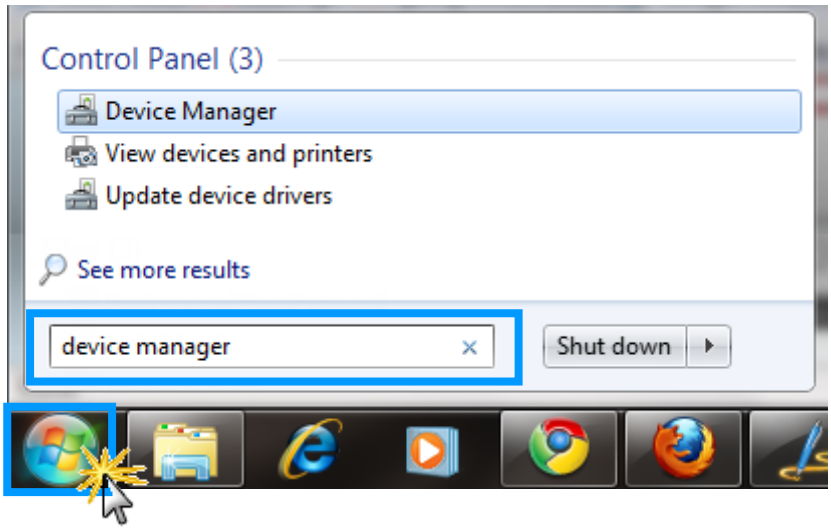
Step 1: Click **"Start"** button, and then click **"Control Panel"**.

Step 2: Click **"System and Maintenance"**, and then click **"Device Manager"**.

Alternatively,

Step 1: Click **"Start"** button.

Step 2: In the **Search field,** type **Device Manager** and the press Enter.



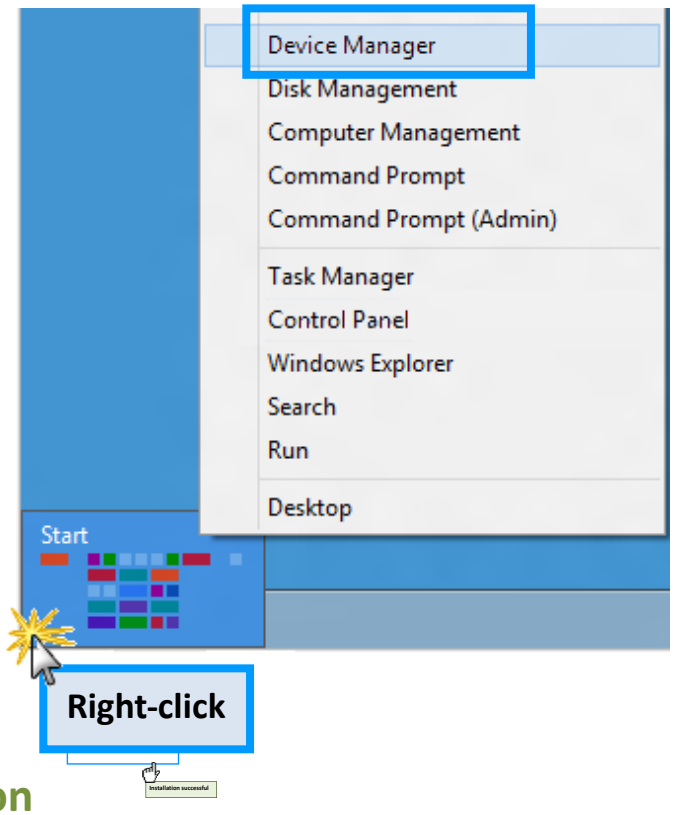
Note that Administrator privileges are required for this operation. If you are prompted for an administrator password or confirmation, type the password or provide confirmation.

■ Microsoft Windows 8

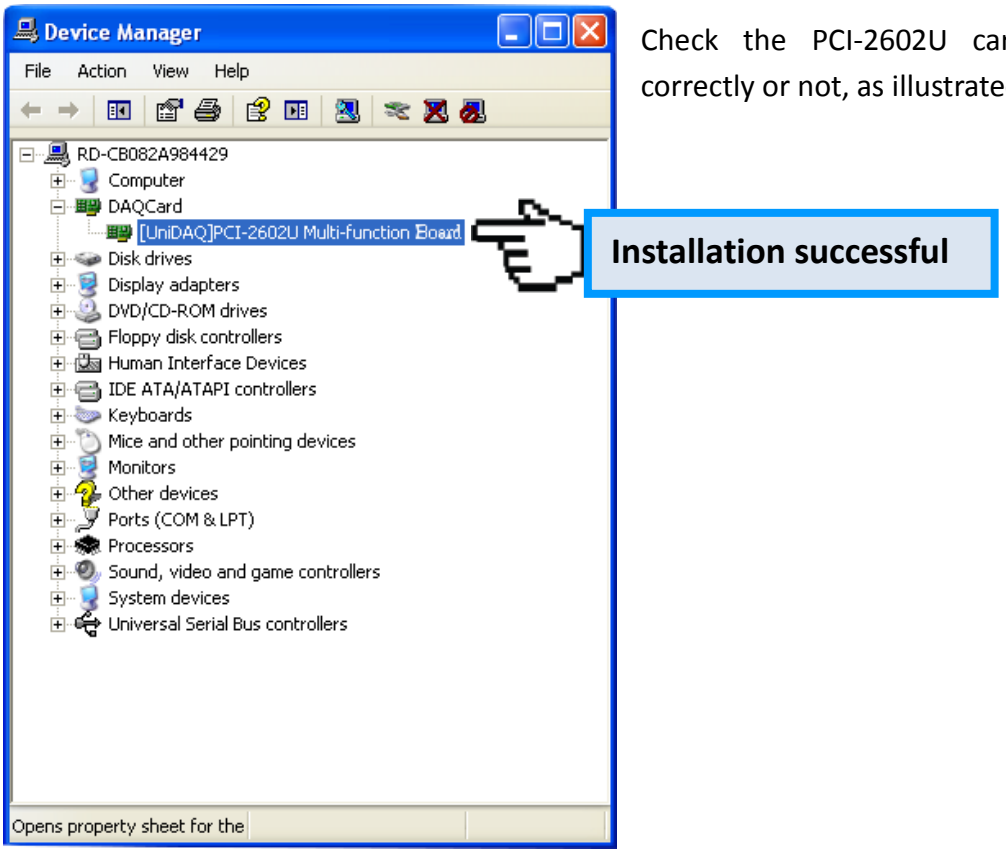
Step 1: To display the **Start screen icon** from the desktop view, simply hover the mouse cursor over the **bottom-left corner** of screen.

Step 2: Right-click **the Start screen icon then click** "Device Manager"**.**

Alternatively,
press **[Windows Key] +[X]** to open the Start Menu, and select Device Manager from the options list.



5.3.2 Check that the Installation



Check the PCI-2602U card which listed correctly or not, as illustrated below.

6. Testing PCI-2602U Card

This chapter can give you the detail steps about self-test. In this way, user can confirm that PIO-D96 series cards well or not. Before the self-test, you must complete the hardware and driver installation. For detailed information about the hardware and driver installation, please refer to Chapter 4 Hardware Installation and Chapter 5 Software Installation.

6.1 Self-Test Wiring

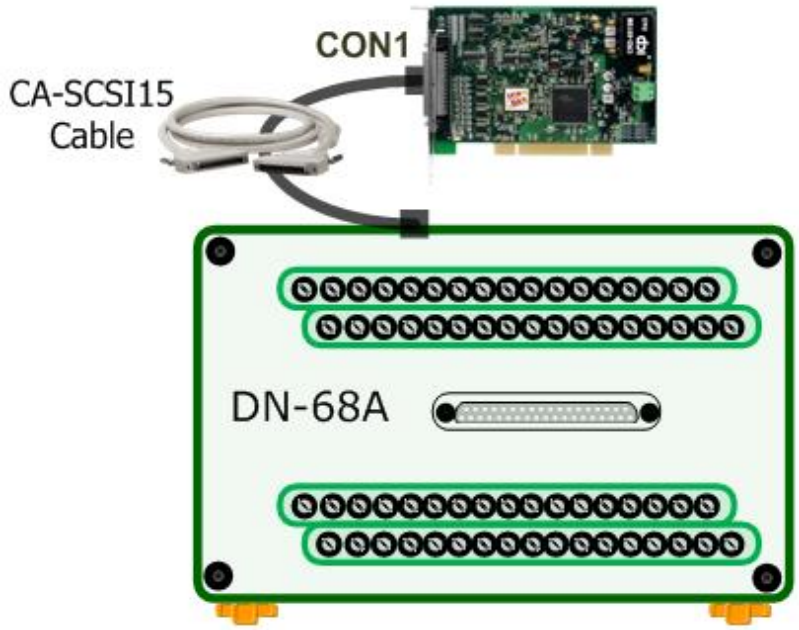
■ **Preparing the device:**

Before beginning the “self-test”, ensure that the following items are available:

☑ A CA-SCSI15-H (optional) cable

☑ A DN-68A (optional) terminal board

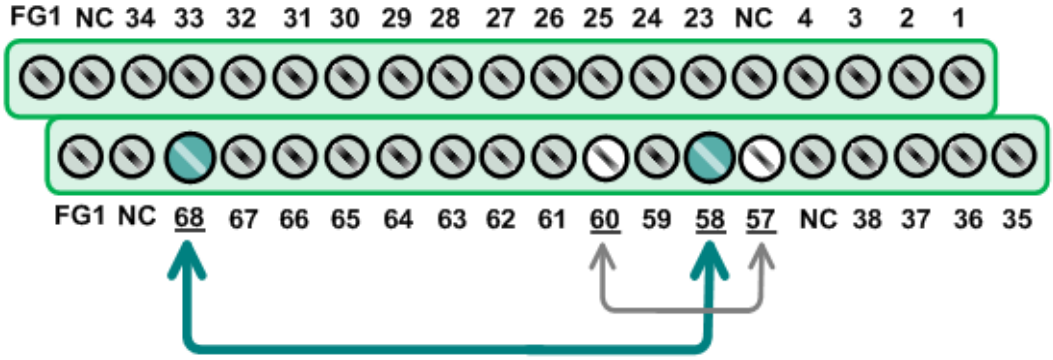
Step 1: Use the DN-68A to connect the CON1 on the PCI-2602U card.



Analog Input/Output Test Wiring:

Step 2: Open the advanced configuration tool in the Windows Device Manager to configuration the Analog Input type for **Single-Ended input**, refer to section 2.2.3 Analog Input Type Setting for more detail information.

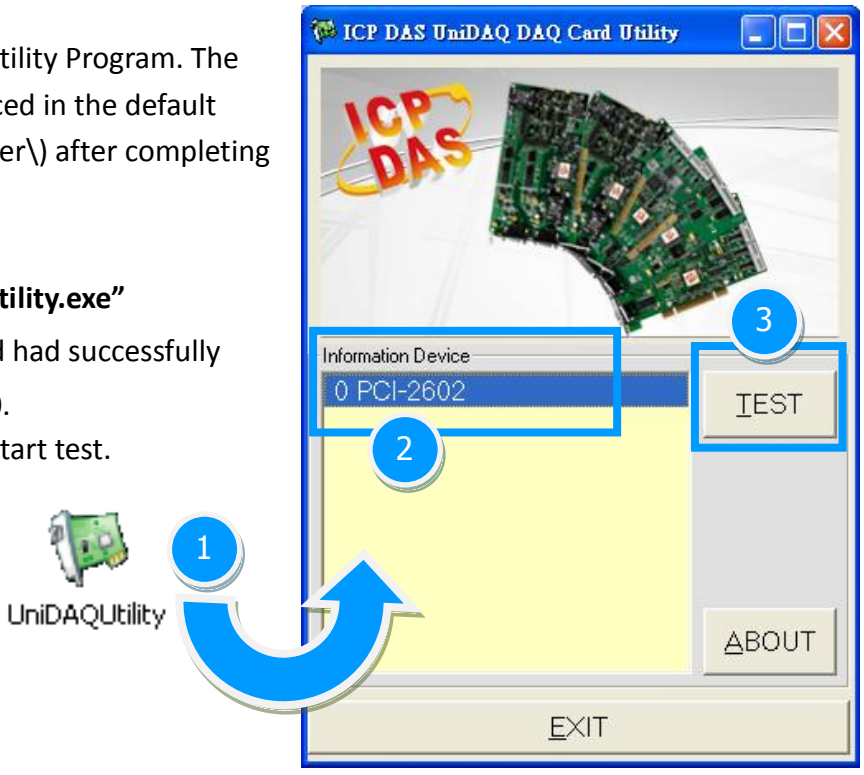
Step 3: Connect the **AO0_Out (Pin58)** to **AI0 (Pin68)**, and connect the **AI_GND(Pin60)** to **AO_GND(Pin57)**.



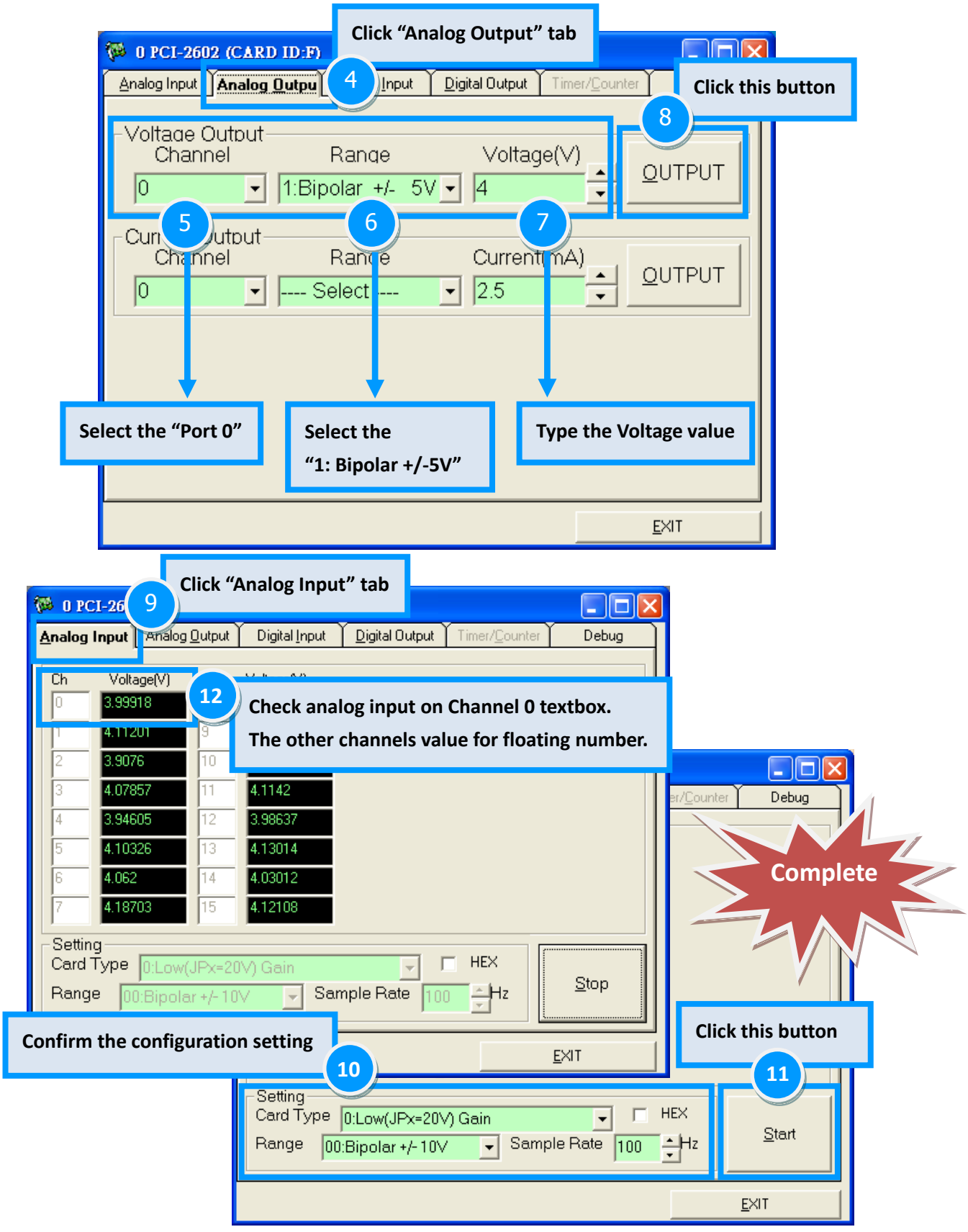
6.2 Execute the Test Program

Step 1: Execute the UniDAQ Utility Program. The UniDAQ Utility.exe will be placed in the default path (C:\ICPDAS\UniDAQ\Driver\) after completing installation.

1. Double click the **"UniDAQUtility.exe"**
2. Confirm the PCI-2602U card had successfully installed to PC. It starts form 0.
3. Click the **"TEST"** button to start test.



Step 2: Get Analog Input/Output function test result.



7. I/O Register Address

7.1. Find the I/O Address on DOS

The Plug&Play BIOS assigns a proper I/O address to every PCI-2602U card in the power-on stage. The IDs of PCI-2602 are as follows:

Model Name	PCI-2602U
Vendor ID	0x10B5
Device ID	0x9054
Sub Vendor ID	0x3577
Sub Device ID	0x2602

We provide the following necessary functions:

1. **P2602_DriverInit(&wTotalBoards)**

   This function detects how many PCI-2602U cards are installed in the system, and also records all their I/O resources information in the library. The function is implemented based on the PCI Plug & Play mechanism.

   - wTotalBoards=1 → only one PCI-2602U in this PC system.
   - wTotalBoards=2 → there are two PCI-2602U in this PC system.

2. **P2602_GetConfigAddressSpace(wBoardNo,**
   ***wBaseAddr,**
   ***wIrqNo,**
   ***wBasePLX,**
   ***dwBaseAddr,**
)

Use this function to get I/O resources information of a PCI-2602U installed in this system. Then the application program can control all functions of PCI-2602U directly.

- wBoardNo=0 to N → totally N+1 cards of **wBaseAddr**
- wBaseAddr, wBasePLX, dwBaseAddr → base address of the board
- wIrq → allocated IRQ channel number of this board

Here's the sample program source code for DOS:

```
// Step1: Detect all PCI-2602U cards first
wRetVal=P2602_DriverInit(&wTotalBoards);
printf("Threr are %d PCI-2602U Cards in this PC\n",wBoards);

// Step2: Save resources of all PCI-2602U cards installed in this PC
for (wBoardNo=0; i<wBoards; i++)
    {
    P2602_GetConfigAddressSpace(i,
                                          &wBaseAddr[wBoardNo],
                                          &wIrqNo[wBoardNo],
                                          &wBasePLX[wBoardNo],
                                          &dwBaseAddr[wBoardNo],
                                          );

    printf("\nCard%d: wBase=%x, wIrq=%x, wBasePLX=%x,dwBaseAddr = %lx",
    , wBoardNo[wBoardNo]
    ,wBaseAddr[wBoardNo]
    ,wIrqNo[wBoardNo]
    ,wBasePLX[wBoardNo]
    ,dwBaseAddr[wBoardNo]); }

// Step3: Control the PCI-2602U directly
// write the DIO states of card0
   mem4g_write_dword(dwBaseAddr[0] +0x214,dwDoValue);

// read the DIO states of card0
   dwDiValue= mem4g_read_dword(dwBaseAddr[0] +0x214);

// write the DIO states of card1
   mem4g_write_dword(dwBaseAddr[1] +0x214,wDoValue);

// read the DIO states of card1
wDiValue= mem4g_read_dword(wBaseDIO+0x0);
```

7.2. The I/O Address Map

The list of PCI-2602U registers is given below. The address of each register is found by simply adding the offset to the base address of the corresponding section. More detailed descriptions of each register will be shown in the following text and the software manual.

Bar No.	Offset	Register Function Script	
		Read	Write
1 (PLX)	68H	PLX Interrupt Control/Status	PLX Interrupt Control/Status
	80H | B8H	DMA Control/Status	DMA Control/Status
3 (MMIO)	200H	Initialize Control/Status	Hardware Status
	204H	Interrupt Control/Status	Interrupt Control/Status
	208H	EEPROM Control/Status	EEPROM Control/Status
	20CH	EEPROM Control/Status	EEPROM Control/Status
	210H	DIO Mode Control/Status	DIO Mode Control/Status
	214H	Read DIO Port	Write DIO Port
	218H	Read DI FIFO Data	N/A
	21CH	DI FIFO Status	N/A
	220H	DO Pattern Output Control/Status	DO Pattern Output Control/Status
	22CH	AI Scan Mode Control/Status	AI Scan Mode Control/Status
	230H	Time Tick Status(ms)	N/A
	234H	Time Tick Status(us)	N/A
	238H	CNT0 Clock Control/Status	CNT0 Clock Control/Status
	23CH	Delay Trigger Clock Control/Status	Delay Trigger Clock Control/Status
	240H	DI Filter Clock Control/Status	DI Filter Clock Control/Status
	244H	AI Internal Clock Control/Status	AI Internal Clock Control/Status
	248H	DI Internal Clock Control/Status	DI Internal Clock Control/Status
	24CH	DO Internal Clock Control/Status	DO Internal Clock Control/Status
	250H	AO0 Internal Clock Control/Status	AO0 Internal Clock Control/Status
	254H	AO1 Interrupt Clock Control/Status	AO1 Interrupt Clock Control/Status
	258H	Internal Clock Control	N/A
	280H	AI External Analog Trigger Control/Status	AI External Analog Trigger Control/Status
	290H	AI Trigger Mode Control/Status	AI Trigger Mode Control/Status
	294H	AI Software Trigger Status	AI Software Trigger Control
	298H	AI Scan Address	AI Scan Address
	2ECH	AI Configuration Control/Status	AI Configuration Control/Status
	2F0H	Save AI Configuration	N/A

Note: The length of the register is **32-bit**.

Bar No.	Offset	Register Function Script	
		Read	Write
3 (MMIO)	2A0H	Read AI FIFO Data	N/A
	2A4H	AI FIFO Status	N/A
	2A8H	AI Data Acquisition Size	AI Data Acquisition Size
	2ACH	AI Data Acquisition Start	AI Data Acquisition Start
	2B0H	AO Configuration Control/Status	AO Configuration Control/Status
	2B4H	Write AO Channel 0 Data	Write AO Channel 0 Data
	2B8H	Write AO Channel 1 Data	Write AO Channel 1 Data
	2BCH	AO Pattern Output Control/Status	AO Pattern Output Control/Status
	2C4H	Connector I/O Control/Status	Connector I/O Control/Status

7.3. Bar 1

7.3.1 PLX Control/Status registers

- (Write/Read)wBase+0x68 **Read/Write interrupt Control/Status**

  The detail information, please refer the PLX9054 document.
  http://www.plxtech.com/products/io/pci9054#technicaldocumentation

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- (Write)wBase+0x80 ~0xB8 **Read/Write DMA Control/Status**

  The detail information, please refer the PLX9054 document.
  http://www.plxtech.com/products/io/pci9054#technicaldocumentation

7.4. Bar 3

7.4.1 Interrupt and Initialize Control/Status Registers

Register 7.4.1-1wBase+0x200 **Initialize Control/Status**

Bit	Description	Write
0	**Reset AI Mode.** Write a 1 and Write a 0 to resets AI Mode.	Yes
1	**Clear AI FIFO.** Write a 1 and Write a 0 to clear AI FIFO.	Yes
2	**Reset AI FIFO Overflow Status.** Write a 1 and Write a 0 to resets AI FIFO over flow status.	Yes
3	**PCI Clear Interrupt.** Write a 1 and Write a 0 to clear PCI interrupts.	Yes
4:5	***Reserved.***	Yes
6	**DI(PC) FIFO Reset.** Write a 1 and Write a 0 to resets digital input FIFO.	Yes
7	**DO(PA) FIFO Reset.** Write a 1 and Write a 0 to resets digital output FIFO.	Yes
8	**AO0 FIFO Reset.** Write a 1 and Write a 0 to resets analog output channel 0 FIFO.	Yes
9:31	***Reserved.***	No

Register 7.4.1-2 wBase+0x200 **Hardware Status**

Bit	Description	Read
0:3	**Card ID.** Reading a data indicates a Card ID of SW1.	Yes
4:7	***Reserved.***	Yes
8	**PA DIO Mode.** Reading a 1 indicates a PA is DO mode. Reading a 0 indicates a PA is DI mode.	Yes
9	**PB DIO Mode.** Reading a 1 indicates a PB is DO mode. Reading a 0 indicates a PB is DI mode.	Yes
10	**PC DIO Mode.** Reading a 1 indicates a PC is DO mode. Reading a 0 indicates a PC is DI mode.	Yes
11	**PD DIO Mode.** Reading a 1 indicates a PD is DO mode. Reading a 0 indicates a PD is DI mode.	Yes
12:31	***Reserved.***	Yes

Register 7.4.1-3 wBase+0x204 **Interrupt Clear/Status**

Bit	Description	Read	Write
0	**AI Pacer Done Int.** Reading a 1 indicates an analog input pacer is complete. Reading a 0 indicates a pacer is not complete. Write a 1 and write a 0 to clear AI Pacer Down interrupt.	Yes	Yes
1	**AI FIFO Half-Full Int.** Reading a 1 indicates an analog input FIFO status is half-full. Reading a 0 indicates an analog input FIFO status is not half-full. Write a 1 and write a 0 to clear AI FIFO Half-Full interrupt.	Yes	Yes
2	**AI FIFO Full Int.** Reading a 1 indicates an analog input FIFO status is full. Reading a 0 indicates an analog input FIFO status is not full. Write a 1 and write a 0 to clear AI FIFO FULL interrupt.	Yes	Yes
3	**DI Pacer Done Int.** Reading a 1 indicates a digital input pacer is complete. Reading a 0 indicates a digital pacer is not complete. Write a 1 and write a 0 to clear DI Pacer Down interrupt.	Yes	Yes
4	**DI(PC) FIFO Half-Full Int.** Reading a 1 indicates a digital input FIFO status is half-full. Reading a 0 indicates a digital input FIFO status is not half-full. Write a 1 and write a 0 to clear DI FIFO Half-Full interrupt.	Yes	Yes
5	**DI(PC) FIFO Full Int.** Reading a 1 indicates a digital input FIFO status is full. Reading a 0 indicates a digital input FIFO status is not full. Write a 1 and write a 0 to clear DI FIFO FULL interrupt.	Yes	Yes
6	**AO0 Pattern Done Int.** Reading a 1 indicates a AO0 Pattern output is complete. Reading a 0 indicates a AO0 Pattern output is not complete. Write a 1 and write a 0 to clear AO0 Pattern Done interrupt.	Yes	Yes
7	**DO(PA) Pattern Done Int.** Reading a 1 indicates a DO(PA) Pattern output is complete. Reading a 0 indicates a PA Pattern output is not complete. Write a 1 and write a 0 to clear PA Pattern Done interrupt.	Yes	Yes
8	**External Trigger Int.** Reading a 1 indicates an external trigger status is ready. Reading a 0 indicates an external trigger status is not ready. Write a 1 and write a 0 to clear external trigger interrupt.	Yes	Yes
9	**SYNC_I Trigger Int.**	Yes	Yes
10	**Analog Trigger Int.** Reading a 1 indicates an analog trigger status is ready. Reading a 0 indicates an analog trigger status is not ready. Write a 1 and write a 0 to clear analog trigger interrupt.	Yes	Yes
11	**Counter Int.** Reading a 1 indicates an Counter Interrupt status is ready. Reading a 0 indicates an analog trigger status is not ready. Write a 1 and write a 0 to clear analog trigger interrupt.	Yes	Yes
12:31	***Reserved.***	Yes	No

Register 7.4.1-4 wBase+0x224 **Interrupt Mode Control/Status**

Bit	Description	Read	Write
0	**Enable AI Pacer Done Interrupt.** Write a 1 enables interrupt when analog input pacer is done.	Yes	Yes
1	**Enable AI FIFO Half-Full Interrupt.** Write a 1 enables interrupt when analog input FIFO is half-full.	Yes	Yes
2	**Enable AI FIFO Full Interrupt.** Write a 1 enables interrupt when analog input FIFO is full.	Yes	Yes
3	**Enable DI(PC) Pacer Done Interrupt.** Write a 1 enables digital input interrupt when pacer done.	Yes	Yes
4	**Enable DI(PC) FIFO Half-Full Interrupt.** Write a 1 enables digital input FIFO half-full interrupt.	Yes	Yes
5	**Enable DI(PC) FIFO Full Interrupt.** Write a 1 enables digital input FIFO full interrupt.	Yes	Yes
6	**Enable AO0 Pattern Done Interrupt.** Write a 1 enables AO0 pattern down interrupt.	Yes	Yes
7	**Enable DO(PA) Pattern Done Interrupt.** Write a 1 enables PA pattern down interrupt.	Yes	Yes
8	**Enable External Trigger Interrupt.** Write a 1 enables external trigger interrupt.	Yes	Yes
9	**Enable SYNC_I Trigger Interrupt.**	Yes	Yes
10	**Enable Analog Trigger Interrupt.** Write a 1 enables analog trigger interrupt.	Yes	Yes
11	**Enable Timer Interrupt.**	Yes	Yes
12:31	***Reserved.***	Yes	No

7.4.2 Digital I/O Registers

Register 7.4.2-1 wBase+0x210 **DIO Mode Control/Status**

Bit	Description	Read	Write
0	**PA DIO Mode.** Write a 1 indicates a PA is DO mode. Write a 0 indicates a PA is DI mode.	Yes	Yes
1	**PB DIO Mode.** Write a 1 indicates a PB is DO mode. Write a 0 indicates a PB is DI mode.	Yes	Yes
2	**PC DIO Mode.** Write a 1 indicates a PC is DO mode. Write a 0 indicates a PC is DI mode.	Yes	Yes
3	**PD DIO Mode.** Write a 1 indicates a PD is DO mode. Write a 0 indicates a PD is DI mode.	Yes	Yes
4	**Enable PA Digital Input Filter.** Write a 1 enables digital input filter.	Yes	Yes
5	**Enable PB Digital Input Filter.** Write a 1 enables digital input filter.	Yes	Yes
6	**Enable PC Digital Input Filter.** Write a 1 enables digital input filter.	Yes	Yes
7	**Enable PD Digital Input Filter.** Write a 1 enables digital input filter.	Yes	Yes
8:10	**DI Clk Select.** Write a 100 enables digital output clock.	Yes	Yes
11:13	**DO Clk Select.** Write a 101 enables digital output clock.	Yes	Yes
14	**PA Output Mode.** Writing a 1 indicates the PA output mode is pattern mode. Writing a 0 indicates the PA output mode is static mode.	Yes	Yes
15:31	***Reserved.***	Yes	No

Register 7.4.2-2 wBase+0x214 **Write DIO Port**

Bit	Description	Read	Write
0:7	**PA Write.** Write the digital output data to specified digital I/O Port-PA, When PA is digital output mode.	Yes	Yes
8:15	**PB Write.** Write the digital output data to specified digital I/O Port-PB, When PB is digital output mode.	Yes	Yes
16:23	**PC Write.** Write the digital output data to specified digital I/O Port-PC, When PC is digital output mode.	Yes	Yes
24:31	**PD Write.** Write the digital output data to specified digital I/O Port-PD, When PD is digital output mode.	Yes	Yes

Register 7.4.2-3 wBase+0x214 **Read DIO Port**

Bit	Description	Read
0:7	**PA Read.** Read the digital input data to specified digital I/O Port-PA, When PA is digital input mode.	Yes
8:15	**PB Read.** Read the digital input data to specified digital I/O Port-PB, When PB is digital input mode.	Yes
16:23	**PC Read.** Read the digital input data to specified digital I/O Port-PC, When PC is digital input mode.	Yes
24:31	**PD Read.** Read the digital input data to specified digital I/O Port-PD, When PD is digital input mode.	Yes

Register 7.4.2-4 wBase+0x218 **Read DI FIFO Data**

Bit	Description	Read
0:7	**FIFO Read.** Read the digital input data to specified FIFO.	Yes
8:31	***Reserved.***	Yes

Register 7.4.2-5 wBase+0x21C **DI FIFO Status**

Bit	Description	Read
0:15	***Reserved.***	Yes
16	**FIFO Empty.** Reading a 1 indicates a FIFO status is empty.	Yes
17	**FIFO Full.** Reading a 1 indicates a FIFO status is full.	Yes
18	**FIFO Half Full.** Reading a 1 indicates a FIFO status is half-full.	Yes
19	**FIFO Almost Full.** Reading a 1 indicates a FIFO status is almost full.	Yes
20	**FIFO Almost Empty.** Reading a 1 indicates a FIFO status is almost empty.	Yes
21	**FIFO Overflow.** Reading a 1 indicates a FIFO status is overflow.	Yes
22:31	***Reserved.***	Yes

Register 7.4.2-6 wBase+0x220 **DO Pattern Control/Status**

Bit	Description	Read	Write
0:10	**DO(PA) Data Num.** Write value indicates the waveform points for PA.	Yes	Yes
11:15	**DO(PA) Cycle Num.** Write 0~30 indicates the PA is burst mode, the write n indicates to generate n+1 pulse. Write 31 indicates the PA output mode is continuous mode.	Yes	Yes
16:31	***Reserved***	Yes	No

7.4.3 Analog Input Registers

Register 7.4.3-1 wBase+0x22C **AI Scan Mode Control/Status**

Bit	Description	Read	Write
0	**Enable AI Scan.** Writing a 1 enables MagicScan Mode to scan analog input channel.	Yes	Yes
1:16	**Total Scan Channel Number.** Indicates the number of channels to MagicScan. Writing a N indicates an N+1 channels. Ex. Writing a 14 indicates 15 channels. Writing an 8 indicates 9 channels.	Yes	Yes
17:31	***Reserved.***	Yes	No

Register 7.4.3-2 wBase+0x244 **AI Internal Clock Control/Status**

Bit	Description	Read	Write
0:23	**Set Div Clock.** Indicates the (WORD)((Base Clock/Sampling Rate)-1) to set internal pacer clock during an analog input operation.	Yes	Yes
24:25	**Select Base Clock.** Writing 00 indicates 40MHz. Writing 01 indicates 10M. Writing 10 indicates 1MHz. Writing 11 indicates 100KHz.	Yes	Yes
26:31	***Reserved.***	Yes	No

Register 7.4.3-3 wBase+0x290 **AI Trigger Mode Control/Status**

Bit	Description	Read	Write
0:2	**Clock Source.** Writing 000 indicates a non-clock source. Writing 001 indicates a Single Clk. Writing 010 indicates a T3 Clk. Writing 101 indicates an external clock source.	Yes	Yes
3:4	**Trigger Source.** Writing 00 indicates an external trigger. Writing 01 indicates an Sync_I.	Yes	Yes
5:7	**Trigger Mode.** Writing 000 indicates an internal trigger mode. Writing 001 indicates a post-trigger mode. Writing 010 indicates a middle-trigger mode. Writing 011 indicates a pre-trigger mode. Writing 100 indicates a delay-trigger mode. Writing 101 indicates a analog-trigger mode.	Yes	Yes
8	**Enable Analog Trigger.** Writing a 1 enables analog trigger mode to acquire the analog data when an external analog signal start.	Yes	Yes
9:11	**Analog Trigger Type.** Writing 000 disable analog trigger mode. Writing 001 enable a above-high. Writing 010 enable a below-low. Writing 011 enable inside-region (V2<AD<V1). Writing 100 enable an outside-region (AD>V1, AD<V2).	Yes	Yes
12:31	***Reserved.***	Yes	No

Register 7.4.3-4 wBase+0x294 **AI Software Trigger Control**

Bit	Description	Read	Write
0	**Software Trigger Start.** Writing a 0 causes the analog input channel to measure analog input data.	No	Yes
1:31	***Reserved.***	Yes	No

Register 7.4.3-5 wBase+0x294 **AI Software Trigger Status**

Bit	Description	Read	Write
0:15	**Software Trigger Data Read.** Read the analog input data.	Yes	No
16	**Trigger Status.** Reading a 1 indicates a Trigger Status is ready. Reading a 0 indicates a Trigger Status is busy.	Yes	No
17:31	***Reserved.***	Yes	No

Register 7.4.3-6 wBase+0x298 **AI Scan Address**

Bit	Description	Read	Write
0:15	**AI Scan Address Register.** Indicates the scan sequence number during a MagicScan operation.	No	Yes
16:31	***Reserved.***	Yes	No

Register 7.4.3-7 wBase+0x2EC **AI Configuration Control/Status**

Bit	Description	Read	Write
0	**1**	Yes	Yes
1	**0**	Yes	Yes
2	**1**	Yes	Yes
3	**1**	Yes	Yes
4	**0**	Yes	Yes
5	**0**	Yes	Yes
6	**1**	Yes	Yes
7:9	**Analog Input Range (Gain).**	Yes	Yes
10	**1**	Yes	Yes
11	**Analog Input Type.** Writing a 1 indicates a signal-ended type. Writing a 0 indicates a differential type.	Yes	Yes
12	**Channel Select 0.** Writing a 1 indicates an odd channel. Writing a 0 indicates an even channel.	Yes	Yes
13	***Reserved.***	Yes	No
14	***Reserved.***	Yes	No
15	**1**	Yes	Yes
16:18	**Channel Select 1.** Indicates value to use analog input channel number div 2.	No	Yes
19:31	***Reserved.***	Yes	No

Register 7.4.3-8 wBase+0x2F0 **Save AI Configuration Data**

Bit	Description	Read	Write
0	**Save AI Configuration Data.** Writing a 0 indicates to save configuration data.	Yes	Yes
1:31	***Reserved.***	Yes	No

Register 7.4.3-9 wBase+0x2A0 **Read AI FIFO Data**

Bit	Description	Read
0:15	**FIFO Read.** Read the analog input data to specified FIFO.	Yes
16:31	***Reserved.***	Yes

Register 7.4.3-10 wBase+0x2A4 **AI FIFO and Trigger Status**

Bit	Description	Read
0:15	***Reserved.***	Yes
16	**FIFO Empty.** Reading a 1 indicates a FIFO status is empty.	Yes
17	**FIFO Full.** Reading a 1 indicates a FIFO status is full.	Yes
18	**FIFO Half Full.** Reading a 1 indicates a FIFO status is half-full.	Yes
19	**FIFO Almost Full.** Reading a 1 indicates a FIFO status is almost full.	Yes
20	**FIFO Almost Empty.** Reading a 1 indicates a FIFO status is almost empty.	Yes
21	**FIFO Overflow.** Reading a 1 indicates a FIFO status is overflow.	Yes
22	**Trigger In.**	Yes
23	**Post Trigger.**	Yes
24	**Analog Trigger Ready**	Yes
25	**Analog Trigger V1A5**	Yes
26	**Analog Trigger V2A5**	Yes
27	**Analog Trigger Fit**	Yes
28:31	***Reserved.***	Yes

Register 7.4.3-11 wBase+0x2A8 **AI Data Acquisition Size**

Bit	Description	Read	Write
0:31	**Data Acquisition Size.** Indicates the number to acquire data during an analog input operation. Writing an 8000000 acquires analog input data continuous.	Yes	Yes

Register 7.4.3-12 wBase+0x2AC **AI Data Acquisition Start**

Bit	Description	Read	Write
0:31	**Acquisition Start.** Writing a 0 to causes channel to start acquisition data if AI Data Acquisition Size register is set.	Yes	Yes

7.4.4 Analog output registers

Register 7.4.4-1 wBase+0x2B0 **AO Configuration Control/Status**

Bit	Description	Read	Write
0	**Channel 0 Enable.** Writing a 1 enables channel to output data. Writing a 0 disables the channel.	Yes	Yes
1	**Channel 0 Polar.** Writing a 1 indicates the channel 0 polar is uni-polar. Writing a 0 indicates the channel 0 polar is Bi-polar.	Yes	Yes
2	**Channel 0 Internal Ref.** Writing a 1 indicates the channel 0 internal reference is 5V.Writing a 0 indicates the channel 0 internal reference is 10V.	Yes	Yes
3	**Channel 0 Reference Mode.** Writing a 1 indicates the channel 0 is internal reference. Writing a 0 indicates the channel 0 is external reference.	Yes	Yes
4	**Channel 1 Enable.** Writing a 1 enables channel to output data. Writing a 0 disables the channel.	Yes	Yes
5	**Channel 1 Polar.** Writing a 1 indicates the channel 1 polar is uni-polar. Writing a 0 indicates the channel 1 polar is Bi-polar.	Yes	Yes
6	**Channel 1 Internal Ref.** Writing a 1 indicates the channel 1 internal reference is 5V.Writing a 0 indicates the channel 1 internal reference is 10V.	Yes	Yes
7	**Channel 1 Reference Mode.** Writing a 1 indicates the channel 1 is internal reference. Writing a 0 indicates the channel 1 is external reference.	Yes	Yes
8	**Channel 0 Output Mode.** Writing a 1 indicates the channel 0 output mode is pattern mode. Writing a 0 indicates the channel 0 output mode is static mode.	Yes	Yes
9	**Channel 1 Output Mode.** Writing a 1 indicates the channel 1 output mode is pattern mode. Writing a 0 indicates the channel 1 output mode is static mode.	Yes	Yes
10:12	**Channel 0 Clk Select.** Write a 110 enables analog output channel 0 clock.	Yes	Yes
13:15	**Channel 1 Clk Select.** Write a 111 enables analog output channel 1 clock.	Yes	Yes
16:31	***Reserved.***	Yes	No

Register 7.4.4-2 wBase+0x2B4 **Write AO Channel 0 Data**

Bit	Description	Read	Write
0:15	**AO Channel 0 Write.** Writing the analog output data to channel 0.	Yes	Yes
16:31	***Reserved.***	Yes	Yes

Register 7.4.4-3 wBase+0x2B8 **Write AO Channel 1 Data**

Bit	Description	Read	Write
0:15	**AO Channel 1 Write.** Read the analog output data to channel 1.	Yes	Yes
16:31	***Reserved.***	Yes	Yes

Register 7.4.4-4 wBase+0x2BC **AO Pattern Output Control/Status**

Bit	Description	Read	Write
0:10	**AO Channel 0 Data Num.** Write value indicates the waveform points for channel 0.	Yes	Yes
11:15	**AO Channel 0 Cycle Num.** Write 0~30 indicates the channel 0 is burst mode, the write n indicates to generate n+1 pulse. Write 31 indicates the channel 0 output mode is continuous mode.	Yes	Yes
16:31	***Reserved***	Yes	No

8. Calibration

8.1. Calibration Introduction

The PCI-2602 is already fully calibrated when shipped from the factory including the calibration coefficients which are stored in the EEPROM on board. For more precise application of voltages at the “system end”, the following procedure provides a method that allows you to calibrate the board within your system, so that you can achieve the correct voltages at your field connection. This calibration allows the user to remove the effects of voltage drops caused by IR loss in the cable and/or connector.

At first the user has to prepare the equipment for calibration: the precise multi-meter. Note that the calibrated values for analog output/input channels are stored within 3 words in the address of the EEPROM, as show in Table 8-1. The calibration procedure will be demonstrated below:

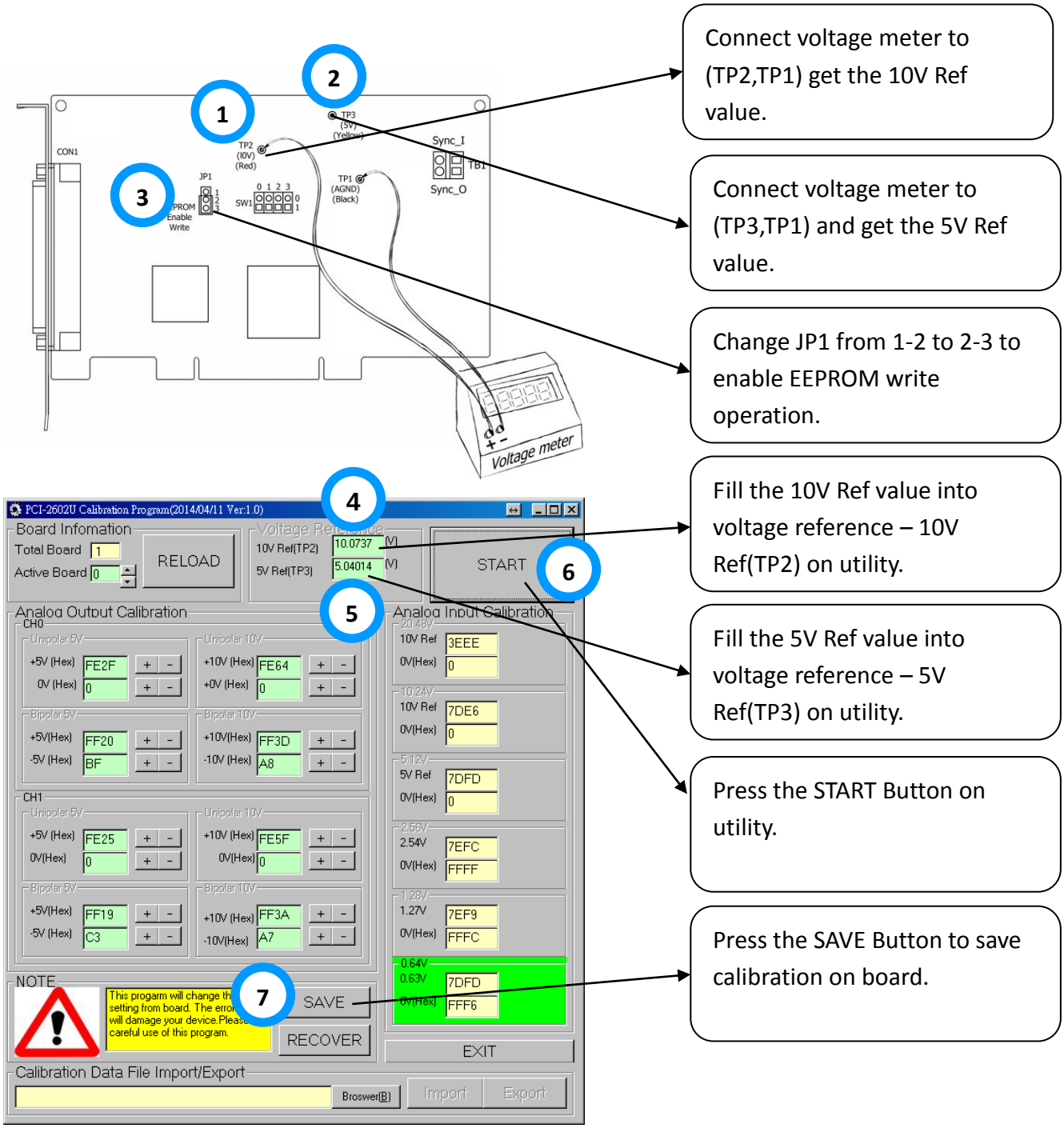
Table 8-1 Calibration values stored in the EEPROM address

EEPROM Address	Reference Calibration
10V	4:5
5V	6:7

EEPROM Address		DA Calibration	
		CH 0	CH 1
BiPolar	+5V	8	16
	+0V	9	17
Uipolar	+10V	10	18
	+0V	11	19
BiPolar	+5V	12	20
	-5V	13	21
Unipolar	+10V	14	22
	-10V	15	23

EEPROM Address		AD Calibration
		AD CH0
BiPolar 10.24V	10V Ref	24
	0V	25
BiPolar 5.12V	5V Ref	28
	0V	29
BiPolar 2.56V	2.54V	32
	0V	33
BiPolar 1.28V	1.27V	36
	0V	37
BiPolar 0.64V	0.63V	40
	0V	41
BiPolar 20.48	10V Ref	48
	0V	49

8.2. Calibration Step-by-Step



Windows Calibration Program download link:
http://ftp.icpdas.com/pub/cd/iocard/pci/napdos/pci/pci-2602/dll/calibration/

9. PCI-2602U Windows API Function

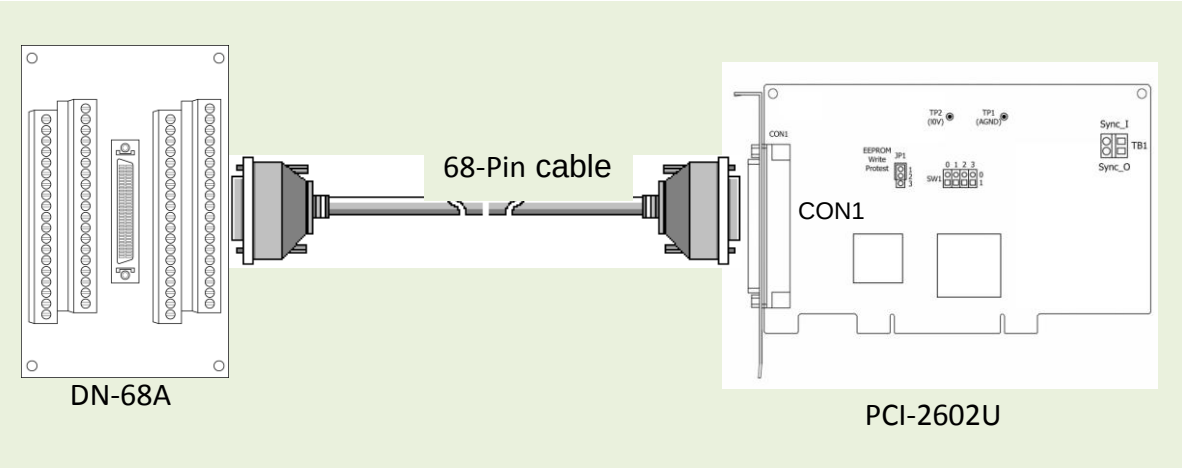
Please refer to software user manual of the UniDAQ SDK, download link from the

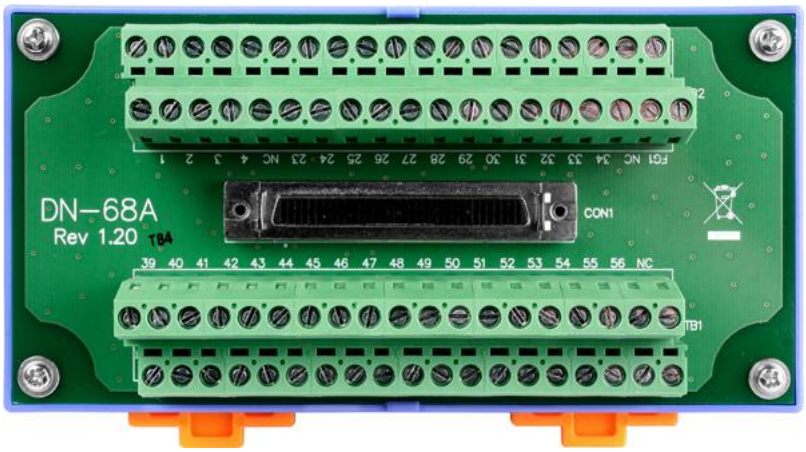
	CD:\NAPDOS\PCI\UniDAQ\Manuql
	http://ftp.icpdas.com/pub/cd/iocard/pci/napdos/pci/unidaq/manual/

Appendix: Daughter Board

A1. DB-68A

The DB-68A is a general-purpose daughter board for D-sub 68 pins. It is designed for easy wire connection.





The 01 ~ 68 of DN-68A is connected to CON1 of PCI-2602 by a 68-pin cable.
The FG of DN-68A is connected to the shielding wire of this 68-pin cable.