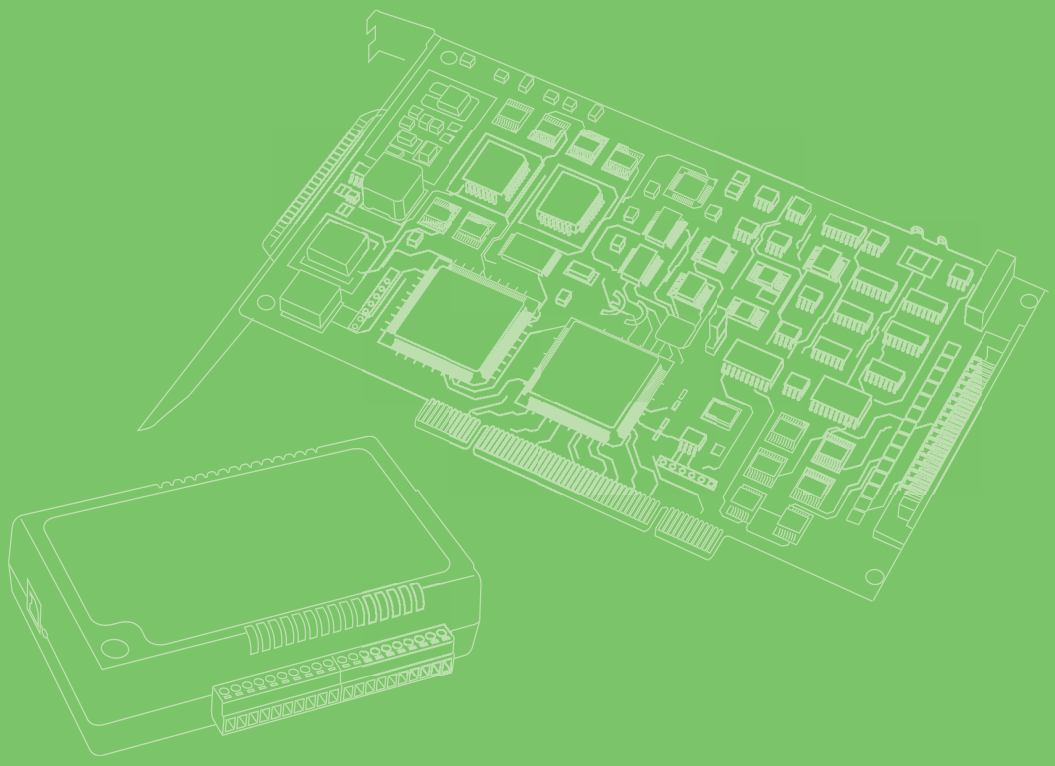

User Manual

PCIE-1810

12-bit Multifunction Card with PCI Express Bus

ADVANTECH

Enabling an Intelligent Planet

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Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

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CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

Technical Support and Assistance

1. Visit the Advantech web site at **http://support.advantech.com.tw/** where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, Contact your dealer immediately.

- PCIE-1810 DA&C card
- Startup or User Manual
- Companion DVD-ROM with DAQNavi drivers included

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

1. To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
2. Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

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Chapter 1

Introduction

This chapter introduces PCIE-1810 and and its typical applications.
Sections include:

- Features
- Applications
- Installation Guide
- Software Overview
- Roadmap
- Accessories

The PCIE-1810 is a PCI Express multifunction card for IBM X86 or compatible computers. It offers the five most desired measurement and control functions:

- 12-bit A/D conversion
- 12-bit D/A conversion
- Digital input
- Digital output
- Timer/counter.

A programmable-gain instrument amplifier lets you acquire different input signals without external signal conditioning. An onboard 4k word FIFO buffer provides high-speed data transfer and predictable performance under Windows. Automatic channel scanning circuitry and onboard SRAM let you perform multiple-channel A/D conversion and individual gains for each channel.

The following sections of this chapter will provide further information about features of the multifunction cards, a Quick Start for installation, together with some brief information on software and accessories for the PCIE-1810 cards.

1.1 Features

- 16 single-ended or 8 differential A/D inputs, programmable
- 12-bit A/D converter, up to 800 kHz sampling rate
- Instant software polling,1.25 μs high-speed response
- Double-Clock acquisition operation for analog input
- Start-, Delay to Start-, Delay to Stop-, Stop-event trigger capable
- Programmable gain for each input channel, automatic channel/gain scanning
- 4K onboard ring buffer for analog input and output
- Two independent 12-bit analog output channels with continuous waveform output function of maximum 500KHz throughput rate
- Auto-Calibration for analog input and output channels
- 24 digital Input and output channels, TTL compatible
- Two 32-bit independent full function counters
- BoardID switch

PCIE-1810 offers the following main features:

PCIe-Bus Plug & Play

The PCIE-1810 card uses a PCIe controller to interface the card to the PCI Express bus. The controller fully implements the PCI bus specification Rev 2.2. All configurations related to the bus, such as base address and interrupt assignment, are automatically controlled by software. No jumper or switch is required for user configuration.

Automatic Channel/Gain Scanning

The PCIE-1810 features an automatic channel/gain scanning circuit. This circuit, instead of your software, controls multiplexer switching during sampling. On-board SRAM stores different gain values for each channel. This combination lets user perform multi-channel high-speed sampling (up to 500 kHz) for each channel.

Onboard Ring Buffer Memory

There are 4k samples ring buffer for A/D and D/A on PCIE-1810. This is an important feature for faster data transfer and more predictable performance under Windows system.

Onboard Programmable Timer/Counter

The PCIE-1810 features two 32-bit timer/counters to provide one shot out-put, PWM output, periodic interrupt output, time-delay output, and the measurement of frequency and pulse width.

BoardID Switch

The PCIE-1810 has a built-in DIP switch that helps define each card's ID when multiple PCIE-1810 cards have been installed on the same PC chassis. The BoardID setting function is very useful when building a system with multiple PCIE-1810 cards. With the correct BoardID settings, you can easily identify and access each card during hardware configuration and software programming.

Note! *For detailed specifications and operation theory of the PCIE-1810, please refer to Appendix A and B.*

1.2 Applications

- Transducer and sensor measurements
- Waveform acquisition and analysis
- Process control and monitoring
- Vibration and transient analysis

1.3 Installation Guide

Before you install your PCIE-1810 card, please make sure you have the following necessary components:

- PCIE-1810 DA&C card
- PCIE-1810 User Manual
- Driver software Advantech DAQNavi software (included in the companion DVD-ROM)
- Personal computer or workstation with a PCI Express interface (running Windows 7/XP)
- Shielded Cable PCL-10168 or Shielded Cable with Noise Rejecting PCL-10168H (optional)
- Wiring Board ADAM-3968 (optional)

Other optional components are also available for enhanced operation:

- DAQ Navi, LabView or other 3rd-party software

After you get the necessary components and maybe some of the accesso-ries for enhanced operation of your multifunction card, you can then begin the installation procedure. Figure 1.1 on the next page provides a concise flow chart to give users a broad picture of the software and hard-ware installation procedures:

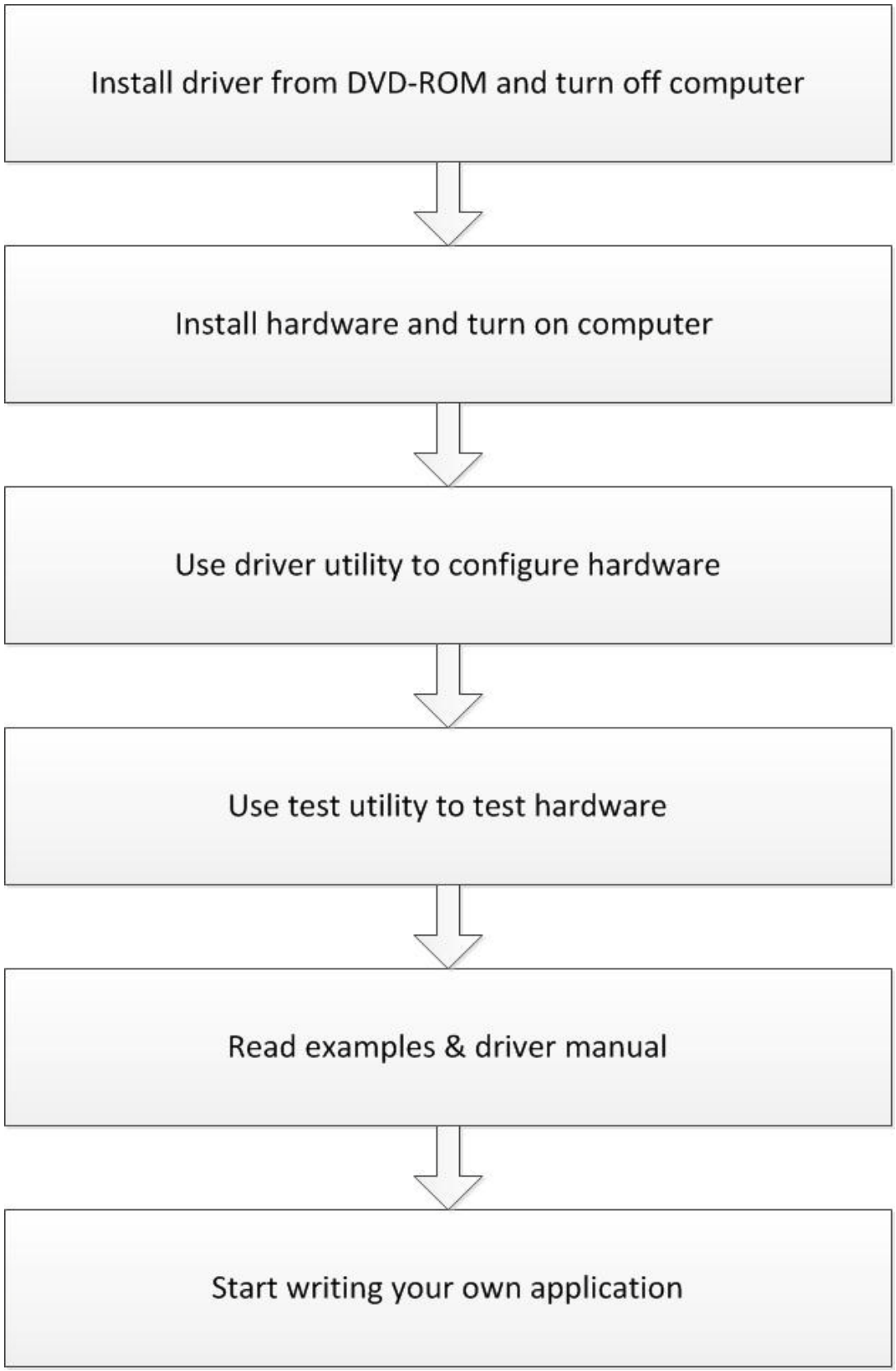


Figure 1.1 Installation Flow Chart

1.4 Software Overview

Advantech offers a rich set of DLL drivers, third-party driver support and application software to help fully exploit the functions of your PCIE-1810 card:

- Device Drivers (on the companion DVD-ROM)
- LabVIEW driver
- Advantech DAQ NAVi
- Datalogger

Programming choices for DA&C cards

You may use Advantech application software such as Advantech Device Drivers. On the other hand, advanced users can use register-level programming, although this is not recommended due to its laborious and time-consuming nature.

DAQNavi Software

Advantech DAQNavi software includes device drivers and SDK which features a complete I/O function library to help boost your application performance. This software is included in the companion DVD-ROM at no extra charge and comes with all Advantech DA&C cards. The Advantech DAQNavi software for Windows XP/Vista/7 works seamlessly with development tools such as Visual Studio .Net, Visual C++, Visual Basic and Borland Delphi.

1.5 DAQNavi Device Driver Programming Roadmap

This section will provide you a roadmap to demonstrate how to build an application from scratch using Advantech DAQNavi Device Driver with your favorite development tools such as Visual Studio .Net, Visual C++, Visual Basic, Delphi and C++ Builder. The step-by-step instructions on how to build your own applications using each development tool will be given in the Device Drivers Manual. Moreover, a rich set of example source code is also given for your reference.

Programming Tools

Programmers can develop application programs with their favorite development tools:

- Visual Studio.Net
- Visual C++ and Visual Basic
- Delphi
- C++ Builder

For instructions on how to begin programming works in each development tool, Advantech offers a Tutorial Chapter in the *DAQNavi SDK Manual* for your reference. Please refer to the corresponding sections in this chapter on the *DAQNavi SDK Manual* to begin your programming efforts. You can also look at the example source code provided for each programming tool, since they can get you very well oriented.

The *DAQNavi SDK Manual* can be found on the companion DVD-ROM. Alternatively, if you have already installed the Device Drivers on your system, The *DAQNavi SDK Manual* can be readily accessed through the Start button:

Start/Programs/Advantech Automation/DAQNavi/DAQNavi Manuals/DAQNavi SDK Manual

The example source code could be found under the corresponding installation folder such as the default installation path:

\Advantech\DAQNavi\Examples

For information about using other function groups or other development tools, please refer to the Using DAQNavi SDK chapter in the DAQNavi SDK Manual, or the video tutorials in the Advantech Navigator.

Programming with DAQNavi Device Drivers Function Library

Advantech DAQNavi Device Drivers offer a rich function library that can be utilized in various application programs. This function library consists of numerous APIs that support many development tools, such as Visual Studio .Net, Visual C++, Visual Basic, Delphi and C++ Builder.

According to their specific functions or services, APIs can be categorized into several function groups:

- Analog Input Function Group
- Analog Output Function Group
- Digital Input/Output Function Group
- Counter Function Group
- Port Function Group (direct I/O)
- Event Function Group

For the usage and parameters of each function, please refer to the *Using DAQNavi SDK* chapter in the *DAQNavi SDK Manual*.

Troubleshooting DAQNavi Device Drivers Error

Driver functions will return a status code when they are called to perform a certain task for the application. When a function returns a code that is not zero, it means the function has failed to perform its designated function. To troubleshoot the Device Drivers error, you can pass the error, you can check the error code and error description within the Error Control of each function in the DAQNavi SDK Manual.

1.6 Accessories

Advantech offers a complete set of accessory products to support the PCIE-1810 card. These accessories include:

Wiring Cables

- **PCL-10168-1E** 68-pin SCSI Shielded Cable, 1 m
- **PCL-10168-2E** 68-pin SCSI Shielded Cable, 2 m
- **PCL-10168H-1E** 68-pin SCSI Shielded Cable with Noise Rejecting, 1 m
- **PCL-10168H-2E** 68-pin SCSI Shielded Cable with Noise Rejecting, 2 m

Wiring Boards

- ADAM-3968 68-pin DIN-rail SCSI Wiring Board

Chapter 2

Installation

This chapter provides a packaged item checklist, proper instructions for unpacking and step-by-step procedures for both driver and card installation.
Sections include:

- Unpacking
- Driver Installation
- Hardware Installation
- Device Setup & Configuration

2.1 Unpacking

After receiving your PCIE-1810 package, inspect the contents first. The package should include the following items:

- PCIE-1810 card
- Companion DVD-ROM (Device Drivers included)
- Startup Manual

The PCIE-1810 card harbor certain electronic components vulnerable to electrostatic discharge (ESD). ESD can easily damage the integrated circuits and certain components if preventive measures are ignored.

Before removing the card from the antistatic plastic bag, you should take following precautions to ward off possible ESD damage:

- Touch the metal part of your computer chassis with your hand to discharge the static electricity accumulated on your body. Alternatively, one can also use a grounding strap.
- Touch the anti-static bag to a metal part of your computer chassis before opening the bag.
- Take hold of the card only by the metal bracket when removing it out of the bag.

After taking out the card, you should first:

- Inspect the card for any possible signs of external damage (loose or damaged components, etc.). If the card is visibly damaged, please notify our service department or our local sales representative immediately. Do not install a damaged card into your system.

Also pay extra attention to the followings to ensure a proper installation:

- Avoid physical contact with materials that could hold static electricity such as plastic, vinyl and Styrofoam.
- Whenever you handle the card, grasp it only by its edges. DO NOT TOUCH the exposed metal pins of the connector or the electronic components.

Note! *Keep the anti-static bag for future use. You might need the original bag to store the card if you have to remove the card from a PC or transport it elsewhere.*

2.2 Driver Installation

We recommend you to install the driver before you install the PCIE-1810 card into your system, since this will guarantee a smooth installation process.

The Advantech DAQNavi Device Drivers Setup program for the PCIE-1810 card is included in the companion DVD-ROM that is shipped with your DA&C card package. Please follow the steps below to install the driver software:

1. Insert the companion DVD-ROM into your DVD-ROM drive.
2. The Setup program will be launched automatically if you have the autoplay function enabled on your system. When the Setup Program is launched, you will see the following Setup Screen.

Note! *If the autoplay function is not enabled on your computer, use Windows Explorer or Windows Run command to execute autorun.exe on the companion DVD-ROM.*

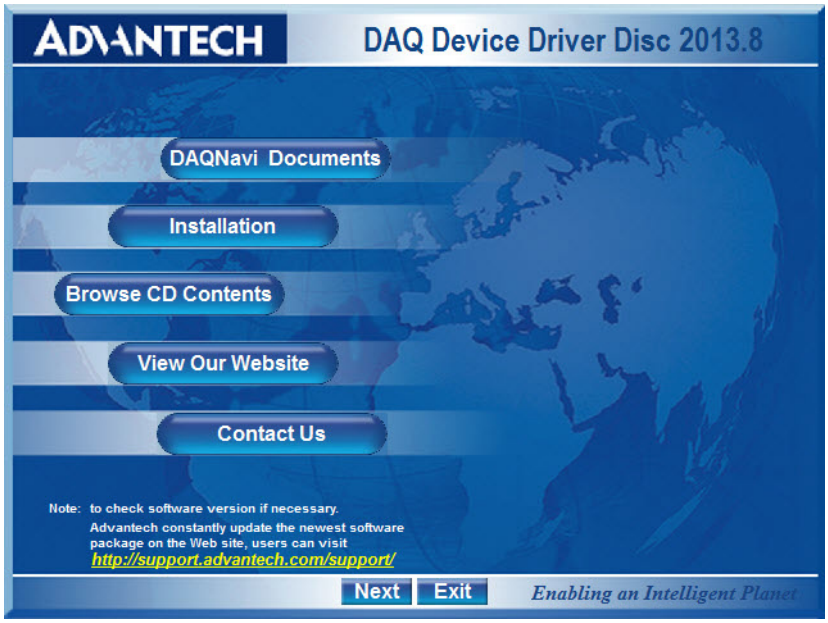


Figure 2.1 Setup Screen of Advantech Automation Software

3. Select the Installation option.
4. Select the Legacy SDK and Drivers option to install.
5. Select the Individual Drivers option.
6. Select the PCIE series and the specific device then follow the installation instructions step by step to complete your device driver installation and setup.
7. Back and select the Windows SDK and Drivers install the Advantech Navigator.

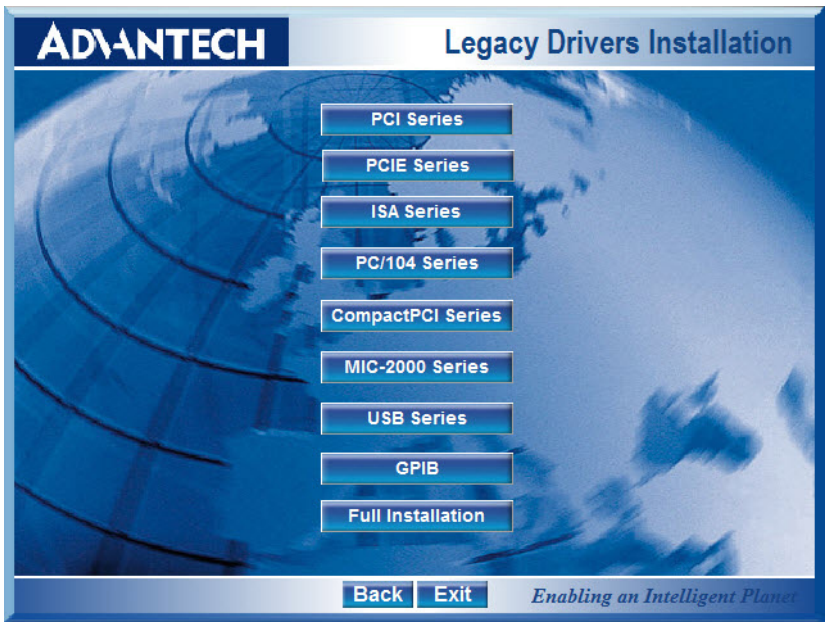


Figure 2.2 Different Options for Driver Setup

For further information on driver-related issues, an online version of the *DAQNavi SDK Manual* is available by accessing the following path:

Start/Programs/Advantech Automation/DAQNavi/DAQNavi Manuals/DAQNavi SDK Manual

2.3 Hardware Installation

Note! *Make sure you have installed the driver first before you install the card (refer to 2.2 Driver Installation)*

After the Device Drivers installation is completed you can install the PCIE-1810 card on your computer. However, it is suggested that you refer to the computer's user manual or related documentation if you have any doubts. Please follow the steps below to install the card onto your system.

1. Turn off your computer and unplug the power cord and cables. TURN OFF your computer before installing or removing any components on the computer.
2. Remove the cover of your computer.
3. Remove the slot cover on the back panel of your computer.
4. Touch the metal part on the surface of your computer to neutralize the static electricity that might be on your body.
5. Insert the PCIE-1810 card into the PCI Express interface. Hold the card only by its edges and carefully align it with the slot. Insert the card firmly into place. Use of excessive force must be avoided; otherwise, the card might be damaged.
6. Connect appropriate accessories (68-pin SCSI Shielded Cable, wiring terminals, etc. if necessary) to the card.
7. Replace the cover of your computer chassis. Re-connect the cables you removed in step 2.
8. Plug in the power cord and turn on the computer.

After your card is properly installed on your system, you can now configure your device using the *Advantech Navigator* Program that has itself already been installed

on your system during driver setup. A complete device installation procedure should include device setup, configuration and testing. The following sections will guide you through the Setup, Configuration and Testing of your device.

2.4 Device Setup & Configuration

The *Advantech Navigator* program is a utility that allows you to set up, configure and test your device, and later stores your settings on the system registry. These settings will be used when you call the APIs of Advantech Device Drivers.

Setting Up the Device

1. To install the I/O device for your card, you must first run the *Advantech Navigator* program (by accessing *Start/Programs/Advantech Automation/DAQNavi/Advantech Navigator*).
2. You can then view the device(s) already installed on your system (if any) on the Installed Devices list box. If the software and hardware installation are completed, you will see PCIE-1810 card in the Installed Devices list.

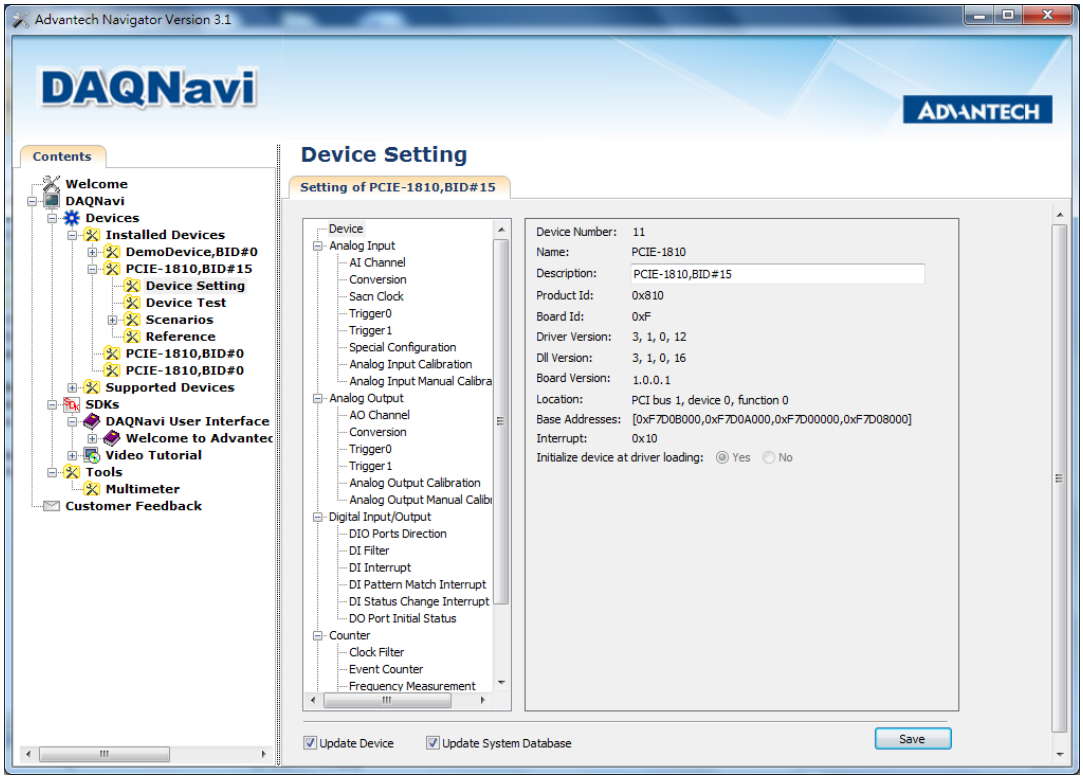


Figure 2.3 The Device Setting of PCIE-1810

Configuring the Device

3. Please go to the Device Setting to configure your device. Here you can configure not only the Analog Input/Output of PCIE-1810 but also Digital Input/Output.

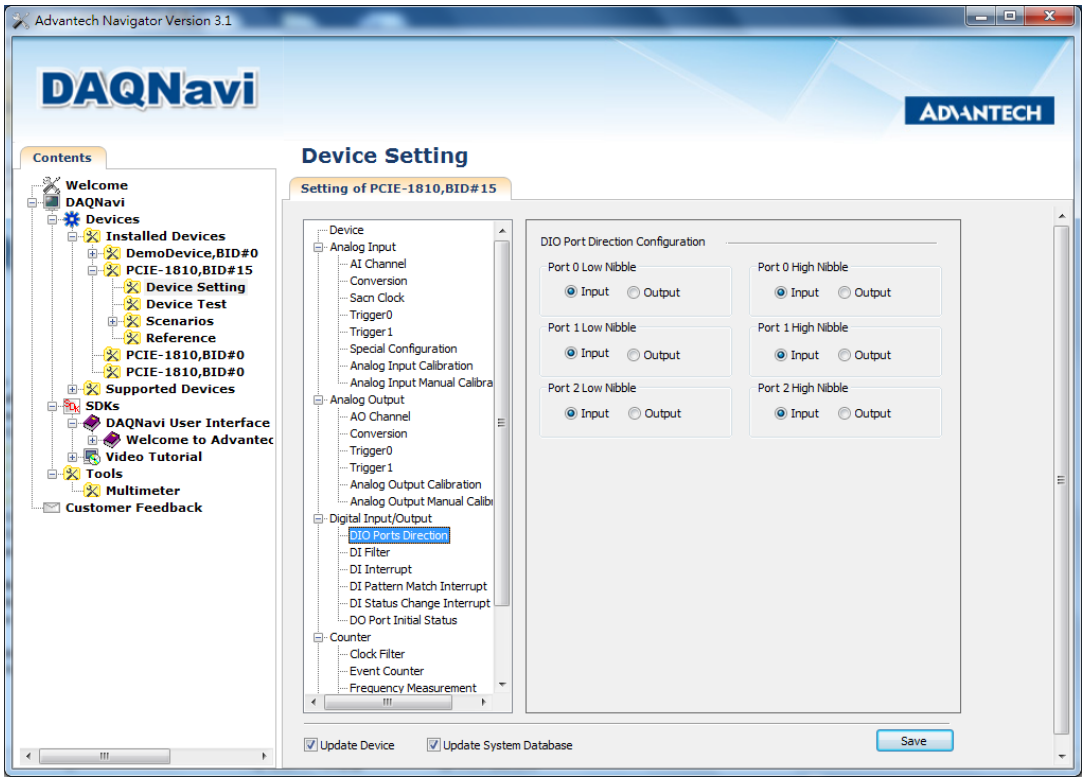


Figure 2.4 The Device Setting page

4. After your card is properly installed and configured, you can go to the *Device Test* page to test your hardware by using the testing utility supplied.

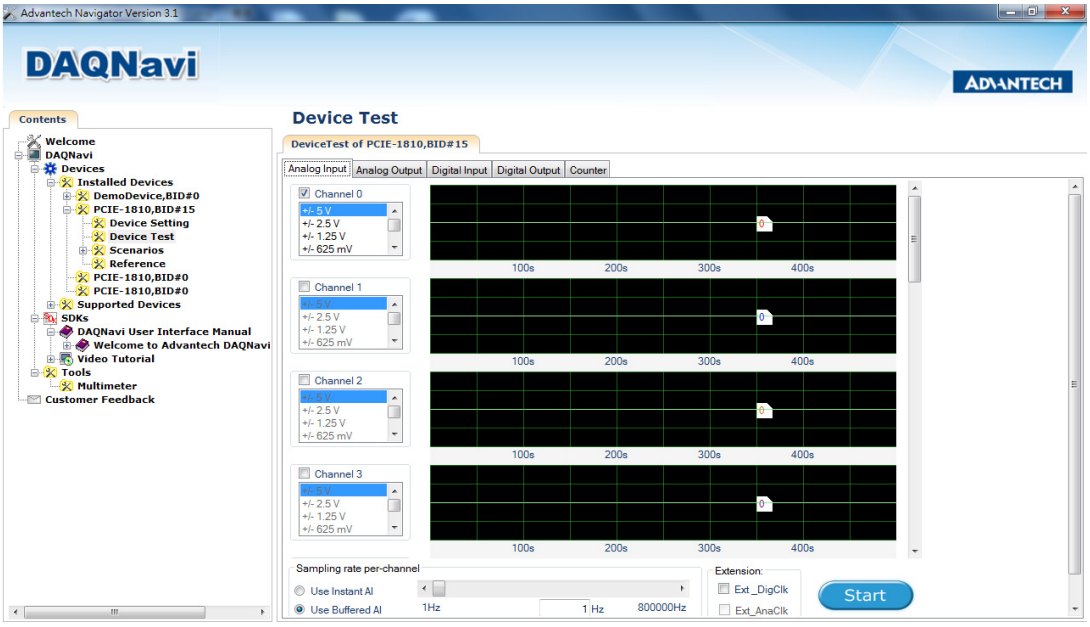


Figure 2.5 The Device Testing of PCIE-1810

For more detailed information, please refer to the DAQNavi SDK Manual or the User Interface Manual in the Advantech Navigator.

Chapter 3

Signal Connections

This chapter provides useful informa-tion about how to con-nect input and output signals to the PCIE-1810 card via the I/O connector.

Sections include:

- Overview
- BoardID Settings
- Signal Connections
- Field Wiring Considerations

3.1 Overview

Maintaining signal connections is one of the most important factors in ensuring that your application system is sending and receiving data correctly. A good signal connection can avoid unnecessary and costly damage to your PC and other hardware devices. This chapter provides useful information about how to connect input and output signals to the PCIE-1810 card via the I/O connector.

3.2 Switch and Jumper Settings

Please refer to Figure 3.1 for jumper and switch locations on PCIE-1810.

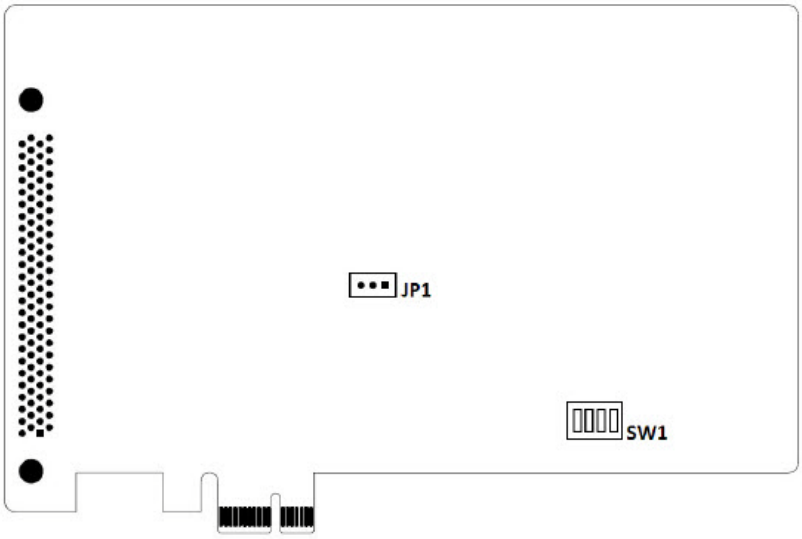


Figure 3.1 Connector and Switch Locations

3.2.1 Board ID (SW1)

The PCIE-1810 has a built-in DIP switch (SW1), which is used to define each card's board ID. When there are multiple cards on the same chassis, this board ID switch is useful for identifying each card's device number.

After setting each PCIE-1810, you can identify each card in system with different device numbers. The default value of board ID is 0 and if you need to adjust it to other value, please set the SW1 by referring to Table 3.1.

Table 3.1: Board ID Setting (SW1)

SW1	Position 1	Position 2	Position 3	Position 4
BoardID	**ID3**	**ID2**	**ID1**	**ID0**
0	ON	ON	ON	ON
1	ON	ON	ON	OFF
2	ON	ON	OFF	ON
3	ON	ON	OFF	OFF
4	ON	OFF	ON	OFF
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	ON
7	ON	OFF	OFF	OFF
8	OFF	ON	ON	ON
9	OFF	ON	ON	OFF
10	OFF	ON	OFF	ON
11	OFF	ON	OFF	OFF
12	OFF	OFF	ON	ON
13	OFF	OFF	ON	OFF
14	OFF	OFF	OFF	ON
15	OFF	OFF	OFF	OFF

Default Setting is 0

3.2.2 Power On Configuration(JP1)

Default configuration after power on, and hardware reset is to set all the analog input and analog output channels to open status (the current of the load can't be sink) so that the external devices will not be damaged when the system starts or resets. When the system is hot reset, then the status of isolated digital output channels are selected by jumper JP1. Table 3.2 shows the configuration of jumper JP1.

Table 3.2: Power on Configuration after Hot Reset (JP1)

JP1	Power on configuration after hot reset
1	Keep last status after hot reset
1	Default configuration (Default setting)

3.3 Signal Connections

Pin Assignments

The I/O connector on the PCIE-1810 is a 68-pin connector that enable you to connect to accessories with the PCL-10168-1 or PCL-10168-2 shielded cable.

Figure 3.2 shows the pin assignments for the 68-pin I/O connector on the PCIE-1810, and Table 3.3 shows its I/O connector signal description.

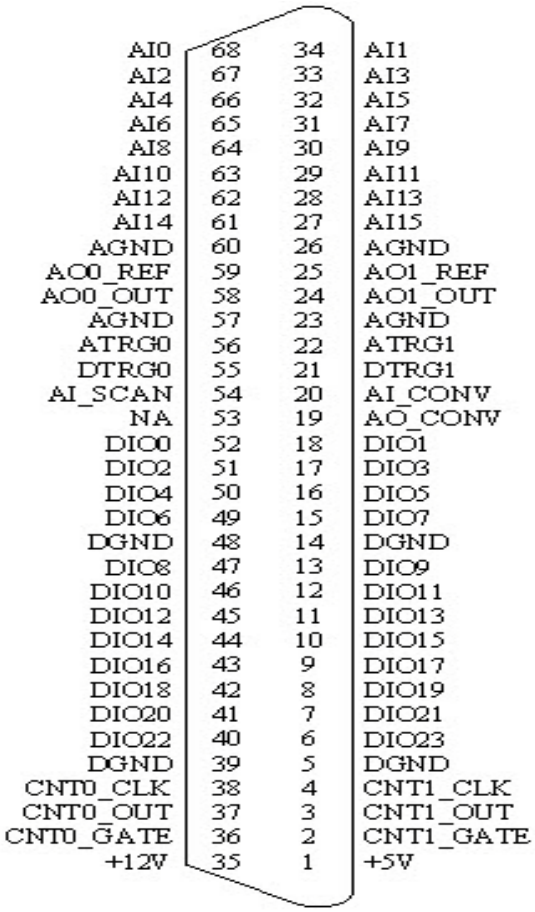


Figure 3.2 68-pin I/O Connector Pin Assignments

3.3.1 I/O Connector Signal Description

Table 3.3: I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Pin description
AI[15:0]	AGND	Input	**AI Channels 0 to 15.** Each channel pair, AI[i+1:i](i=0,2,4…14), can be configured as either two single-ended inputs or one differential input.
AGND	-	-	**Analog Ground.** These pins are the reference points for single-ended measurements and the bias current return point for differential measurement. The ground reference (AGND and DGND) are connected together on the PCIE-1810.
ATRG0 ATRG1	AGND	Input	**Analog Threshold Trigger.** These pins are the analog input threshold trigger input. **Digital Trigger.** These pins are the digital input. The left pins are used to start or stop a data acquisition. **Analog Threshold Trigger** and **Digital Trigger** are used to execute a specific data acquisition mode – an acquisition which consists of one or more scans. And then a data acquisition behavior needs a stop trigger signal while the pin is used to stop function. The active edge of the start and stop function could be programmed to be rising or falling.
DTRG0 DTRG1	DGND	Input	
AI_SCAN	DGND	Input	**AI Scan Clock.** This pin is used to initiate a set of data acquisition. The card samples the AI signals of every channel in the scan list once for every AI Scan Clock.
AI_CONV	DGND	Input	**AI Conversion Clock.** This pin is to initiate a single AI conversion on a single channel. A Scan (controlled by the AI Scan Clock) consists of one or more conversions.
AO0_REF AO1_REF	AGND	Input	**AO Channel 0/1 External Reference.** This is the external reference input for the analog output channel 0/1.
AO0_OUT AO1_OUT	AGND	Output	**AO Channels 0/1.** This pin supplies the voltage output of analog output channel 0/1.
AO_CONV	DGND	Input	**AO Convert Clock.** This pin is to initiate AO conversion. Each sample updates the output of all of the DACs. You can specify an internal or external source for AO Convert Clock.
DIO[23:0]	DGND	Input/ Output	**Digital Input/ Output Channel [23:0].** These pins are digital input/output which could be configured as general purpose digital inputs or outputs.
DGND	-	-	**Digital Ground.** This pin supplies the reference for the digital channels at the I/O connector as well as the +5V and +12V DC supply. The ground references (AGND and DGND) are connected together on the PCIE-1810.
CNT0.CLK CNT1.CLK	DGND	Input	**Counter 0/1 External Clock Input.** The clock input of counters can be either external (up to 10MHz) or internal (20MHz), as set by software.

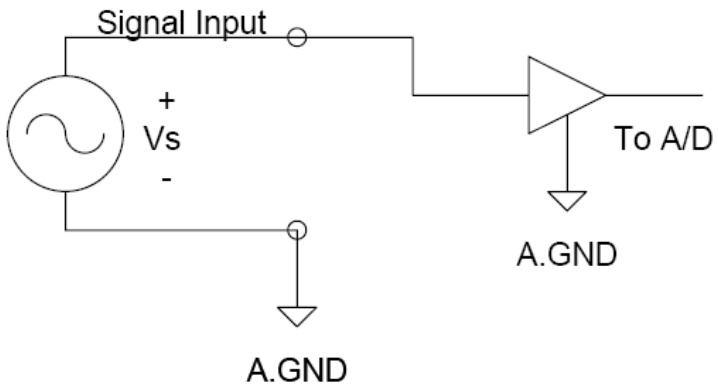
Table 3.3: I/O Connector Signal Descriptions			
CNT0.OUT CNT1.OUT	DGND	Output	Counter 0/1 Output.
CNT0.GATE CNT1.GATE	DGND	Input	Counter 0/1 Gate Control.
+12V	DGND	Output	**+12V DC Source.** This pin is +12V DC power supply for external use. (0.1A maximum)
+5V	DGND	Output	**+5V DC Source.** This pin is +5V DC power supply for external use. (0.3A maximum)

3.3.2 Analog Input Connections

PCIE-1810 supports either 16 single-ended or 8 differential analog inputs.

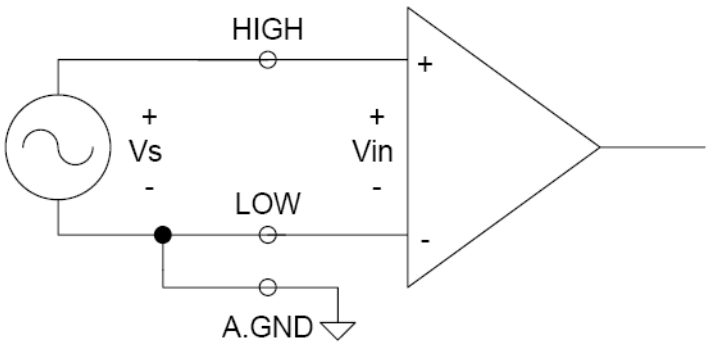
Single-ended Channel Connections

Single-ended connections use only one signal wire per channel. The voltage on the line references to the common ground on the card. A signal source without a local ground is called a “floating” source. It is fairly simple to connect a single ended channel to a floating signal source. A standard wiring diagram looks like this:



Differential Channel Connections

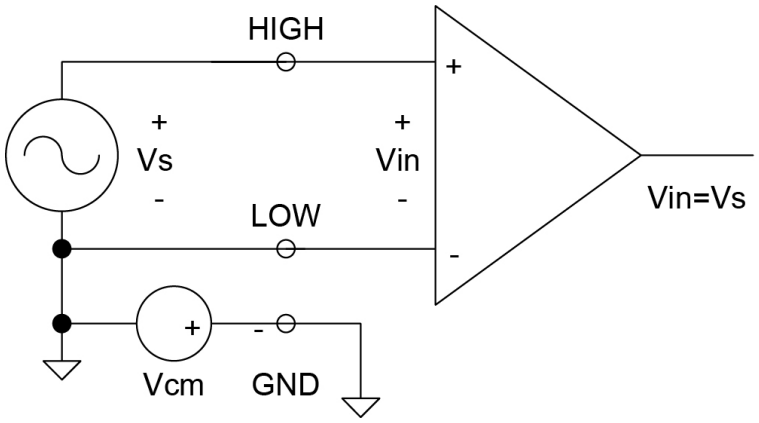
Differential input connections use two signal wires per channel. The card measures only the voltage difference between these two wires, the HIGH wire and the LOW wire. If the signal source has no connection to ground, it is called a "floating" source. A connection must exist between LOW and ground to define a common reference point for floating signal sources. To measure a floating sources connect the input channels as shown below:



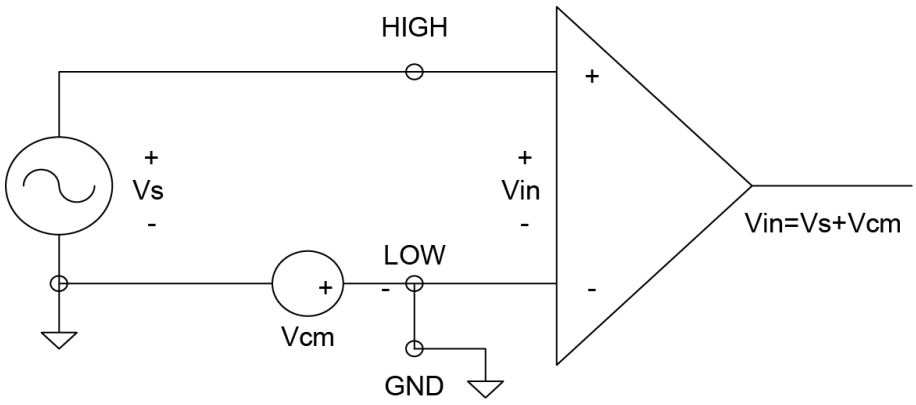
If the signal source has one side connected to a local ground, the signal source ground and the PCIE-1810 ground will not be at exactly the same voltage, as they are connected through the ground return of the equipment and building wiring. The difference between the ground voltages forms a common-mode voltage.

To avoid the ground loop noise effect caused by common-mode voltages, connect the signal ground to the LOW input. Do not connect the LOW input to the PCIE-1810 ground directly. In some cases you may also need a wire connection between the PCIE-1810 ground and the signal source ground for better grounding. The following two diagrams show correct and incorrect connections for a differential input with local ground:

Correct Connection



Incorrect Connection



Analog Output Connection

The PCIE-1810 provides two D/A output channels. You can use the internal precision -5 V or -10 V reference to generate 0 to +5 V or 0 to +10 V D/A output. Use an external reference for other D/A output ranges. The maximum reference input voltage is ±10 V and maximum output scaling is ±10 V. Loading current for D/A outputs should not exceed 5 mA.

Fig. 3-3 shows how to make analog output and external reference input connections on the PCIE-1810.

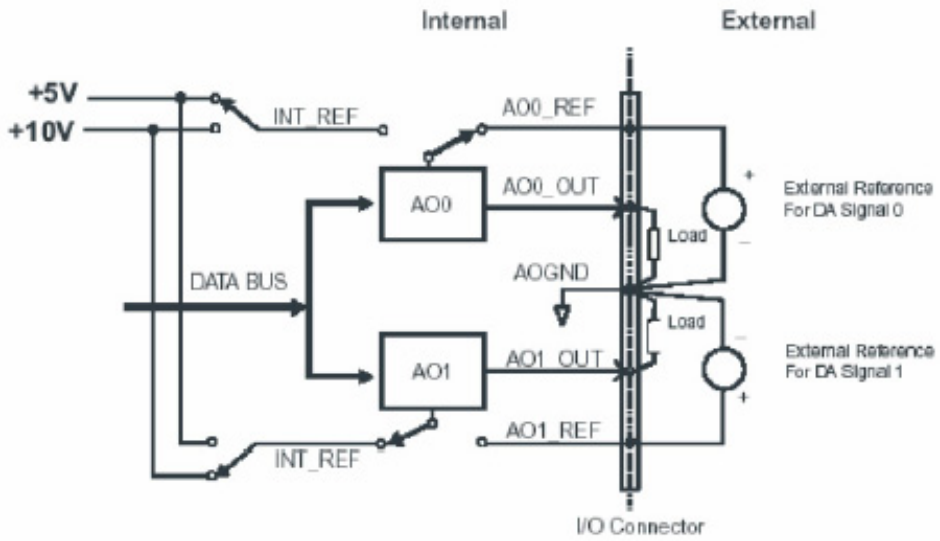
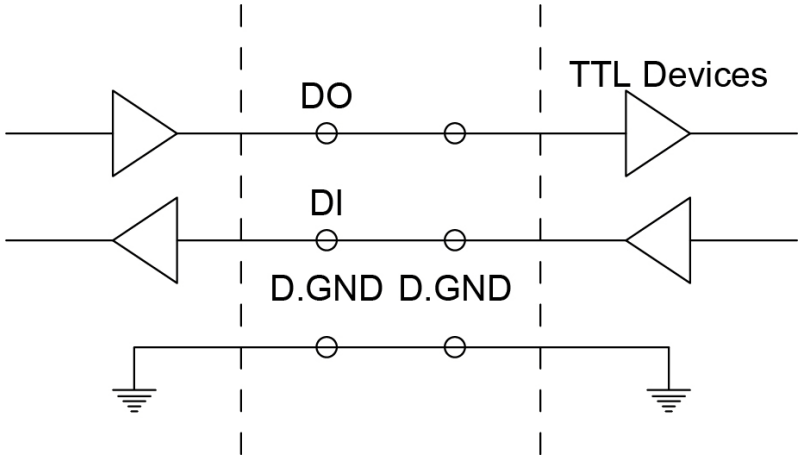


Figure 3.3 Analog Output Connections

3.3.3 Digital Signal Connections

The PCIE-1810 has 24 digital input/output channels and they can be con-figured as input or output channels. The digital I/O levels are TTL compatible. The following figure shows connections to exchange digital signals with other TTL devices:



3.4 Field Wiring Considerations

When you use PCIE-1810 cards to acquire data from outside, noises in the environment might significantly affect the accuracy of your measurements if due cautions are not taken. The following measures will be helpful to reduce possible interference running signal wires between signal sources and the PCIE-1810 card.

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- The signal cables must be kept away from strong electromagnetic sources such as power lines, large electric motors, circuit breakers or welding machines, since they may cause strong electromagnetic interference. Keep the analog signal cables away from any video monitor, since it can significantly affect a data acquisition system.
- If the cable travels through an area with significant electromagnetic interference, you should adopt individually shielded, twisted-pair wires as the analog input cable. This type of cable has its signal wires twisted together and shielded with a metal mesh. The metal mesh should only be connected to one point at the signal source ground.
- Avoid running the signal cables through any conduit that might have power lines in it.
- If you have to place your signal cable parallel to a power line that has a high voltage or high current running through it, try to keep a safe distance between them. Alternatively, you can place the signal cable at a right angle to the power line to minimize the undesirable effect.
- The signals transmitted on the cable will be directly affected by the quality of the cable. In order to ensure better signal quality, we recommend that you use the PCL-10168 shielded cable.

Appendix A

Specifications

A.1 Analog Input

Channels		16 single-ended / 8 differential				
Resolution		12-bit				
Built-in memory		4K samples				
Sampling Rate		Single-channel	800 KS/s			
		Multi-channel	500 KS/s			
Input Range and Gain List		Gain	0.5	1	2	4	8
		Unipolar	NA	0~10	0~5	0~2.5	0~1.25
		Bipolar	±10	±5	±2.5	±1.25	±0.625
Drift		Gain	0.5	1	2	4	8
		Zero	25 ppm/°C				
		Span	15 ppm/°C				
Input Signal Band Width (-3dB)		Gain	0.5	1	2	4	8
		BW (MHz)	1	1.6	1.2	1.2	1.2
Max. Input Voltage		± 15 V					
Input Impedance		1G Ω / 2pF					
Clock Source		Software or external					
Trigger Mode		Start trigger, Delay to Start trigger, Stop trigger, Delay to Stop trigger					
Accuracy	DC	INLE: ± 1 LSB (Under manual adjustment)					
		DNLE: ± 1 LSB (Under manual adjustment)					
		Offset error: Adjustable to zero					
		Gain	0.5	1	2	4	8
		Gain Error (%FSR)	0.1	0.1	0.2	0.2	0.4
		Channel Type	Single-Ended / Differential				
	AC	SNR: 68 dB					
		ENOB : 10.5 bits					
External Digital Trigger		Low: 0.8V max. ; High: 2.0V min.					
		Min. pulse width : 50 ns					
External Analog Trigger		Range: -10V ~ +10V					
		Resolution: 12-bit (4.88mV/step)					

A.2 Analog Output

Channels	2	
Resolution	12-bit	
FIFO Size	4k samples	
Output Rate	500 kS/s	
Output Range	Using Internal Reference	0~5, 0~10, ±5, ±10 V
	Using External Reference	0 ~ +x V @ +x V (-10 ≤x ≤10) -x ~ +x V @ +x V (-10 ≤x ≤ 10)
Slew Rate	20 V/μs	
Accuracy	Relative	±1 LSB
	Differential Non-linearity	±1 LSB (monotonic)
Gain Error	Adjustable to zero	
Drift	30 ppm / °C	
Driving Capability	5 mA	
Update Rate	Static update, waveform	
Output Impedance	0.1 ohm max.	

A.3 Digital Input/Output

Channels	24 (shared), TTL compatible	
Input Voltage	Low	0.8V max.
	High	2.0 V min.
Output Voltage	Low	0.8 V max.@ +15 mA (sink)
	High	2.0 V min.@ -15 mA (source)

A.4 Counter/Timer

Channels	2 channels (independent)	
Resolution	32-bit	
Compatibility	TTL level	
Clock Source	Internal 20MHz or external clock (10 MHz max.). Selected by software	
Output Frequency	Max. 10MHz	
Clock Input	Low	0.8 V max.
	High	2.0 V min.
Gate Input	Low	0.8 V max.
	High	2.0 V min.
Counter Output	Low	0.8 V max. @+15mA
	High	2.0 V min. @-15mA
Error in Advanced Functions	Frequency Measurement	0.1% when input signal frequency ≥ 40KHz
	Pulse Width Measurement	0.1% when input signal frequency ≥ 40KHz
	Pulse Output	within 2% when output frequency > 1MHz
	PWM Output	within 2% when output frequency > 1MHz

Note! *When performing advanced functions, like frequency measurement and pulse output, there will be errors. And the error will vary depending on the parameter selections and the OS performance.*

A.5 General

I/O Connector Type	68-pin SCSI female	
Dimensions	167 x 100 mm	
Power Consumption	**Typical**	3.3 V @ 488 mA, 12 V @ 112 mA
	Max.	3.3 V @ 2.25 A, 12 V @ 390 mA
Temperature	**Operating**	0~60°C (32~140°F) (refer to IEC 68-2-1,2)
	Storage	-40 ~ 70°C (-40 ~ 158°F)
Relative Humidity	**Operating**	5~85%RH non-condensing (refer to IEC 68-1,-2,-3)
	Storage	5~95%RH non-condensing (refer to IEC 68-1,-2,-3)
Certifications	CE/FCC certified	

Appendix B

Operation Theory

B.1 Analog Input Operation

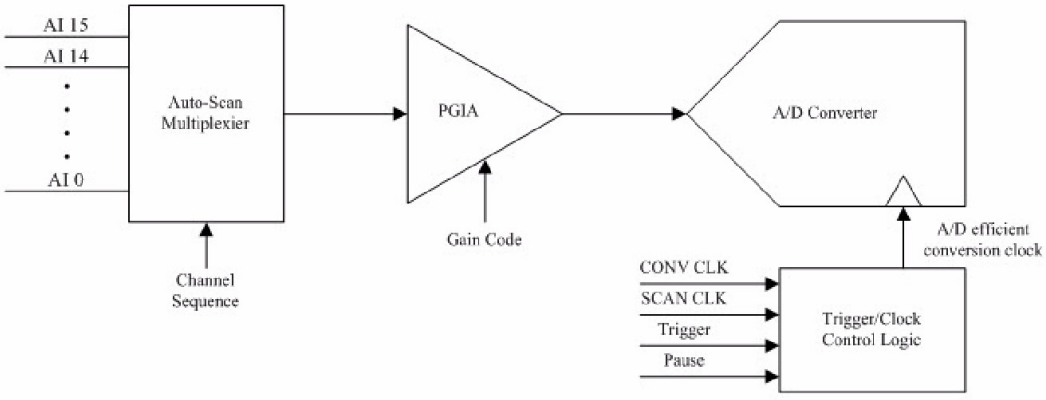
This section describes the following features of analog input operation theory that can help you realize how to configure the functions and parameters to match various applications.

- A/D Hardware Structure
- Analog input ranges and gains
- Analog data acquisition mechanism
- Analog input acquisition modes
- A/D SCAN/CONV clock source
- A/D trigger sources
- Analog input data format

B.1.1 A/D Hardware Structure

The A/D conversion hardware structure includes four major parts:

- **Auto-scan multiplexer** routes the analog input signals into A/D converter channel by channel in a software-defined sequence.
- **PGIA** (Programmable Gain Instrument Amplifier) rectifies the input range and amplify/alleviate input signal to match the input range of A/ D converter.
- **A/D converter** conceives the rectified voltage from PGIA and transfers it into the corresponding digital data format.
- **Trigger/Clock control logic** enables/disables the whole process and determines acquisition timing interval.



A/D Conversion Hardware Structure

B.1.2 Analog Input Ranges and Gains

The PCIE-1810 can measure both unipolar and bipolar analog input signals. A unipolar signal can range from 0 to 10 V FSR (Full Scale Range), while a bipolar signal extends within ±10 V FSR. The PCIE-1810 provides various programmable gain levels and each channel is allowed to set its own input range individually. Table B.1 lists the effective ranges supported by the PCIE-1810 with gains.

Table B.1: Gains and Analog Input Range

Gain	Unipolar Analog Input Range	Bipolar Analog Input Range
0.5	N/A	±10 V
1	0 ~ 10 V	±5 V
2	0 ~ 5 V	±2.5 V
4	0 ~ 2.5 V	±1.25 V
8	0 ~ 1.25 V	±0.625 V

For each channel, choose the gain level providing the most optimal range that can accommodate the signal range you want to measure.

B.1.3 Analog Input Acquisition Mode

The PCIE-1810 can acquire data in either single value or pacer mode.

■ Single Value Acquisition (Polling) Mode

The single value acquisition mode is the simplest way to acquire data. User can simply poll the data register of the desired channel to get the latest acquired value. Each analog input channel has its own dedicated data register (buffer) and in this mode the PCIE-1810 updates each channel cyclically. The update rate is sampling rate/num. of active channels.

■ Buffer Mode

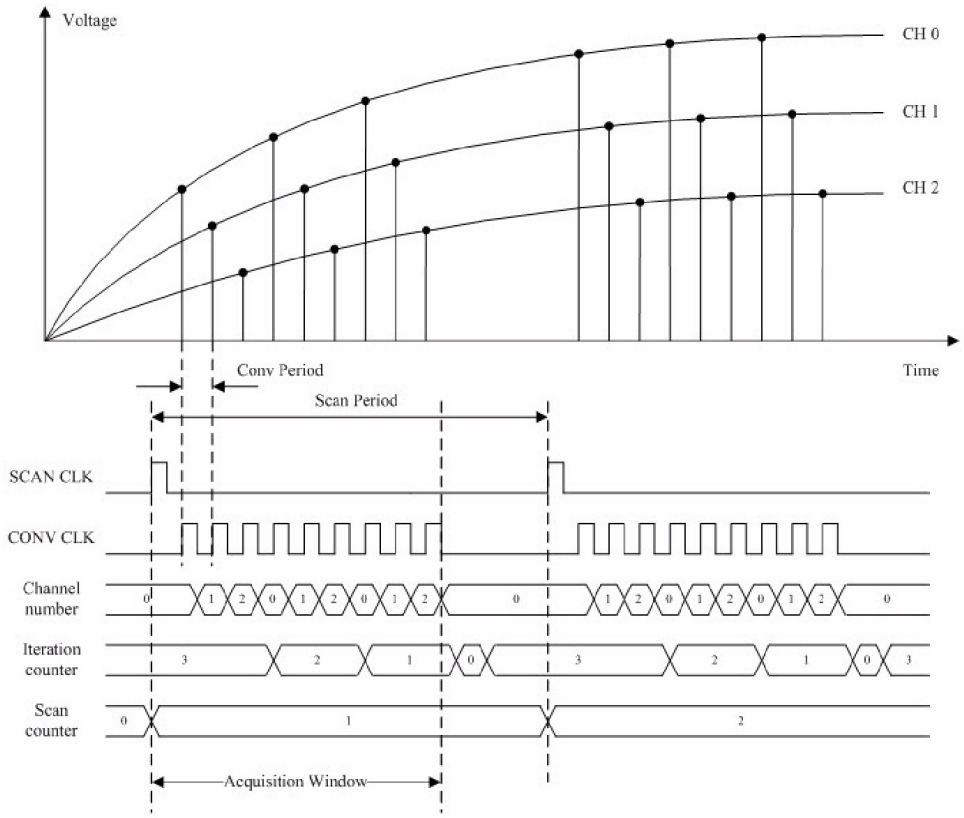
Adopt buffer mode to acquire data if you wanna accurately control the time interval between conversions. A/D conversion clocks come from internal clock sources or external signals on connector. A/D conversion starts when the clocks signal come in, and will not stop if the clocks are continuously sent. Conversion data is accumulated into the on-board A/D buffer and waiting the transfer to PC memory. Further, you can specify Trigger to acquire the desired periods. We will discuss the detail in the next sections.

■ A/D Data Acquisition Clock Timing

The PCIE-1810 introduces a double-clock system, with SCAN clock and CONV clock, to generate efficient A/D conversion clocks at dedicated timing. You can control acquisition timing interval precisely and just acquire the desired period. It can save the waste of PCI bandwidth with continuing acquisition and post data processing by filtering-out the redundant data beforehand. In this section, we will describe how it works and its timing reference in detail.

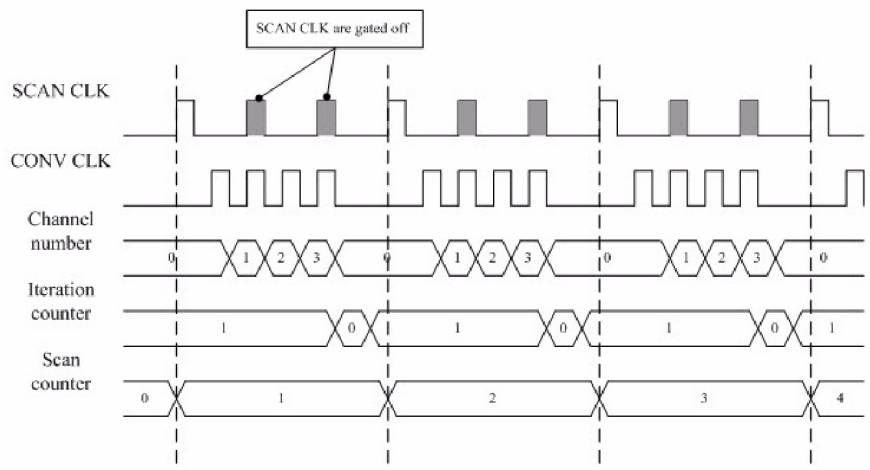
Double-Clock Procedure

Double clock procedure is the fundamental A/D conversion mechanism of the PCIE-1810, regardless of which mode selected. The incoming SCAN CLK launches an acquisition period called Acquisition Window. The arriving CONV CLKs within the Acquisition Window will become an efficient A/D conversion clock to trigger A/D converter. The number of efficient CONV CLK depends on the number of active scanning (multiplex) channels and software-programed iteration counters. One scanning iteration is defined as the time auto-scan multiplexer routes input channels from Start channel to Stop channel once. On the other words, all the active channels are sampled once in a single iteration. After the iteration counter counts down to zero, the Acquisition Window will be disable automatically and wait for the next incoming SCAN CLK. The end of Acquisition Window resets the iteration counter to its user-specified value. Users can specify the iteration counter by software and read back the number of incoming SCAN CLKs from SCAN CLK counter.

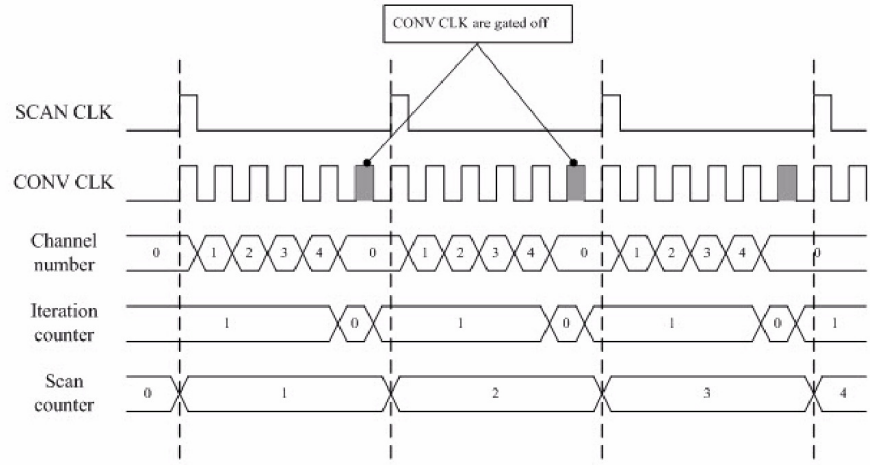


Double Clock timing Diagram

Once the acquisition procedure inside Acquisition Windows is set, the incoming CLKs must fit in the user-specified acquisition sequence, or the CLKs may be gated off. Refer to the following figures for more details.

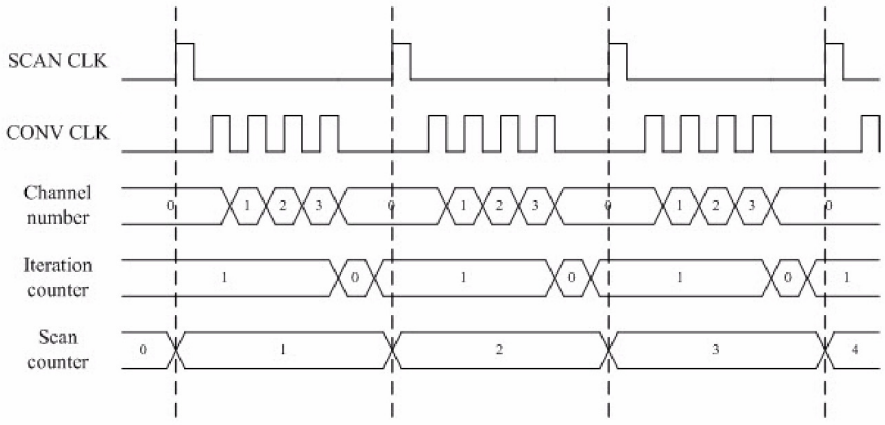


SCAN CLK is too fast

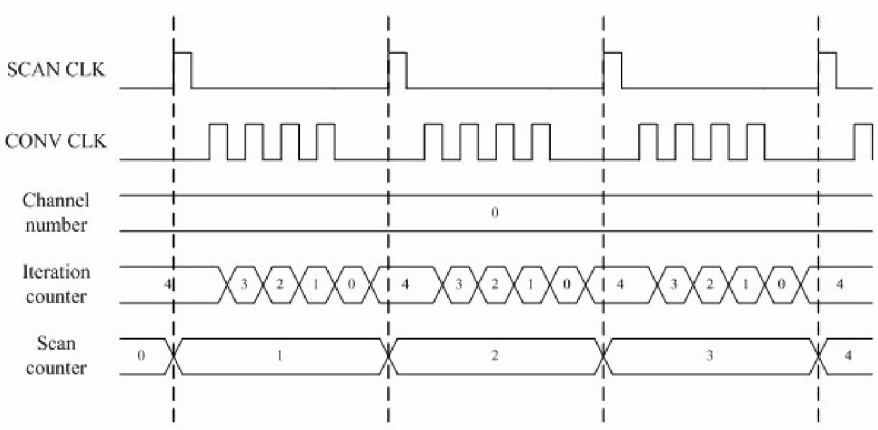


CONV CLK is too fast

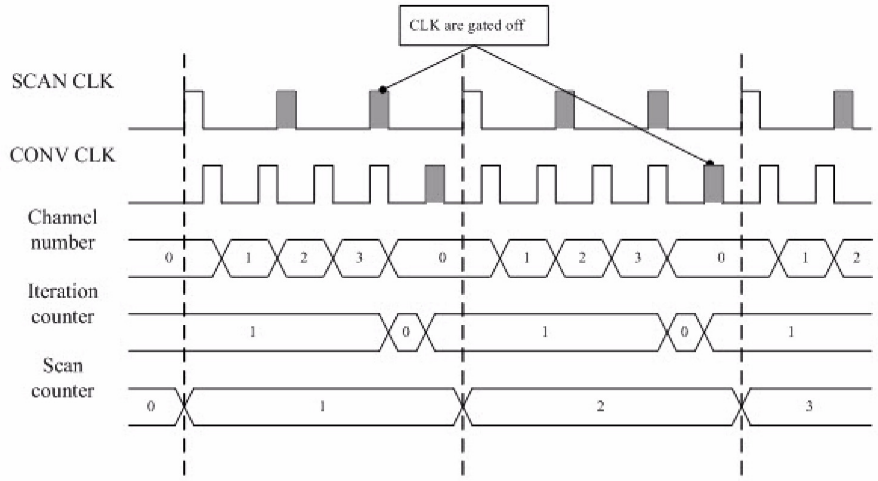
Other scanning procedure applications timing diagram.



Single Iteration



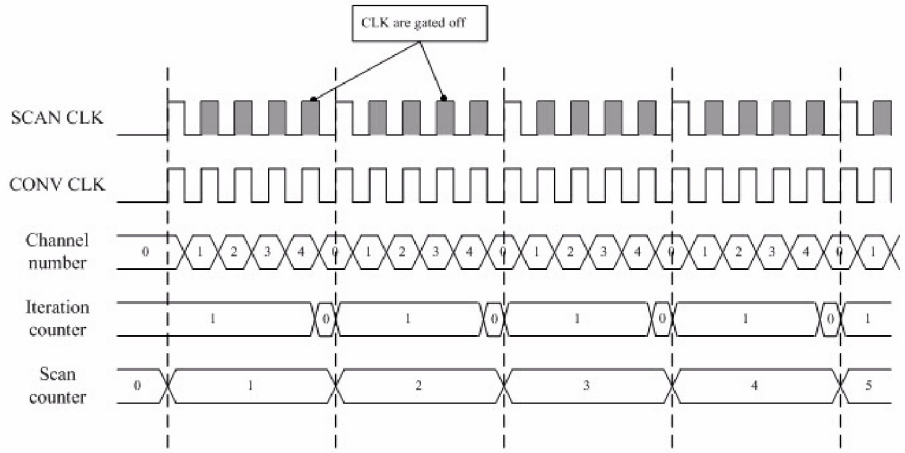
Multiple Iteration timing with fixed channel



Improperly matched SCAN CLK and CONV CLK

Single Clock Source Driving

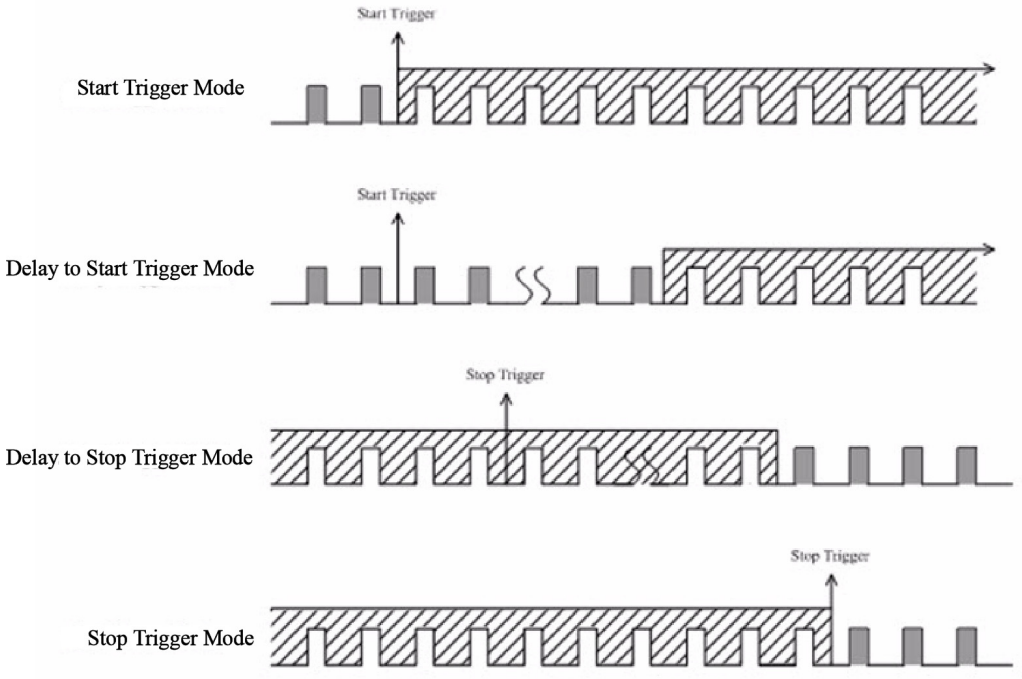
Single clock source driving is a specific function well-suited for consecutive data acquisition while there is only one clock signal available. CONV CLKs will be internally routed as SCAN CLKs. And the external SCAN CLKs input will not be accepted. Figure describes how it works.



Single clock source driving both CLKs

B.1.4 A/D Trigger Modes

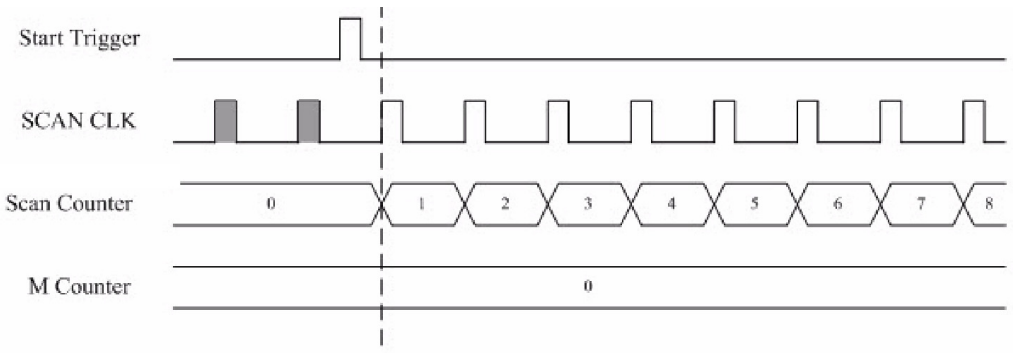
The PCIE-1810 supports four trigger modes and pause function. User can start or stop the operation by trigger mode selection. An extra 32-bit counter is dedicated to delay-trigger mode and about-trigger mode, and user can set it as the number of delay SCAN CLKs before trigger or the number of holding SCAN CLKs after trigger. Figure shows the four different trigger modes.



Trigger Modes

Start Trigger Acquisition Mode

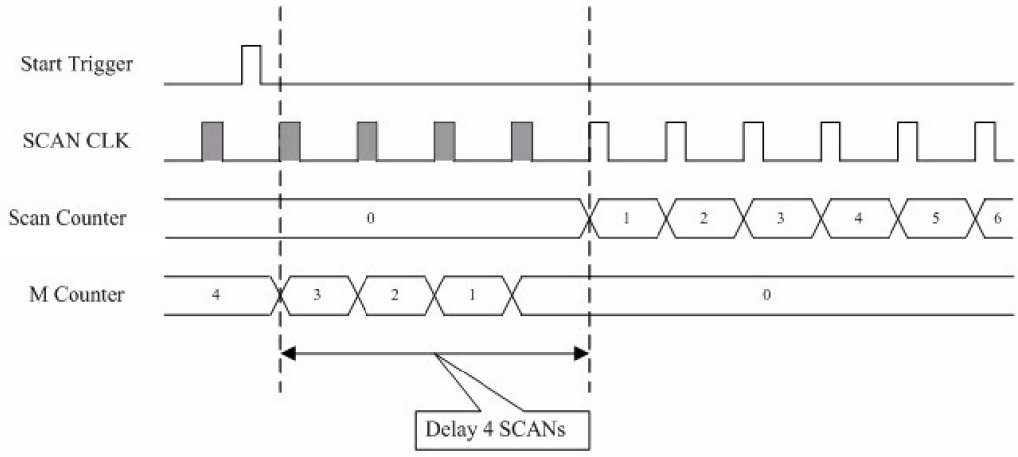
Start trigger acquisition starts when the PCIE-1810 detects the trigger event and stops when you stop the operation. The SCAN CLKs before Trigger will be blocked out. You can set post-trigger acquisition mode by software.



Start Trigger (M = 0)

Delay to Start Trigger Acquisition Mode

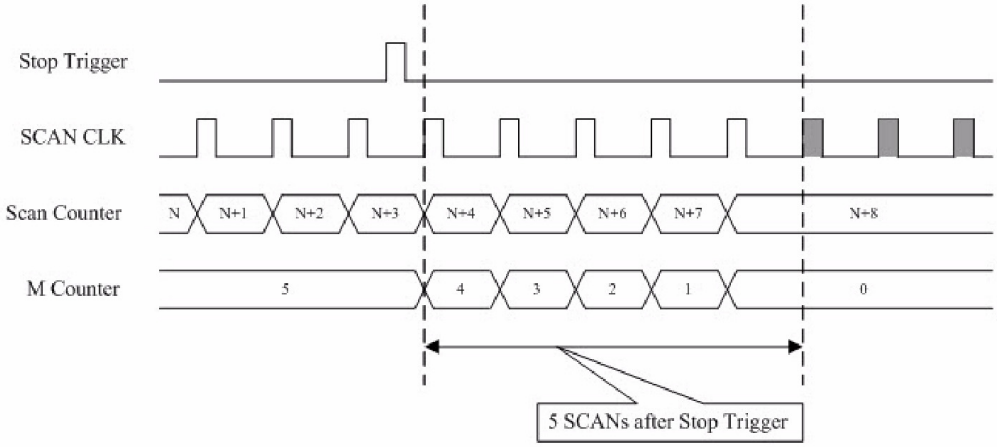
In delay to start trigger mode, data acquisition will be activated after a preset delay number of SCAN CLKs has been taken after the trigger event. User can set the delay number of SCAN CLKs by a 32-bit counter. Delay to start trigger acquisition starts when the PCIE-1810 detects the trig-ger event and stops when you stop the opera-tion.



Delay to Start Trigger (M = 4)

Delay to Stop Trigger Acquisition Mode

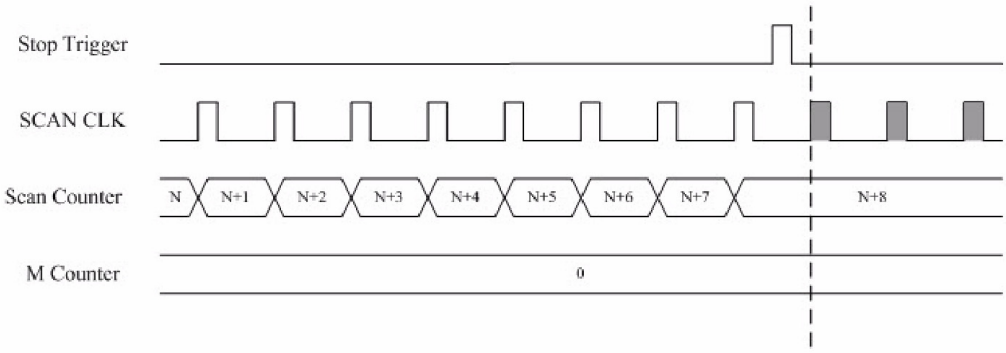
When you want to acquire data both before and after a specific trigger event occurs, users should take advantage of the delay to stop trigger mode. First designate the size of the allocated memory and the amount of samples to be snatched after the trigger event happens. The about-trig-ger acquisition starts when the first SCAN CLK signal comes in. Once a trigger event happens, the on-going data acquisition will continue until the designated amount of SCAN CLKs have been reached. When the PCIE-1810 detects the selected about-trigger event, the card keeps acquiring the preset number of samples, and kept them on the buffer.



Delay to Stop Trigger (M = 5)

Stop Trigger Acquisition Mode

Stop trigger mode is a particular application of about-trigger mode. Use pre-trigger acquisition mode when you want to acquire data before a specific trigger event occurs. Stop-trigger acquisition starts when you start the operation and stops when the trigger event happens.



Stop Trigger (M = 0)

B.1.5 A/D SCAN/CONV Clock Source

The PCIE-1810 can adopt both internal and external clock sources to accomplish pacer acquisition. You can set the clock and trigger sources conveniently by software. The figure can help you understand the routing route of clock and trigger generation.

SCAN Clock

- Internal A/D SCAN clock derived from 32-bit divider
- External A/D SCAN clock from terminal board
- External A/D CONV clock from terminal board

■ Internal A/D SCAN Clock

The internal A/D SCAN clock uses a 100 MHz time base divided by a 32-bit divider programmable by software. You can program SCAN clock source to internal and its frequency the clock source as internal and the frequency, 500 KS/s maximum for multi-channel and 800 KS/s maximum for single-channel, to activate A/D conversions. To ensure system stability, SCAN clock frequency should be less or equal to CONV clock.

■ External A/D SCAN Clock

The external A/D SCAN clock is useful when you want to execute acquisitions at rates not available from the internal A/D SCAN clock, or when you want to pace at uneven intervals. Acquisitions will start the rising edge of the external A/D SCAN clock input. And the frequency should be always limited under 500 KHz. The exceeding frequency may result in data loss or unexpected data acquisition.

■ External A/D CONV clock

This setting is useful when single external clock source is available. Instead of hardwire, the internal routing can protect signals from different line transmission delay.

CONV Clock

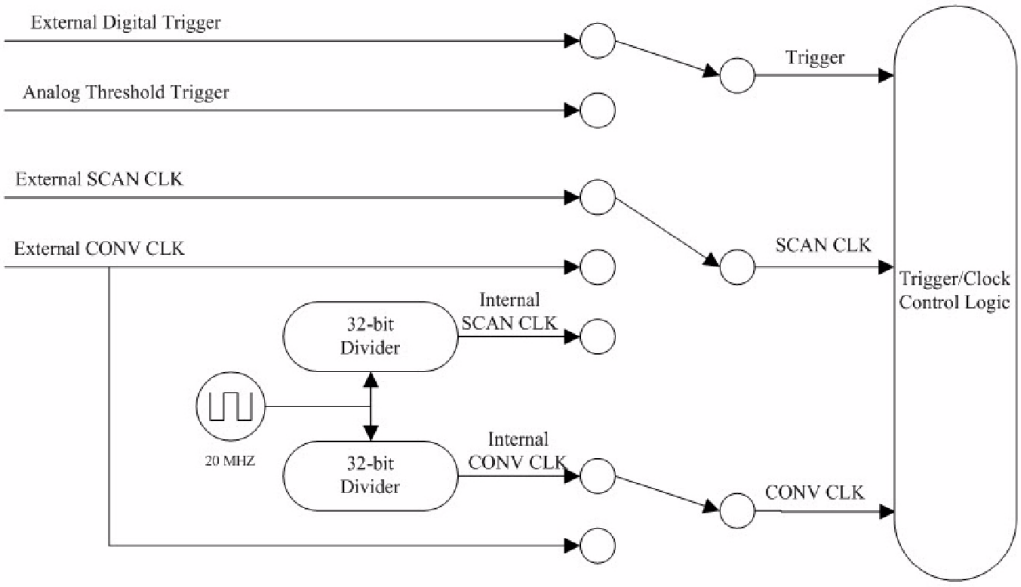
- Internal A/D CONV clock derived from 32-bit divider
- External A/D CONV clock from terminal board

■ Internal A/D CONV Clock

The same as internal SCAN clock, the internal A/D CONV clock applies 100 MHz time base accompanied with 32-bit divider. The maximum frequency is 500 KS/s. According to the sampling theory (Nyquist Theorem), you must specify a frequency that is at least twice as fast as the input's highest frequency component to achieve a valid sampling. For example, to accurately sample a 20 kHz signal, you have to specify a sampling frequency of at least 40 kHz. This consideration can avoid an error condition often know as aliasing, in which high frequency input components appear erroneously as lower frequencies when sampling.

External A/D CONV Clock

The external A/D CONV Clock is convenient in uneven sampling internal. A/D conversion will start by each arriving rising edge. The sampling frequency is always limited to a maximum of 500 KHz.



Trigger/Clock Routing Diagram

B.1.6 A/D Trigger Source

The PCIE-1810 supports the following trigger sources for start, delay to start, delay to stop, stop trigger acquisition modes:

- External digital (TTL) trigger
- Analog threshold trigger

With PCIE-1810, user can also define the type of trigger source as rising-edge or falling-edge. These following sections describe these trigger sources in more detail.

External Digital (TTL) Trigger

For analog input operations, an external digital trigger event occurs when the PCIE-1810 detects either a rising or falling edge on the External A/D TTL trigger input. The trigger signal is TTL compatible.

- **Analog Threshold Trigger**

For analog input operations, an analog trigger event occurs when the PCIE-1810 detects a transition from above a threshold level to below a threshold level (falling edge), or a transition from below a threshold level to above a threshold level (rising edge). User should connect ana-log signals from external device or analog output channel on board to external input signal ATRG0/1. On the PCIE-1810, the threshold level is set using a dedicated 12-bit DAC. By software, you can program the threshold level by writing a voltage value to this DAC; this value can range from -10 V to +10 V.

Table B.2: Analog Input Data Format

A/D Code		Mapping Voltage	
Hex.	Dec.	Unipolar	Bipolar
000 h	0 d	0	- FS/2
7FF h	2047 d	FS/2 - 1 LSB	- 1LSB
800 h	2048 d	FS/2	0
FFF h	4095 d	FS - 1 LSB	FS/2 - 1 LSB
1 LSB		FS/4096	FS/4096

Table B.3: Full Scale Values for Input Voltage Ranges

Gain	Unipolar		Bipolar	
	Range	FS	Range	FS
0.5	N/A	N/A	± 10 V	20
1	0 ~ 10 V	10	± 5 V	10
2	0 ~ 5 V	5	± 2.5 V	5
4	0 ~ 2.5 V	2.5	± 1.25 V	2.5
8	0 ~ 1.25 V	1.25	± 0.625 V	1.25

B.2 PCIE-1810 Analog Output Operation

The PCIE-1810 card provides two 12-bit multi-range analog output (D/ A) channels. This section describes the following features:

- Analog output ranges
- Analog output operation modes
- Synchronous Analog output waveform
- D/A clock sources
- D/A Trigger sources
- Analog Output Data Format

B.2.1 Analog Output Ranges

The PCIE-1810 provides two 12-bit analog output channels, both of which can be configured internally to be applicable within 0 ~ 5 V, 0 ~ 10 V, ± 5 V, ± 10 V output voltage range. Otherwise, users can use external reference voltage to apply 0 ~ x V or ± x V output range, where the value x is from -10 to +10. Users can configure the output range during driver installation or in software programming.

B.2.2 Analog Output Operation Modes

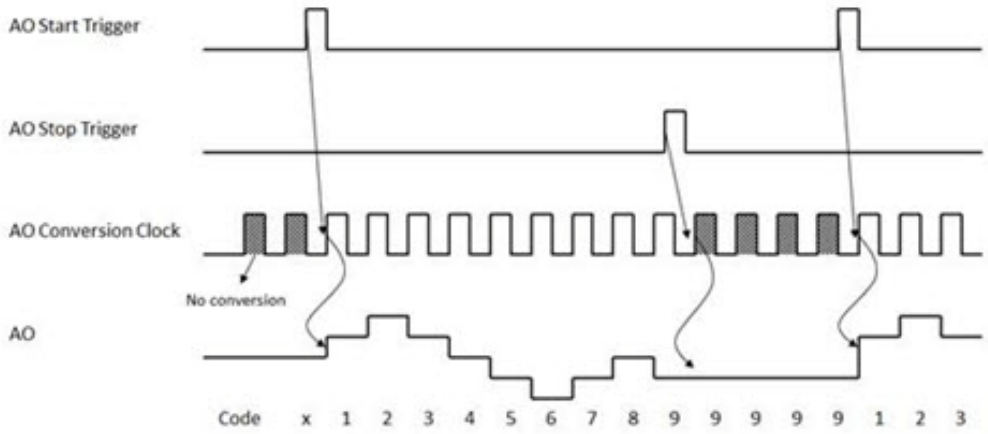
Single Value Operation Mode

The single value conversion mode is the simplest way for analog output operation. Users can set the mode of each channel individually. Then users just need to use software to write output data to specific register. The analog output channels will output the corresponding voltage immediately. In the single value operation mode, users need not set any clock source and trigger source, but only output voltage range.

Waveform Mode

In waveform mode, all D/A channels can change output voltage at the same time. Users can accurately control the update rate (up to 500 kS/s) between conversions of individual analog output channels, and takes full advantage of the PCIE-1810. In this mode you can specify a clock and trigger source and either of the two analog output channels to work in this mode.

Before operating in this mode, users need to set the clock and trigger source first, and then generate the output data stored in the memory buffers of host PC. The host computer then transfers those data to the DACs' buffers on PCIE-1810. When PCIE-1810 detects a trigger, it outputs the values stored in its buffer. When the buffer's storage decreases, the card sends an interrupt request to the host PC which in turn sends samples to the buffer. This output operation will repeat until either all the data is sent from the buffers or until you stop the operation. If the two D/A channels are both operating in continuous output mode, the data in buffer will be sent in an interlaced manner, i.e. the "Even-Address" samples in the buffer are sent to D/A channel 0, while the "Odd-Address" samples to D/A channel 1.



Waveform Mode Output

B.2.3 D/A Clock Sources

The PCIE-1810 can adopt both internal and external clock sources for pacing the analog output of each channel:

- Internal D/A output clock with 32-bit Divider
- External D/A output clock from connector

The internal and external D/A output clocks are described in more detail as follows:

- Internal D/A Output Clock

The internal D/A output clock applies a 100 MHz time base divided by a 32-bit counter. Conversions start on the rising edges of counter output. Through software, user can specify the clock source and clock frequency to pace the analog output operation. The maximum frequency is 500 kS/s.

- External D/A Output Clock

The external D/A output clock is useful when you want to pace analog output operations at rates not available with the internal D/A output clock, or when you want to pace at uneven intervals. Connect an external D/A output clock to the pin and then the conversions will start on input signal's rising edge. You can use software to specify the clock source as external. The maximum input clock frequency is 500 kS/s.

B.2.4 D/A Trigger Sources

The PCIE-1810 supports External digital (TTL) trigger to activate D/A conversions for waveform mode. An external digital trigger event occurs when the PCIE-1810 detects either a rising or falling edge on the External D/A TTL trigger input signal from the pin of connector. User can define the type of trigger source as rising-edge or falling-edge by software. The trigger signal is TTL-compatible.

Table B.4: Analog Output Data Format

D/A Code		Mapping Voltage	
Hex.	Dec.	Unipolar	Bipolar
000 h	0 d	0	- FS/2
7FF h	2047 d	FS/2 - 1 LSB	- 1LSB
800 h	2048 d	FS/2	0
FFF h	4095 d	FS - 1 LSB	FS/2 - 1 LSB
1 LSB		FS/4096	FS/4096

Table B.5: Full Scale Values for Output Voltage Ranges

Reference Source	Unipolar		Bipolar	
	Range	FS	Range	FS
Internal	0 ~ 5 V	5	± 5 V	10
	0 ~ 10 V	10	± 10 V	20
External	0 ~ x V	x	± x V	2x

B.3 Digital Input/Output Operation

The PCIE-1810 supports 24 digital I/O channels. You can use each byte as either an input port or an output port by configuring the corresponding parameter; and all four channels of the byte have the same configuration.

You do not need to specify the clock source or trigger source. To output the data, you just need to write it to the digital output channel directly. In the same way, you can directly read back data from digital input channel. The default configuration after reset sets all the digital I/O channels to logic-low so users don't need to worry about damaging external devices during system start up or reset.

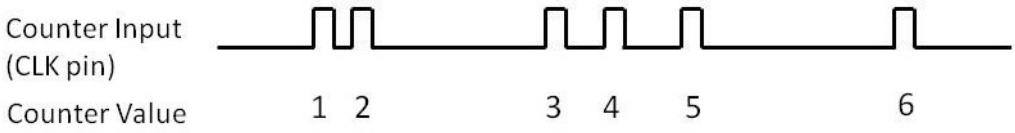
B.4 Counter Input and PWM Input/Output

PCIE-1810 offer two 32-bit counters inputs which can perform event counting, frequency measurement and pulse width measurement.

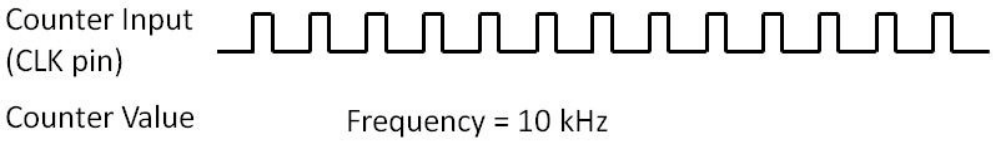
Counters on PCIE-1810 have a counter value match interrupt function. When this interrupt function is enabled, an interrupt signal will be generated if the counter value reaches a pre-set counter match value. The counter will continue to count until an overflow occurs, then it will go back to its reset value zero and continue the counting process. A user can set each individual counter channel to count either falling edge (high-to-low) or rising edge (low-to-high) signals.

Except measurement functionality, counter input channels can combine with PWM output channels to generate single pulse, pulse train or PWM (pulse-width modulated) output signal. A pulse-width modulated waveform is created when the High and Low periods of a periodic rectangular signal are varied. Using PCIE-1810, user can individually set each PWM channel's High and Low periods for from 2 to (2^{32} -1) units (1 unit = 50 ns), depending on his needs.

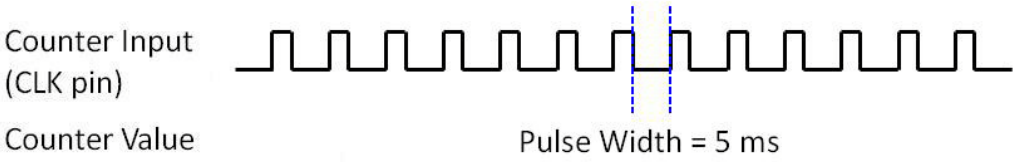
1. Event counter: PCIE-1810 built-in counter can calculate how many pulse are sent into the input channel.



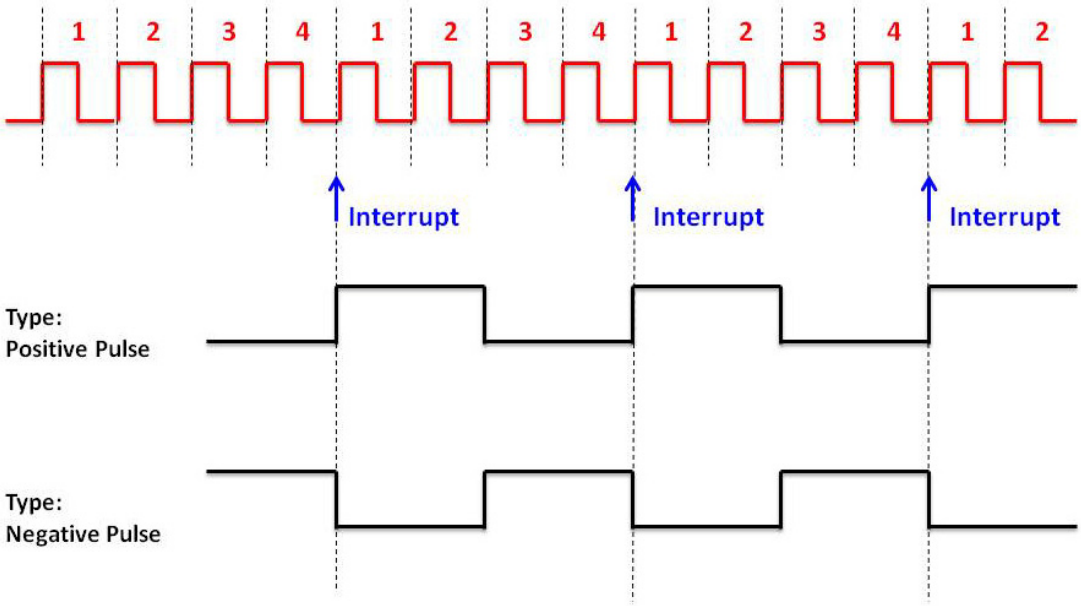
2. Frequency measurement: PCIE-1810 built-in counter can measure the frequency value of the signal connected to counter input.



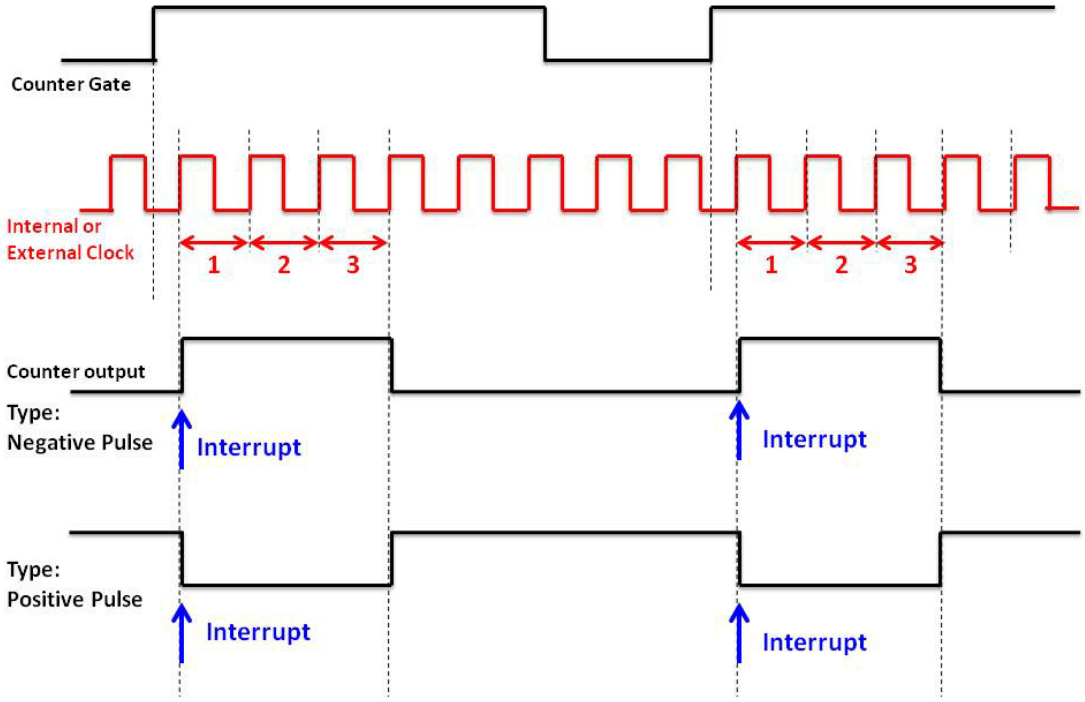
3. Pulse Width measurement: PCIE-1810 built-in counter can measure the pulse width value of the signal connected to counter input. The measurable range is 50 ns to 107 seconds. You can measure both the logic high time and logic low time within the measurable range.



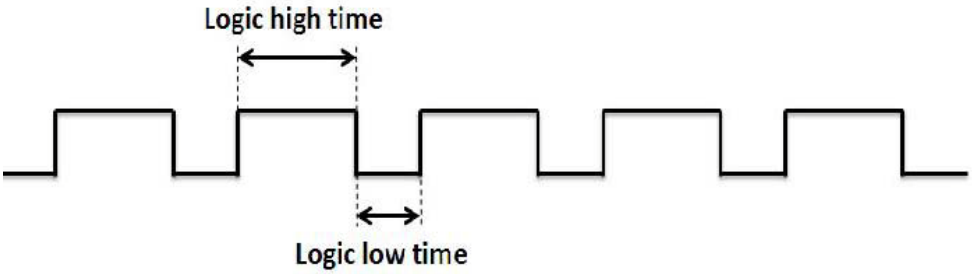
4. Pulse Output with Timer Interrupt: PCIE-1810 counter has internal clock that you can produce periodic output signal with interrupt generated at the same time. PCIE-1810 counter will use internal clock as time base, to fulfill the frequency you want to set. See the figure below as example, the desired frequency is 5 MHz. The internal clock is 20 MHz, so PCIE-1810 will periodically generate output signal and interrupt every 4 pulses of the internal clock. (20 MHz / 5 MHz = 4). Available output frequency range is 0.005 Hz ~ 5 MHz.



5. Delay Pulse Generation: Using PCIE-1810 internal clock, you can change the logic level within a specific period, starting from a trigger signal connecting to counter gate input. For example, if you define the count equals to 3 (as figure below), a counter output will change its status after 3 pulses of internal clock signals pass, after a trigger signal from counter gate becomes high.



6. PWM Output: PCIE-1810 can generate PWM (pulse width modulation) signal which you can configure its logic high time and logic low time as figure below. The available period range for logic high time and logic low time is 100 ns ~ 214 second.



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