

SSD1331

Advance Information

96RGB x 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

<http://www.solomon-systech.com>

SSD1331

Rev 1.0

P 1/68

Jul 2006

Copyright © 2006 **Solomon Systech Limited**



CONTENTS

CONTENTS	2
1 GEREAL INFORMATION	6
2 FEATURES	6
3 ORDERING INFORMATION	6
4 BLOCK DIAGRAM	7
5 SSD1331Z GOLD BUMP DIE PAD ASSIGNMENT	8
6 PIN DESCRIPTION	12
7 FUNCTIONAL BLOCK DESCRIPTIONS	15
7.1 MCU INTERFACE SELECTION	15
7.1.1 6800-series Parallel Interface	15
7.1.2 8080-series Parallel Interface	16
7.1.3 Serial Interface.....	17
7.2 COMMAND DECODER.....	18
7.3 OSCILLATOR CIRCUIT AND DISPLAY TIME GENERATOR	18
7.3.1 Oscillator	18
7.3.2 FR synchronization	19
7.4 RESET CIRCUIT	19
7.5 GRAPHIC DISPLAY DATA RAM (GDDRAM).....	20
7.5.1 GDDRAM structure	20
7.5.2 Data bus to RAM mapping under different input mode	20
7.5.3 RAM mapping and Different color depth mode.....	21
7.6 GRAY SCALE DECODER	21
7.7 SEG / COM DRIVING BLOCK.....	23
7.8 COMMON AND SEGMENT DRIVERS.....	24
7.9 POWER ON AND OFF SEQUENCE.....	27
8 COMMAND TABLE	28
8.1 DATA READ / WRITE	34
9 COMMAND DESCRIPTIONS	35
9.1 FUNDAMENTAL COMMAND.....	35
9.1.1 Set Column Address (15h).....	35
9.1.2 Set Row Address (75h).....	35
9.1.3 Set Contrast for Color A, B, C (81h, 82h, 83h)	36
9.1.4 Master Current Control (87h).....	36
9.1.5 Set Second Pre-charge Speed for Color A, B, C (8Ah).....	37
9.1.6 Set Re-map & Data Format (A0h)	37
9.1.7 Set Display Start Line (A1h).....	42
9.1.8 Set Display Offset (A2h)	42
9.1.9 Set Display Mode (A4h ~ A7h)	45
9.1.10 Set Multiplex Ratio (A8h)	45
9.1.11 Dim mode setting (ABh).....	45
9.1.12 Set Master Configuration (ADh).....	45
9.1.13 Set Display On/Off (ACh / AEh / AFh)	45
9.1.14 Power Save Mode (B0h).....	46
9.1.15 Phase 1 and 2 Period Adjustment (B1h)	46
9.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (B3h)	46
9.1.17 Set Gray Scale Table (B8h).....	46
9.1.18 Enable Linear Gray Scale Table (B9h).....	47
9.1.19 Set Pre-charge voltage (BBh).....	47
9.1.20 Set V _{COMH} Voltage (BEh).....	47
9.1.21 NOP (BCh, BDh, E3h)	47
9.1.22 Set Command Lock (FDh)	47
9.2 GRAPHIC ACCELERATION COMMAND SET DESCRIPTION.....	48
9.2.1 Draw Line (21h)	48
9.2.2 Draw Rectangle (22h).....	48

9.2.3	Copy (23h)	49
9.2.4	Dim Window (24h)	49
9.2.5	Clear Window (25h)	50
9.2.6	Fill Enable/Disable (26h).....	50
9.2.7	Continuous Horizontal & Vertical Scrolling Setup (27h)	51
9.2.8	Deactivate scrolling (2Eh).....	51
9.2.9	Activate scrolling (2Fh)	51
10	MAXIMUM RATINGS.....	52
11	DC CHARACTERISTICS.....	53
12	AC CHARACTERISTICS.....	54
13	APPLICATION EXAMPLE	58
14	PACKAGE OPTIONS.....	59
14.1	SSD1331Z DIE TRAY INFORMATION.....	59
14.2	SSD1331U1R1 COF PACKAGE DIMENSIONS.....	60
14.3	SSD1331U1R1 COF PACKAGE PIN ASSIGNMENT.....	62
14.4	SSD1331U3R1 COF PACKAGE DIMENSIONS.....	64
14.5	SSD1331U3R1 COF PACKAGE PIN ASSIGNMENT.....	66

TABLES

Table 1 - Ordering Information	6
Table 2 - SSD1331Z Die Pad Coordinates.....	9
Table 3 - Bus Interface selection	12
Table 4 - MCU interface assignment under different bus interface mode.....	15
Table 5 - Control pins of 6800 interface	15
Table 6 - Control pins of 8080 interface (Form 1)	16
Table 7 - Control pins of 8080 interface (Form 2)	16
Table 8 - Control pins of Serial interface	17
Table 9 - Data bus usage under different bus width and color depth mode.....	20
Table 10 - Command Table.....	28
Table 11 - Address increment table (Automatic).....	34
Table 12 - Illustration of different COM output settings	39
Table 13 - Example of Set Display Offset and Display Start Line with no Remap	43
Table 14 - Example of Set Display Offset and Display Start Line with Remap	44
Table 15 - Result of Change of Brightness by Dim Window Command.....	49
Table 16 - Maximum Ratings.....	52
Table 17 - DC Characteristics	53
Table 18 - AC Characteristics.....	54
Table 19 - 6800-Series MPU Parallel Interface Timing Characteristics	55
Table 20 - 8080-Series MPU Parallel Interface Timing Characteristics	56
Table 21 - Serial Interface Timing Characteristics	57
Table 22 - SSD1331U1R1 pin assignment	63
Table 23 - SSD1331U3R1 pin assignment	67

FIGURES

Figure 1 - SSD1331 Block Diagram	7
Figure 2 - SSD1331Z Die Drawing	8
Figure 3 - SSD1331Z Alignment mark dimensions	11
Figure 4 - Display data read back procedure - insertion of dummy read	15
Figure 5 - Example of Write procedure in 8080 parallel interface mode	16
Figure 6 - Example of Read procedure in 8080 parallel interface mode	16
Figure 7 - Display data read back procedure - insertion of dummy read	17
Figure 8 - Write procedure in SPI mode	17
Figure 9 - Oscillator Circuit	18
Figure 10 - 65k Color Depth Graphic Display Data RAM Structure	20
Figure 11 - 256-color mode mapping	21
Figure 12 - Relation between GDRAM content and gray scale table entry for three colors in 65K color mode	21
Figure 13 - Illustration of relation between graphic display RAM value and gray scale control	22
Figure 14 - I_{REF} Current Setting by Resistor Value	23
Figure 15 - I_{SEG} current vs V_{CC} setting at constant I_{REF} , Contrast = FFh	23
Figure 16 - Segment and Common Driver Block Diagram	24
Figure 17 - Segment and Common Driver Signal Waveform	25
Figure 18 - Gray Scale Control by PWM in Segment	26
Figure 19 : The Power ON sequence	27
Figure 20 : The Power OFF sequence	27
Figure 21 - Example of Column and Row Address Pointer Movement	35
Figure 22 - Segment Output Current for Different Contrast Control and Master Current Setting	36
Figure 23 - Effect of setting the second pre-charge under different speeds	37
Figure 24 - Address Pointer Movement of Horizontal Address Increment Mode	37
Figure 25 - Address Pointer Movement of Vertical Address Increment Mode	37
Figure 26 - Example of Column Address Mapping	38
Figure 27 - COM Pins Hardware Configuration (MUX ratio: 64)	40
Figure 28 - Transition between different modes	45
Figure 29 - Typical Oscillator frequency adjustment by B3 command ($V_{DD} = 2.7V$)	46
Figure 30 - Example of gamma correction by gray scale table setting	47
Figure 31 - Typical Pre-charge voltage level setting by command BBh	47
Figure 32 - Example of Draw Line Command	48
Figure 33 - Example of Draw Rectangle Command	48
Figure 34 - Example of Copy Command	49
Figure 35 - Example of Copy + Clear = Move Command	50
Figure 36 - Examples of Continuous Horizontal and Vertical Scrolling command setup	51
Figure 37 - 6800-series parallel interface characteristics	55
Figure 38 - 8080-series parallel interface characteristics (Form 1)	56
Figure 39 - 8080-series parallel interface characteristics (Form 2)	56
Figure 40 - Serial interface characteristics	57
Figure 41 - Application Example for SSD1331U1R1	58
Figure 42 - Die Tray Information	59
Figure 43 - SSD1331U1R1 outline drawing	60
Figure 44 - SSD1331U1R1 pin assignment drawing	62
Figure 45 - SSD1331U3R1 outline drawing	64
Figure 46 - SSD1331U3R1 pin assignment drawing	66

1 GERENAL INFORMATION

The SSD1331 is a single chip CMOS OLED/PLED driver with 288 segments and 64 commons output, supporting up to 96RGB x 64 dot matrix display. This chip is designed for Common Cathode type OLED/PLED panel.

The SSD1331 had embedded Graphic Display Data RAM (GDDRAM). It supports with 8, 9, 16 bits 8080 / 6800 parallel interface as well as serial peripheral interface. It has 256-step contrast and 65K color control. To facilitate communication between lower operating voltages MCU, it has separate power for I/O interface logic. SSD1331 is suitable for mobile phones, MP3, MP4 and other industrial devices.

2 FEATURES

- Resolution: 96RGB x 64 dot matrix panel
- 65k color depth support by embedded 96x64x16 bit GDDRAM display buffer
- Power supply:
 - $V_{DD} = 2.4V$ to $3.5V$ for IC logic
 - $V_{CC} = 8.0V$ to $18.0V$ for Panel driving
 - $V_{DDIO} = 1.6V$ to V_{DD} for MCU interface
- Segment maximum source current: 200uA
- Common maximum sink current: 60mA
- 256 step contrast control for the each color component plus 16 step master current control
- Pin selectable MCU interface
 - 8/9/16 bits 6800-series parallel Interface
 - 8/9/16 bits 8080-series Parallel Interface
 - Serial Peripheral Interface
- Color swapping function (RGB <-> BGR)
- Graphic Accelerating Command (GAC) set with Continuous Horizontal, Vertical and Diagonal Scrolling
- Programmable Frame Rate
- Wide range of operating temperature: -40 to 85 °C

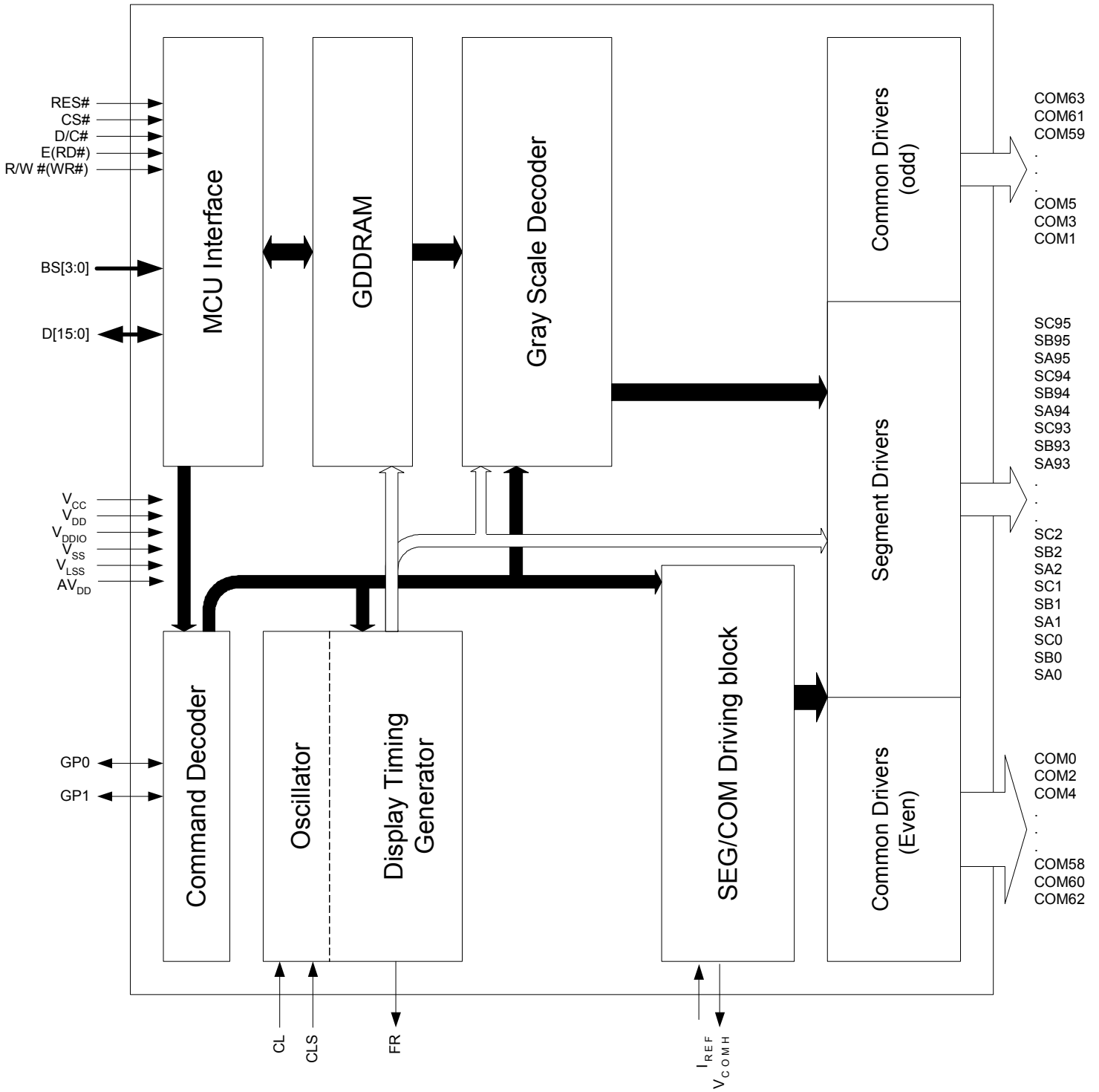
3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1331Z	96x3	64	COG	Page 8, 59	-
SSD1331U1R1	96x3	64	COF	Page 60	<ul style="list-style-type: none">• 35mm film, 5 sprocket hole• 8 bit or SPI interface• Output lead pitch: 0.06mm for SEG, 0.09mm for COM
SSD1331U3R1	96x3	64	COF	Page 64	<ul style="list-style-type: none">• 35mm film, 4 sprocket hole• 8 bit or SPI interface• Output lead pitch: 0.06mm for SEG, 0.09mm for COM

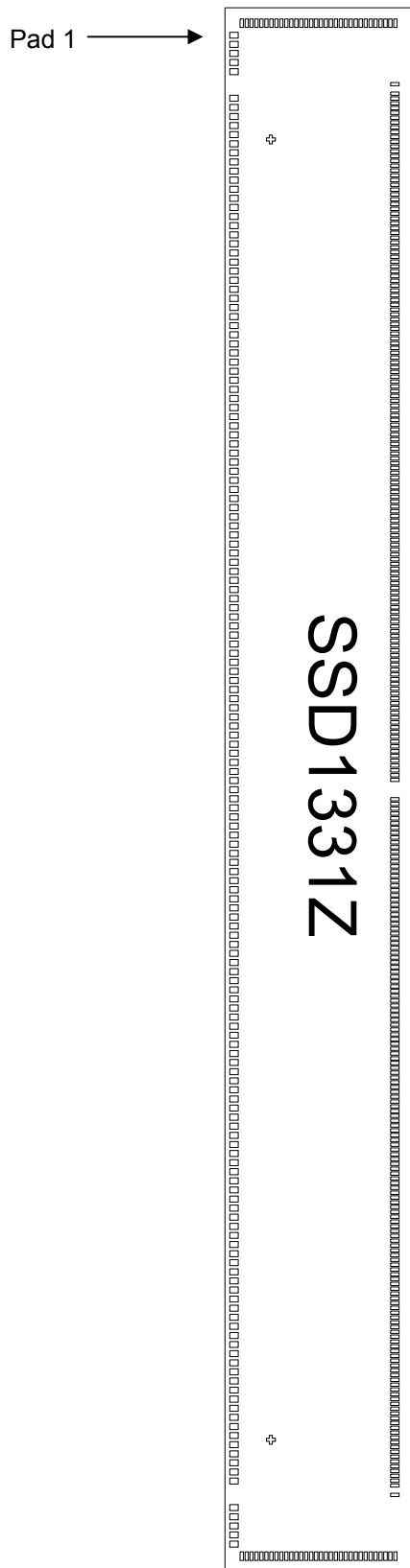
4 BLOCK DIAGRAM

Figure 1 - SSD1331 Block Diagram



5 SSD1331Z GOLD BUMP DIE PAD ASSIGNMENT

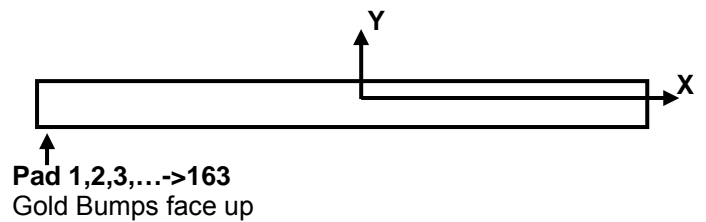
Figure 2 - SSD1331Z Die Drawing



Die size	13.1mm x 1.58mm
Die height	457um
Min I/O pad pitch	76.2 um
Min SEG pad pitch	40.2 um
Min COM pad pitch	41.8 um
Bump height	Nominal 15um

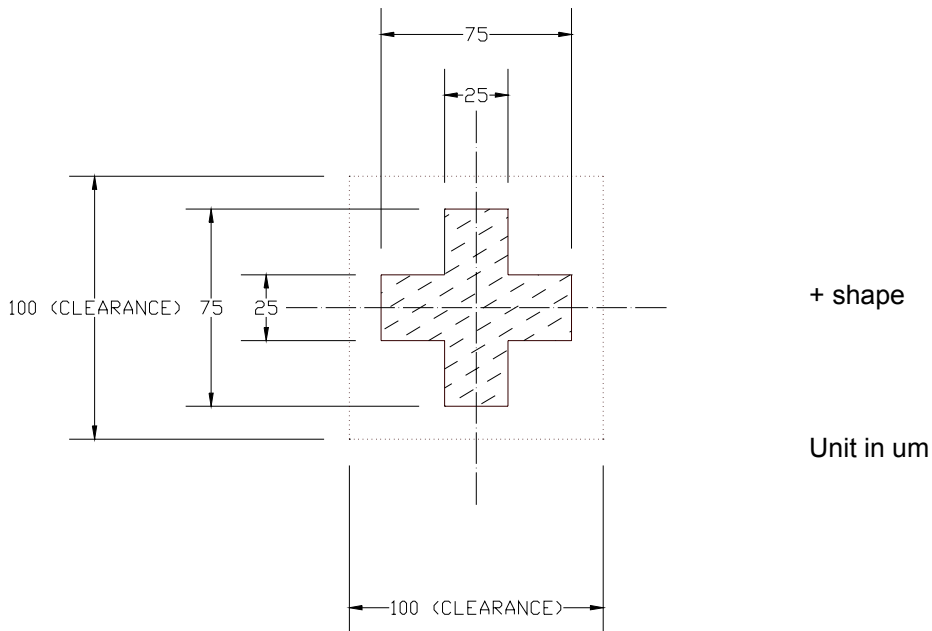
Bump size	
Pad 1-163	50um x 72um
Pad164-195, 486-517	72um x 28um
Pad 196-485	28um x 72um

Alignment mark		
+ shape	(5446.0, -402.0)	75um x 75um
+ shape	(-5446.0, -402.0)	75um x 75um



Pad no.	Pad Name	X-Axis	Y-Axis
481	SC94	-5709.3	643.6
482	SA95	-5749.5	643.6
483	SB95	-5789.7	643.6
484	SC95	-5829.9	643.6
485	VLSS	-5910.3	643.6
486	COM 32	-6420.1	647.9
487	COM 33	-6420.1	606.1
488	COM 34	-6420.1	564.3
489	COM 35	-6420.1	522.5
490	COM 36	-6420.1	480.7
491	COM 37	-6420.1	438.9
492	COM 38	-6420.1	397.1
493	COM 39	-6420.1	355.3
494	COM 40	-6420.1	313.5
495	COM 41	-6420.1	271.7
496	COM 42	-6420.1	229.9
497	COM 43	-6420.1	188.1
498	COM 44	-6420.1	146.3
499	COM 45	-6420.1	104.5
500	COM 46	-6420.1	62.7
501	COM 47	-6420.1	20.9
502	COM 48	-6420.1	-20.9
503	COM 49	-6420.1	-62.7
504	COM 50	-6420.1	-104.5
505	COM 51	-6420.1	-146.3
506	COM 52	-6420.1	-188.1
507	COM 53	-6420.1	-229.9
508	COM 54	-6420.1	-271.7
509	COM 55	-6420.1	-313.5
510	COM 56	-6420.1	-355.3
511	COM 57	-6420.1	-397.1
512	COM 58	-6420.1	-438.9
513	COM 59	-6420.1	-480.7
514	COM 60	-6420.1	-522.5
515	COM 61	-6420.1	-564.3
516	COM 62	-6420.1	-606.1
517	COM 63	-6420.1	-647.9

Figure 3 - SSD1331Z Alignment mark dimensions



6 PIN DESCRIPTION

Pin Name	Pin Type	Description																
V _{DD}	Power	Power supply pin for core V _{DD}																
AV _{DD}	Power	Analog power supply. It must be connected to V _{DD} during operation.																
V _{DDIO}	Power	Power supply for interface logic level. It should be match with the MCU interface voltage level. V _{DDIO} must always be equal or lower than V _{DD} .																
V _{CC}	Power	Power supply for panel driving voltage. This is also the most positive power voltage supply pin.																
V _{SS}	Power	Ground pin																
V _{LSS}	Power	Analog system ground pin.																
V _{COMH}	O	COM signal deselected voltage level. A capacitor should be connected between this pin and V _{SS} .																
BGGND	Power	Connect to Ground																
V _{DDB}	Power	Reserved pin. It should be connect to V _{DD} externally.																
V _{SSB}	Power	Reserved pin. It should be connected to V _{SS} externally.																
GDR	O	Reserved pin. Keep NC (i.e. no connection).																
FB	I	Reserved pin. Keep NC (i.e. no connection).																
V _{BREF}	O	Reserved pin. Keep NC (i.e. no connection).																
GP0	I/O	Reserved pin. Keep NC (i.e. no connection).																
GP1	I/O	Reserved pin. Keep NC (i.e. no connection).																
V _{CIR}	O	Reserved pin. Keep NC (i.e. no connection).																
BS[3:0]	I	MCU bus interface selection pins. Table 3 - Bus Interface selection																
		<table border="1"> <thead> <tr> <th>BS[3:0]</th> <th>Bus Interface Selection</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>SPI</td> </tr> <tr> <td>0100</td> <td>8-bit 6800 parallel</td> </tr> <tr> <td>0101</td> <td>16-bit 6800 parallel</td> </tr> <tr> <td>0110</td> <td>8-bit 8080 parallel</td> </tr> <tr> <td>0111</td> <td>16-bit 8080 parallel</td> </tr> <tr> <td>1100</td> <td>9-bit 6800 parallel</td> </tr> <tr> <td>1110</td> <td>9-bit 8080 parallel</td> </tr> </tbody> </table>	BS[3:0]	Bus Interface Selection	0000	SPI	0100	8-bit 6800 parallel	0101	16-bit 6800 parallel	0110	8-bit 8080 parallel	0111	16-bit 8080 parallel	1100	9-bit 6800 parallel	1110	9-bit 8080 parallel
BS[3:0]	Bus Interface Selection																	
0000	SPI																	
0100	8-bit 6800 parallel																	
0101	16-bit 6800 parallel																	
0110	8-bit 8080 parallel																	
0111	16-bit 8080 parallel																	
1100	9-bit 6800 parallel																	
1110	9-bit 8080 parallel																	
I _{REF}	I	This pin is the segment output current reference pin. A resistor should be connected between this pin and V _{SS} to maintain the I _{REF} current at 10uA. Please refer to Figure 14 for the details formula of resistor value.																

Pin Name	Pin Type	Description
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. Keep NC if not used. Refer to section 7.3.2 for details usage.
CL	I	External clock input pin. When internal clock is enable, this pin is not used and should be kept NC. When internal clock is disable, this pin is the external clock source input pin.
CLS	I	Internal clock selection pin. When this pin is pulled high (i.e. connect to V_{DDIO}), internal oscillator is enable (normal operation). When this pin is pulled low, an external clock signal should be connected to CL.
CS#	I	This pin is the chip select input connecting to the MCU.
RES#	I	This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin high (i.e. connect to V_{DDIO}) during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled high (i.e. connect to V_{DDIO}), the data at D[15:0] will be interpreted as display data. When the pin is pulled low, the data at D[15:0] will be interpreted as command.
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high (i.e. connect to V_{DDIO}) and write mode when low. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W#(WR#) must be connected to V_{SS} .
E (RD#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high (i.e. connect to V_{DDIO}) and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to V_{SS} .
D[15:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie low. (Except for D2 pin in serial mode) Refer to Section 7.1 for different bus interface connection.
SA[95:0] SB[95:0] SC[95:0]	O	These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off by command Set Display Off. These 288 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.

Pin Name	Pin Type	Description
COM[63:0]	I/O	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off by command Set Display Off.
TR[11:0]	I	Testing reserved pins. These pins should be kept float.
NC	NC	Dummy pins. These pins should be kept float and should not be connected to any other signal pins nor any electrical signal. Do not connect NC pins together.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface Selection

SSD1331 MCU interface consist of 16 data pin and 5 control pins. The pin assignment at different interface mode is summarized in Table 4. Different MCU mode can be set by hardware selection on BS[3:0] pins (refer to Table 3 for BS pins setting)

Table 4 - MCU interface assignment under different bus interface mode

Pin Name Bus Interface	Data / Command Interface																Control Signal				
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8b / 8080	Tie Low								D7-D0								RD#	WR#	CS#	D/C#	RES#
8b / 6800	Tie Low								D7-D0								E	R/W#	CS#	D/C#	RES#
9b / 8080	Tie Low								D8-D0								RD#	WR#	CS#	D/C#	RES#
9b / 6800	Tie Low								D8-D0								E	R/W#	CS#	D/C#	RES#
16b / 8080	D15-D0																RD#	WR#	CS#	D/C#	RES#
16b / 6800	D15-D0																E	R/W#	CS#	D/C#	RES#
SPI	Tie Low												NC	SDIN	SCLK	Tie Low		CS#	D/C#	RES#	

7.1.1 6800-series Parallel Interface

A low in R/W# indicates WRITE operation and high in R/W# indicates READ operation. A low in D/C# indicates COMMAND read/write and high in D/C# indicates DATA read/write. The E input serves as data latch signal while CS# is low. Data is latched at the falling edge of E signal.

Table 5 - Control pins of 6800 interface

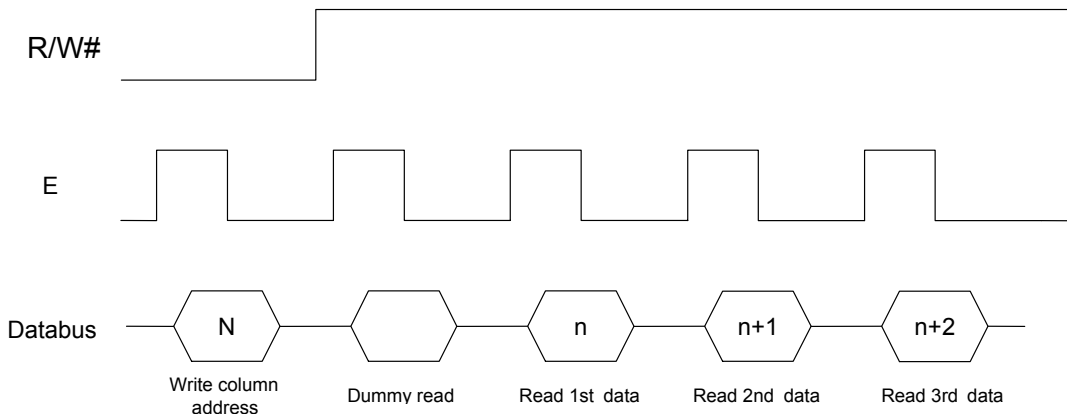
Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note

- (1) ↓ stands for falling edge of signal
- (2) H stands for high in signal
- (3) L stands for low in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 4

Figure 4 - Display data read back procedure - insertion of dummy read



7.1.2 8080-series Parallel Interface

A low in D/C# indicates COMMAND read/write and high in D/C# indicates DATA read/write.
 A rising edge of RD# input serves as a data READ latch signal while CS# is kept low.
 A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept low.

Figure 5 – Example of Write procedure in 8080 parallel interface mode

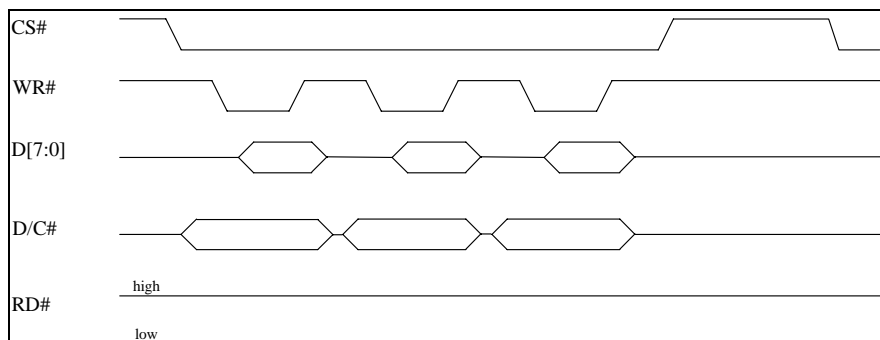


Figure 6 – Example of Read procedure in 8080 parallel interface mode

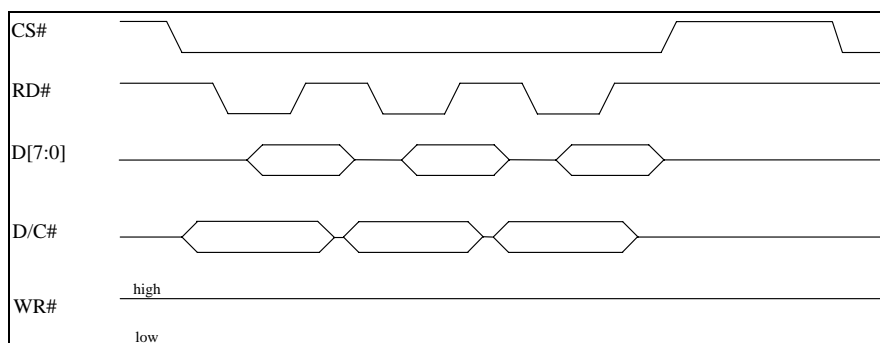


Table 6 - Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note

- (1) ↑ stands for rising edge of signal
- (2) H stands for high in signal
- (3) L stands for low in signal
- (4) Refer to Figure 38 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

Alternatively, E(RD#) and R/W#(WR#) can be keep stable while CS# is serve as the data/command latch signal.

Table 7 - Control pins of 8080 interface (Form 2)

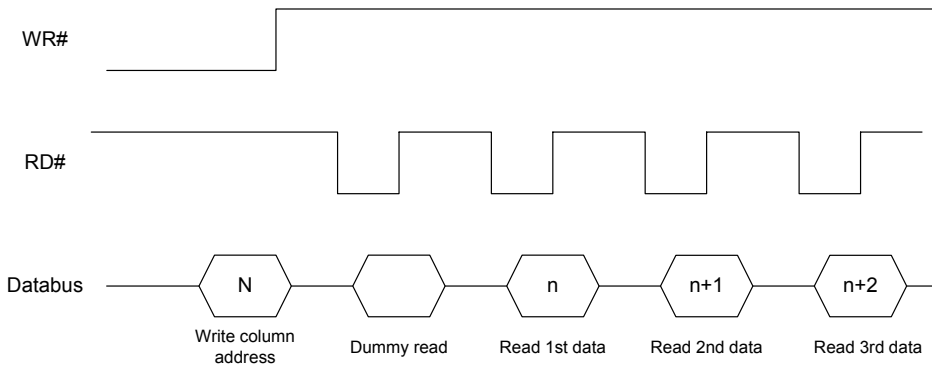
Function	RD#	WR#	CS#	D/C#
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note

- (1) ↑ stands for rising edge of signal
- (2) H stands for high in signal
- (3) L stands for low in signal
- (4) Refer to Figure 39 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7.

Figure 7 - Display data read back procedure - insertion of dummy read



7.1.3 Serial Interface

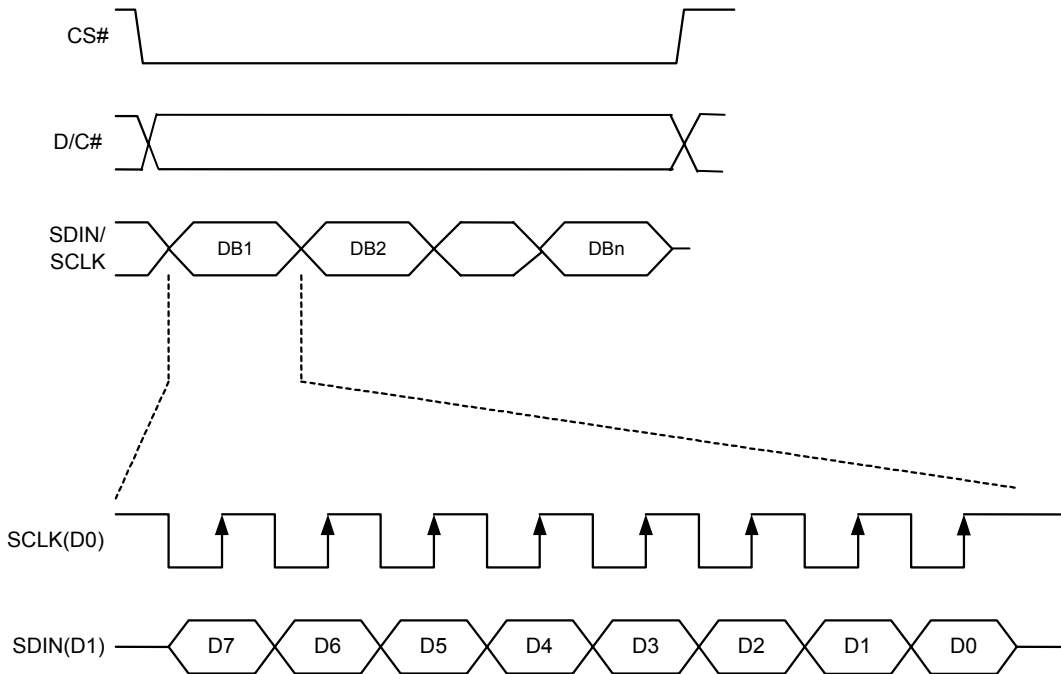
The serial interface consists of serial clock SCLK (D0), serial data SDIN (D1), D/C# and CS#. SCLK is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

Under serial mode, only write operations are allowed.

Table 8 - Control pins of Serial interface

Function	E	R/W#	CS#	D/C#
Write command	Tie low	Tie low	L	L
Write data	Tie low	Tie low	L	H

Figure 8 - Write procedure in SPI mode



7.2 Command Decoder

This module determines whether the input should be interpreted as data or command based upon the input of the D/C# pin.

If D/C# pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it is low, the inputs at D0-D15 are interpreted as a Command and it will be decoded and be written to the corresponding command register.

7.3 Oscillator Circuit and Display Time Generator

7.3.1 Oscillator

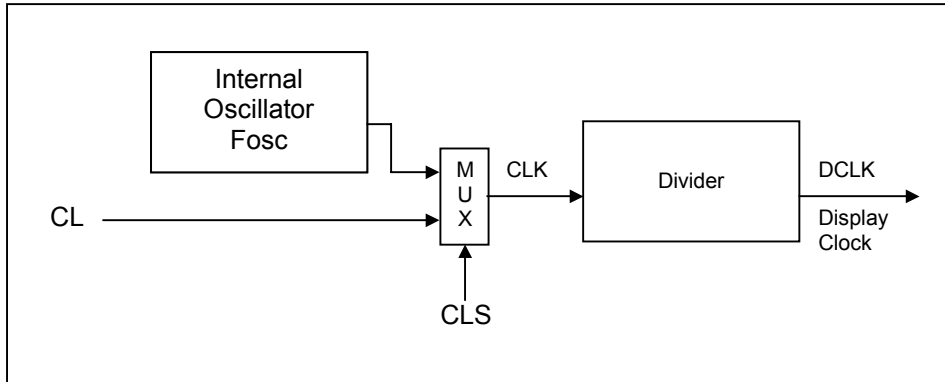


Figure 9 - Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 9). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is high, internal oscillator is selected. If CLS pin is low, external clock from CL pin will be used for CLK. The frequency of internal oscillator F_{OSC} can be programmed by command B3h (Set oscillator frequency).

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command B3h.

$$DCLK = F_{osc} / D$$

The frame frequency of display is determined by the following formula.

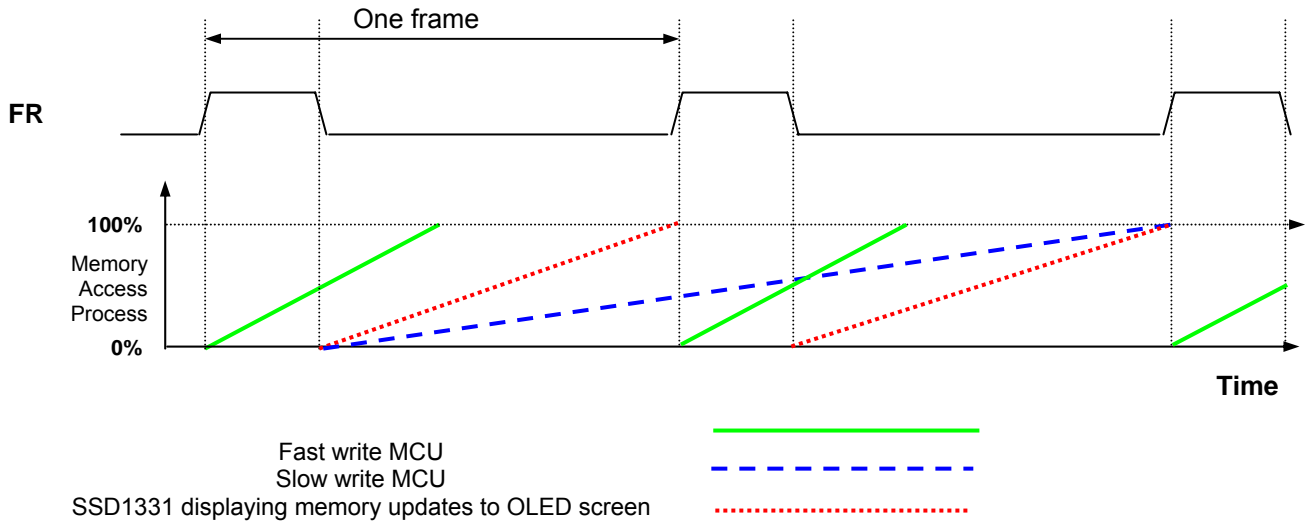
$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
 $K = \text{Phase 1 period} + \text{Phase 2 period} + \text{PW63 (longest current drive pulse width)}$
 $= 4 + 7 + 125 = 136$ at power on reset
- Number of multiplex ratio is set by command A8h. The power on reset value is 64
- F_{OSC} is the oscillator frequency. It can be adjusted by command B3h A[7:4]

7.3.2 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

7.4 Reset Circuit

When RES# input is pulled low, the chip is initialized with the following status:

1. Display is OFF
2. 64 MUX Display Mode
3. Display start line is set at display RAM address 0
4. Display offset set to 0
5. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
6. Column address counter is set at 0
7. Master contrast control register is set at 0FH
8. Individual contrast control registers of color A, B, and C are set at 80H
9. Shift register data clear in serial interface
10. Normal display mode (Equivalent to A4 command)

7.5 Graphic Display Data RAM (GDDRAM)

7.5.1 GDDRAM structure

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 96 x 64 x 16bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 16-bit data. Three sub-pixels for color A, B and C have 6 bits, 5 bits and 6 bits respectively. The arrangement of data pixel in graphic display data RAM is shown below.

Figure 10 - 65k Color Depth Graphic Display Data RAM Structure

Column Address	Normal	0	1	2	:	93	94	95													
	Remap	95	94	93	:	2	1	0													
Data Format		A4 B5 C4	A4 B5 C4	A4 B5 C4	:	A4 B5 C4	A4 B5 C4	A4 B5 C4													
		A3 B4 C3	A3 B4 C3	A3 B4 C3	:	A3 B4 C3	A3 B4 C3	A3 B4 C3													
		A2 B3 C2	A2 B3 C2	A2 B3 C2	:	A2 B3 C2	A2 B3 C2	A2 B3 C2													
		A1 B2 C1	A1 B2 C1	A1 B2 C1	:	A1 B2 C1	A1 B2 C1	A1 B2 C1													
		A0 B1 C0	A0 B1 C0	A0 B1 C0	:	A0 B1 C0	A0 B1 C0	A0 B1 C0													
Row Address		B0	B0	B0	:	B0	B0	B0													
Normal	Remap																				
0	63	5	6	5	5	6	5	5	6	5	:	5	6	5	5	6	5	5	6	5	
1	62										:										
2	61										:										
:	:	no. of bits of data in this cell																			
61	2										:										
62	1										:										
63	0										:										

SEG OUTPUT

SA0	SB0	SC0	SA1	SB1	SC1	SA2	SB2	SC2	:	SA93	SB93	SC93	SA94	SB94	SC94	SA95	SB95	SC95
-----	-----	-----	-----	-----	-----	-----	-----	-----	---	------	------	------	------	------	------	------	------	------

COM OUTPUT

COM0
COM1
COM2
:
COM61
COM62
COM63

7.5.2 Data bus to RAM mapping under different input mode

Table 9 - Data bus usage under different bus width and color depth mode

Bus width	Color Depth	Input order	Data bus																	
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
8 bits	256		X	X	X	X	X	X	X	X	X	C ₄	C ₃	C ₂	B ₅	B ₄	B ₃	A ₄	A ₃	
8 bits	65k format 1	1st	X	X	X	X	X	X	X	X	X	C ₄	C ₃	C ₂	C ₁	C ₀	B ₅	B ₄	B ₃	
		2nd	X	X	X	X	X	X	X	X	X	B ₂	B ₁	B ₀	A ₄	A ₃	A ₂	A ₁	A ₀	
8 bits	65k format 2	1st	X	X	X	X	X	X	X	X	X	X	X	C ₄	C ₃	C ₂	C ₁	C ₀	X	
		2nd	X	X	X	X	X	X	X	X	X	X	X	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀	
		3rd	X	X	X	X	X	X	X	X	X	X	X	A ₄	A ₃	A ₂	A ₁	A ₀	X	
16 bits	65k		C ₄	C ₃	C ₂	C ₁	C ₀	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀	A ₄	A ₃	A ₂	A ₁	A ₀		
9 bits	65k	1st	X	X	X	X	X	X	X	X	X	C ₄	C ₃	C ₂	C ₁	C ₀	X	B ₅	B ₄	B ₃
		2nd	X	X	X	X	X	X	X	X	X	B ₂	B ₁	B ₀	A ₄	A ₃	A ₂	A ₁	A ₀	X

7.5.3 RAM mapping and Different color depth mode

At 65k color depth mode, color A, B, C are directly mapped to the RAM content. At 256-color mode, the RAM content will be filled up to 65k format.

Figure 11 - 256-color mode mapping

	SCn					SBn						SAn				
65k color	C ₄	C ₃	C ₂	C ₁	C ₀	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀	A ₄	A ₃	A ₂	A ₁	A ₀
256 color	C ₄	C ₃	C ₂	*C ₄	*C ₄	B ₅	B ₄	B ₃	B ₅	*B ₅	*B ₅	A ₄	A ₃	*A ₄	*A ₄	*A ₄

Note:

(1) n = 0 ~ 95

(2) bits with * are copied from corresponding bits in order to fill up 65K format.

7.6 Gray Scale Decoder

The gray scale effect is generated by controlling the pulse width of segment drivers in current drive phase. The gray scale table stores the corresponding pulse widths of the 63 gray scale levels (GS0~GS63). The wider the pulse width, the brighter the pixel will be. A single gray scale table supports all the three colors A, B and C. The pulse widths can be set by software commands.

As shown in Figure 12, color B sub-pixel RAM data has 6 bits, represent the 64 gray scale levels from GS0 to GS63. color A and color C sub-pixel RAM data has only 5 bits, represent 32 gray scale levels from GS0, GS2, ..., GS62.

Figure 12 - Relation between GDRAM content and gray scale table entry for three colors in 65K color mode

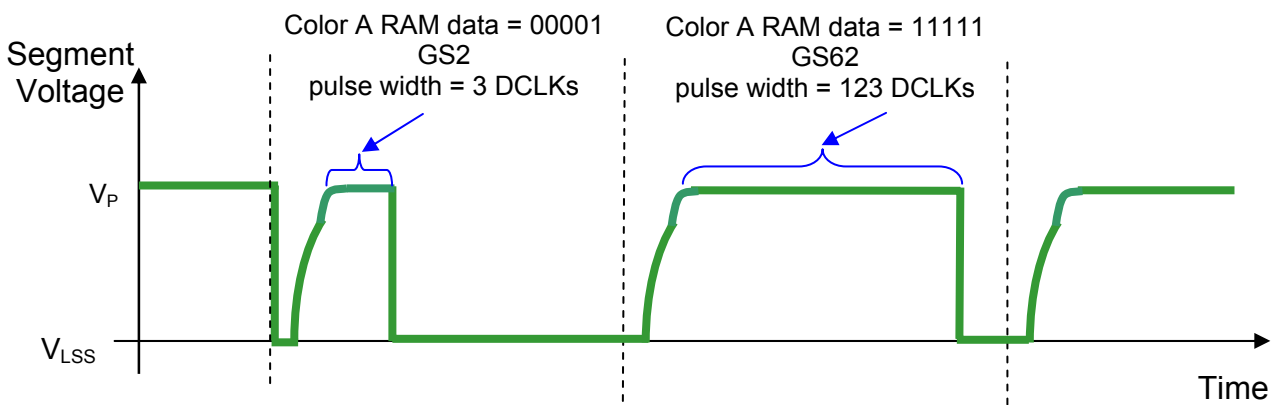
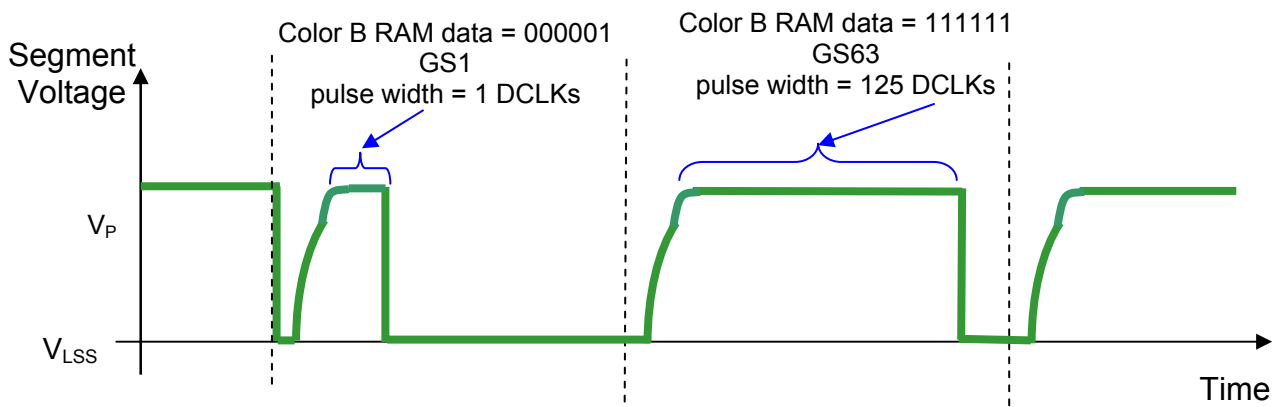
Color A, C RAM data (5 bits)	Color B RAM data (6 bits)	Gray Scale	Default pulse width of GS[0:63] in terms of DCLK
00000	000000	GS0	0
-	000001	GS1	1
00001	000010	GS2	3
-	000011	GS3	5
00010	000100	GS4	7
:	:	:	:
:	:	:	:
:	:	:	:
11110	111100	GS60	119
-	111101	GS61	121
11111	111110	GS62	123
-	111111	GS63	125

The duration of different GS are programmable.

Figure 13 - Illustration of relation between graphic display RAM value and gray scale control

Gray scale table

Gray Scale	Value/DCLKs
GS0	0
GS1	1
GS2	3
⋮	⋮
GS62	123
GS63	125



7.7 SEG / COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG} . The relationship between reference current and segment current of a color is:

$$I_{SEG} = \text{Contrast} / 256 \times I_{REF} \times \text{scale factor}$$

in which

the contrast (0~255) is set by Set Contrast command; and
the scale factor (1 ~ 16) is set by Master Current Control command.

For example, in order to achieve $I_{SEG} = 160\mu\text{A}$ at maximum contrast 255, I_{REF} is set to around $10\mu\text{A}$. This current value is obtained by connecting an appropriate resistor from I_{REF} pin to V_{SS} as shown in Figure 14.

Recommended range for $I_{REF} = 10\mu\text{A} \pm 2\mu\text{A}$

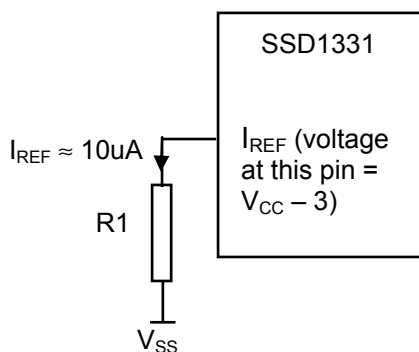
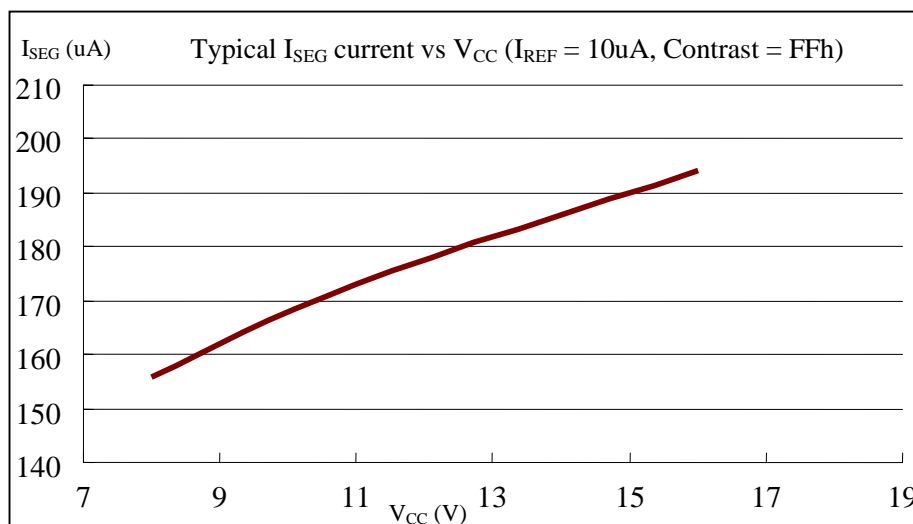


Figure 14 - I_{REF} Current Setting by Resistor Value

Since the voltage at I_{REF} pin is $V_{CC} - 3\text{V}$, the value of resistor $R1$ can be found as below.

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} = (V_{CC} - 3) / 10\mu\text{A} \approx 1.3\text{M}\Omega \text{ for } V_{CC} = 16\text{V}.$$

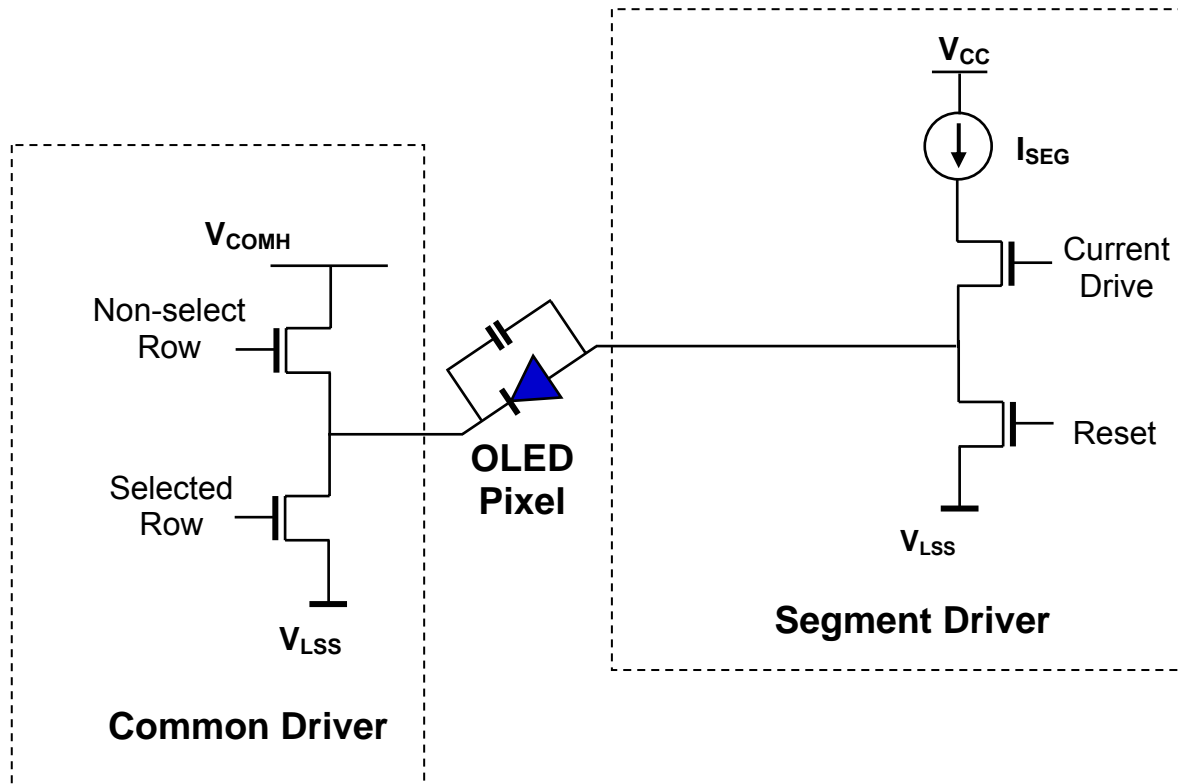
Figure 15 - I_{SEG} current vs V_{CC} setting at constant I_{REF} , Contrast = FFh



7.8 Common and Segment Drivers

Segment drivers consist of 288 (96 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 160uA with 256 steps by contrast setting command (81h,82h,83h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

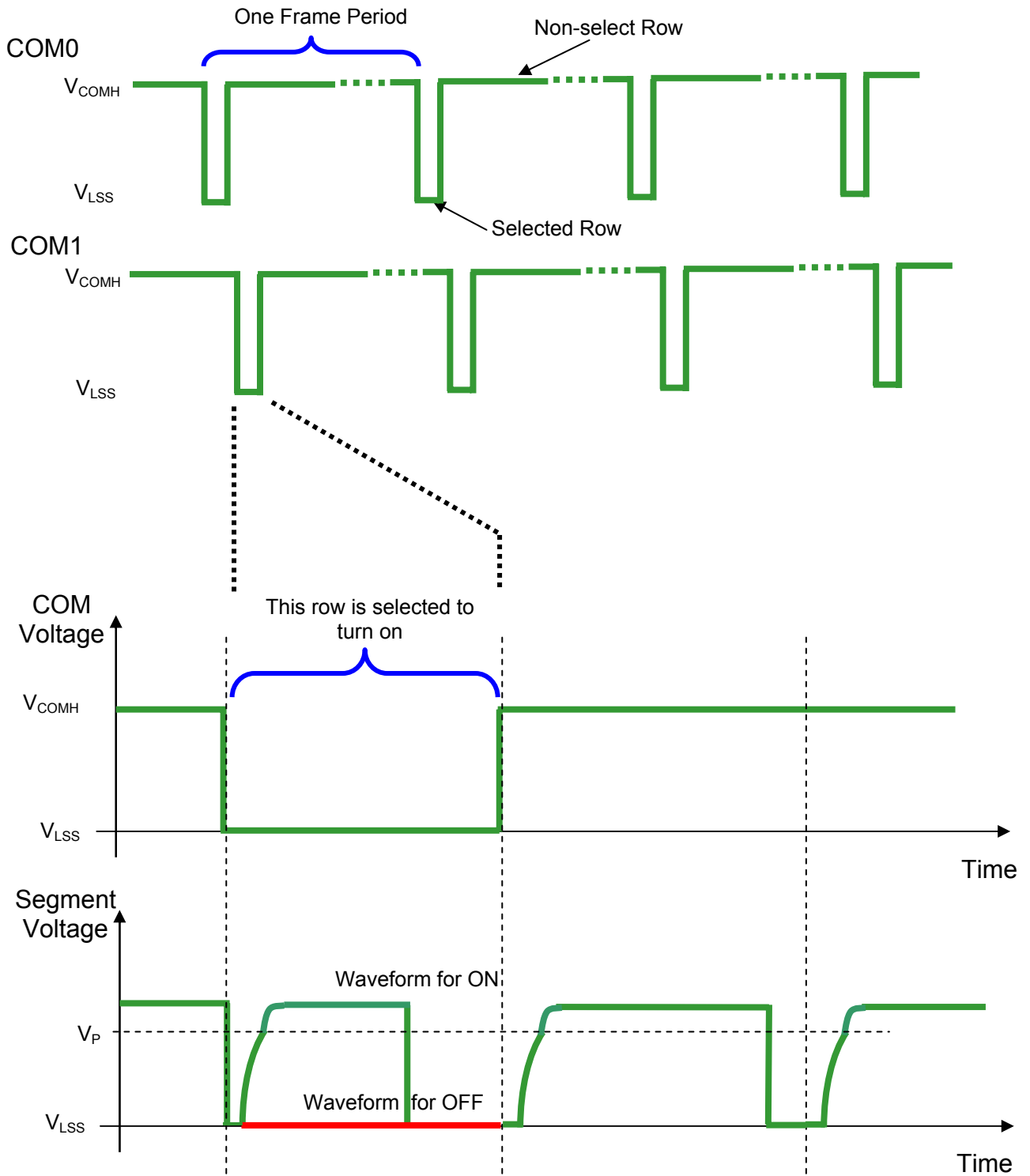
Figure 16 - Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 17

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 17 - Segment and Common Driver Signal Waveform



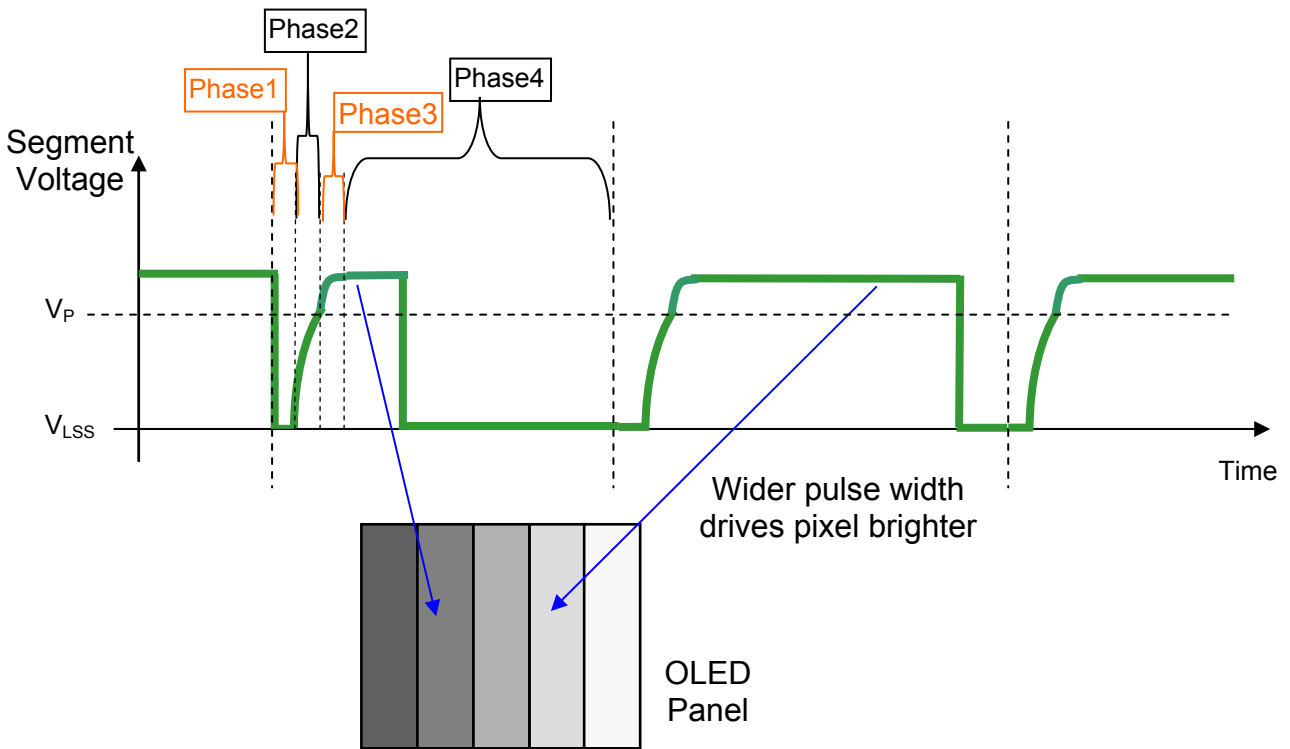
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0] from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS} . The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed in length from 1 to 16 DCLK by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by commands 8Ah, 8Bh and 8Ch.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs Pulse Width Modulation (PWM) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

Figure 18 - Gray Scale Control by PWM in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B8h "Set Gray Scale Table" or B9h "Enable Linear Gray Scale Table". In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

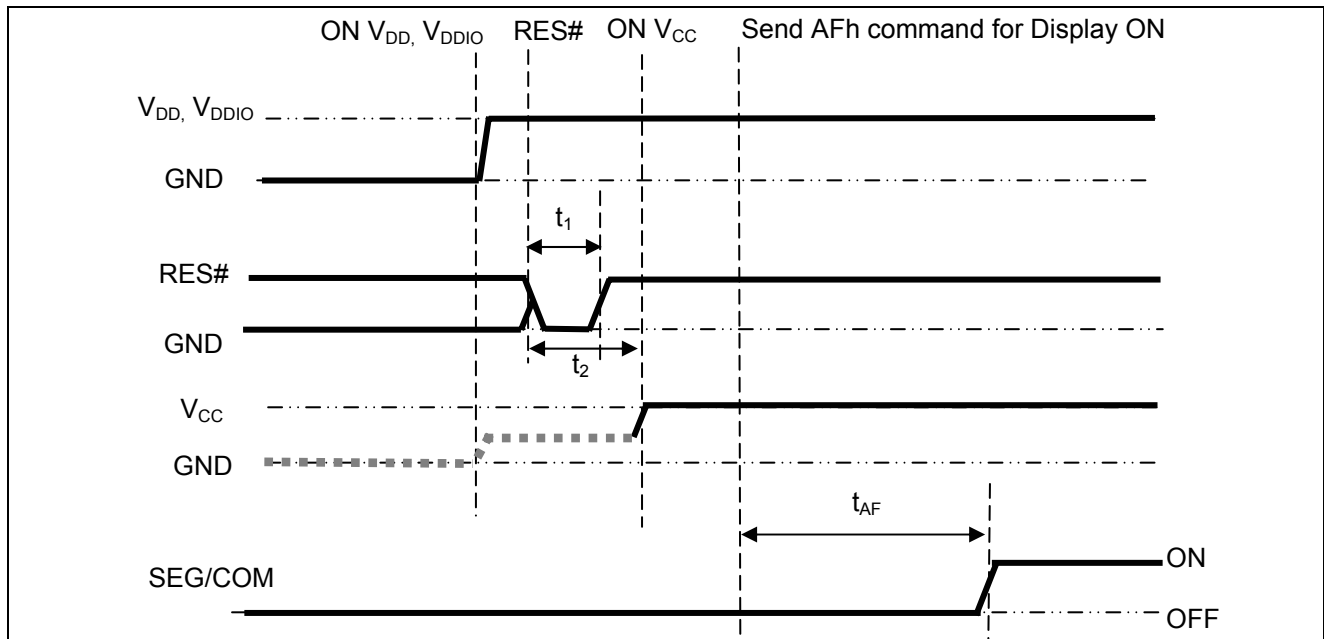
7.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1331 (assume V_{DD} and V_{DDIO} are at the same voltage level).

Power ON sequence:

1. Power ON V_{DD} , V_{DDIO} .
2. After V_{DD} , V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3 μ s (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3 μ s (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

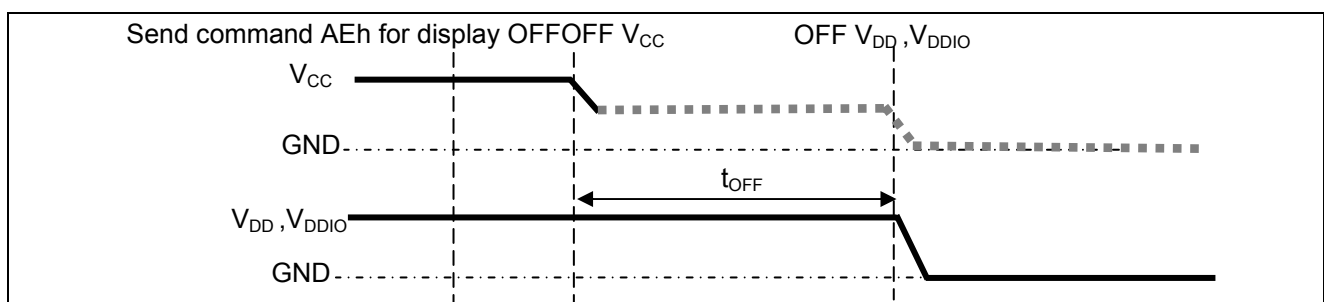
Figure 19 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2)}
3. Wait for t_{OFF} . Power OFF V_{DD} , V_{DDIO} . (where Minimum t_{OFF} =0ms, Typical t_{OFF} =100ms)

Figure 20 : The Power OFF sequence



Note:

⁽¹⁾ Since an ESD protection circuit is connected between V_{DD} , V_{DDIO} and V_{CC} , V_{CC} becomes lower than V_{DD} whenever V_{DD} , V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 19 and Figure 20 .

⁽²⁾ V_{CC} should be kept float when it is OFF.

8 COMMAND TABLE

Table 10 - Command Table

Fundamental Commands											Command	Description	Default
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0				
0 0 0	15 A[6:0] B[6:0]	0 * *	0 A ₆ B ₆	0 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀		Set Column Address	Setup Column start and end address A[6:0] start address from 00d-95d B[6:0] end address from 00d-95d	00d (00h) 95d (5Fh)
0 0 0	75 A[5:0] B[5:0]	0 * *	1 * *	1 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀		Set Row Address	Setup Row start and end address A[5:0] start address from 00d-63d B[5:0] end address from 00d-63d	00d (00h) 63d (3Fh)
0 0	81 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀		Set Contrast for Color "A"	Set contrast for all color "A" segment (Pins:SA0 – SA95) A[7:0] valid range: 00d to 255d	128d (80h)
0 0	82 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀		Set Contrast for Color "B"	Set contrast for all color "B" segment (Pins:SB0 – SB95). A[7:0] valid range: 00d to 255d	128d (80h)
0 0	83 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀		Set Contrast for Color "C"	Set contrast for all color "C" segment (Pins:SC0 – SC95). A[7:0] valid range: 00d to 255d	128d (80h)
0 0	87 A[3:0]	1 0	0 0	0 0	0 0	0 A ₃	1 A ₂	1 A ₁	1 A ₀		Master Current Control	Set master current attenuation factor A[3:0] from 00d to 15d corresponding to 1/16, 2/16... to 16/16 attenuation.	15d (0Fh)

Fundamental Commands																				
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	Default								
0 0 0 0 0 0	8A A[7:0] 8B A[7:0] 8C A[7:0]	1 A ₇ 1 A ₇ 1 A ₇	0 A ₆ 0 A ₆ 0 A ₆	0 A ₅ 0 A ₅ 0 A ₅	0 A ₄ 0 A ₄ 0 A ₄	1 A ₃ 1 A ₃ 1 A ₃	0 A ₂ 0 A ₂ 1 A ₂	1 A ₁ 1 A ₁ 1 A ₁	0 A ₀ 1 A ₀ 0 A ₀	Set Second Pre-charge Speed for Color "A", "B" and "C"	<p>A[7:0]: Set Second Pre-charge Speed Ranges: 0000000b to 1111111b, a higher value of A[7:0] gives a higher Second Pre-charge speed.</p> <p>Note (1) The default values of A[7:0] in 8Ah, A[7:0] in 8Bh and A[7:0] in 8Ch are equal to the contrast values for color A, B and C (refer to commands: 81h, 82h, 83h) respectively. (2) All six bytes (8Ah A[7:0], 8Bh A[7:0] and 8Ch A[7:0]) must be inputted together. For example: the original value is like that</p> <table border="1"> <thead> <tr> <th colspan="2">Original value</th> </tr> </thead> <tbody> <tr> <td>8Ah A[7:0]:</td> <td>80h</td> </tr> <tr> <td>8Bh A[7:0]:</td> <td>80h</td> </tr> <tr> <td>8Ch A[7:0]:</td> <td>80h</td> </tr> </tbody> </table> <p>If it is wanted to change the value of 8Bh A[7:0] to 75h, then all the following 6 bytes must be inputted: 8Ah, 80h, 8Bh, 75h, 8Ch, 80h.</p>	Original value		8Ah A[7:0]:	80h	8Bh A[7:0]:	80h	8Ch A[7:0]:	80h	A[7:0] of 81h A[7:0] of 82h A[7:0] of 83h
Original value																				
8Ah A[7:0]:	80h																			
8Bh A[7:0]:	80h																			
8Ch A[7:0]:	80h																			
0 0	A0 A[7:0]	1 A ₇	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	0 A ₀	Remap & Color Depth setting	<p>Set driver remap and color depth A[0]=0, Horizontal address increment A[0]=1, Vertical address increment</p> <p>A[1]=0, RAM Column 0 to 95 maps to Pin Seg (SA,SB,SC) 0 to 95 A[1]=1, RAM Column 0 to 95 maps to Pin Seg (SA,SB,SC) 95 to 0</p> <p>A[2]=0, normal order SA,SB,SC (e.g. RGB) A[2]=1, reverse order SC,SB,SA (e.g. BGR)</p> <p>A[3]=0, Disable left-right swapping on COM A[3]=1, Set left-right swapping on COM</p> <p>A[4]=0, Scan from COM 0 to COM [N -1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the multiplex ratio.</p> <p>A[5]=0, Disable COM Split Odd Even (RESET) A[5]=1, Enable COM Split Odd Even</p> <p>A[7:6] = 00; 256 color format A[7:6] = 01; 65k color format A[7:6] = 10; 65k color format 2 If 9 / 18 bit mode is selected, color depth will be fixed to 65k regardless of the setting.</p>	A[0]=0 A[1]=0 A[2]=0 A[3]=0 A[4]=0 A[5]=0 A[7:6]=01								
0 0	A1 A[5:0]	1 0	0 0	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Display Start Line	Set display start line register by Row A[5:0]: from 00d to 63d	00d (00h)								
0 0	A2 A[5:0]	1 0	0 0	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Display Offset	Set vertical offset by Com A[5:0]: from 00d to 63d	00d (00h)								

Fundamental Commands												
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	Default
0 0 0 0	A4 / A5 / A6 / A7 /	1 0 1 0	0 1 0 1	1 0 0 0	0 0 1 1	0 1 0 0	1 0 0 1	X ₁ A ₁	X ₀ A ₀	Set Display Mode	A4h=Normal Display A5h=Entire Display On, all pixels turn on at GS63 A6h=Entire Display Off, all pixels turn off A7h=Inverse Display	A4h
0 0	A8 A[5:0]	1 0	0 0	1 A ₅	0 A ₄	1 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Multiplex Ratio	Set MUX ratio to N+1 Mux N = A[5:0] from 15d to 63d A[5:0] from 00d to 14d are invalid entry	63d (3Fh)
0 0 0 0 0 0	AB A[7:0] B[7:0] C[7:0] D[7:0] E[4:0]	1 A ₇ B ₇ C ₇ D ₇ 0	0 A ₆ B ₆ C ₆ D ₆ 0	1 A ₅ B ₅ C ₅ D ₅ 0	0 A ₄ B ₄ C ₄ D ₄ E ₄	1 A ₃ B ₃ C ₃ D ₃ E ₃	0 A ₂ B ₂ C ₂ D ₂ E ₂	1 A ₁ B ₁ C ₁ D ₁ E ₁	1 A ₀ B ₀ C ₀ D ₀ E ₀	Dim Mode Setting	Configure dim mode setting A[7:0] = Reserved. (Set as 00h) B[7:0] = Contrast setting for Color A, valid range 0 to 255d. C[7:0] = Contrast setting for Color B, valid range 0 to 255d. D[7:0] = Contrast setting for Color C, valid range 0 to 255d. E[4:0] = Precharge voltage setting, valid range 0 to 31d.	\
0 0	AD A[0]	1 1	0 0	1 0	0 0	1 1	1 1	0 1	1 A ₀	Set Master Configuration	A[0]=0b, Select external V _{CC} supply A[0]=1b, Reserved (RESET) Note (1) Bit A[0] must be set to 0b after RESET. (2) The setting will be activated after issuing Set Display ON command (AFh)	A[0] = 1
0	AC AE AF	1	0	1	0	1	1	A ₁	A ₀	Set Display On/Off	ACh = Display ON in dim mode AEh = Display off (sleep mode) AFh = Display on in normal mode	AEh
0 0	B0 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	0 A ₀	Power Save Mode	A[7:0]=1Ah, Enable Power save mode (RESET) A[7:0]=0Bh, Disable Power save mode	1Ah
0 0	B1 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Phase 1 and 2 period adjustment	A[3:0] Phase 1 period in N DCLK. 1~15 DCLK allowed. A[7:4] Phase 2 period in N DCLK. 1~15 DCLK allowed	74h
0 0	B3 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Display Clock Divider / Oscillator Frequency	A[3:0]: Define the divide ratio (D) of the display clocks (DCLK): Divide ratio (D) = A[3:0] + 1 (i.e., 1 to 16) A[7:4] Fosc frequency. Frequency increases as setting value increases	D0h

Fundamental Commands													
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	Default	
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	These 32 parameters define pulse widths of GS1 to GS63 in terms of DCLK A[6:0]: Pulse width for GS1, RESET=01d B[6:0]: Pulse width for GS3, RESET=05d C[6:0]: Pulse width for GS5, RESET=09d ... AE[6:0]: Pulse width for GS61, RESET=121d AF[6:0]: Pulse width for GS63, RESET=125d Note: (1) GS0 has no pre-charge and current drive stages. (2) GS2, GS4...GS62 are derived by $P_n = (P_{n-1} + P_{n+1})/2$ (3) P_n will be truncated to integer if it is with decimal point. (4) P_{n+1} should always be set to larger than P_{n-1} (5) Max pulse width is 125	\	
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀				
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀				
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀				
0				
0	AE[6:0]	*	AE ₆	AE ₅	AE ₄	AE ₃	AE ₂	AE ₁	AE ₀				
0	AF[6:0]	*	AF ₆	AF ₅	AF ₄	AF ₃	AF ₂	AF ₁	AF ₀				
0	B9	1	0	1	1	1	0	0	1	Enable Linear Gray Scale Table	Reset built in gray scale table (Linear) Pulse width for GS1 = 1d; Pulse width for GS2 = 3d; Pulse width for GS3 = 5d; ... Pulse width for GS61 = 121d; Pulse width for GS62 = 123d; Pulse width for GS63 = 125d.	\	
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge level	Set pre-charge voltage level. All three color share the same pre-charge voltage.	3Eh	
0	A[5:0]	0	0	A ₅	A ₄	A ₃	A ₂	A ₁	0				
				A[5:1]	Hex code	pre-charge voltage							
				00000	00h	0.10 x V _{CC}							
				:	:	:							
				11111	3Eh	0.50 x V _{CC}							
											Refer to Figure 31 for the details setting of A[5:1].		
0	BC-BD	1	0	1	1	1	1	0	X ₀	NOP	Command for No operation	\	
0	BE	1	0	1	1	1	1	1	0	Set V _{COMH}	Set COM deselect voltage level (V _{COMH})	3Eh	
0	A[5:1]	0	0	A ₅	A ₄	A ₃	A ₂	A ₁	0				
				A[5:1]	Hex code	V_{COMH}							
				00000	00h	0.44 x V _{CC}							
				01000	10h	0.52 x V _{CC}							
				10000	20h	0.61 x V _{CC}							
				11000	30h	0.71 x V _{CC}							
				11111	3Eh	0.83 x V _{CC}							
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No operation	\	
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command	12h	
0	A[2]	0	0	0	1	0	A ₂	1	0				
											Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.		

Graphic Acceleration Commands											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	21	0	0	1	0	0	0	0	1	Draw Line	A[6:0]: Column Address of Start B[5:0]: Row Address of Start C[6:0]: Column Address of End D[5:0]: Row Address of End E[5:1]: Color C of the line F[5:0]: Color B of the line G[5:1]: Color A of the line
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	D[5:0]	*	*	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	E[5:1]	*	*	E ₅	E ₄	E ₃	E ₂	E ₁	*		
0	F[5:0]	*	*	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		
0	G[5:1]	*	*	G ₅	G ₄	G ₃	G ₂	G ₁	*		
0	22	0	0	1	0	0	0	1	0	Drawing Rectangle	A[6:0]: Column Address of Start B[5:0]: Row Address of Start C[6:0]: Column Address of End D[5:0]: Row Address of End E[5:1]: Color C of the line F[5:0]: Color B of the line G[5:1]: Color A of the line H[5:1]: Color C of the fill area I[5:0]: Color B of the fill area J[5:1]: Color A of the fill area
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	D[5:0]	*	*	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	E[5:1]	*	*	E ₅	E ₄	E ₃	E ₂	E ₁	*		
0	F[5:0]	*	*	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		
0	G[5:1]	*	*	G ₅	G ₄	G ₃	G ₂	G ₁	*		
0	H[5:1]	*	*	H ₅	H ₄	H ₃	H ₂	H ₁	*		
0	I[5:0]	*	*	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
0	J[5:1]	*	*	J ₅	J ₄	J ₃	J ₂	J ₁	*		
0	23	0	0	1	0	0	0	1	1	Copy	A[6:0]: Column Address of Start B[5:0]: Row Address of Start C[6:0]: Column Address of End D[5:0]: Row Address of End E[6:0]: Column Address of New Start F[5:0]: Row Address of New Start
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	D[5:0]	*	*	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	E[6:0]	*	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		
0	F[5:0]	*	*	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		
0	24	0	0	1	0	0	1	0	0	Dim Window	A[6:0]: Column Address of Start B[5:0]: Row Address of Start C[6:0]: Column Address of End D[5:0]: Row Address of End The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	D[5:0]	*	*	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	25	0	0	1	0	0	1	0	1	Clear Window	A[6:0]: Column Address of Start B[5:0]: Row Address of Start C[6:0]: Column Address of End D[5:0]: Row Address of End
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	D[5:0]	*	*	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	26	0	0	1	0	0	1	1	0	Fill Enable / Disable	A0 0 : Disable Fill for Draw Rectangle Command (RESET) 1 : Enable Fill for Draw Rectangle Command A[3:1] 000: Reserved values A4 0 : Disable reverse copy (RESET) 1 : Enable reverse during copy command.
0	A[4:0]	*	*	*	A ₄	0	0	0	A ₀		

Graphic Acceleration Commands											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	27	0	0	1	0	0	1	1	1	Continuous Horizontal & Vertical Scrolling Setup	A[6:0]: Set number of column as horizontal scroll offset Range: 0d-95d (no horizontal scroll if equals to 0)
0	A[6:0]	*	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B[5:0]: Define start row address
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		C[6:0]: Set number of rows to be horizontal scrolled B[5:0]+C[6:0] <=64
0	C[6:0]	*	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		D[5:0]: Set number of row as vertical scroll offset Range: 0d-63d (no vertical scroll if equals to 0)
0	D[5:0]	*	*	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		E[1:0]: Set time interval between each scroll step 00b 6 frames 01b 10 frames 10b 100 frames 11b 200 frames
0	E[1:0]	*	*	*	*	*	*	E ₁	E ₀		Note: (1) Vertical scroll is run with 64MUX setting only (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Deactivate scrolling	This command deactivates the scrolling action. Note (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scrolling	This command activates the scrolling function according to the setting done by Continuous Horizontal & Vertical Scrolling Setup command 27h.

8.1 Data Read / Write

To read data from the GDDRAM, input HIGH to R/W#(WR#) pin and D/C# pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read.

To write data to the GDDRAM, input LOW to R/W#(WR#) pin and HIGH to D/C# pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

Table 11 - Address increment table (Automatic)

D/C#	R/W#(WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

9 COMMAND DESCRIPTIONS

9.1 Fundamental Command

9.1.1 Set Column Address (15h)

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

9.1.2 Set Row Address (75h)

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The figure below shows the way of column and row address pointer movement through the example: column start address is set to 2 and column end address is set to 93, row start address is set to 1 and row end address is set to 62. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 93 and from row 1 to row 62 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 21*). Whenever the column address pointer finishes accessing the end column 93, it is reset back to column 2 and row address is automatically increased by 1 (*solid line in Figure 21*). While the end row 62 and end column 93 RAM location is accessed, the row address is reset back to 1 (*dotted line in Figure 21*).

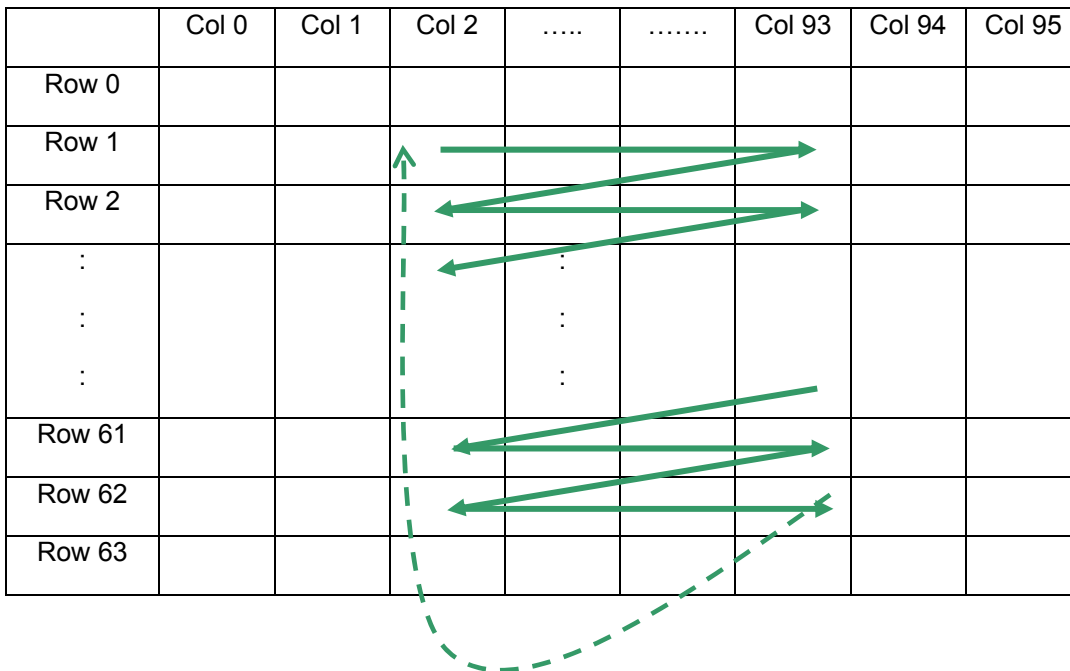


Figure 21 - Example of Column and Row Address Pointer Movement

9.1.3 Set Contrast for Color A, B, C (81h, 82h, 83h)

This command is to set Contrast Setting of each color A, B and C. The chip has three contrast control circuits for color A, B and C. Each contrast circuit has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter of the color. This relation is shown in Figure 22.

9.1.4 Master Current Control (87h)

This command is to control the segment output current by a scaling factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000b] to 16 [1111b]. RESET is 16 [1111b]. The smaller the master current value, the dimmer the OLED panel display is set. For example, if original segment output current of a color is 160uA at scale factor = 16, setting scale factor to 8 to reduce the current to 80uA. Please see Figure 22.

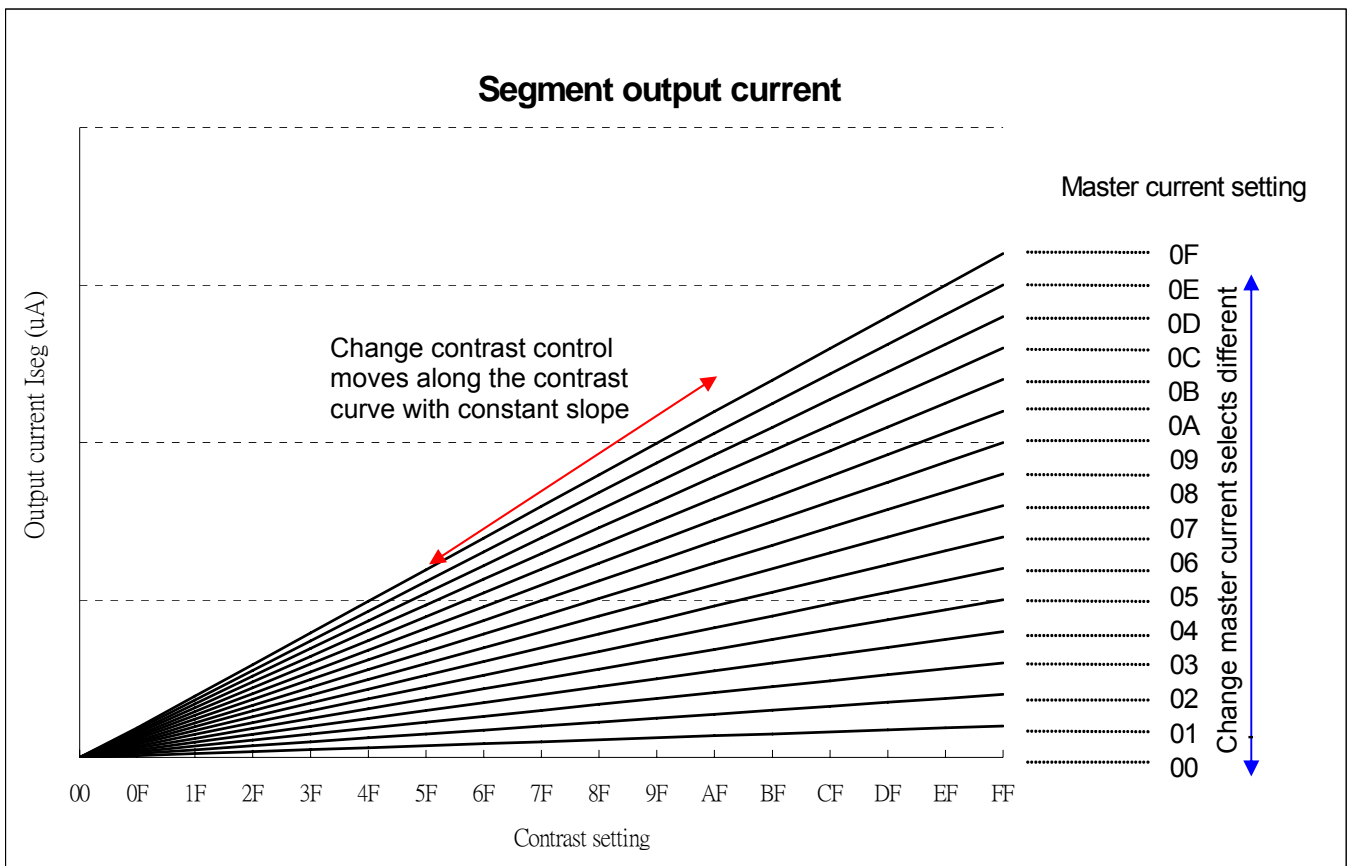
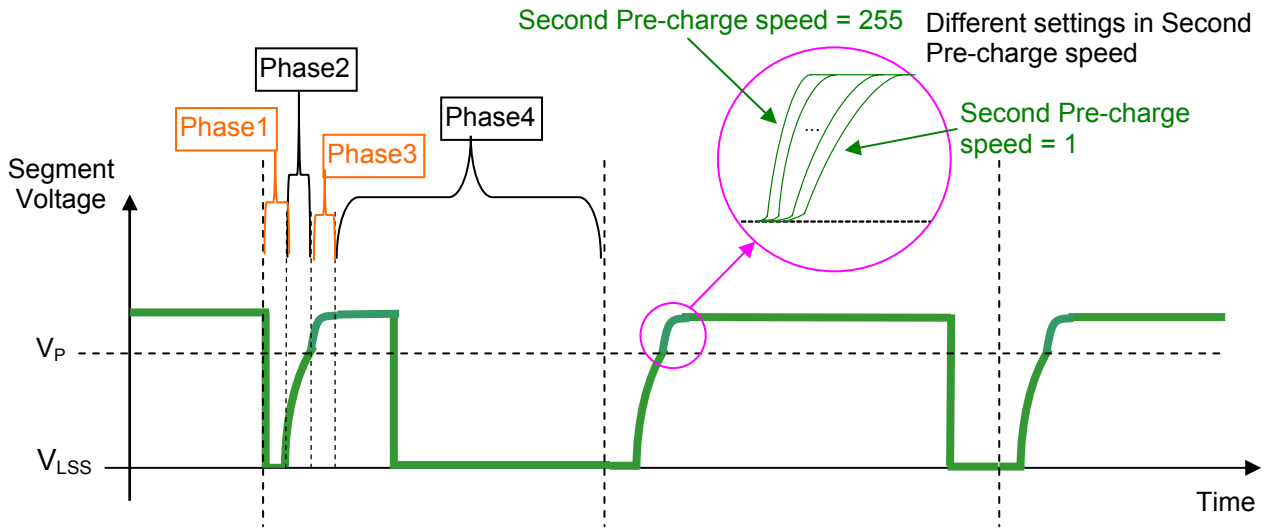


Figure 22 - Segment Output Current for Different Contrast Control and Master Current Setting

9.1.5 Set Second Pre-charge Speed for Color A, B, C (8Ah)

The value set should match with the contrast of the color A, B, C. An initial trial should be the value same as the contrast A, B, C. When faster speed is needed, higher value can be set and vice versa. Figure 23 shows the effect of setting second pre-charge under different speeds through using command 8Ah, 8Bh and 8Ch.

Figure 23 - Effect of setting the second pre-charge under different speeds



9.1.6 Set Re-map & Data Format (A0h)

This command has multiple configurations and each bit setting is described as follows.

- Address increment mode (A[0])
When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address pointer for horizontal address increment mode is shown in Figure 24.

Figure 24 - Address Pointer Movement of Horizontal Address Increment Mode

	Col 0	Col 1	Col 94	Col 95
Row 0	→				
Row 1	←				
:	:	:	:	:	:
Row 62	←				
Row 63	←				

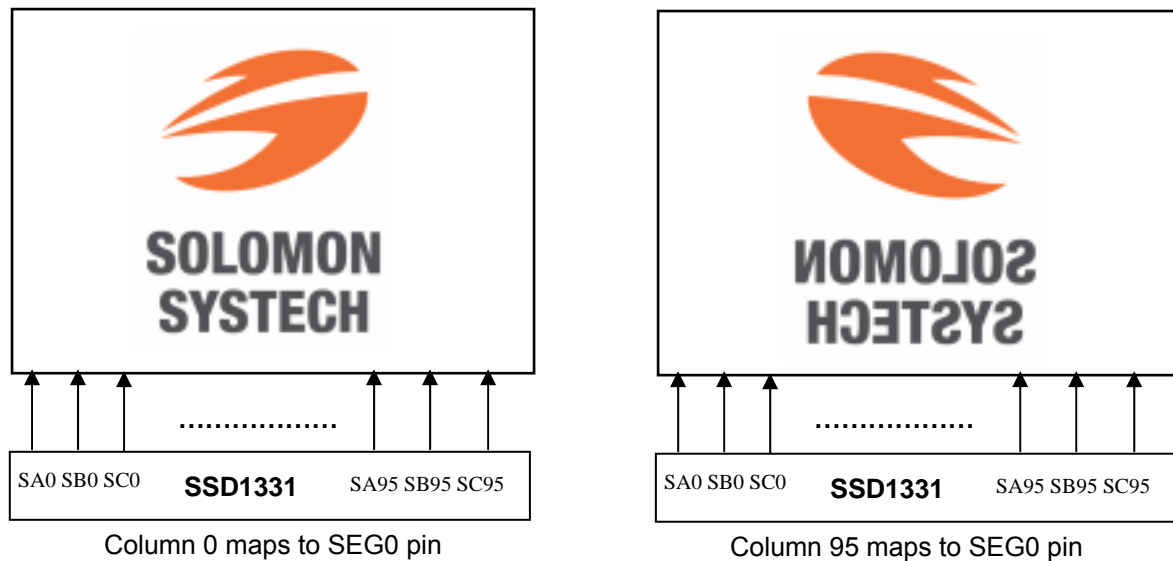
When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address pointer for vertical address increment mode is shown in Figure 25.

Figure 25 - Address Pointer Movement of Vertical Address Increment Mode

	Col 0	Col 1	Col 94	Col 95
Row 0	↓	↗	↗	↗	↗
Row 1	↓	↗	↗	↗	↗
:	:	:	:	:	:
Row 62	↓	↗	↗	↗	↗
Row 63	↓	↗	↗	↗	↗

- **Column Address Mapping (A[1])**
This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa. The display direction is either mapping display data RAM column 0 to SEG0 pin (A[1] = 0), or mapping display data RAM column 95 to SEG0 pin (A[1] = 1). The effects of both are shown in Figure 26.

Figure 26 - Example of Column Address Mapping

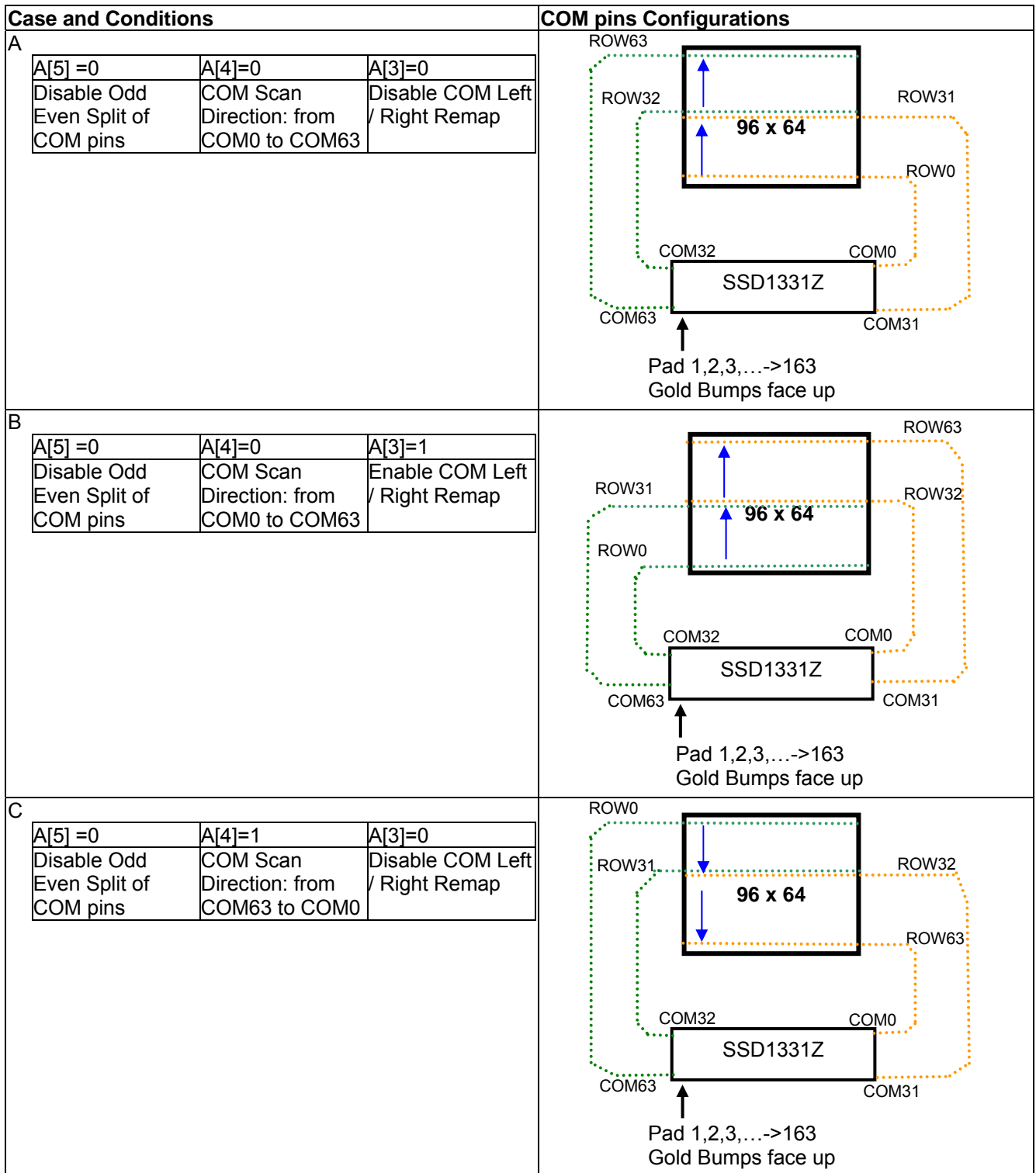


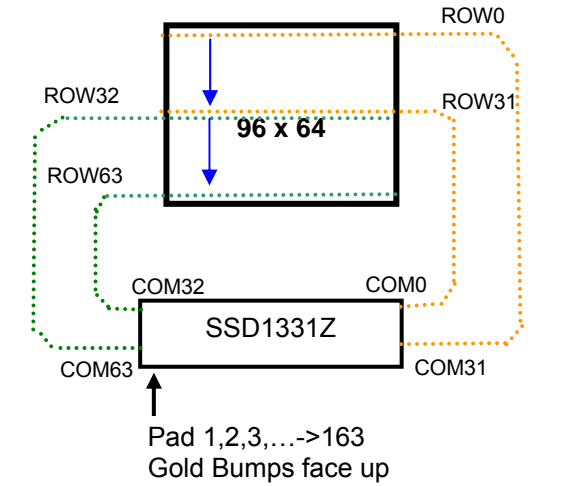
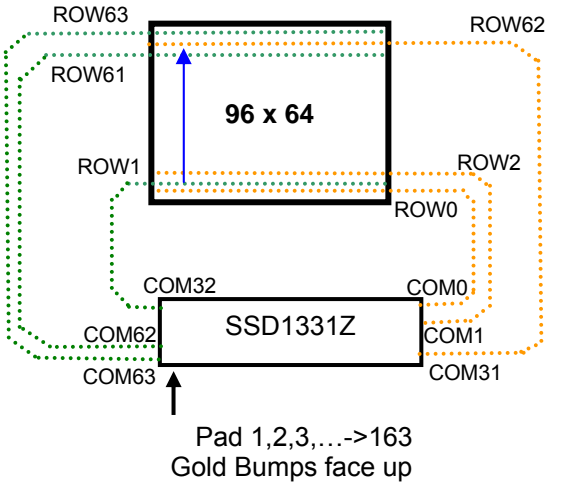
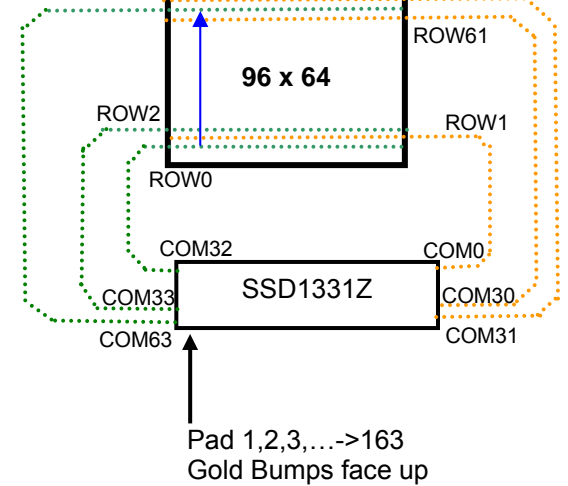
- **RGB Mapping (A[2])**
This command bit is made for flexible layout of segment signals in OLED module to match filter design.
- **COM Left / Right Remap (A[3])**
This command bit is made for flexible layout of common signals in OLED module with COM0 arranged on either left or right side. Details of pin arrangement can be found in Table 12 and Figure 27.
- **COM Scan Direction Remap (A[4])**
This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa. Details of pin arrangement can be found in Table 12 and Figure 27.
- **Odd Even Split of COM pins (A[5])**
This bit can set the odd even arrangement of COM pins.
A[5] = 0: Disable COM split odd even, pin assignment of common is in sequential as
COM63 COM62 COM 33 COM32..SC95..SA0..COM0 COM1.... COM30 COM31
A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
COM63 COM61.... COM3 COM1..SC95..SA0..COM0 COM2.... COM60 COM62
Details of pin arrangement can be found in Table 12 and Figure 27.
- **Display color mode (A[7:6])**
Select either 65k or 256 color mode. The display RAM data format in different mode is described in section 7.5

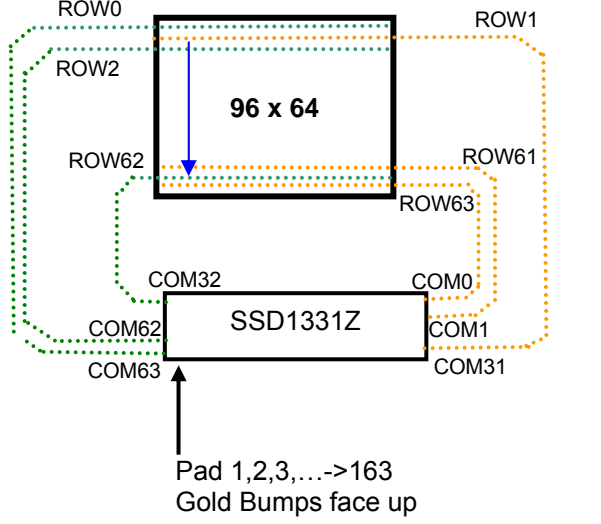
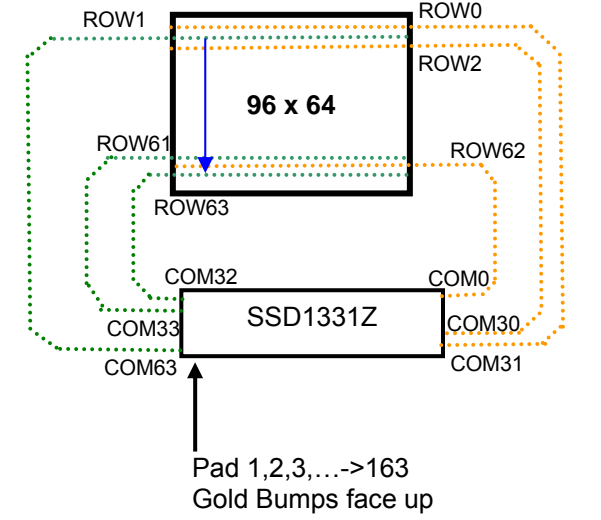
Table 12 - Illustration of different COM output settings

		Case A	Case B	Case C	Case D	Case E	Case F	Case G	Case H
		A[5:3]=000	A[5:3]=001	A[5:3]=010	A[5:3]=011	A[5:3]=100	A[5:3]=101	A[5:3]=110	A[5:3]=111
IC Pad no.	Pin name	Output signal							
195	COM0	Row0	Row32	Row63	Row31	Row0	Row1	Row63	Row62
194	COM1	Row1	Row33	Row62	Row30	Row2	Row3	Row61	Row60
193	COM2	Row2	Row34	Row61	Row29	Row4	Row5	Row59	Row58
192	COM3	Row3	Row35	Row60	Row28	Row6	Row7	Row57	Row56
191	COM4	Row4	Row36	Row59	Row27	Row8	Row9	Row55	Row54
190	COM5	Row5	Row37	Row58	Row26	Row10	Row11	Row53	Row52
...
169	COM26	Row26	Row58	Row37	Row5	Row52	Row53	Row11	Row10
168	COM27	Row27	Row59	Row36	Row4	Row54	Row55	Row9	Row8
167	COM28	Row28	Row60	Row35	Row3	Row56	Row57	Row7	Row6
166	COM29	Row29	Row61	Row34	Row2	Row58	Row59	Row5	Row4
165	COM30	Row30	Row62	Row33	Row1	Row60	Row61	Row3	Row2
164	COM31	Row31	Row63	Row32	Row0	Row62	Row63	Row1	Row0
488	COM32	Row32	Row0	Row31	Row63	Row1	Row0	Row62	Row63
489	COM33	Row33	Row1	Row30	Row62	Row3	Row2	Row60	Row61
490	COM34	Row34	Row2	Row29	Row61	Row5	Row4	Row58	Row59
491	COM35	Row35	Row3	Row28	Row60	Row7	Row6	Row56	Row57
492	COM36	Row36	Row4	Row27	Row59	Row9	Row8	Row54	Row55
493	COM37	Row37	Row5	Row26	Row58	Row11	Row10	Row52	Row53
...
514	COM58	Row58	Row26	Row5	Row37	Row53	Row52	Row10	Row11
515	COM59	Row59	Row27	Row4	Row36	Row55	Row54	Row8	Row9
516	COM60	Row60	Row28	Row3	Row35	Row57	Row56	Row6	Row7
517	COM61	Row61	Row29	Row2	Row34	Row59	Row58	Row4	Row5
518	COM62	Row62	Row30	Row1	Row33	Row61	Row60	Row2	Row3
519	COM63	Row63	Row31	Row0	Row32	Row63	Row62	Row0	Row1

Figure 27 - COM Pins Hardware Configuration (MUX ratio: 64)



Case and Conditions	COM pins Configurations						
<p>D</p> <table border="1" data-bbox="172 170 823 297"> <tr> <td>A[5] =0</td> <td>A[4]=1</td> <td>A[3]=1</td> </tr> <tr> <td>Disable Odd Even Split of COM pins</td> <td>COM Scan Direction: from COM63 to COM0</td> <td>Enable COM Left / Right Remap</td> </tr> </table>	A[5] =0	A[4]=1	A[3]=1	Disable Odd Even Split of COM pins	COM Scan Direction: from COM63 to COM0	Enable COM Left / Right Remap	
A[5] =0	A[4]=1	A[3]=1					
Disable Odd Even Split of COM pins	COM Scan Direction: from COM63 to COM0	Enable COM Left / Right Remap					
<p>E</p> <table border="1" data-bbox="172 669 823 797"> <tr> <td>A[5] =1</td> <td>A[4]=0</td> <td>A[3]=0</td> </tr> <tr> <td>Enable Odd Even Split of COM pins</td> <td>COM Scan Direction: from COM0 to COM63</td> <td>Disable COM Left / Right Remap</td> </tr> </table>	A[5] =1	A[4]=0	A[3]=0	Enable Odd Even Split of COM pins	COM Scan Direction: from COM0 to COM63	Disable COM Left / Right Remap	
A[5] =1	A[4]=0	A[3]=0					
Enable Odd Even Split of COM pins	COM Scan Direction: from COM0 to COM63	Disable COM Left / Right Remap					
<p>F</p> <table border="1" data-bbox="172 1191 823 1319"> <tr> <td>A[5] =1</td> <td>A[4]=0</td> <td>A[3]=1</td> </tr> <tr> <td>Enable Odd Even Split of COM pins</td> <td>COM Scan Direction: from COM0 to COM63</td> <td>Enable COM Left / Right Remap</td> </tr> </table>	A[5] =1	A[4]=0	A[3]=1	Enable Odd Even Split of COM pins	COM Scan Direction: from COM0 to COM63	Enable COM Left / Right Remap	
A[5] =1	A[4]=0	A[3]=1					
Enable Odd Even Split of COM pins	COM Scan Direction: from COM0 to COM63	Enable COM Left / Right Remap					

Case and Conditions	COM pins Configurations						
<p>G</p> <table border="1" data-bbox="172 174 821 297"> <tr> <td>A[5] =1</td> <td>A[4]=1</td> <td>A[3]=0</td> </tr> <tr> <td>Enable Odd Even Split of COM pins</td> <td>COM Scan Direction: from COM63 to COM0</td> <td>Disable COM Left / Right Remap</td> </tr> </table>	A[5] =1	A[4]=1	A[3]=0	Enable Odd Even Split of COM pins	COM Scan Direction: from COM63 to COM0	Disable COM Left / Right Remap	
A[5] =1	A[4]=1	A[3]=0					
Enable Odd Even Split of COM pins	COM Scan Direction: from COM63 to COM0	Disable COM Left / Right Remap					
<p>H</p> <table border="1" data-bbox="172 703 821 826"> <tr> <td>A[5] =1</td> <td>A[4]=1</td> <td>A[3]=1</td> </tr> <tr> <td>Enable Odd Even Split of COM pins</td> <td>COM Scan Direction: from COM63 to COM0</td> <td>Enable COM Left / Right Remap</td> </tr> </table>	A[5] =1	A[4]=1	A[3]=1	Enable Odd Even Split of COM pins	COM Scan Direction: from COM63 to COM0	Enable COM Left / Right Remap	
A[5] =1	A[4]=1	A[3]=1					
Enable Odd Even Split of COM pins	COM Scan Direction: from COM63 to COM0	Enable COM Left / Right Remap					

9.1.7 Set Display Start Line (A1h)

This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. Table 13 and Table 14 show examples of this command. In there, “Row” means the graphic display data RAM row.

9.1.8 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-63. For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second command should be given by 0010000b. Table 13 and Table 14 show examples of this command. In there, “Row” means the graphic display data RAM row.

9.1.9 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display On, Entire Display Off and Inverse Display.

- Normal Display (A4h)
Reset the above effect and turn the data to ON at the corresponding gray level.
- Set Entire Display On (A5h)
Forces the entire display to be at "GS63" regardless of the contents of the display data RAM.
- Set Entire Display Off (A6h)
Forces the entire display to be at gray level "GS0" regardless of the contents of the display data RAM.
- Inverse Display (A7h)
The gray level of display data are swapped such that "GS0" <-> "GS63", "GS1" <-> "GS62",

9.1.10 Set Multiplex Ratio (A8h)

This command switches default 1:64 multiplex mode to any multiplex mode from 16 to 64. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h.

9.1.11 Dim mode setting (ABh)

This command contains multiple bits to configure the dim mode display parameters. Contrast setting of color A, B, C and precharge voltage can be set different to normal mode (AFh).

9.1.12 Set Master Configuration (ADh)

This command selects the external V_{CC} power supply. External V_{CC} power should be connected to the V_{CC} pin. A[0] bit must be set to 0b after RESET.

This command will be activated after issuing Set Display ON command (AFh)

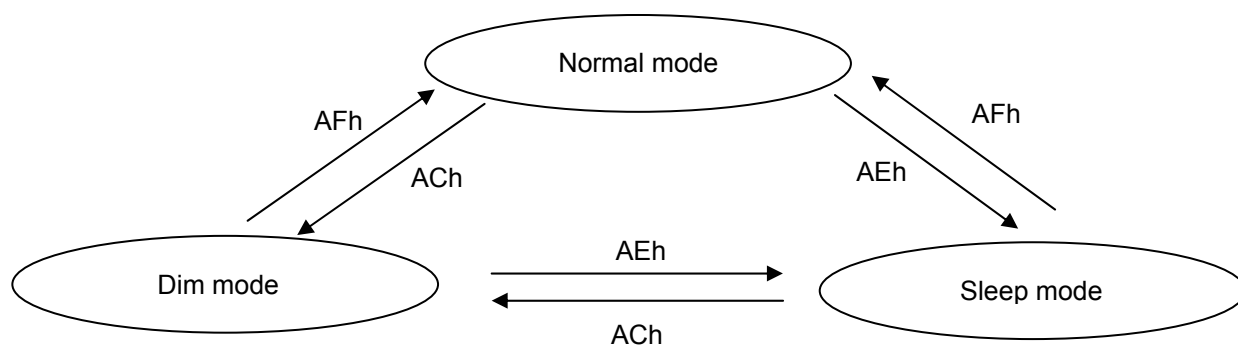
9.1.13 Set Display On/Off (ACh / AEh / AFh)

These single byte commands are used to turn the OLED panel display on or off. When the display is on, the selected circuits by Set Master Configuration command will be turned on. When the display is off, those circuits will be turned off and the segment and common output are in high impedance state.

These commands set the display to one of the three states:

- ACh : Dim Mode Display On
 - AEh : Display Off (sleep mode)
 - AFh : Normal Brightness Display On
- where the dim mode settings are controlled by command ABh.

Figure 28 – Transition between different modes



9.1.14 Power Save Mode (B0h)

This command is used in enabling or disabling the power save mode.

9.1.15 Phase 1 and 2 Period Adjustment (B1h)

This command sets the length of phase 1 and 2 of segment waveform of the driver.

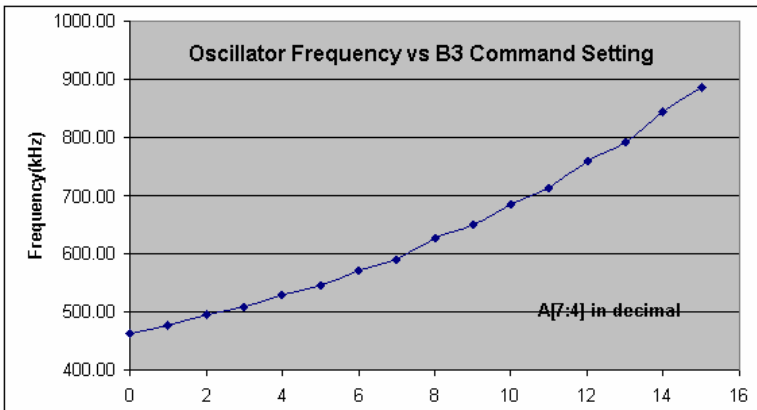
- Phase 1 (A[3:0]): Set the period from 1 to 15 in the unit of DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 1 to 15 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_p for color A, B and C.

9.1.16 Set Display Clock Divide Ratio/ Oscillator Frequency (B3h)

This command consists of two functions:

- Display Clock Divide Ratio (A[3:0])
Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with power on reset value = 1. Please refer to section 7.3.1 for the details relationship of DCLK and CLK.
- Oscillator Frequency (A[7:4])
Program the oscillator frequency F_{osc} that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1101b

Figure 29 - Typical Oscillator frequency adjustment by B3 command ($V_{DD} = 2.7V$)



9.1.17 Set Gray Scale Table (B8h)

This command is used to set the gray scale table for the display. Except gray scale entry 0, which is zero as it has no pre-charge and current drive, each odd entry gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter is the OLED pixel when it's turned on. Please refer to section 7.6 for more detailed explanation of relation of display data RAM, gray scale table and the pixel brightness.

Following the command B8h, the user has to set the pulse width for GS1, GS3, GS5, ..., GS59, GS61, and GS63 one by one in sequence and complies the following conditions.

$$GS1 > 0; GS3 > GS1 + 1; GS5 > GS3 + 1; \dots$$

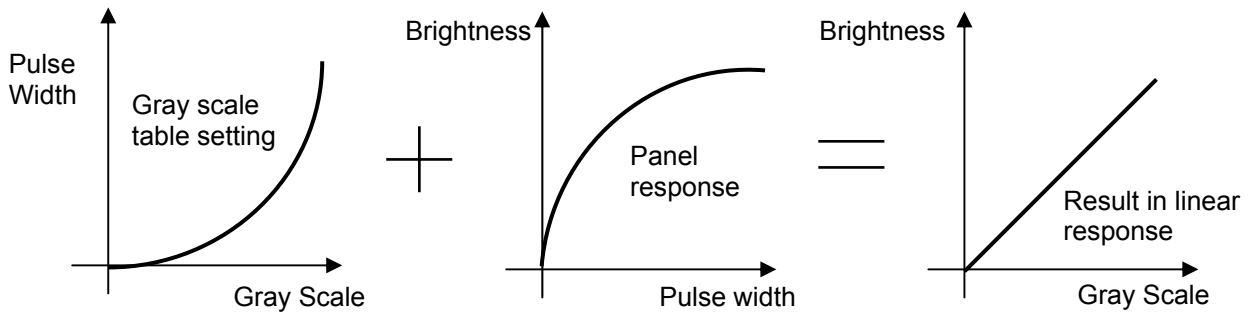
Afterwards, the driver automatically derives the pulse width of even entry of gray scale table GS2, GS4, ..., GS62 with the formula like below.

$$GS_n = (GS_{n-1} + GS_{n+1}) / 2$$

For example, if $GS1 = 3$ DCLKs and $GS3 = 7$ DCLKs, $GS2 = (3+7)/2 = 5$ DCLKs

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

Figure 30 - Example of gamma correction by gray scale table setting



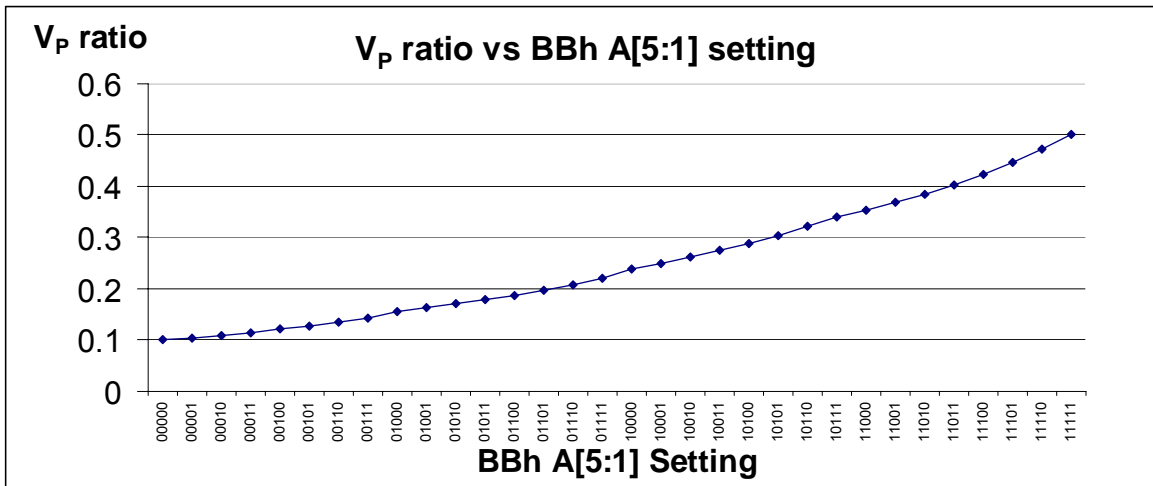
9.1.18 Enable Linear Gray Scale Table (B9h)

This command reloads the preset linear gray scale table as GS1 = 1, GS2 = 3, GS3 = 5, ..., GS62 = 123, GS63 = 125 DCLKs.

9.1.19 Set Pre-charge voltage (BBh)

This command sets the pre-charge voltage level of segment pins. The level of V_P is programmed with reference to V_{CC} . Figure 31 shows the details of setting Pre-charge voltage level by command BBh A[5:1].

Figure 31 – Typical Pre-charge voltage level setting by command BBh.



Note

⁽¹⁾ V_P ratio = 0.1 refers to V_P voltage = 0.1 x V_{CC} .

9.1.20 Set V_{COMH} Voltage (BEh)

This command sets the high voltage level of common pins. The level of V_{COMH} is programmed with reference to V_{CC} .

9.1.21 NOP (BCh, BDh, E3h)

These are command for no operation.

9.1.22 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the “Lock” state. And the driver IC will then respond to the command and memory access.

9.2 GRAPHIC ACCELERATION COMMAND SET DESCRIPTION

9.2.1 Draw Line (21h)

This command draws a line by the given start, end column and row coordinates and the color of the line.

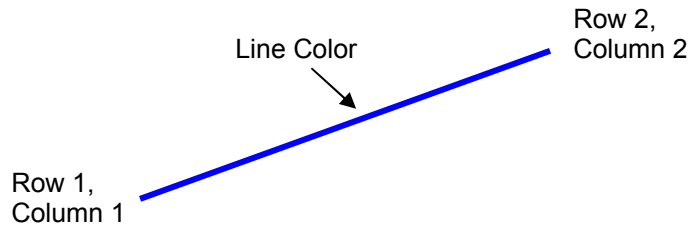


Figure 32 - Example of Draw Line Command

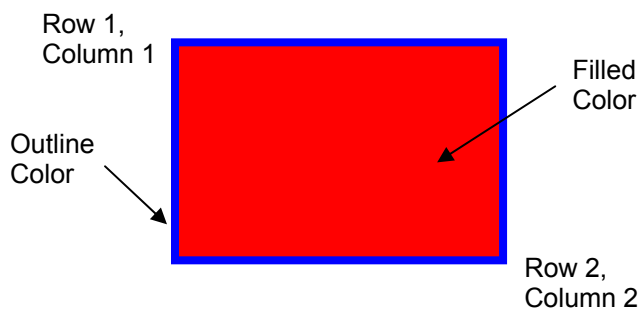
For example, the line above can be drawn by the following command sequence.

1. Enter into draw line mode by command 21h
2. Send column start address of line, column1, for example = 1h
3. Send row start address of line, row 1, for example = 10h
4. Send column end address of line, column 2, for example = 28h
5. Send row end address of line, row 2, for example = 4h
6. Send color C, B and A of line, for example = 35d, 0d, 0d for blue color

9.2.2 Draw Rectangle (22h)

Given the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2), specify the outline and fill area colors, a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.

Figure 33 - Example of Draw Rectangle Command



The following example illustrates the rectangle drawing command sequence.

1. Enter the "draw rectangle mode" by execute the command 22h
2. Set the starting column coordinates, Column 1. e.g., 03h.
3. Set the starting row coordinates, Row 1. e.g., 02h.
4. Set the finishing column coordinates, Column 2. e.g., 12h
5. Set the finishing row coordinates, Row 2. e.g., 15h
6. Set the outline color C, B and A. e.g., (28d, 0d, 0d) for blue color
7. Set the filled color C, B and A. e.g., (0d, 0d, 40d) for red color

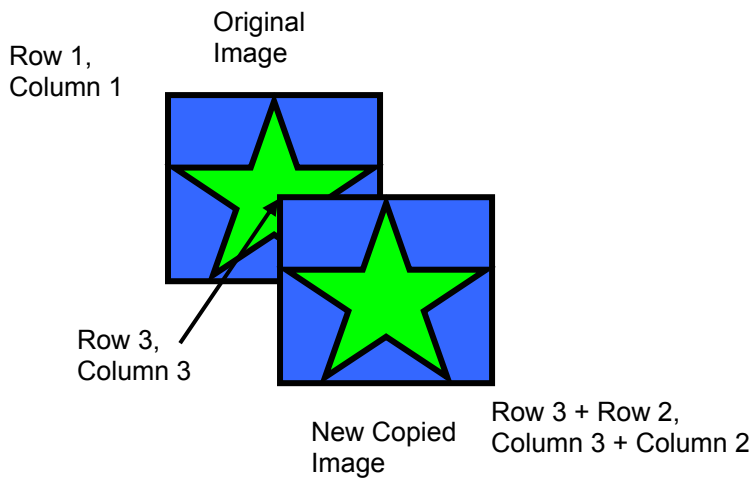
9.2.3 Copy (23h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

1. Enter the "copy mode" by execute the command 23h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 03h
7. Set the new row coordinates, Row 3. E.g., 03h

Figure 34 - Example of Copy Command



9.2.4 Dim Window (24h)

This command will dim the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2). After the execution of this command, the selected window area will become darker as follow.

Table 15 - Result of Change of Brightness by Dim Window Command

Original gray scale	New gray scale after dim window command
GS0 ~ GS15	No change
GS16 ~ GS19	GS4
GS20 ~ GS23	GS5
:	:
GS60 ~ GS63	GS15

Additional execution of this command over the same window area will not change the data content.

9.2.5 Clear Window (25h)

This command sets the window area specify by starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to clear the window display. The graphic display data RAM content of the specified window area will be set to zero.

This command can be combined with Copy command to make as a “move” result. The following example illustrates the copy plus clear procedure and results in moving the window object.

1. Enter the “copy mode” by execute the command 23h
2. Set the starting column coordinates, Column 1. E.g., 00h.
3. Set the starting row coordinates, Row 1. E.g., 00h.
4. Set the finishing column coordinates, Column 2. E.g., 05h
5. Set the finishing row coordinates, Row 2. E.g., 05h
6. Set the new column coordinates, Column 3. E.g., 06h
7. Set the new row coordinates, Row 3. E.g., 06h
8. Enter the “clear mode” by execute the command 25h
9. Set the starting column coordinates, Column 1. E.g., 00h.
10. Set the starting row coordinates, Row 1. E.g., 00h.
11. Set the finishing column coordinates, Column 2. E.g., 05h
12. Set the finishing row coordinates, Row 2. E.g., 05h

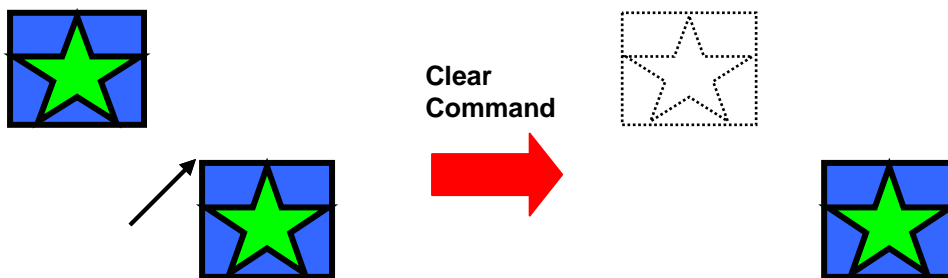


Figure 35 - Example of Copy + Clear = Move Command

9.2.6 Fill Enable/Disable (26h)

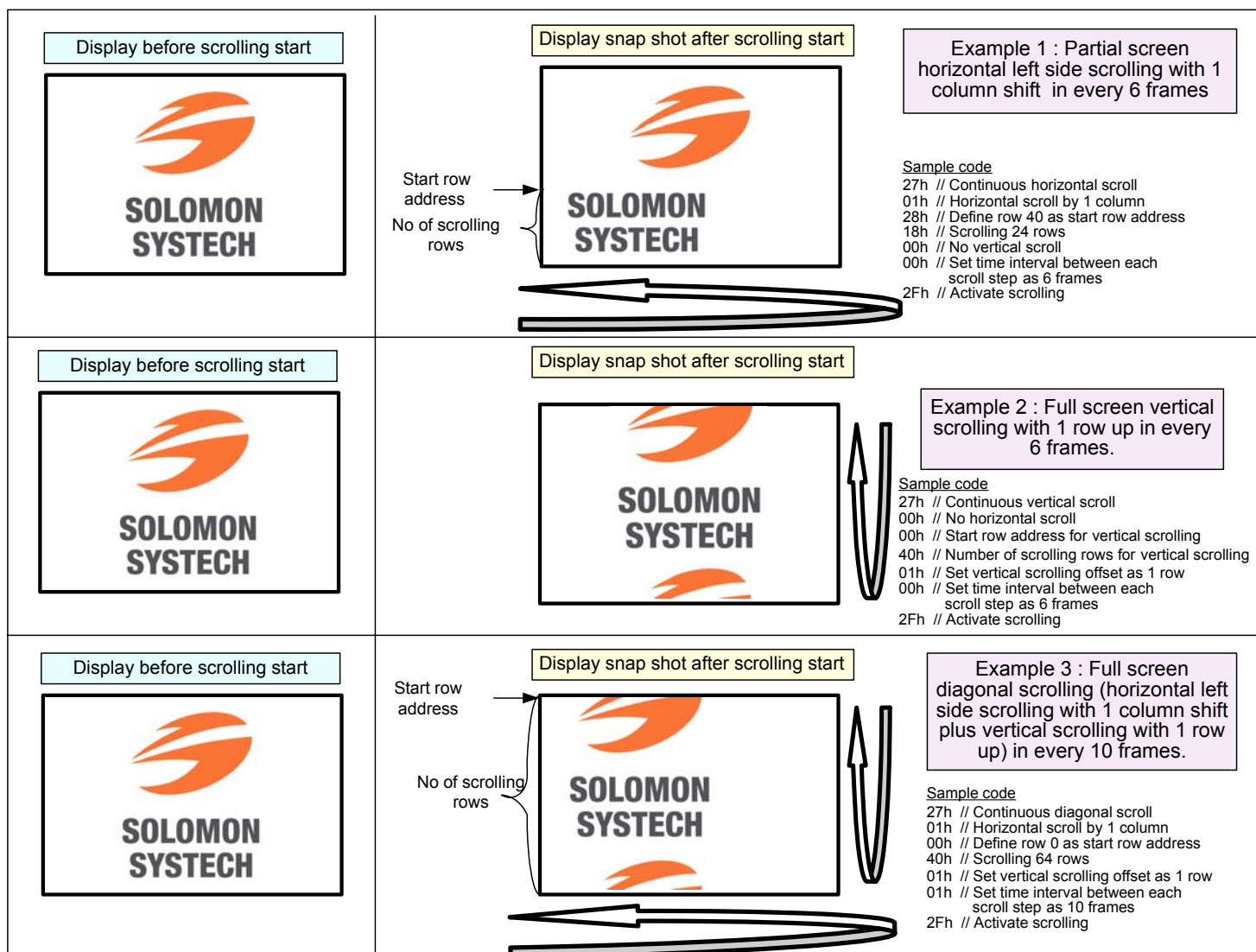
This command has two functions.

- Enable/Disable fill (A[0])
 - 0 = Disable filling of color into rectangle in draw rectangle command. (RESET)
 - 1 = Enable filling of color into rectangle in draw rectangle command.
- Enable/Disable reverse copy (A[4])
 - 0 = Disable reverse copy (RESET)
 - 1 = During copy command, the new image colors are swapped such that “GS0” <-> “GS63”, “GS1” <-> “GS62”,

9.2.7 Continuous Horizontal & Vertical Scrolling Setup (27h)

This command setup the parameters required for horizontal and vertical scrolling. The parameters should not be changed after scrolling is activated

Figure 36 - Examples of Continuous Horizontal and Vertical Scrolling command setup



9.2.8 Deactivate scrolling (2Eh)

This command deactivates the scrolling action. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

9.2.9 Activate scrolling (2Fh)

This command activates the scrolling function according to the setting done by Continuous Horizontal & Vertical Scrolling Setup command 27h.

10 MAXIMUM RATINGS

Table 16 - Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{DDIO}		-0.3 to $V_{DD}+0.5$	V
V_{CC}		0 to 19.0	V
V_{SEG} / V_{COM}	SEG/COM output voltage	0 to 19.0	V
I_{SEG}	SEG output current	0 to 220	μ A
V_{in}	Input voltage	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
T_A	Operating Temperature	-40 to +85	$^{\circ}$ C
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}$ C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

11 DC CHARACTERISTICS

Table 17 - DC Characteristics

Conditions (unless specified):

Voltage referenced to V_{SS}

$V_{DD} = 2.7$, $V_{DDIO} = 1.8V$, $V_{CC} = 11.0V$, $I_{REF} = 10\mu A$, at $T_A = 25^\circ C$.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	8	11	18	V
V_{DD}	Logic Supply Voltage	-	2.4	2.7	3.5	V
V_{DDIO}	Power Supply for I/O pins	-	1.6	1.8	V_{DD}	V
V_{OH}	High Logic Output Level	$I_{OUT} = 100\mu A$, 3.3MHz	$0.9 \times V_{DDIO}$	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level	$I_{OUT} = 100\mu A$, 3.3MHz	0	-	$0.1 \times V_{DDIO}$	V
V_{IH}	High Logic Input Level	-	$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	-	0	-	$0.2 \times V_{DDIO}$	V
I_{DD_SLEEP}	Sleep mode V_{DD} Current	Display OFF, No panel attached	-	0	10	μA
I_{DDIO_SLEEP}	Sleep mode V_{DDIO} Current	Display OFF, No panel attached	-	0	10	μA
I_{CC_SLEEP}	Sleep mode V_{CC} Current	Display OFF, No panel attached	-	0	10	μA
I_{CC}	V_{CC} Supply Current	Display ON, Contrast = FFh, No panel attached	-	700	1200	μA
I_{DD}	V_{DD} Supply Current	Display ON, Contrast = FFh, No panel attached	-	170	500	μA
I_{SEG}	Segment Output Current: $V_{CC} = 8V$, Display ON, All 1's pattern. (Segment pin under test is connected with a 20K Ω resistive load to V_{SS})	Contrast = FFh	142	155	168	μA
		Contrast = 7Fh	-	78	-	μA
		Contrast = 3Fh	-	39	-	μA
Dev	Segment Output Current Uniformity: $Dev = (I_{SEG} - I_{MID}) / I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN}) / 2$ $I_{SEG} [0:287] =$ Segment current at contrast settings $V_{CC} = 12V$	Contrast = FFh	-3	-	+3	%
Adj. Dev	Adjacent pin output current uniformity: $Adj\ Dev = (I[n] - I[n+1]) / (I[n] + I[n+1])$	Contrast = FFh	-2	-	+2	%
R_{COM_ON}	COM pin output resistance	COM[0:63], $I = 20mA$	-	25	30	Ω

12 AC CHARACTERISTICS

Table 18 - AC Characteristics

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}
 $V_{DD} = V_{DDIO} = 2.4V$ to $3.5V$
 $V_{CC} = 8.0V$ to $18.0V$
 $T_A = 25^\circ C$

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	$V_{DD} = 2.7V$	774	860	946	KHz
F_{FRM}	Frame Frequency	Display ON, Internal Oscillator Enabled	-	$F_{OSC} \times 1 / (D \times K \times N)$	-	Hz
RES#	Reset low pulse width	-	3	-	-	us
	Reset completion time	-	-	-	2	us

Note

- (1) Fosc stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4]=1101b [default value]
- (2) D stands for divide ratio
- (3) K stands for total number of display clocks per row. (RESET=136, i.e. phase1 DCLK+phase2 DCLK + phase3 DCLK =4+7+125)
- (4) N stands for number of MUX selected by command A8h

Table 19 - 6800-Series MPU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4V$ to $3.5V$, $V_{DDIO} = 2.4V$ to V_{DD} , $T_A = -40$ to $+85^{\circ}C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	130	-	-	ns
PW_{CSL}	Control Pulse Low Width (write cycle)	60	-	-	ns
PW_{CSH}	Control Pulse High Width (write cycle)	60	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	200	-	-	ns
PW_{CSL}	Control Pulse Low Width (read cycle)	100	-	-	ns
PW_{CSH}	Control Pulse High Width (read cycle)	100	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	40	-	-	ns
t_{DHW}	Data Hold Time	10	-	-	ns
t_{ACC}	Data Access Time	-	-	140	ns
t_{OH}	Output Hold time	-	-	70	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

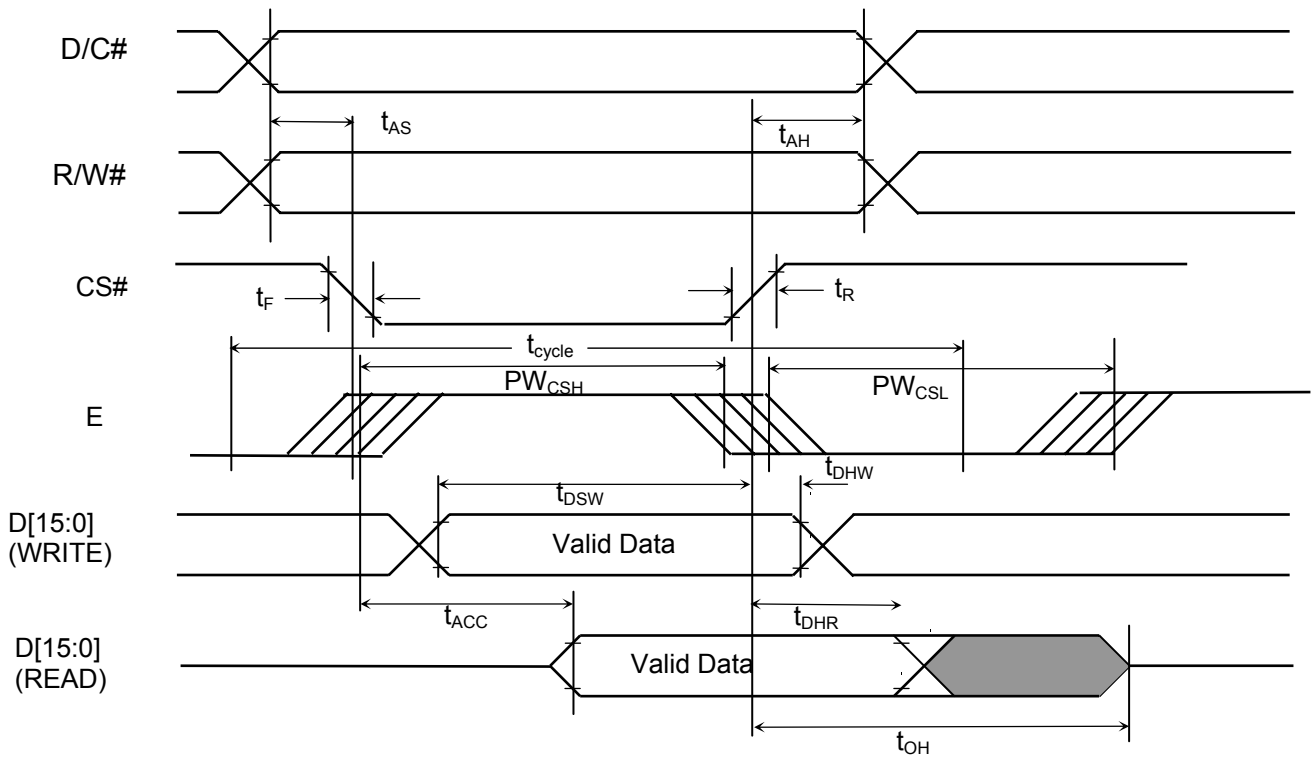


Figure 37 - 6800-series parallel interface characteristics

Table 20 - 8080-Series MPU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4V$ to $3.5V$, $V_{DDIO} = 2.4V$ to V_{DD} , $T_A = -40$ to $85^{\circ}C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	130	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

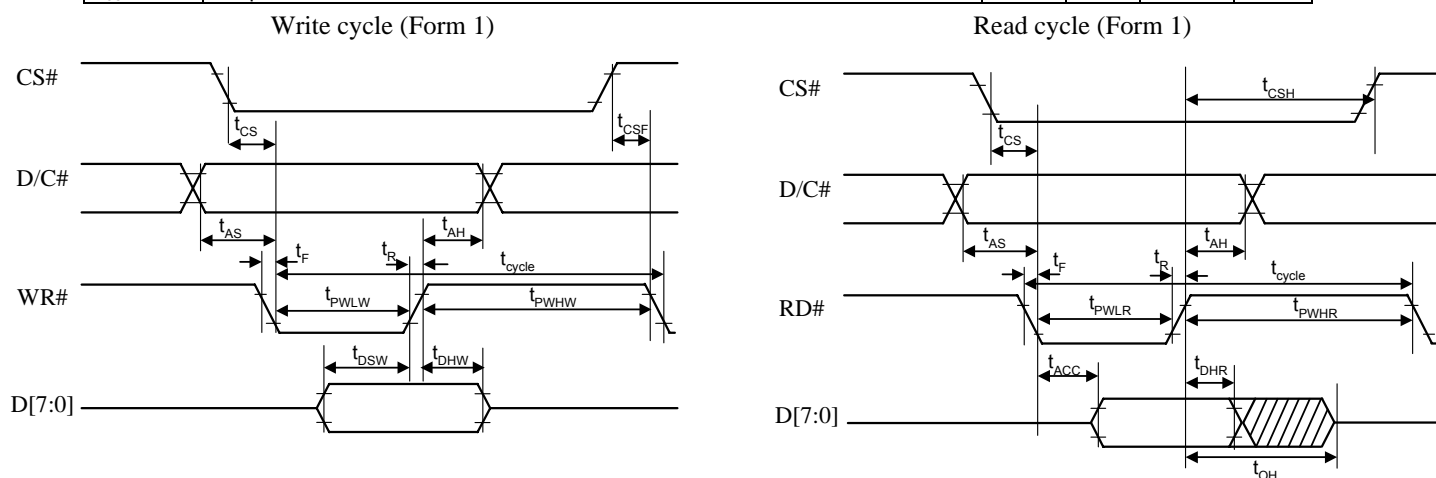


Figure 38 - 8080-series parallel interface characteristics (Form 1)

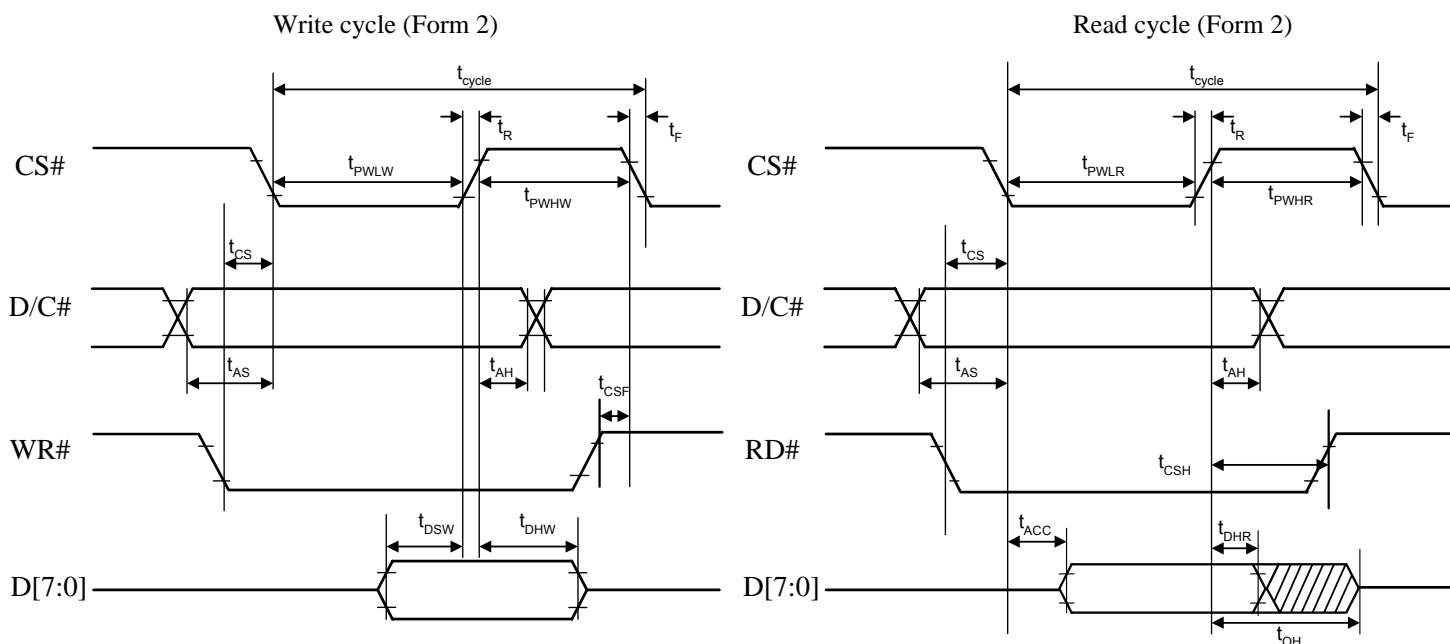


Figure 39 - 8080-series parallel interface characteristics (Form 2)

Table 21 - Serial Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4V$ to $3.5V$, $V_{DDIO} = 2.4V$ to V_{DD} , $T_A = -40$ to $85^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	150	-	-	ns
t_{AS}	Address Setup Time	40	-	-	ns
t_{AH}	Address Hold Time	40	-	-	ns
t_{CSS}	Chip Select Setup Time	75	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	40	-	-	ns
t_{CLKL}	Clock Low Time	75	-	-	ns
t_{CLKH}	Clock High Time	75	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

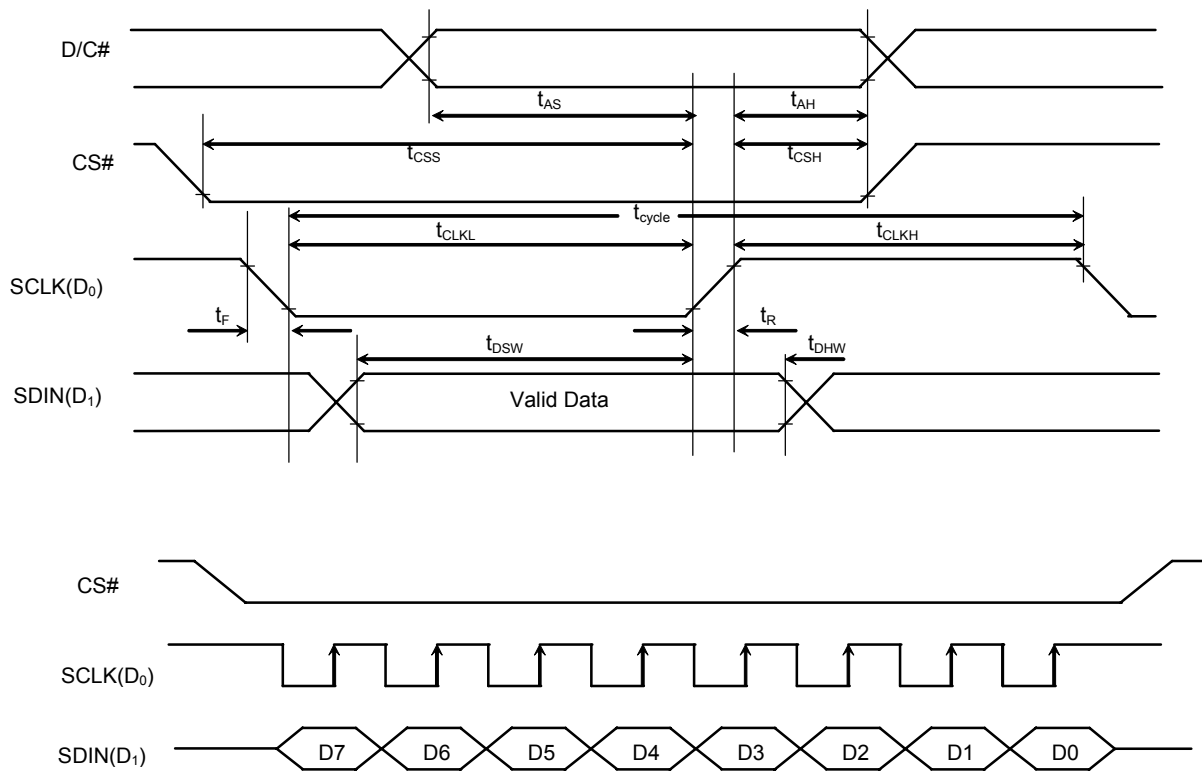


Figure 40 - Serial interface characteristics

13 APPLICATION EXAMPLE

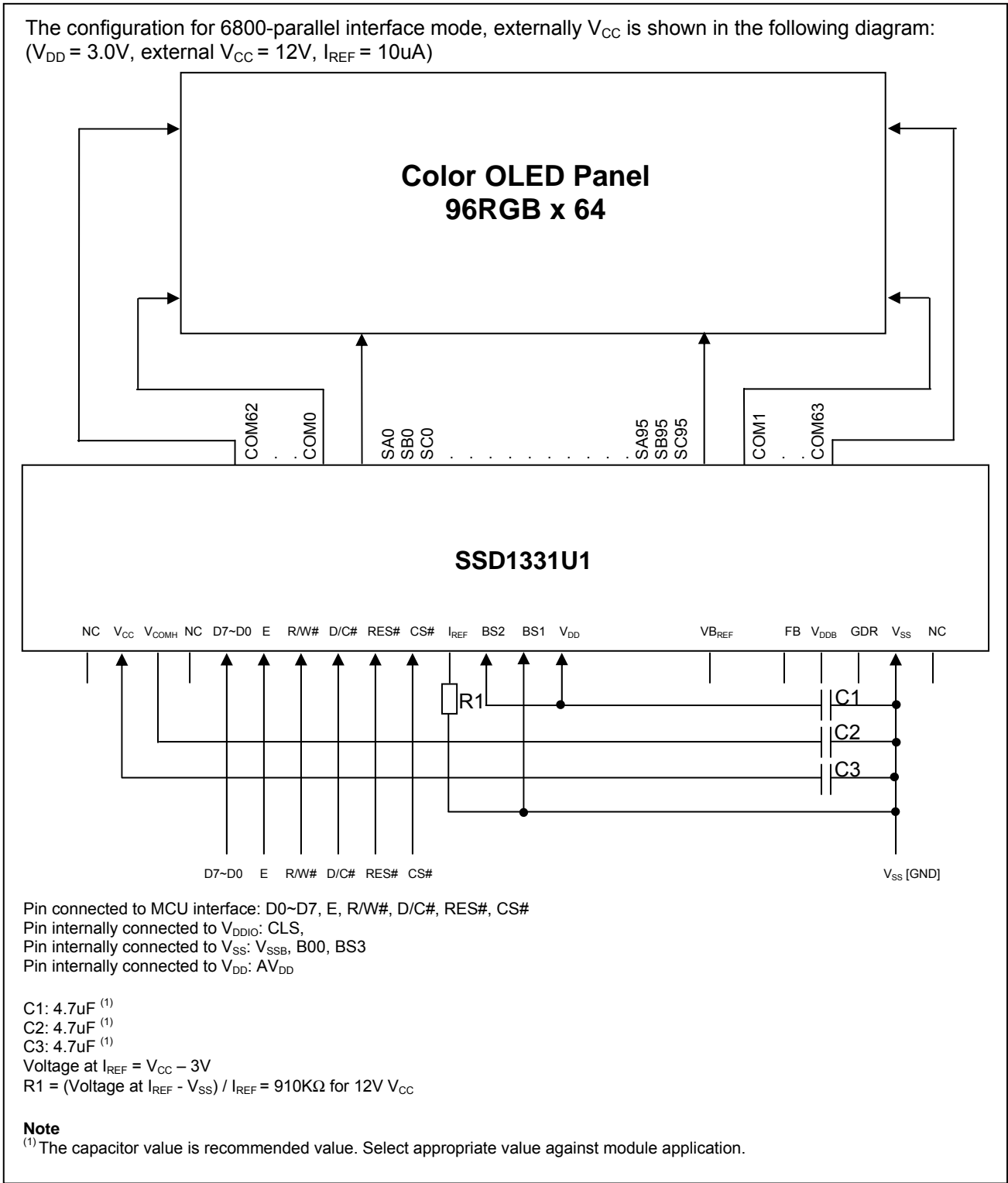
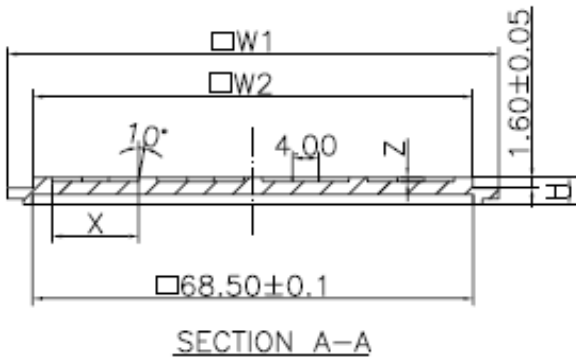
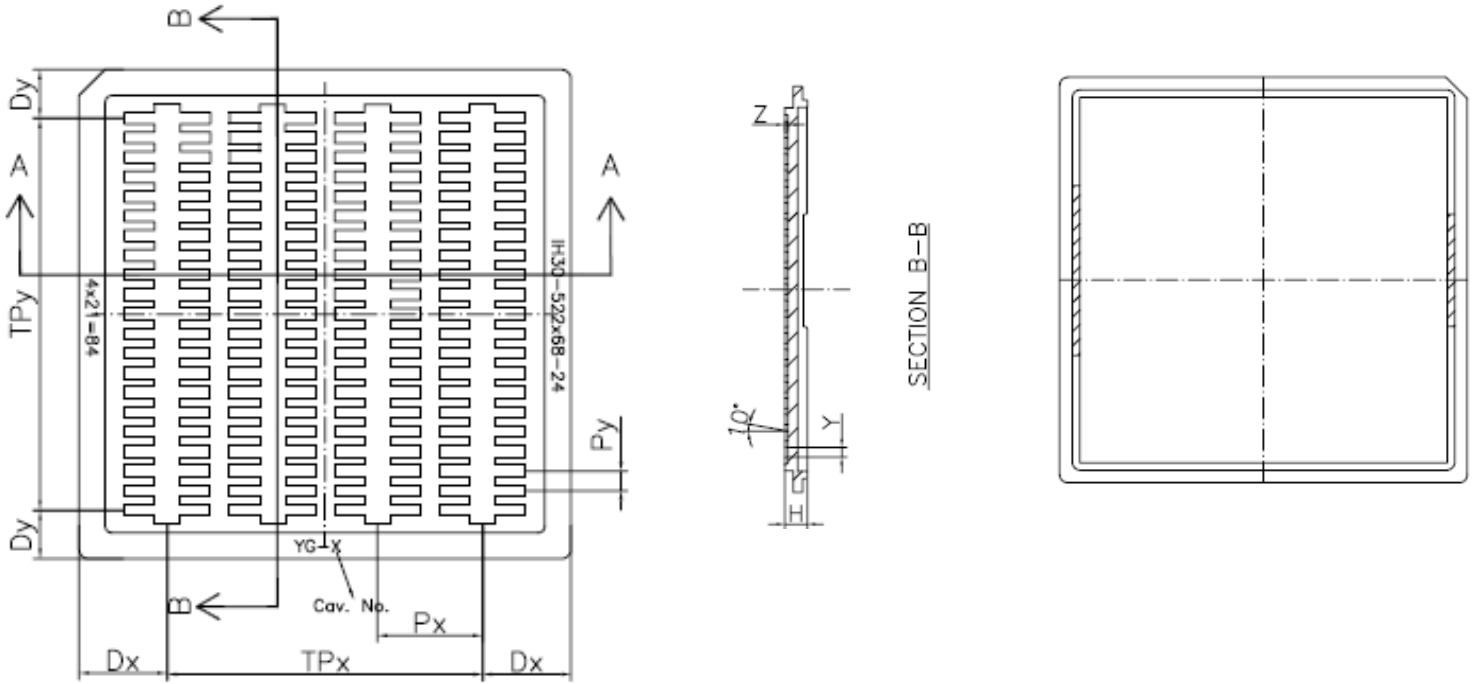


Figure 41 - Application Example for SSD1331U1R1

14 PACKAGE OPTIONS

14.1 SSD1331Z Die Tray Information

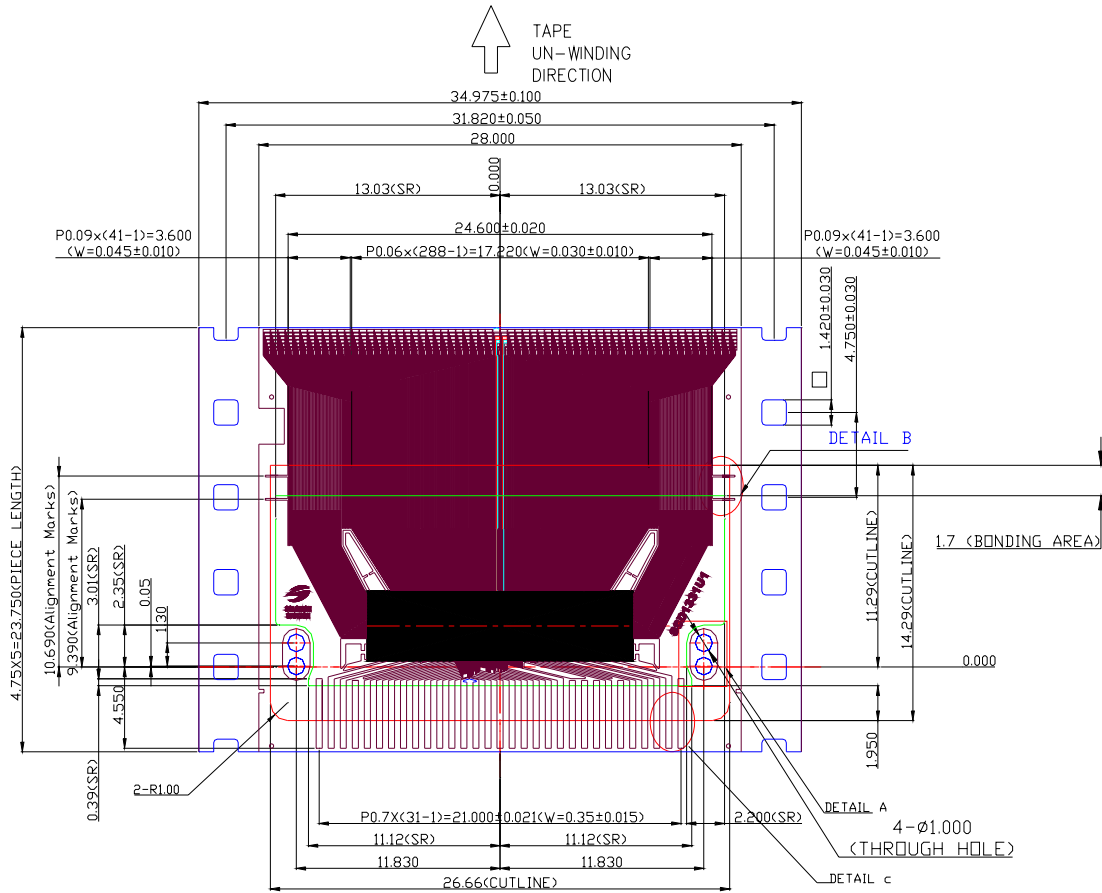
Figure 42 - Die Tray Information



	Spec	
	mm	(mil)
W1	76.00 ± 0.10	(2992)
W2	68.00 ± 0.10	(2677)
H	4.20 ± 0.10	(165)
Dx	13.66 ± 0.10	(538)
TPx	48.78 ± 0.10	(1920)
Dy	7.55 ± 0.10	(297)
TPy	61.00 ± 0.10	(2402)
Px	16.26 ± 0.05	(640)
Py	3.05 ± 0.05	(120)
X	13.25 ± 0.01	(522)
Y	1.73 ± 0.01	(68)
Z	0.62 ± 0.05	(24)
N	84 (Pocket number)	

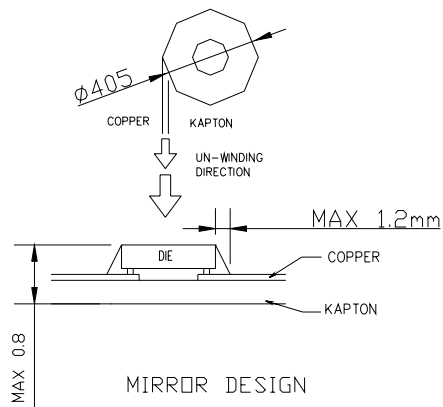
14.2 SSD1331U1R1 COF PACKAGE DIMENSIONS

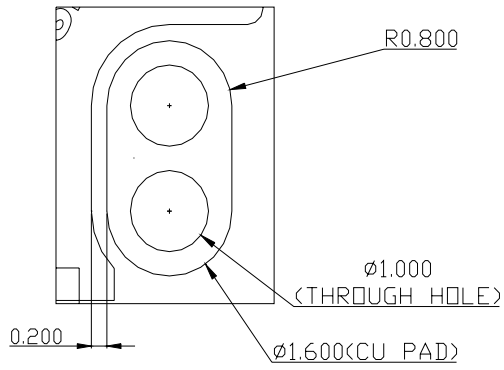
Figure 43 - SSD1331U1R1 outline drawing



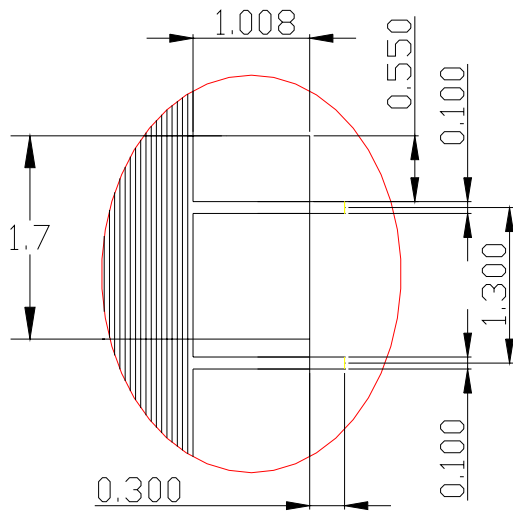
NOTE:

- GENERAL TOLERANCE: ± 0.05 mm
- MATERIAL
 - PI: 38 ± 4 um
 - CU: 8 ± 2 um
 - SR: 15 ± 10 um
 - (OTHER TOLERANCE: ± 0.200 mm)
- SN PLATING: 0.23 ± 0.05 um
- TAP SITE: 5 SPH, 23.75mm

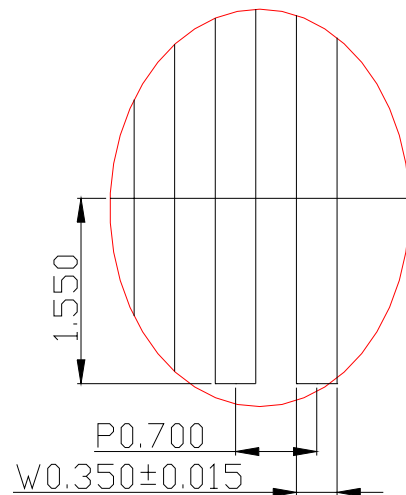




DETAIL A (3:1)



DETAIL B (3:1)



DETAIL C (3:1)

14.3 SSD1331U1R1 COF PACKAGE PIN ASSIGNMENT

Figure 44 - SSD1331U1R1 pin assignment drawing

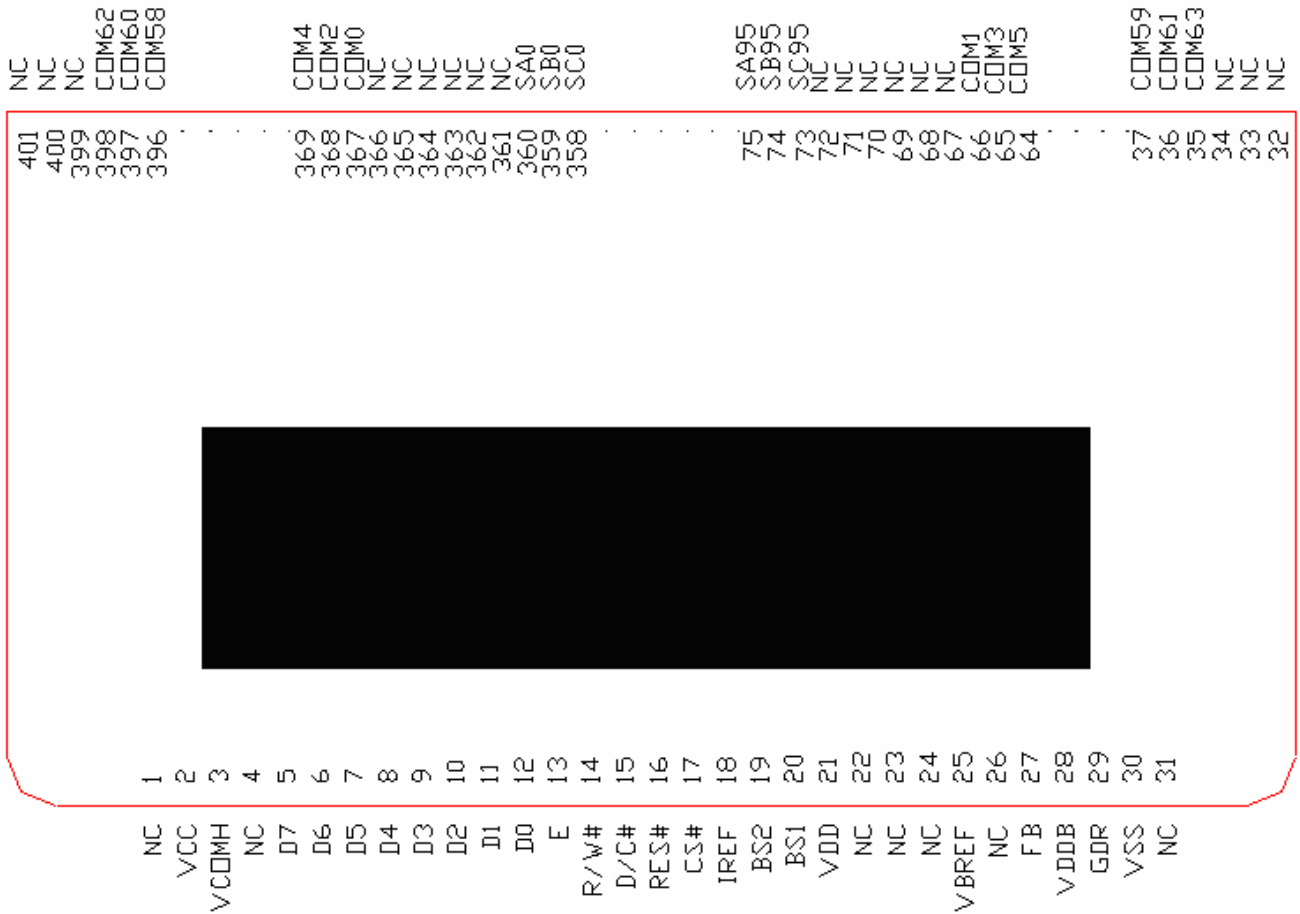
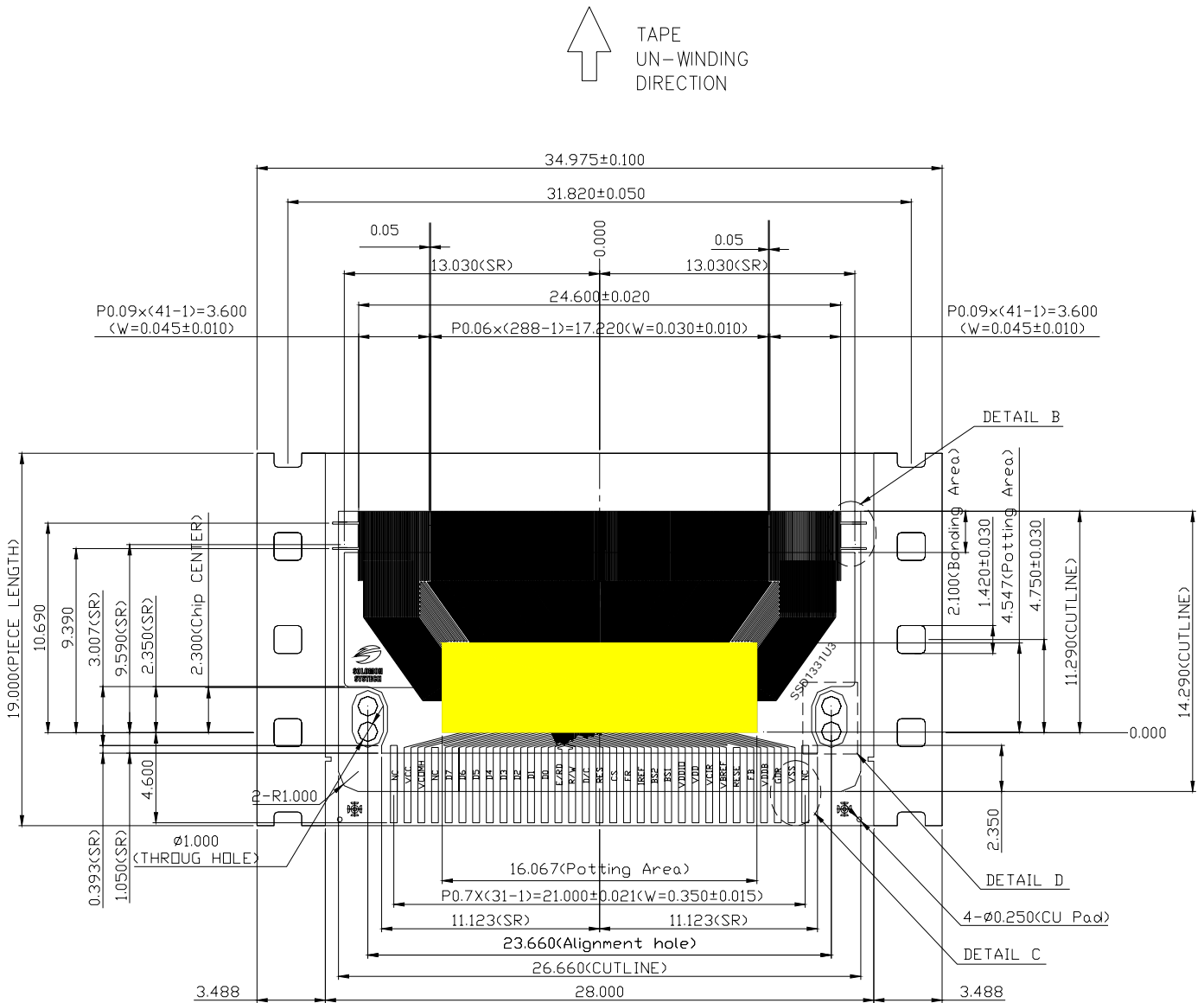


Table 22 - SSD1331U1R1 pin assignment

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
1	NC	81	SA93	161	SB66	241	SC39	321	SA13	401	NC
2	VCC	82	SC92	162	SA66	242	SB39	322	SC12		
3	VCOMH	83	SB92	163	SC65	243	SA39	323	SB12		
4	NC	84	SA92	164	SB65	244	SC38	324	SA12		
5	D7	85	SC91	165	SA65	245	SB38	325	SC11		
6	D6	86	SB91	166	SC64	246	SA38	326	SB11		
7	D5	87	SA91	167	SB64	247	SC37	327	SA11		
8	D4	88	SC90	168	SA64	248	SB37	328	SC10		
9	D3	89	SB90	169	SC63	249	SA37	329	SB10		
10	D2	90	SA90	170	SB63	250	SC36	330	SA10		
11	D1	91	SC89	171	SA63	251	SB36	331	SC9		
12	D0	92	SB89	172	SC62	252	SA36	332	SB9		
13	E	93	SA89	173	SB62	253	SC35	333	SA9		
14	R/W#	94	SC88	174	SA62	254	SB35	334	SC8		
15	D/C#	95	SB88	175	SC61	255	SA35	335	SB8		
16	RES#	96	SA88	176	SB61	256	SC34	336	SA8		
17	CS#	97	SC87	177	SA61	257	SB34	337	SC7		
18	IREF	98	SB87	178	SC60	258	SA34	338	SB7		
19	BS2	99	SA87	179	SB60	259	SC33	339	SA7		
20	BS1	100	SC86	180	SA60	260	SB33	340	SC6		
21	VDD	101	SB86	181	SC59	261	SA33	341	SB6		
22	NC	102	SA86	182	SB59	262	SC32	342	SA6		
23	NC	103	SC85	183	SA59	263	SB32	343	SC5		
24	NC	104	SB85	184	SC58	264	SA32	344	SB5		
25	VBREF	105	SA85	185	SB58	265	SC31	345	SA5		
26	NC	106	SC84	186	SA58	266	SB31	346	SC4		
27	FB	107	SB84	187	SC57	267	SA31	347	SB4		
28	VDDB	108	SA84	188	SB57	268	SC30	348	SA4		
29	GDR	109	SC83	189	SA57	269	SB30	349	SC3		
30	VSS	110	SB83	190	SC56	270	SA30	350	SB3		
31	NC	111	SA83	191	SB56	271	SC29	351	SA3		
32	NC	112	SC82	192	SA56	272	SB29	352	SC2		
33	NC	113	SB82	193	SC55	273	SA29	353	SB2		
34	NC	114	SA82	194	SB55	274	SC28	354	SA2		
35	COM63	115	SC81	195	SA55	275	SB28	355	SC1		
36	COM61	116	SB81	196	SC54	276	SA28	356	SB1		
37	COM59	117	SA81	197	SB54	277	SC27	357	SA1		
38	COM57	118	SC80	198	SA54	278	SB27	358	SC0		
39	COM55	119	SB80	199	SC53	279	SA27	359	SB0		
40	COM53	120	SA80	200	SB53	280	SC26	360	SA0		
41	COM51	121	SC79	201	SA53	281	SB26	361	NC		
42	COM49	122	SB79	202	SC52	282	SA26	362	NC		
43	COM47	123	SA79	203	SB52	283	SC25	363	NC		
44	COM45	124	SC78	204	SA52	284	SB25	364	NC		
45	COM43	125	SB78	205	SC51	285	SA25	365	NC		
46	COM41	126	SA78	206	SB51	286	SC24	366	NC		
47	COM39	127	SC77	207	SA51	287	SB24	367	COM0		
48	COM37	128	SB77	208	SC50	288	SA24	368	COM2		
49	COM35	129	SA77	209	SB50	289	SC23	369	COM4		
50	COM33	130	SC76	210	SA50	290	SB23	370	COM6		
51	COM31	131	SB76	211	SC49	291	SA23	371	COM8		
52	COM29	132	SA76	212	SB49	292	SC22	372	COM10		
53	COM27	133	SC75	213	SA49	293	SB22	373	COM12		
54	COM25	134	SB75	214	SC48	294	SA22	374	COM14		
55	COM23	135	SA75	215	SB48	295	SC21	375	COM16		
56	COM21	136	SC74	216	SA48	296	SB21	376	COM18		
57	COM19	137	SB74	217	SC47	297	SA21	377	COM20		
58	COM17	138	SA74	218	SB47	298	SC20	378	COM22		
59	COM15	139	SC73	219	SA47	299	SB20	379	COM24		
60	COM13	140	SB73	220	SC46	300	SA20	380	COM26		
61	COM11	141	SA73	221	SB46	301	SC19	381	COM28		
62	COM9	142	SC72	222	SA46	302	SB19	382	COM30		
63	COM7	143	SB72	223	SC45	303	SA19	383	COM32		
64	COM5	144	SA72	224	SB45	304	SC18	384	COM34		
65	COM3	145	SC71	225	SA45	305	SB18	385	COM36		
66	COM1	146	SB71	226	SC44	306	SA18	386	COM38		
67	NC	147	SA71	227	SB44	307	SC17	387	COM40		
68	NC	148	SC70	228	SA44	308	SB17	388	COM42		
69	NC	149	SB70	229	SC43	309	SA17	389	COM44		
70	NC	150	SA70	230	SB43	310	SC16	390	COM46		
71	NC	151	SC69	231	SA43	311	SB16	391	COM48		
72	NC	152	SB69	232	SC42	312	SA16	392	COM50		
73	SC95	153	SA69	233	SB42	313	SC15	393	COM52		
74	SB95	154	SC68	234	SA42	314	SB15	394	COM54		
75	SA95	155	SB68	235	SC41	315	SA15	395	COM56		
76	SC94	156	SA68	236	SB41	316	SC14	396	COM58		
77	SB94	157	SC67	237	SA41	317	SB14	397	COM60		
78	SA94	158	SB67	238	SC40	318	SA14	398	COM62		
79	SC93	159	SA67	239	SB40	319	SC13	399	NC		
80	SB93	160	SC66	240	SA40	320	SB13	400	NC		

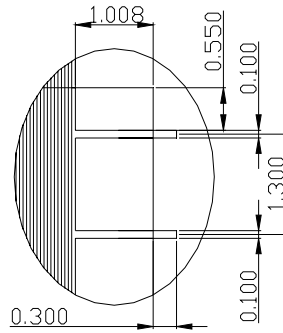
14.4 SSD1331U3R1 COF PACKAGE DIMENSIONS

Figure 45 - SSD1331U3R1 outline drawing

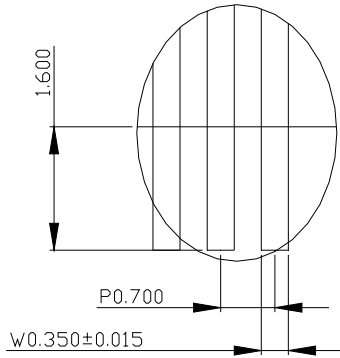


NOTE:

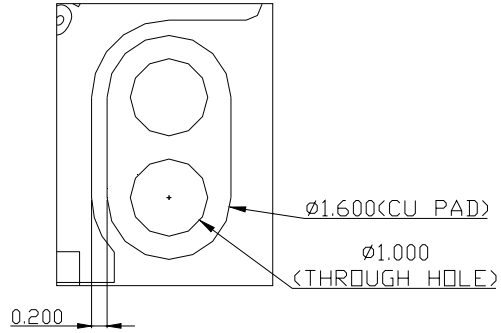
1. GENERAL TOLERANCE: ±0.05mm
2. MATERIAL
PI: KAPTON (150EN) 38±4µm
CU: 8±2µm
SR: SN9000 15±10µm
(OTHER TOLERANCE: ±0.200mm)
3. SN PLATING: 0.23±0.05µm
4. TAPSITE: 4 SPH, 19.00mm



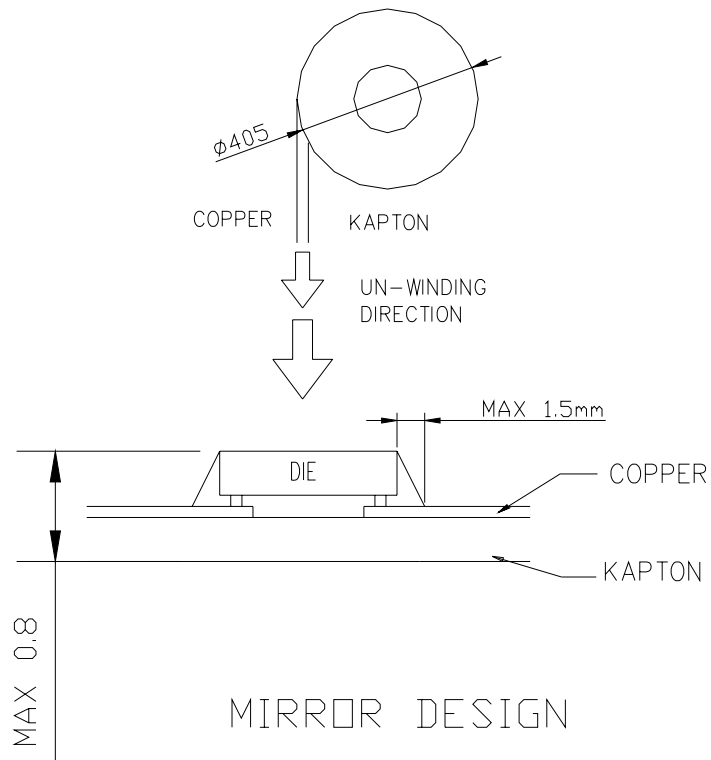
DETAIL B (3:1)



DETAIL C (3:1)



DETAIL D (3:1)



14.5 SSD1331U3R1 COF PACKAGE PIN ASSIGNMENT

Figure 46 - SSD1331U3R1 pin assignment drawing

1	NC	401	NC
2	VCC	400	NC
3	VCOMH	399	NC
4	NC	398	COM62
5	D7	397	COM60
6	D6	396	COM58
7	D5		
8	D4	369	COM4
9	D3	368	COM2
10	D2	367	COM0
11	D1	366	NC
12	D0	365	NC
13	E/RD#	364	NC
14	R/W#	363	NC
15	D/C#	362	NC
16	RES#	361	NC
17	CS#	360	SA0
18	FR	359	SB0
19	IREF	358	SC0
20	BS2		
21	BS1	75	SA95
22	VDDIO	74	SB95
23	VDD	73	SC95
24	VCIR	72	NC
25	VBREF	71	NC
26	NC	70	NC
27	FB	69	NC
28	VDDDB	68	NC
29	GDR	67	COM1
30	VSS	66	COM3
31	NC	65	COM5
		64	
		37	COM59
		36	COM61
		35	COM63
		34	NC
		33	NC
		32	NC

Solomon Systech reserves the right to make changes without further notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part

<http://www.solomon-systech.com>