SSD1312

Advance Information

128 x 64 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Appendix: IC Revision history of SSD1312 Specification

Version	Change Items	Effective Date
1.0	1st Release	17-Jan-19

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1312 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 128 segments and 64 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1312 displays data directly from its internal 128 x 64 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable I2C Interface, 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

The 256 steps contrast control and oscillator which embedded in SSD1312 reduces the number of external components. SSD1312 is suitable for portable applications requiring a compact size and high output brightness, such as set-top box, car audio, wearable electronics, etc.

2 FEATURES

- Resolution: 128 x 64 dot matrix panel
- Power supply
  - V_{DD} = 1.65V – 3.5V, ≤ V_{BAT} (for IC logic)
  - V_{BAT} = 3.0V – 4.5V (for charge bump regulator circuit)
  - V_{CC} = 7.5V – 16.5V (for Panel driving)
- Segment maximum source current: 480uA
- Common maximum sink current: 61.5mA
- Embedded 128 x 64 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8 bits 6800/8080-series parallel Interface
  - 3/4 wire Serial Peripheral Interface
  - I^2C Interface
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Screen saving infinite content scrolling function
- Internal or external I_{REF} selection
- Internal charge pump regulator
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- Portrait Addressing Mode
- Power On Reset (POR)
- Dynamic Grayscale
- On-Chip Oscillator
- Chip layout for COG, COF
- Wide range of operating temperature: -40°C to 85°C

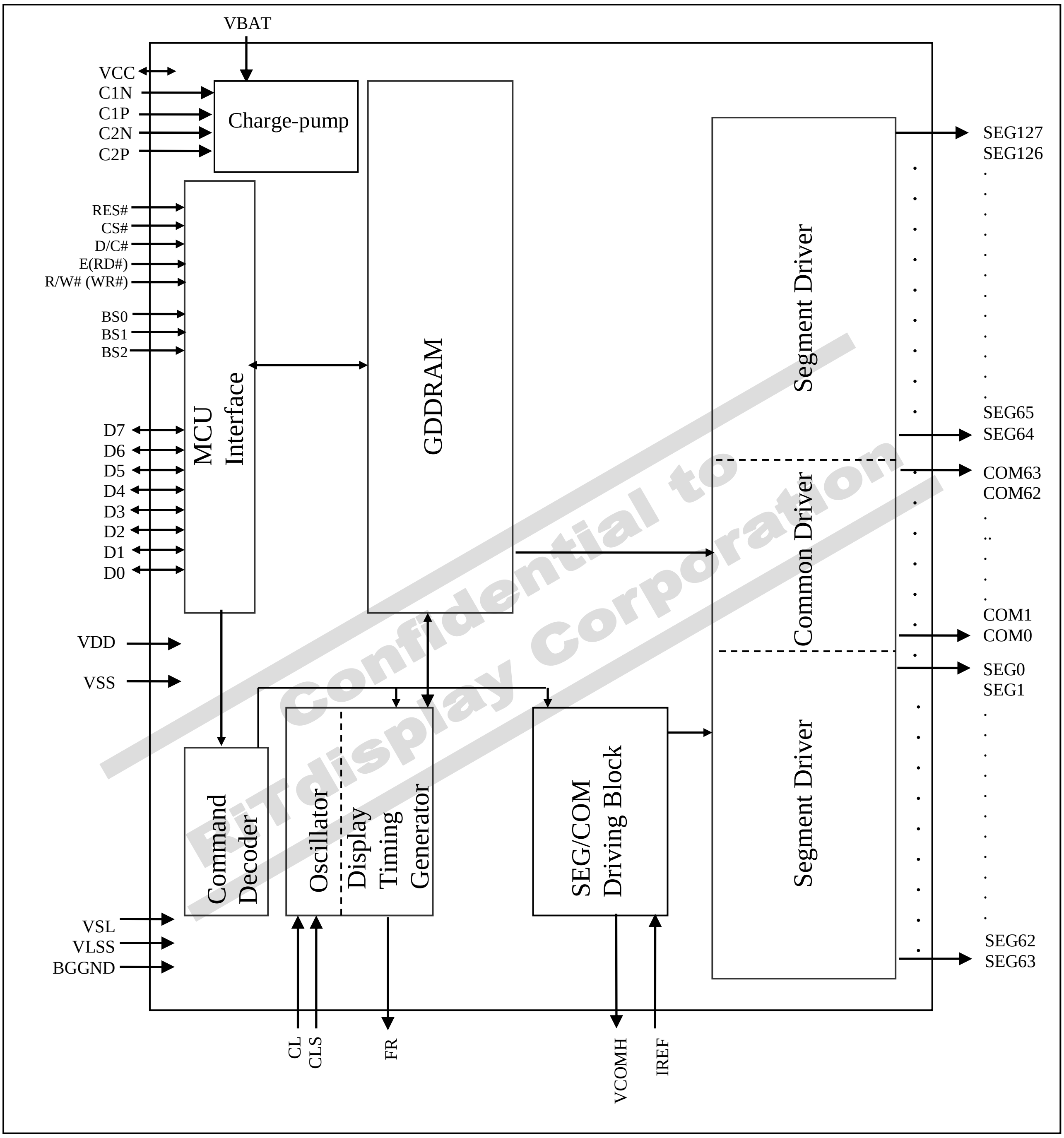
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Remark
SSD1312Z2	128	64	COG	○ Min SEG pad pitch : 27um ○ Min COM pad pitch : 27um ○ Min I/O pad pitch : 30um ○ Die thickness: 250um ○ Bump height: nominal 9um

4 BLOCK DIAGRAM

Figure 4-1: SSD1312 Block Diagram



5 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O = Output	Pull LOW = connect to Ground / V_{LL}
I/O = Bi-directional (input/output)	Pull HIGH = connect to V_{DD} / V_{LH}
P = Power pin	

Table 5-1: Pin Description

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>V_{DD}</td><td>P</td><td>Power supply pin for core logic operation.</td></tr>
<tr><td>V_{CC}</td><td>P</td><td>Power supply for panel driving voltage. This is also the most positive power voltage supply pin.
When charge pump is enabled, a capacitor should be connected between this pin and V_{SS}.</td></tr>
<tr><td>V_{SS}</td><td>P</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>V_{LSS}</td><td>P</td><td>This is an analog ground pin. It should be connected to V_{SS} externally.</td></tr>
<tr><td>V_{COMH}</td><td>O</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and V_{SS}.</td></tr>
<tr><td>V_{BAT}</td><td>P</td><td>Power supply for charge pump regulator circuit.
<table>
<tr><td>Status</td><td>V_{BAT}</td><td>V_{DD}</td><td>V_{CC}</td></tr>
<tr><td>Enable charge pump</td><td>Connect to external V_{BAT} source</td><td>Connect to external V_{DD} source</td><td>A capacitor should be connected between this pin and V_{SS}</td></tr>
<tr><td>Disable charge pump</td><td>Keep float</td><td>Connect to external V_{DD} source</td><td>Connect to external V_{CC} source</td></tr>
</table>
</td></tr>
<tr><td>BGGND</td><td>P</td><td>Reserved pin. It should be connected to V_{SS} externally.</td></tr>
<tr><td>V_{LH}</td><td>P</td><td>Logic high (same voltage level as V_{DD}) for internal connection of input and I/O pins. No need to connect to external power source.</td></tr>
<tr><td>V_{LL}</td><td>P</td><td>Logic low (same voltage level as V_{SS}) for internal connection of input and I/O pins. No need to connect to external ground.</td></tr>
<tr><td>C1P/C1N
C2P/C2N</td><td>I</td><td>C1P/C1N – Pin for charge pump capacitor; connect to each other with a capacitor.
C2P/C2N – Pin for charge pump capacitor; connect to each other with a capacitor.</td></tr>
<tr><td>BS[2:0]</td><td>I</td><td>MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select.

Table 5-2: Bus Interface selection
<table>
<tr><td>BS[2:0]</td><td>Interface</td></tr>
<tr><td>000</td><td>4 line SPI</td></tr>
<tr><td>001</td><td>3 line SPI</td></tr>
<tr><td>010</td><td>I^2C</td></tr>
<tr><td>110</td><td>8-bit 8080 parallel</td></tr>
<tr><td>100</td><td>8-bit 6800 parallel</td></tr>
</table>
Note
(1) 0 is connected to V_{SS} / V_{LL}
(2) 1 is connected to V_{DD} / V_{LH}</td></tr>
</table>

Pin Name	Type	Description
I_{REF}	I	This is segment output current reference pin. When external I_{REF} is used, a resistor should be connected between this pin and V_{SS} to maintain the I_{REF} current at 10uA. Please refer to **Figure 6-15** for the details of resistor value. When internal I_{REF} is used, this pin should be kept NC.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.
CL	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS} / V_{LL}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V_{DD} / V_{LH}), internal clock is enabled. When it is pulled LOW (i.e. connect to V_{SS} / V_{LL}), the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to V_{DD} / V_{LH}) during normal operation.
CS#	I	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS} / V_{LL}. For detail relationship to MCU interface signals, refer to Timing Characteristics Diagrams **Figure 9-1** to **Figure 9-3**.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS} / V_{LL}.
R/W#(WR#)	I	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to V_{DD}) and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS} / V_{LL}.

Pin Name	Type	Description
D[7:0]	IO	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D2, D1 should be tied together as the serial data input: SDIN, and D0 will be the serial clock input: SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
VREF	IO	This is a reserved pin. It should be kept NC.
TR[15:0]	-	Reserved pin. It should be kept NC.
SEG0 ~ SEG127	O	These pins provide Segment switch signals to OLED panel. These pins are V_{SS} state when display is OFF.
COM0 ~ COM63	O	These pins provide Common switch signals to OLED panel. They are in high impedance state when display is OFF.
NC	-	This is dummy pin. It should be kept NC.

6 FUNCTIONAL BLOCK DESCRIPTIONS

6.1 MCU Interface Selection

SSD1312 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in **Table 6-1**. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to **Table 5-2** for BS[2:0] setting).

Table 6-1: MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					SDIN(1)		SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					SDIN(1)		SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

Note: (1) When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 and D2 should be tied together as the serial data input: SDIN.

6.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

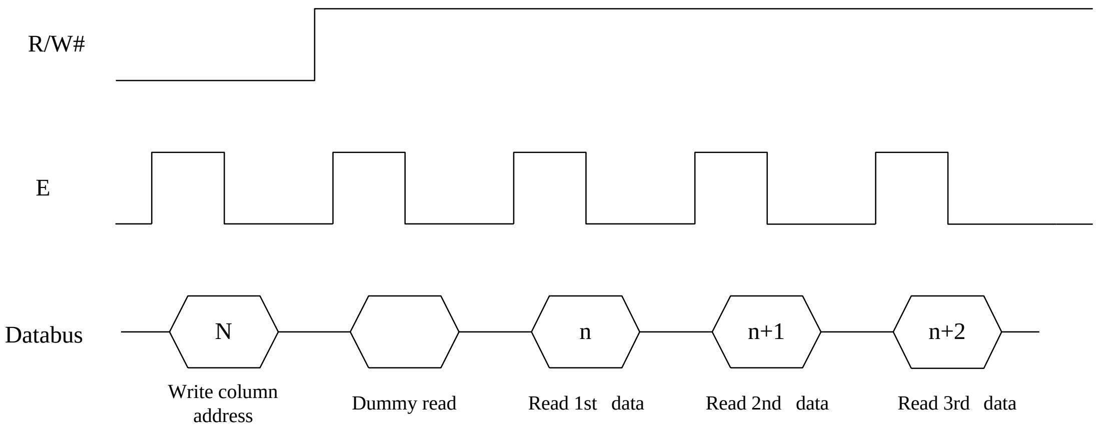
Table 6-2: Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in **Figure 6-1**.

Figure 6-1: Data read back procedure - insertion of dummy read



6.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 6-2: Example of Write procedure in 8080 parallel interface mode

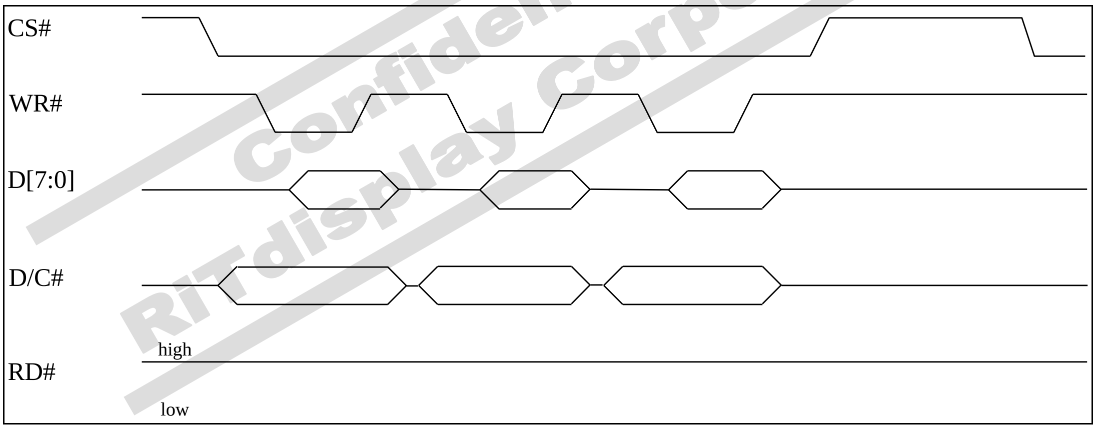


Figure 6-3: Example of Read procedure in 8080 parallel interface mode

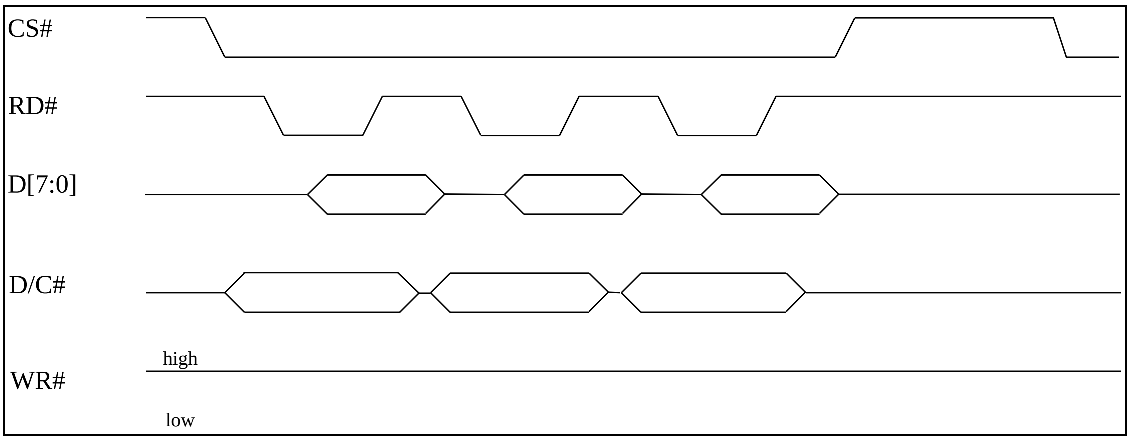


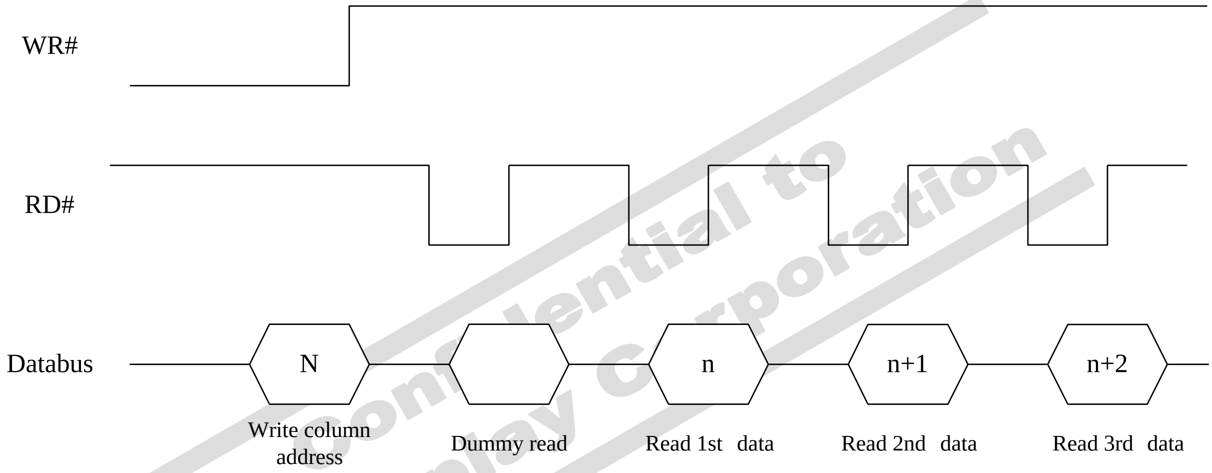
Table 6-3: Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in **Figure 6-4**.

Figure 6-4: Display data read back procedure - insertion of dummy read



6.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 and D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, E(RD#) and R/W#(WR#) can be connected to an external ground.

Table 6-4: Control pins of 4-wire Serial interface

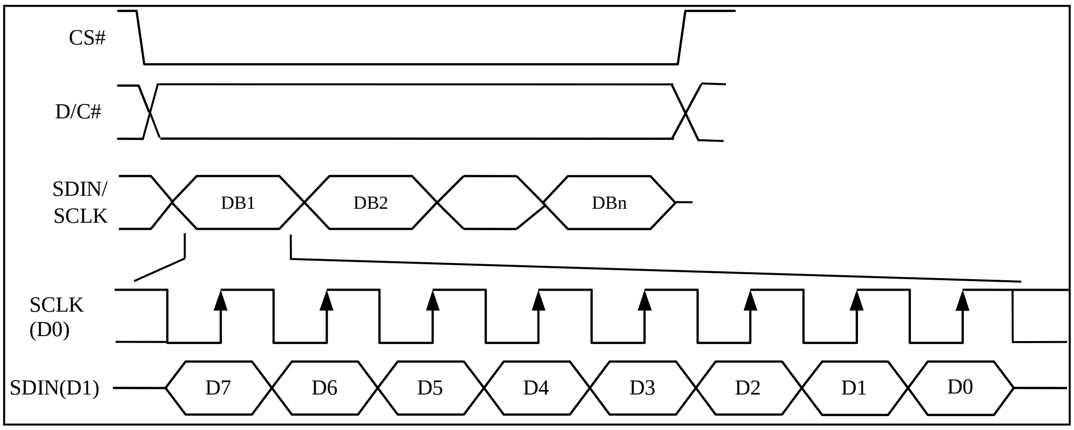
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ..., D0. D/C# is sampled on every eighth clock and D/C# should be kept stable throughout eight clock period. The data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 6-5: Write procedure in 4-wire Serial interface mode



6.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 and D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

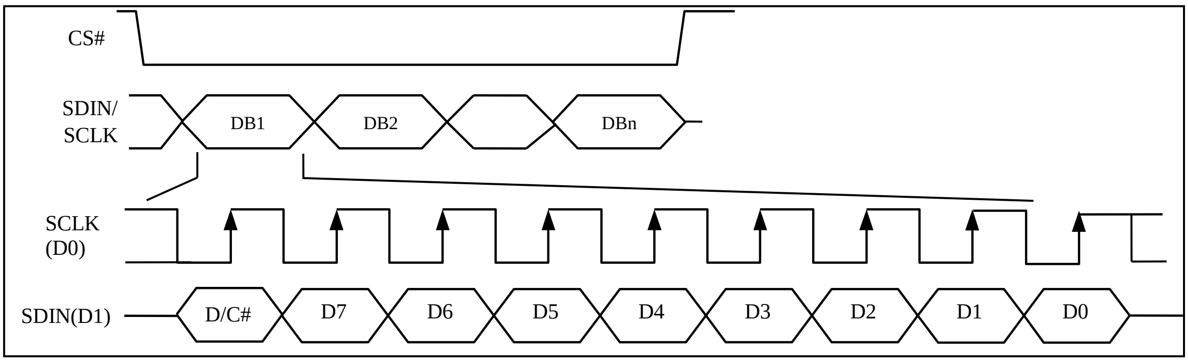
Under serial mode, only write operations are allowed.

Table 6-5: Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 6-6: Write procedure in 3-wire Serial interface mode



6.1.5 MCU I^{2}C Interface

The I^{2}C communication interface consists of slave address bit SA0, I^{2}C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I^{2}C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1312 has to recognize the slave address before transmitting or receiving any information by the I^{2}C-bus. The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format,

b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
0 1 1 1 1 0 SA0 R/W#

“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101”, can be selected as the slave address of SSD1312. D/C# pin acts as SA0 for slave address selection.
“R/W#” bit is used to determine the operation mode of the I^{2}C-bus interface. R/W# = 1, it is in read mode. R/W# = 0, it is in write mode.

b) I^{2}C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at “SDA” pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in “SDA”.

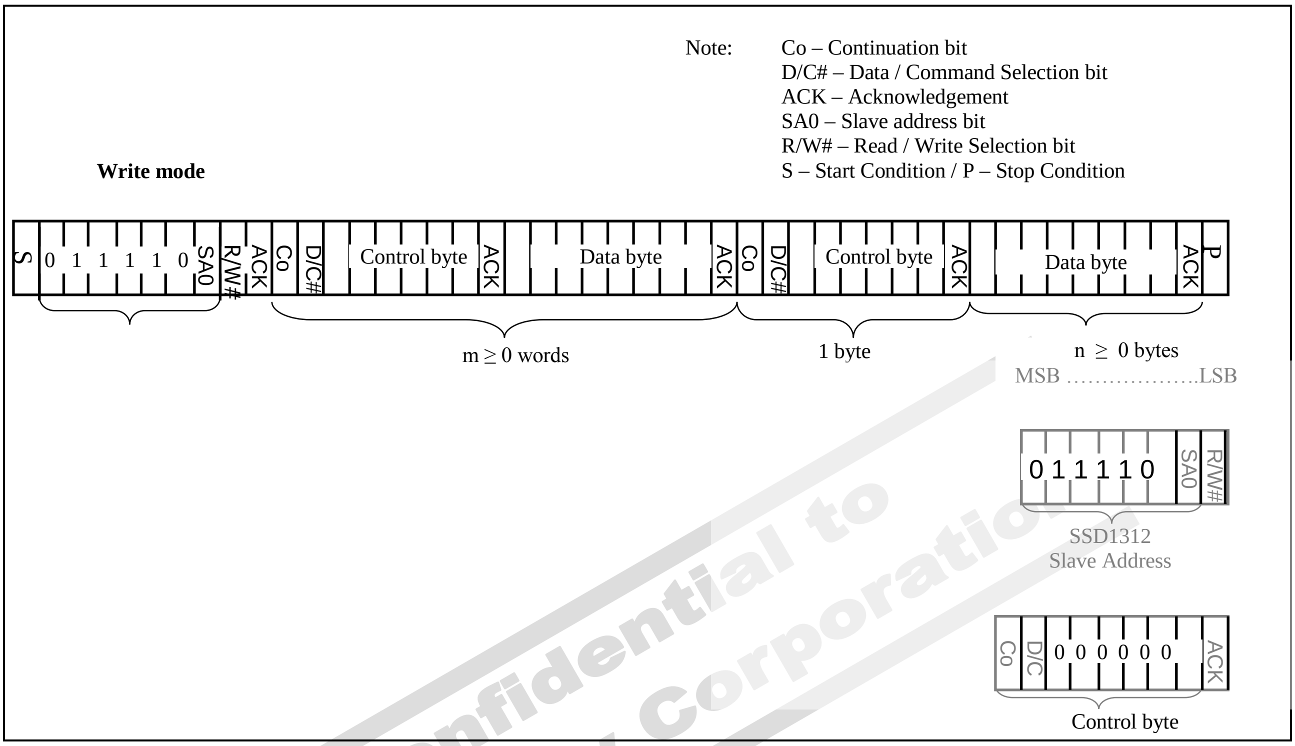
“SDA_{IN}” and “SDA_{OUT}” are tied together and serve as SDA. The “SDA_{IN}” pin must be connected to act as SDA. The “SDA_{OUT}” pin may be disconnected. When “SDA_{OUT}” pin is disconnected, the acknowledgement signal will be ignored in the I^{2}C-bus.

c) I^{2}C-bus clock signal (SCL)
The transmission of information in the I^{2}C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

6.1.5.1 I²C-bus Write Data

The I²C-bus interface gives access to write data and command into the device. Please refer to for the write mode of I²C-bus in chronological order.

Figure 6-7: I²C-bus data format



6.1.5.2 Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in **Figure 6-8**. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1312, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the **Figure 6-9** for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
    a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in **Figure 6-8**. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 6-8: Definition of the Start and Stop Condition

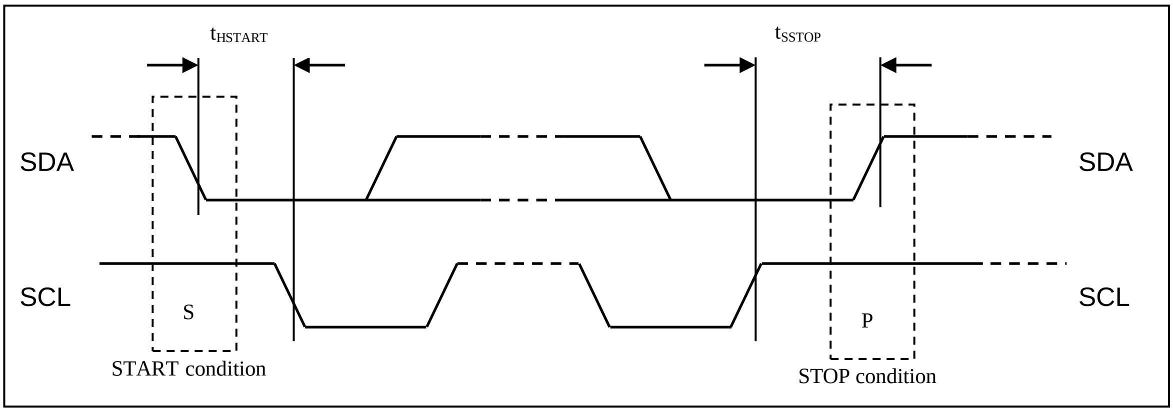
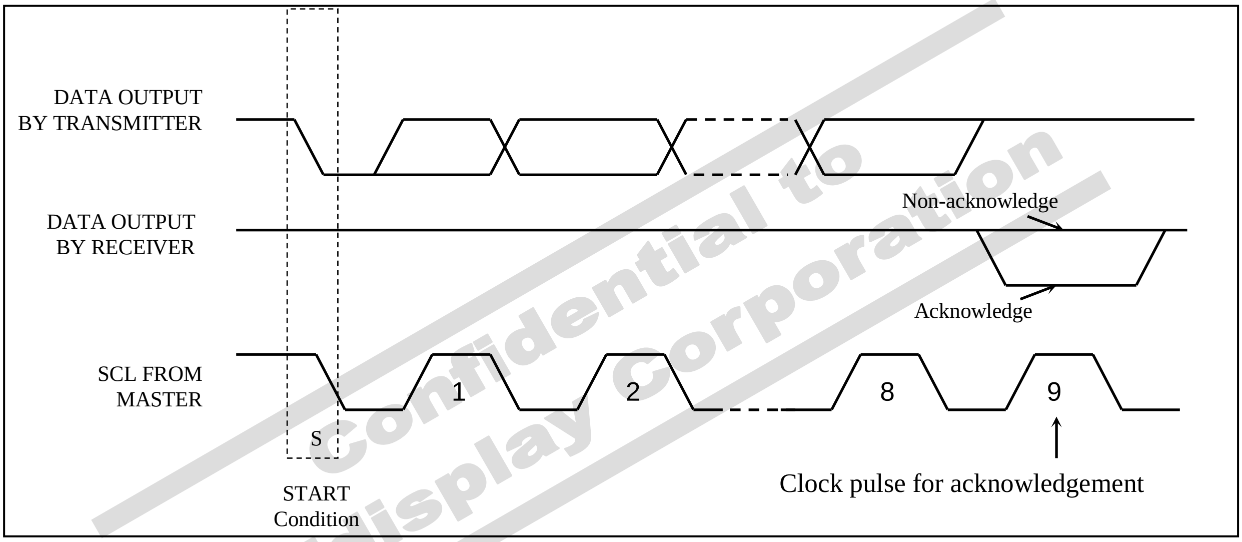


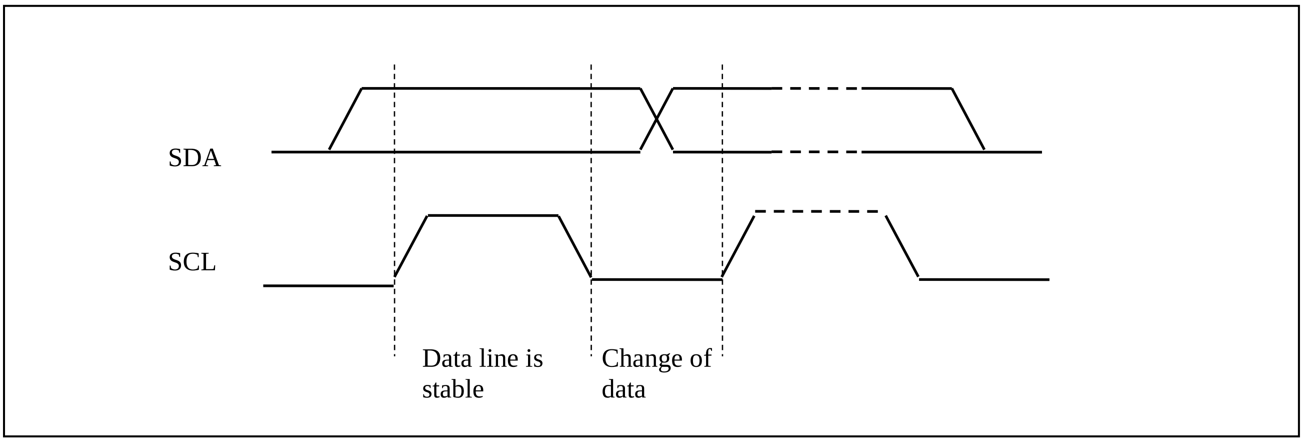
Figure 6-9: Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the **Figure 6-10** for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 6-10: Definition of the data transfer condition



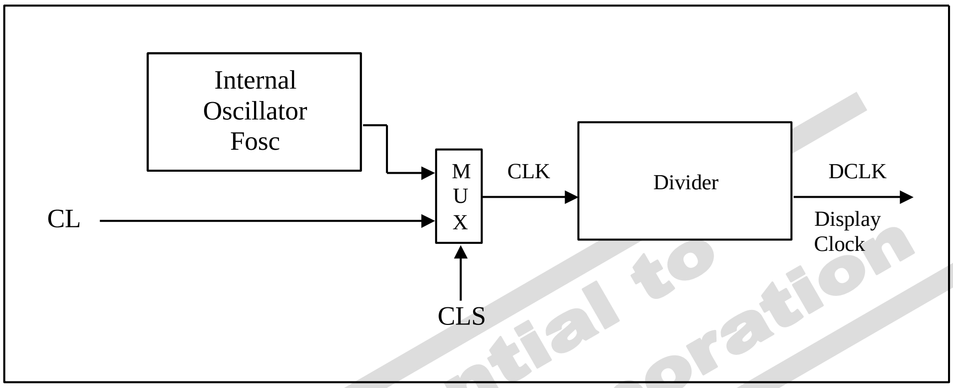
6.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

6.3 Oscillator Circuit and Display Time Generator

Figure 6-11: Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency F_{OSC} can be changed by command D5h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D5h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

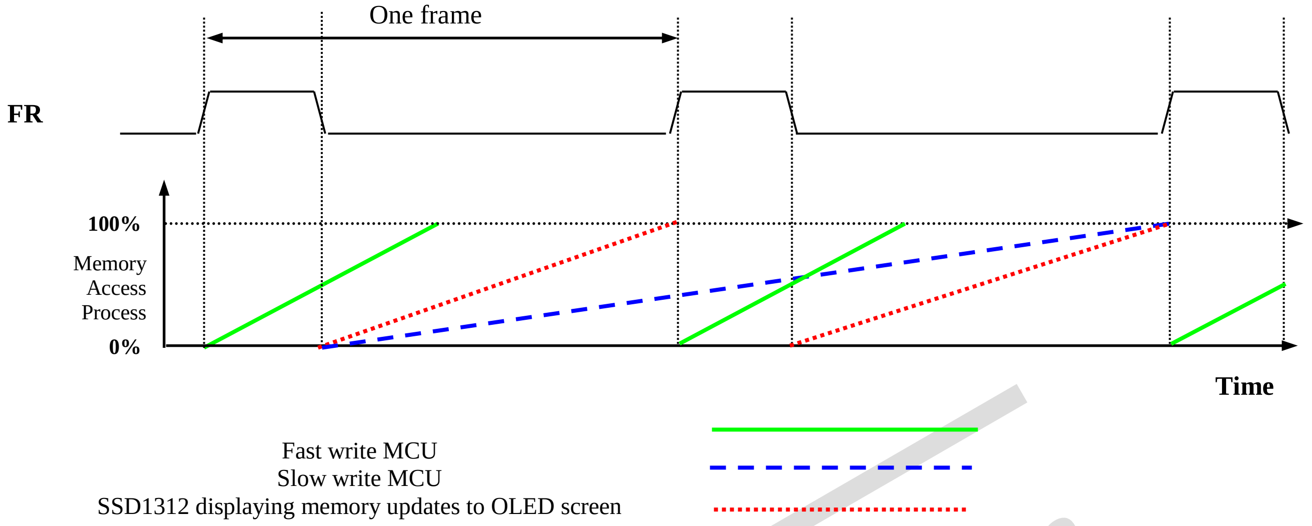
$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command D5h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_0 = 4 + 4 + 95 = 103 at power on reset (i.e. K_0 = 103)
  Please refer to **Section 6.6** for the details of the "Phase".
- Number of multiplex ratio is set by command A8h. The power on reset value is 63 (i.e. 64 MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command D5h A[7:4]. The higher the register setting results in higher frequency.

6.4 FR Synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

6.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 x 64 Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

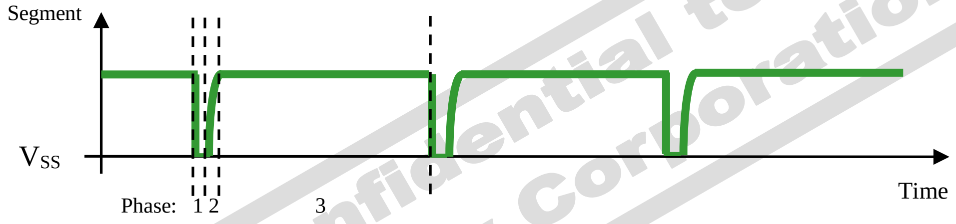
6.6 Segment Drivers / Common Drivers

Segment drivers deliver 128 current sources to drive the OLED panel. The driving current can be adjusted by altering the registers of the contrast setting command (81h). Common drivers generate voltage-scanning pulses.

The segment driving waveform is divided into three phases:

1. In phase 1, the OLED pixel charges of previous image are discharged in order to prepare for next image content display.
2. In phase 2, the OLED pixel is driven to the targeted voltage. The pixel is driven to attain the corresponding voltage level from VSS. The period of phase 2 can be programmed in length from 2 to 30 DCLKs. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.
3. In phase 3, the OLED driver switches to use current source to drive the OLED pixels and this is the current drive stage.

Figure 6-12: Segment Output Waveform in three phases



After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

In phase 3, if the length of current drive pulse width is set to 103, after finishing 103 DCLKs in current drive phase, the driver IC will go back to phase 1 for next row display.

6.7 Graphic Display Data RAM (GDDRAM)

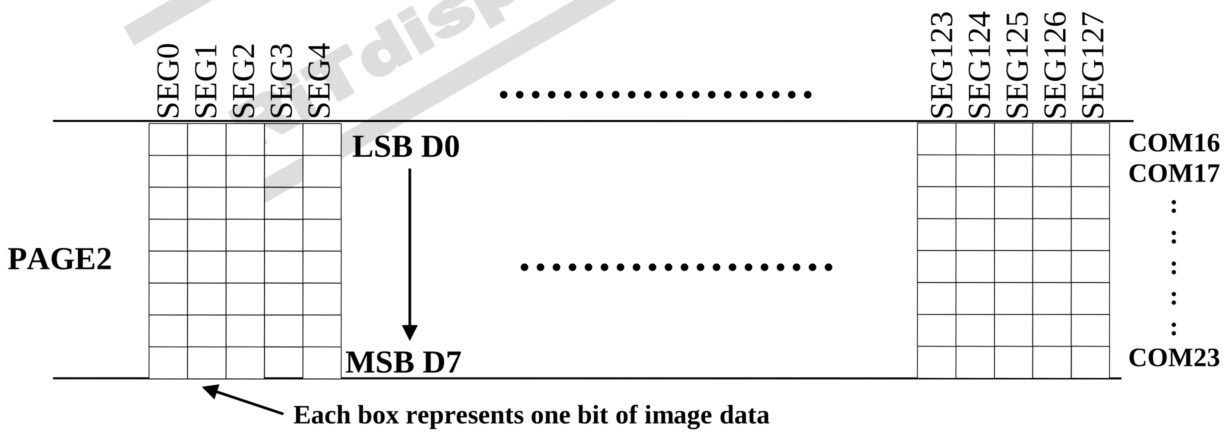
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in **Figure 6-13**.

Figure 6-13: GDDRAM pages structure

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 --SEG127	
Column re-mapping	SEG127 ---SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in **Figure 6-14**.

Figure 6-14: Enlargement of GDDRAM (No row re-mapping and column-remapping)



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software as shown in **Figure 6-13**.

For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

6.8 SEG/COM Driving Block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

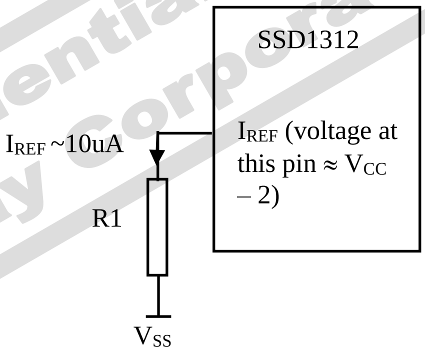
- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

  I_{SEG} = (Contrast / 255) x 48 x I_{REF}

  in which the contrast (1~255) is set by Set Contrast command 81h

When external I_{REF} is used, the magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in **Figure 6-15**. It is recommended to set I_{REF} to 10±2uA so as to achieve I_{SEG} = 480uA at maximum contrast 255.

Figure 6-15: I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 2V, the value of resistor R1 can be found as below:

For I_{REF} = 10uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 2) / 10uA
= 1MΩ

When internal I_{REF} is used, the I_{REF} pin should be kept NC. The selection of external or internal I_{REF} is controlled by command ADh. For details, please refer to SSD1312 Command Table.

6.9 Power ON and OFF Sequence

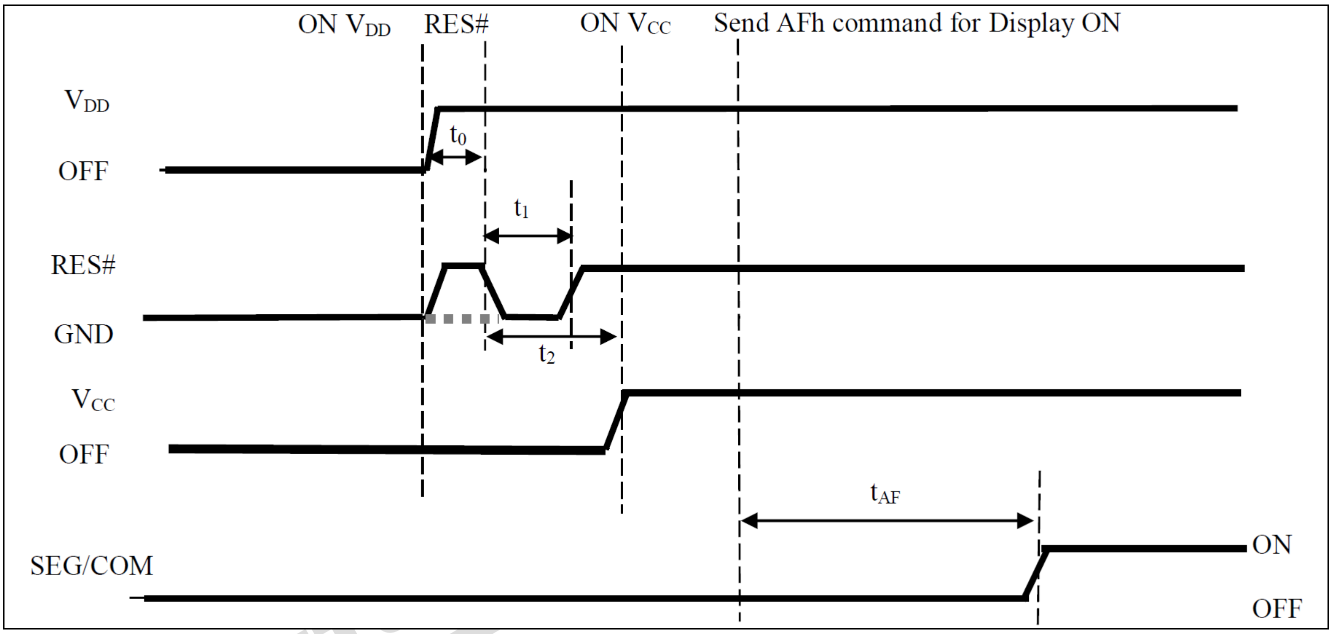
The following figures illustrate the recommended power ON and power OFF sequence of SSD1312.

6.9.1 Power ON and OFF sequence with External V_{CC}

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

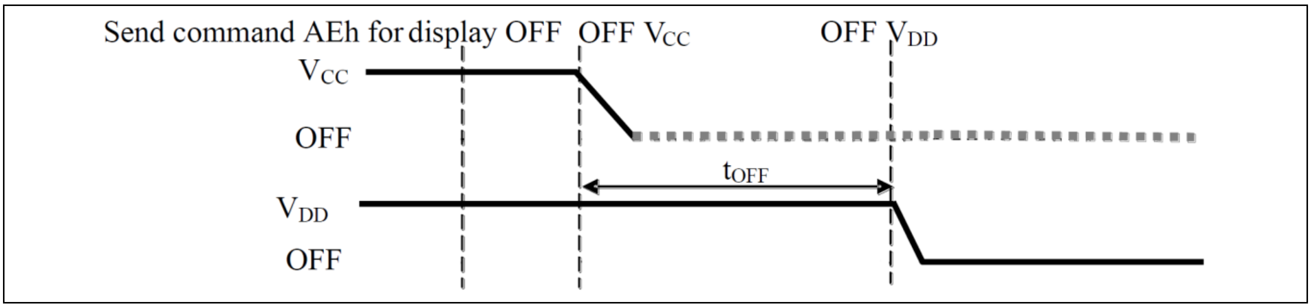
Figure 6-16: The Power ON Sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.(1), (2)
3. Power OFF V_{DD} after t_{OFF}. (4) (where Minimum t_{OFF}=0ms, typical t_{OFF}=100ms)

Figure 6-17: The Power OFF Sequence



Note:

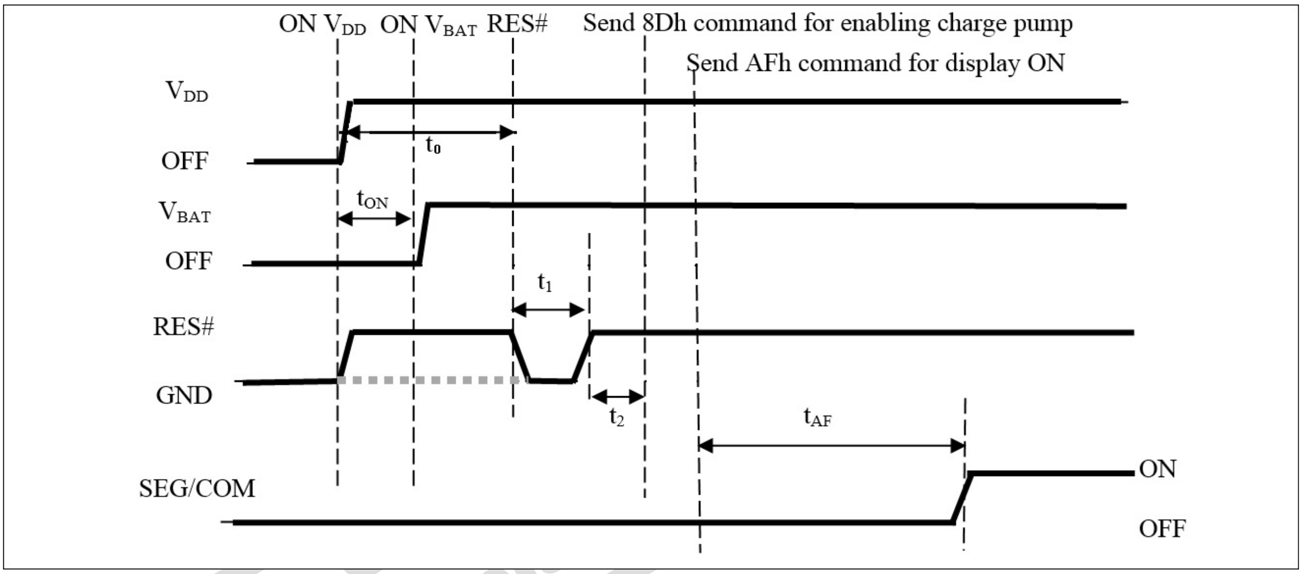
(1) V_{CC} should be kept float (i.e. disable) when it is OFF.
(2) Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
(3) The register values are reset after t_1.
(4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

6.9.2 Power ON and OFF sequence with Charge Pump Application

Power ON sequence:

1. Power ON V_{DD}
2. Wait for t_{ON}. Power ON V_{BAT}. (where Minimum t_{ON} = 0ms)
3. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) (3) and then HIGH (logic high).
4. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then input commands with below sequence:
   a. 8Dh for enabling internal charge pump
   b. AFh for display ON
5. SEG/COM will be ON after 100ms (t_{AF}).

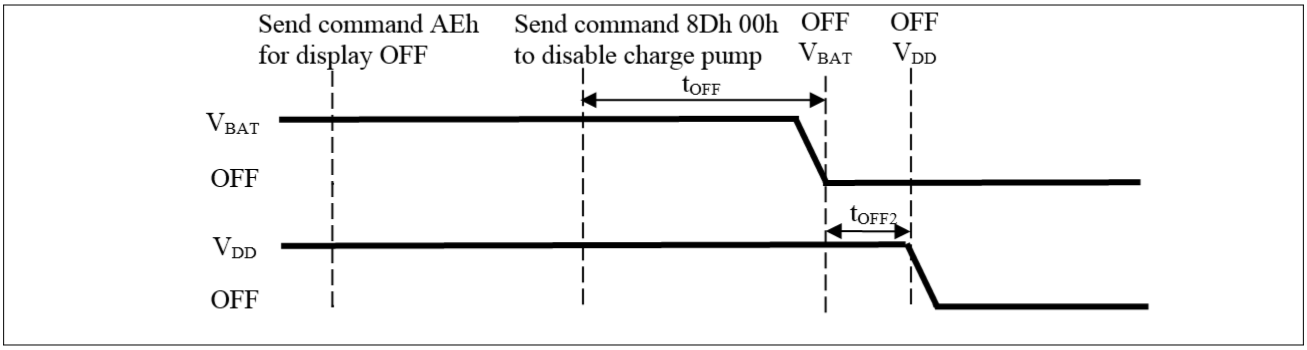
Figure 6-18: The Power ON sequence with Charge Pump Application



Power OFF sequence:

1. Send command AEh for display OFF
2. Send command 8Dh 10h to disable charge pump
3. Power OFF V_{BAT} after t_{OFF}. (1), (2) (Typical t_{OFF} =100ms)
4. Power OFF V_{DD} after t_{OFF2}. (where Minimum t_{OFF2} = 0ms (4) , Typical t_{OFF2}=5ms)

Figure 6-19: The Power OFF sequence with Charge Pump Application



Note:
(1) V_{BAT} should be kept float (i.e. disable) when it is OFF.
(2) Power Pins (V_{BAT}) can never be pulled to ground under any circumstance.
(3) The register values are reset after t_1.
(4) V_{DD} should not be Power OFF before V_{BAT} Power OFF.

6.10 Charge Pump Regulator

The internal regulator circuit in SSD1312 accompanying only 2 external capacitors can generate a maximum of 10.0V voltage supply, V_{CC} and a maximum output loading of 12mA from a low voltage supply input, V_{BAT}. In SSD1312, there are 4 charge pump output V_{CC} setting, 7.5V, 8.5V, 9V, and 10V, which can be selected by software command 8Dh setting. The V_{CC} is the voltage supply to the OLED driver block. This regulator can be turned ON/OFF by software command 8Dh setting. For details, please refer to SSD1312 Command Table.

7 MAXIMUM RATINGS

Table 7-1: Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{BAT}		-0.3 to +6	V
V_{CC}		0 to 18	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	V_{SS}-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

8 DC CHARACTERISTICS

Condition (Unless otherwise specified):

Voltage referenced to V_{SS}
V_{DD} = 1.65V to 3.5V
T_A = 25°C

Table 8-1: DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-	7.5	-	16.5	V
V_{DD}	Logic Supply Voltage	-	1.65	-	3.5	V
V_{BAT}	Charge Pump Regulator Supply Voltage	-	3.0	-	4.5	V
Charge Pump V_{CC}	Charge Pump Output Voltage	7.5V mode	7	7.5	-	V
		8.5V mode	8	8.5	-	
		9V mode	8.5	9	-	
		10V mode	9.5	10	-	
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9 x V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1 x V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8 x V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2 x V_{DD}	V
$I_{CC, SLEEP}$	$I_{CC,}$ Sleep mode Current	V_{DD} = 1.65V~3.5V, V_{CC} = 7.5V~16.5V Display OFF, No panel attached	-	-	10	uA
$I_{DD, SLEEP}$	$I_{DD,}$ Sleep mode Current	V_{DD} = 1.65V~3.5V, V_{CC} = 7.5V~16.5V Display OFF, No panel attached	-	-	10	uA
$I_{BAT, SLEEP}$	$I_{BAT,}$ Sleep mode Current	V_{DD} = 1.65V~3.5V, V_{BAT} = 3V~4.5V Display OFF, No panel attached	-	-	10	uA
I_{CC}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =12V, I_{REF} = 10uA, No loading, Display ON, All ON	Contrast = FFh	-	700	900	uA
I_{DD}	V_{CC} Supply Current V_{DD} = 2.8V, V_{CC} =12V, I_{REF} = 10uA, No loading, Display ON, All ON		-	305	375	uA
I_{SEG}	Segment Output Current V_{DD}= 2.8V, V_{CC}= 12V, I_{REF}=10uA, Display ON.	Contrast=FFh	-	480	-	uA
		Contrast=AFh	-	330	-	
		Contrast=3Fh	-	120	-	
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:127] = Segment current at contrast = FFh	-3	-	+3	%
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	+2	%

9 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DD}=1.65 to 3.5V
T_A = 25°C

Table 9-1: AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} = 2.8V	620	688	755	kHz
F_{FRM}	Frame Frequency	128x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} x 1/(DxKx64)(2)	-	Hz
RES#	Reset low pulse width		3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D5h A[7:4] is in default value.

(2) D: divide ratio (default value = 1)
K: number of display clocks per row period (default value = 103)

Table 9-2: 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	180 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 9-1: 6800-series MCU parallel interface characteristics

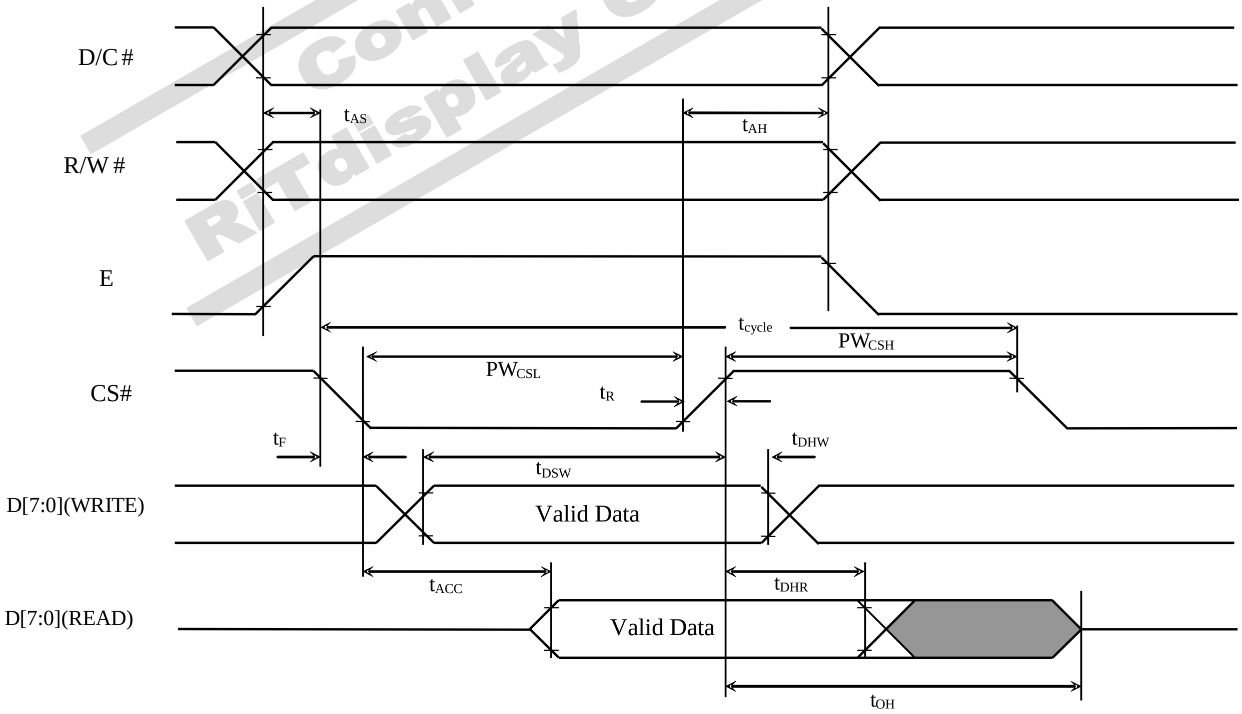
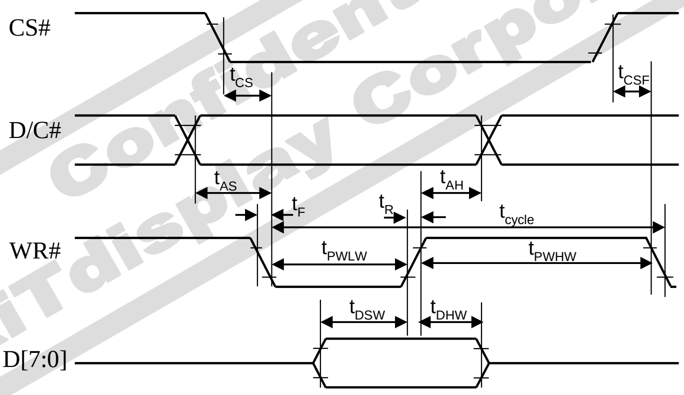


Table 9-3: 8080-Series MCU Parallel Interface Timing Characteristics

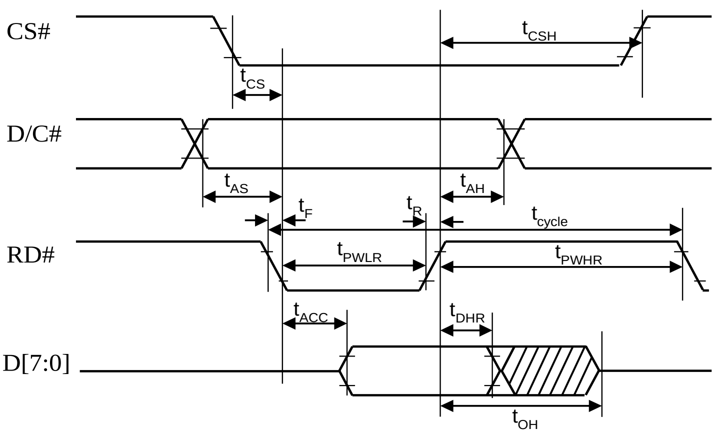
(V_{DD} - V_{SS} = 1.65V ~3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
t_{PWLR}	Read Low Time	180	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 9-2: 8080-series parallel interface characteristics



Write Cycle



Read Cycle

Table 9-4: Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 9-3: Serial interface characteristics (4-wire SPI)

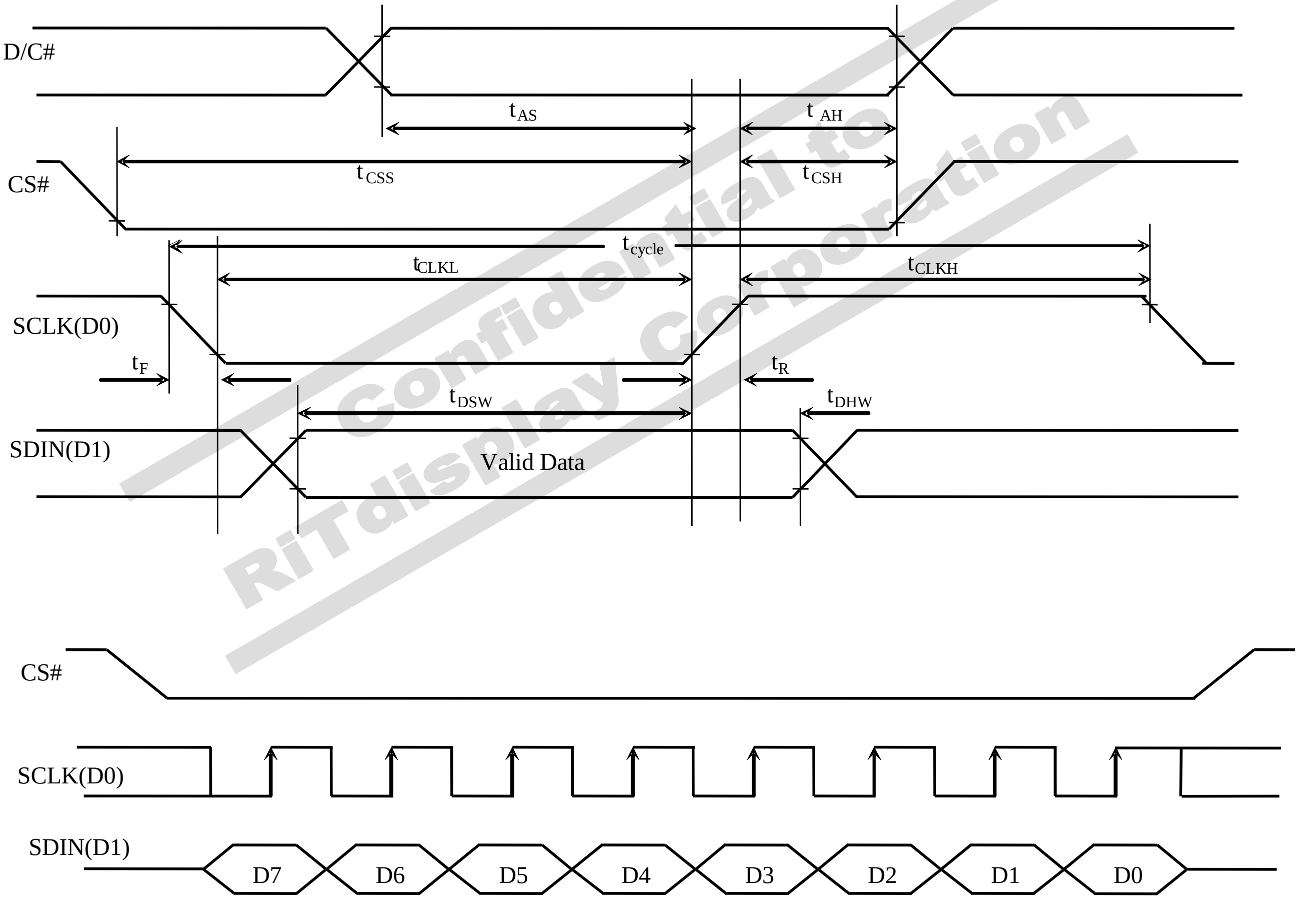


Table 9-5: Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 1.65V~3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 9-4: Serial interface characteristics (3-wire SPI)

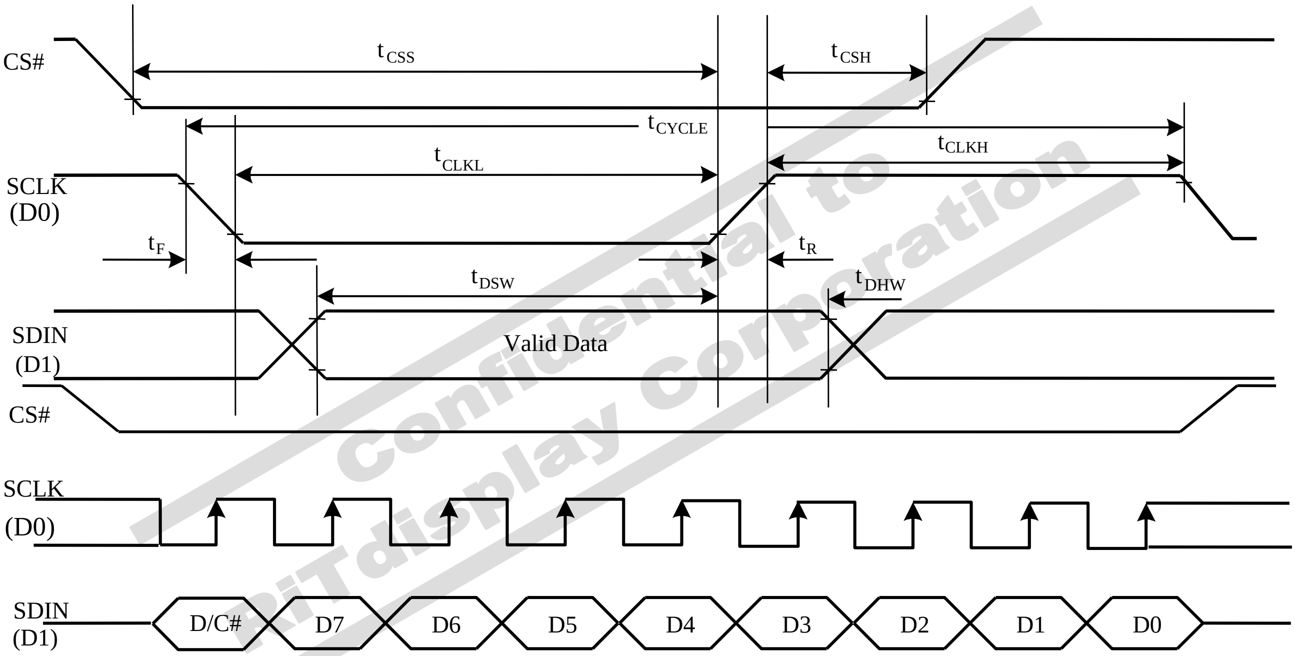
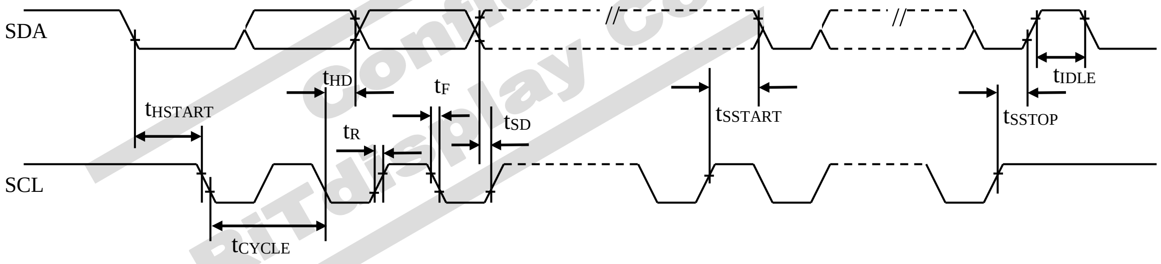


Table 9-6: I2C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

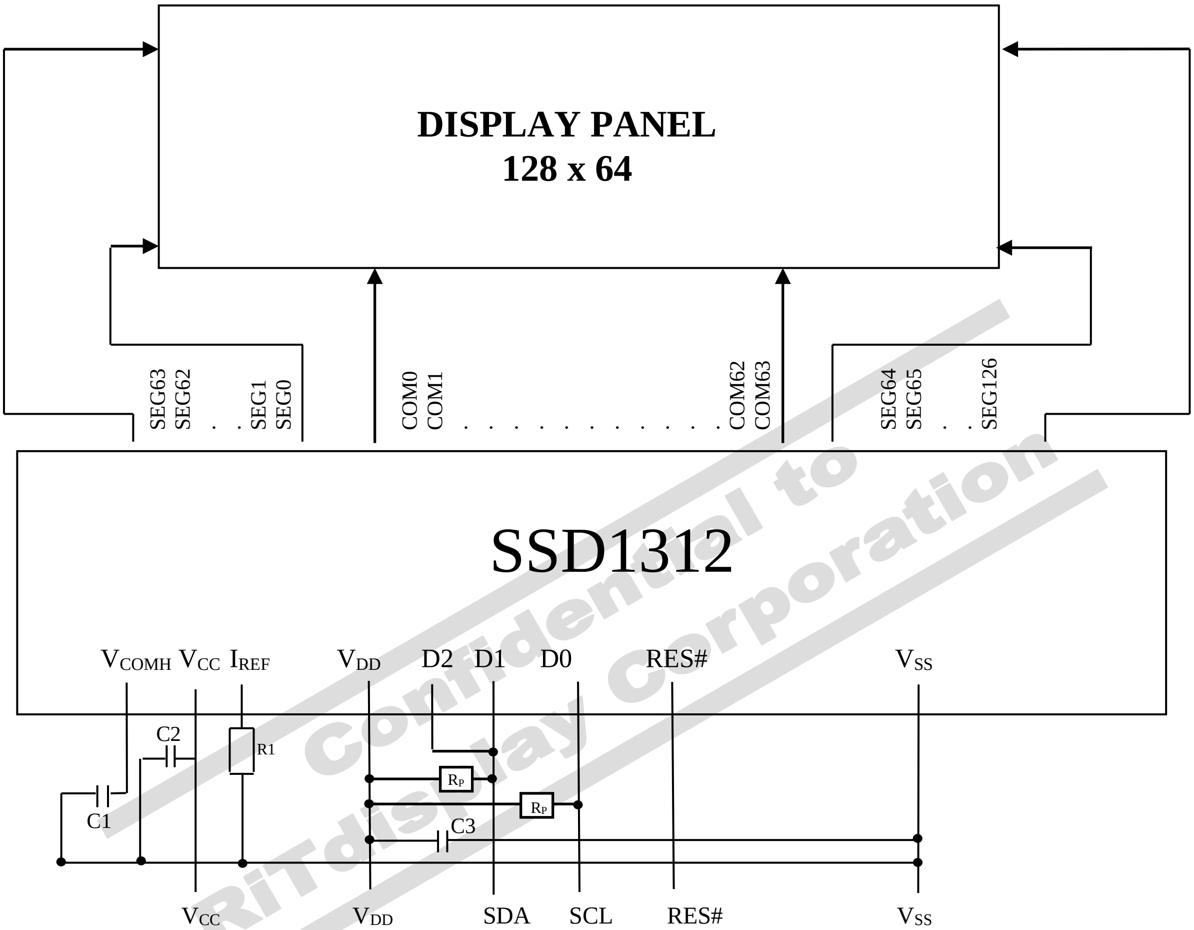
Figure 9-5 I2C interface Timing characteristics



10 APPLICATION EXAMPLE

Figure 10-1: Application Example of SSD1312 with External V_{CC} and I^2C interface

The configuration for I^2C interface mode is shown in the following diagram:
(V_{DD}= 2.8V, V_{CC} =12V, I_{REF} =10uA)



Pin connected to MCU interface: RES#, SDA, SCL
Pin internally connected to V_{SS} / V_{LL}: BS0, BS2, CL, D[7:3], E, R/W#, CS#, D/C#, BGGND
Pin internally connected to V_{DD} / V_{LH}: BS1, CLS
$V_{BAT,}$ C1P, C1N, C2P, C2N, FR should be left open.

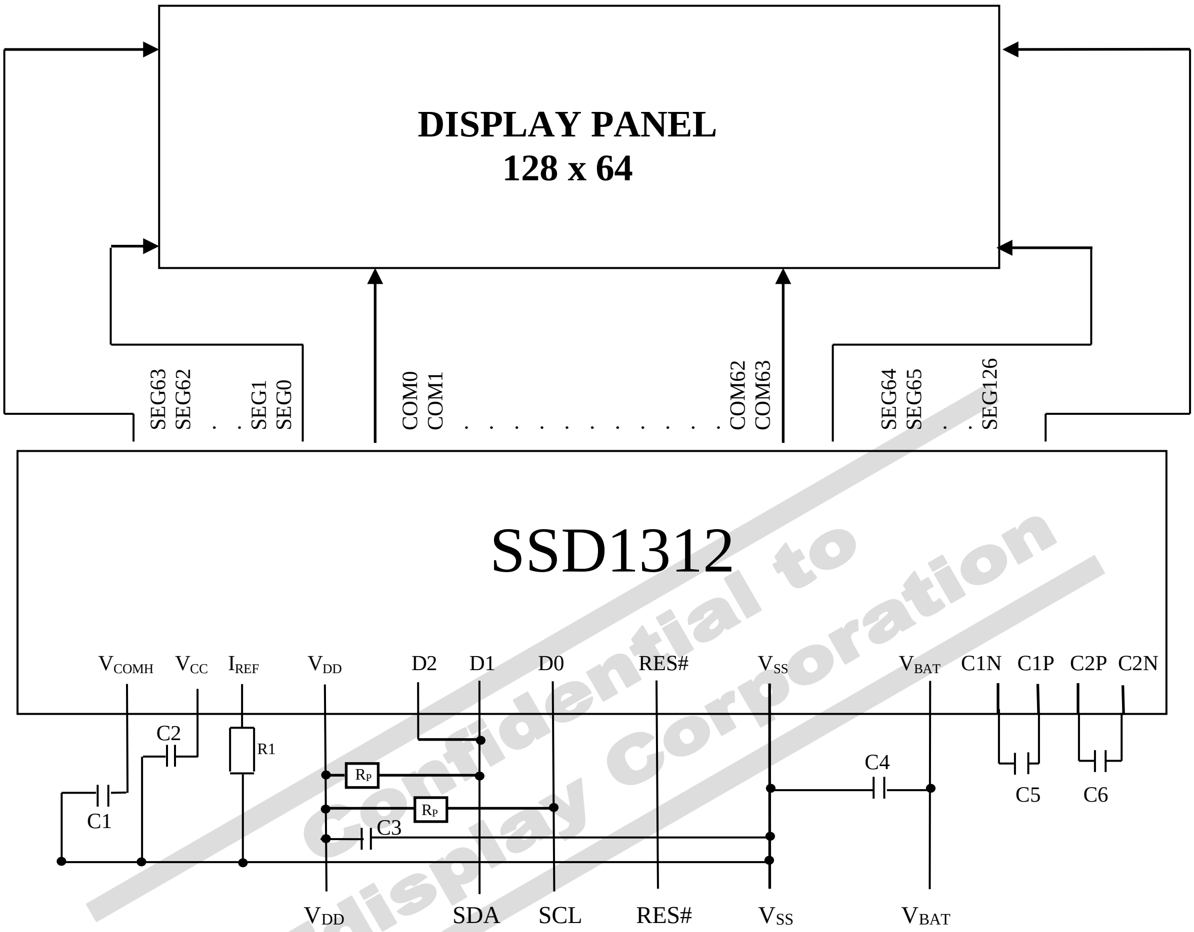
C1, C2: 2.2uF [(1)]
C3: 1.0uF [(1)]
R_P: Pull up resistor

Voltage at I_{REF} = V_{CC} – 2V. For V_{CC} = 12V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (12-2)V / 10uA
= 1MΩ

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) V_{LSS} of IC pad no. 34-37 are recommended to be connected to the V_{LSS} of pad no. 97-100 to form a larger area of GND.
(3) V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

Figure 10-2: Application Example of SSD1312 with Internal Charge Pump and I²C interface

The configuration for I²C interface mode is shown in the following diagram:
(V_{DD}= 1.65V ~ 3.5V, V_{BAT}=3.0V~4.5V, I_{REF}=10uA)



Pin connected to MCU interface: RES#, SDA, SCL
Pin internally connected to V_{SS} / V_{LL}: BS0, BS2, CL, D[7:3], E, R/W#, CS#, D/C#, BGGND
Pin internally connected to V_{DD} / V_{LH}: BS1, CLS
FR should be left open.

C1, C2: 2.2uF (1)
C3, C4 : 1.0uF (1)
C5, C6: 1.0uF/10V (1)
R_P: Pull up resistor

Voltage at I_{REF} = V_{CC} – 2V. For V_{CC} = 7.5V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (7.5-2)V / 10uA
≈ 550KΩ

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) V_{LSS} of IC pad no. 34-37 are recommended to be connected to the V_{LSS} of pad no. 94-100 to form a larger area of GND.
(3) V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard GB/T 26572-2011 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)". Hazardous Substances test report is available upon request.

http://www.solomon-systech.com

Appendix III: SSD1312 Command Table and Command Descriptions

1 COMMAND TABLE

Table 1-1: SSD1312 Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

<table>
<tr><th colspan="12">Fundamental Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>00~0F</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X_3</td><td>X_2</td><td>X_1</td><td>X_0</td><td>Set Lower Column Start Address for Page Addressing Mode</td><td>Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.

Note
(1) This command is only for page addressing mode</td></tr>
<tr><td>0</td><td>10~17</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>X_2</td><td>X_1</td><td>X_0</td><td>Set Higher Column Start Address for Page Addressing Mode</td><td>Set the higher nibble of the column start address register for Page Addressing Mode using X[2:0] as data bits. The initial display line register is reset to 0000b after RESET.

Note
(1) This command is only for page addressing mode</td></tr>
<tr><td>0
0</td><td>20
A[3]
A[1:0]</td><td>0
*</td><td>0
*</td><td>1
*</td><td>0
*</td><td>0
A_3</td><td>0
*</td><td>0
A_1</td><td>0
A_0</td><td>Set Memory Addressing Mode</td><td><table><tr><td>A[3]</td><td>A[1:0]</td><td>Addressing Modes</td></tr><tr><td>0b</td><td>01b</td><td>COM-Page H-Mode</td></tr><tr><td>0b</td><td>10b</td><td>Page Addressing Mode (RESET)</td></tr><tr><td>1b</td><td>01b</td><td>SEG-Page H-Mode</td></tr></table>
Note
(1) Setting other than the above table is invalid.</td></tr>
<tr><td>0
0
0</td><td>21
A[6:0]
B[6:0]</td><td>0
*
*</td><td>0
A_6
B_6</td><td>1
A_5
B_5</td><td>0
A_4
B_4</td><td>0
A_3
B_3</td><td>0
A_2
B_2</td><td>0
A_1
B_1</td><td>1
A_0
B_0</td><td>Set Line Address</td><td>Setup line start and end address

In COM-Page H-mode,
A[6:0] : Set Row start address,
range : 0-127d, (RESET=0d)
B[6:0]: Set Row end address,
range : 0-127d, (RESET =127d)

In SEG-Page H-mode,
A[6:0] : Set Column start address,
range : 0-63d, (RESET=0d)
B[6:0]: Set Column end address,
range : 0-63d, (RESET=63d)

Note
(1) This command is only for COM-Page H-mode and SEG-Page H-mode.
(2) Column defines the graphic display data RAM column (along COM direction) while Row defines the Graphic display data RAM row (along SEG direction).</td></tr>
</table>

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	22 A[3:0] B[3:0]	0 * *	0 * *	1 * *	0 * *	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address In COM-Page H-mode, A[4:0] : Set COM-Page start Address, range 0-7d, (RESET = 0d) B[4:0]: Set COM-Page end address, range : 0-7d, (RESET = 7d) In SEG-Page H-mode, A[4:0] : Set SEG-Page start Address, range 0-15d, (RESET = 0d) B[4:0]: Set SEG-Page end address, range : 0-15d, (RESET = 15d) **Note** (1) This command is only for COM-Page H-mode and SEG-Page H-mode. (2) The Page in SEG-Page is a transpose of the Page in COM-Page mode. Page in COM-Page mode defines a group of 8-bit COM data on the same SEG line, while Page in SEG-Page mode defines a group of 8-bit SEG data in the same COM line.
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5 X_4X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select one of the contrast steps. Contrast increases as the value increases. (RESET = 7Fh) A[7:0] valid range: 01h to FFh
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 128 is mapped to SEG0
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX. RESET= 11 1111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0 0	AD A[4]	1 0	0 1	1 0	0 A_4	1 0	1 0	0 0	1 0	External or internal I_{REF} Selection	Select external or internal I_{REF} : A[4] = ‘0’ Select external I_{REF} (RESET) A[4] = ‘1’ Enable internal I_{REF} during display ON **Note** (1) Refer to section 6.8 in SSD1312 datasheet for details.
0	AE/AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address PAGE0~PAGE7 for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set line shift by COM from 0d~63d The value is reset to 00h after RESET.
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0]: Define divide ratio (D) of display clock (DCLK) (i.e. 1, 2, 3, …, 16) (RESET is 0000b, i.e. divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (RESET is 1000b) Range: 0000b~1111b.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 30 DCLK (i.e. 2, 4, 6, …30) Clock 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 30 DCLK (i.e. 2, 4, 6, …30) Clock 0 is invalid entry (RESET=2h)

<table>
<tr><th colspan="12">Fundamental Command Table</th></tr>
<tr><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0
0</td><td>DA
A[5:4]</td><td>1
0</td><td>1
0</td><td>0
A_5</td><td>1
A_4</td><td>1
0</td><td>0
0</td><td>1
0</td><td>0
0</td><td>Set SEG Pins Hardware Configuration</td><td>A[4]=0b, Sequential SEG pin configuration
A[4]=1b (RESET), Alternative (odd/even) SEG pin configuration

A[5]=0b (RESET), Disable SEG Left/Right remap
A[5]=1b, Enable SEG Left/Right remap</td></tr>
<tr><td>0
0</td><td>DB
A[5:3]</td><td>1
0</td><td>1
0</td><td>0
A_5</td><td>1
A_4</td><td>1
0</td><td>0
0</td><td>1
0</td><td>1
0</td><td>Set V_{COMH} select Level</td><td>Set COM select voltage level.<table>
<tr><th>A[5:4]</th><th>Hex code</th><th>V_{COMH} deselect level</th></tr>
<tr><td>00b</td><td>00h</td><td>~ 0.65 x V_{CC}</td></tr>
<tr><td>01b</td><td>10h</td><td>~ 0.71 x V_{CC}</td></tr>
<tr><td>10b</td><td>20h</td><td>~ 0.77 x V_{CC} (RESET)</td></tr>
<tr><td>11b</td><td>30h</td><td>~ 0.83 x V_{CC}</td></tr>
</table></td></tr>
<tr><td>0</td><td>E3</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>NOP</td><td>Command for no operation</td></tr>
<tr><td>0
0</td><td>8D
A[7:0]</td><td>1
A_7</td><td>0
A_6</td><td>0
A_5</td><td>0
1</td><td>1
0</td><td>1
0</td><td>0
A_1</td><td>1
0</td><td>Charge Pump Setting</td><td>Enable / Disable internal charge pump:
A[2] = 0b, Disable charge pump (RESET)
A[2] = 1b, Enable charge pump during display on<table>
<tr><th>A[7:5]</th><th>Hex code</th><th>Charge Pump Mode</th></tr>
<tr><td>000b</td><td>12h</td><td>7.5V (RESET)</td></tr>
<tr><td>010b</td><td>52h</td><td>8.0V</td></tr>
<tr><td>011b</td><td>72h</td><td>9.0V</td></tr>
<tr><td>100b</td><td>92h</td><td>10.0V</td></tr>
</table>Note
(1) The Charge Pump must be enabled by the following command sequence:
8Dh ; Charge Pump Setting
12h / 52h / 72h / 92h ; Enable Charge Pump
AFh; Display ON</td></tr>
<tr><td>0
0</td><td>FD
A[2]</td><td>1
0</td><td>1
0</td><td>1
0</td><td>1
1</td><td>1
0</td><td>1
A_2</td><td>0
1</td><td>1
0</td><td>Set Command Lock</td><td>A[2]: MCU protection status.

A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET)
A[2] = 1b, Lock OLED driver IC MCU interface from entering command

Note
(1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command</td></tr>
</table>

Note

(1) “*” stands for “Don’t care”.

Table 1-2 : Read Command Table

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D[7] : Reserved D[6] : "1" for display OFF / "0" for display ON D[5] : Reserved D[4] : Reserved D[3] : Reserved D[2] : Reserved D[1] : Reserved D[0] : Reserved

Note

(1) Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

1.1 Data Read / Write

To read data from the GDDRAM, select HIGH for both the R/W# (WR#) pin and the D/C# pin for 6800-series parallel mode and select LOW for the E (RD#) pin and HIGH for the D/C# pin for 8080-series parallel mode. No data read is provided in serial mode operation.
In normal data read mode the GDDRAM column address pointer will be increased automatically by one after each data read.
Also, a dummy read is required before the first data read.
To write data to the GDDRAM, select LOW for the R/W# (WR#) pin and HIGH for the D/C# pin for both 6800-series parallel mode and 8080-series parallel mode. The serial interface mode is always in write mode. The GDDRAM column address pointer will be increased automatically by one after each data write.

Table 1-3 : Address increment table (Automatic)

D/C#	R/W# (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

2 COMMAND DESCRIPTIONS

2.1 Fundamental Command

2.1.1 Set Lower Column Start Address for Page Addressing Mode (00h~0Fh)

This command specifies the lower nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 1-1 and Section 2.1.3 for details.

2.1.2 Set Higher Column Start Address for Page Addressing Mode (10h~17h)

This command specifies the higher nibble of the 8-bit column start address for the display data RAM under Page Addressing Mode. The column address will be incremented by each data access. Please refer to Table 1-1 and Section 2.1.3 for details.

2.1.3 Set Memory Addressing Mode (20h)

There are different memory addressing modes in SSD1312: page addressing mode, COM-Page H-mode and SEG-Page H-mode. User can sets the way of memory addressing by command 20h.

<u>Page addressing mode (A[3:0]=0010b)</u>

In page addressing mode, after the display RAM is read / written, the column address pointer is increased automatically by 1 and page address pointer is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. The sequence of movement of the PAGE and column address point for page addressing mode is shown in Figure 2-1.

Figure 2-1 : Address Pointer Movement of Page addressing mode

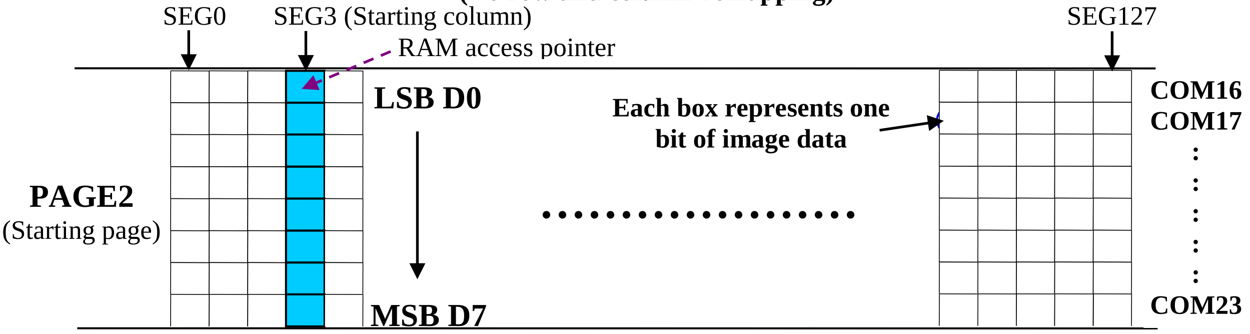
	COL0	COL 1	…..	COL 126	COL 127
PAGE0					
PAGE1					
:					
PAGE6					
PAGE7					

In normal display data RAM read or write and page addressing mode, the following steps are required to define the starting RAM access pointer location:

- Set the page start address of the target display location by command B0h.
- Set the lower start column address of pointer by command 00h~0Fh.
- Set the higher start column address of pointer by command 10h~17h.

For example, if the page start address is set to B0h 02h, lower column address is 03h and higher column address is 10h, then that means the starting column is SEG3 of PAGE2. The RAM access pointer is located as shown in Figure 2-3. The input data byte will be written into RAM position of column 3.

Figure 2-2 : Example of GDDRAM access pointer setting in Page Addressing Mode (No row and column-remapping)



COM-Page and SEG-Page

SEG-Page provides a flexibility to transpose the RAM write orientation from COM-Page. Page in COM-Page mode defines a group of 8-bit COM data on the same SEG line, while Page in SEG-Page mode defines a group of 8-bit SEG data in the same COM line. The term "COL" means the graphic display data RAM column (along COM direction) while "ROW" means the graphic display data RAM row (along SEG direction). Figure 2-3 and Figure 2-4 show the RAM orientation of a Page in COM-Page mode and SEG-Page mode respectively.

Figure 2-3 : GDDRAM access pointer setting and orientation (No row and column-remapping) in COM-Page Mode

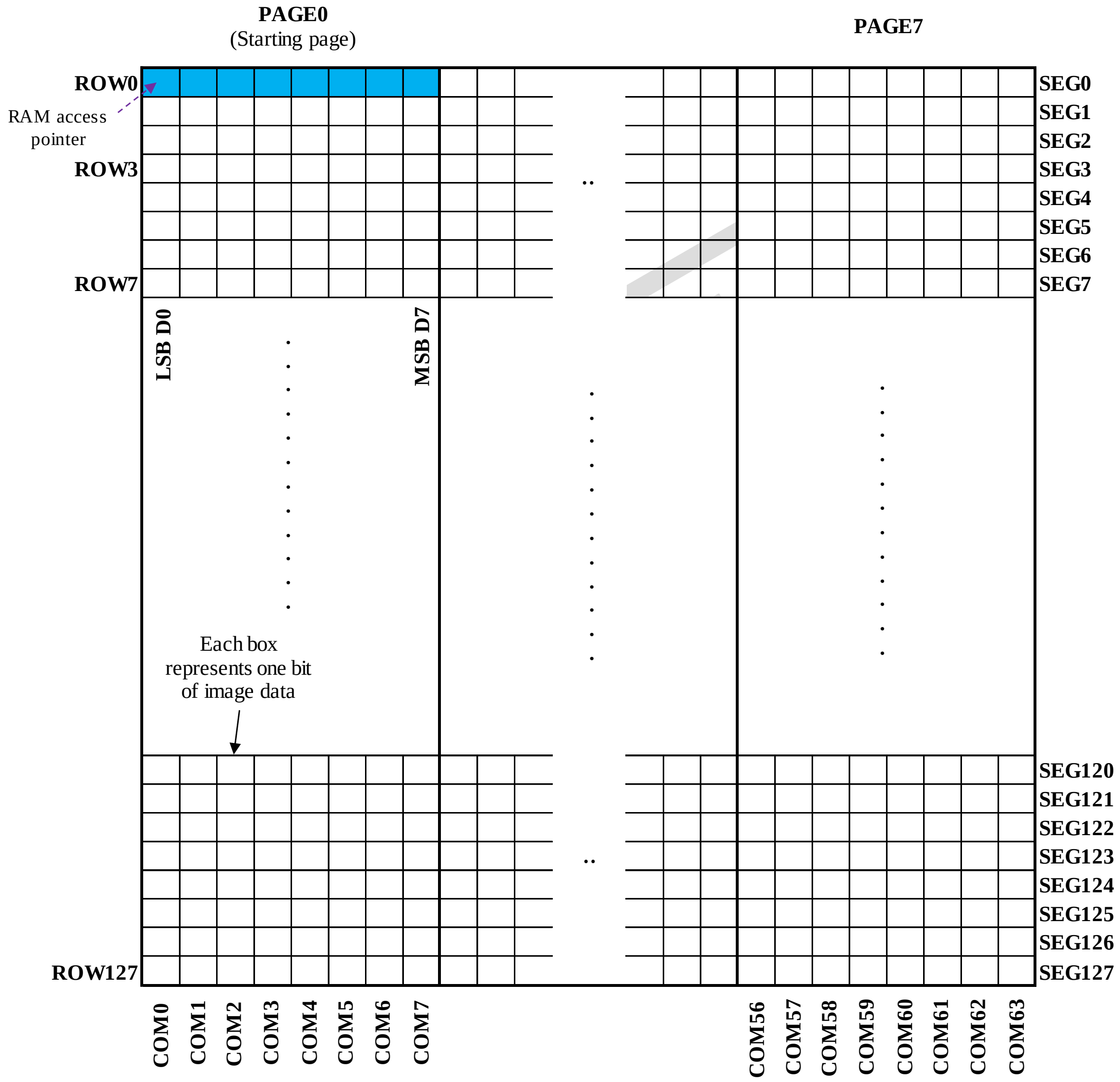
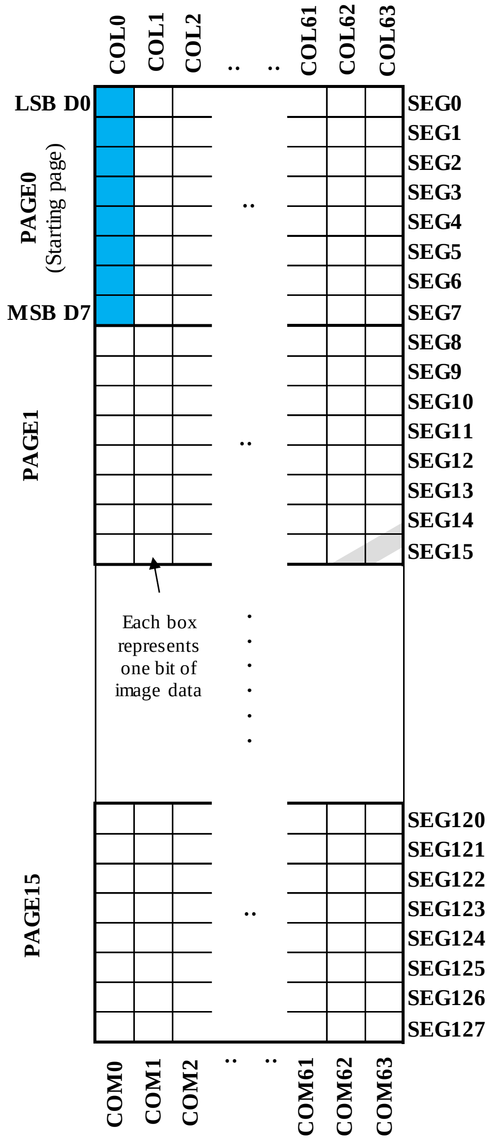


Figure 2-4 : GDDRAM access pointer setting and orientation (No row and column-remapping) in SEG-Page Mode



COM-Page H-mode (A[3:0]=0001b)

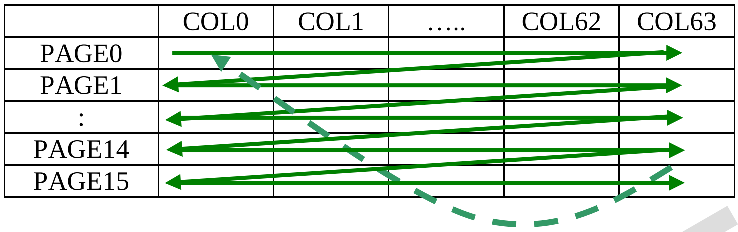
In COM-Page H-mode, after the display RAM is read / written, the page (COM-Page) address pointer is increased automatically by 1. If the page address pointer reaches the page end address, the page address pointer is reset to page start address and row (line) address pointer is increased by 1. The sequence of movement of the page and row address point for COM-Page H-mode is shown in Figure 2-5. When both row and page address pointers reach the end address, the pointers are reset to row start address and page start address (Dotted line in Figure 2-5.)

Figure 2-5 : Address Pointer Movement of COM-Page H-mode

	PAGE0	PAGE1	…..	PAGE6	PAGE7
ROW0					
ROW1					
:					
ROW126					
ROW127					

SEG-Page H-mode (A[3:0]=1001b)
In SEG-Page H-mode, the column (line) address pointer increased automatically by 1 every time the display RAM is written. The column address pointer reset to column start address and page (SEG-Page) address pointer is increased by 1 if the column address pointer reaches column end address. The column address and page address pointers are reset to column start address and page start address if both column and page address pointers reach the end address. The sequence of movement of the page and column address pointer for SEG-Page H-mode is shown in Figure 2-6.

Figure 2-6 : Address Pointer Movement of SEG-Page H-mode



In normal display data RAM read or write in COM-Page or SEG-Page mode, the following steps are required to define the RAM access pointer location:

- Set the line start and end address of the target display location by command 21h.
- Set the page start and end address of the target display location by command 22h.

Example is shown in Figure 2-7.

2.1.4 Set Line Address (21h)

This triple byte command specifies line start address and end address of the display data RAM. This command also sets the row address pointer to row start address in COM-Page mode and sets the column address pointer to column start address in SEG-Page mode. This pointer is used to define the current read/write line address in graphic display data RAM. If COM-Page H mode or SEG-Page H-mode is enabled by command 20h, after finishing read/write one line data (one row in COM-Page H-mode or one column in SEG-Page H-mode), it is incremented automatically to the next line address. Whenever the line address pointer finishes accessing the end line address, it is reset back to start line address and the page address is incremented to the next page.

2.1.5 Set Page Address (22h)

This triple byte command specifies page start address and end address of the display data RAM. This command also sets the page address pointer to page start address. This pointer is used to define the current read/write page address in graphic display data RAM. If COM-Page H-mode or SEG-Page H-mode is enabled by command 20h, after finishing read/write one page data, it is incremented automatically to the next page address. Whenever the page address pointer finishes accessing the end page address, it is reset back to start page address.

The figure below shows the way of line (row or column) and page address pointer movement in COM-Page H-mode through the example: page start address is set to 1 and page end address is set to 5, row start address is set to 2 and row end address is set to 97; COM-Page H-mode is enabled by command 20h. In this case, the graphic display data RAM row accessible range is from page 1 to page 5 and from row 2 to row 97 only. In addition, the page address pointer is set to 1 and row address pointer is set to 2. After finishing read/write one pixel of data, the page address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 2-7*). Whenever the page address pointer finishes accessing the end page 5, it is reset back to page 1 and row address is automatically increased by 1 (*solid line in Figure 2-7*). While the end page 5 and end row 97 RAM location is accessed, the page address is reset back to 1 and the row address is reset back to 2 (*dotted line in Figure 2-7*).

Figure 2-7: Example of Address Pointer Movement

	PAGE0	PAGE1	PAGE2	…..	PAGE5	PAGE6	PAGE7
Row 0							
Row 1							
Row 2							
:							
:							
Row 97							
Row98							
:							
Row 126							
Row 127							

2.1.6 Set Display Start Line (40h~7Fh)

This command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 63. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on. Refer to Table 2-1 for more illustrations.

2.1.7 Set Contrast Control (81h)

This command sets the Contrast Setting of the display, with a valid range from 01h to FFh. The segment output current increases as the contrast step value increase.

2.1.8 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design. Please refer to Table 1-1.

This command only affects subsequent data input. Data already stored in GDDRAM will have no changes.

2.1.9 Entire Display ON (A4h/A5h)

A4h command enable display outputs according to the GDDRAM contents.
If A5h command is issued, then by using A4h command, the display will resume to the GDDRAM contents.
In other words, A4h command resumes the display from entire display “ON” stage.
A5h command forces the entire display to be “ON”, regardless of the contents of the display data RAM.

2.1.10 Set Normal/Inverse Display (A6h/A7h)

This command sets the display to be either normal or inverse. In normal display a RAM data of 1 indicates an “ON” pixel while in inverse display a RAM data of 0 indicates an “ON” pixel.

2.1.11 Set Multiplex Ratio (A8h)

This command switches the default 64 multiplex mode to any multiplex ratio, ranging from 16 to 63. The output pads COM0~COM63 will be switched to the corresponding COM signal.

2.1.12 External or internal IREF Selection (ADh)

This double byte command supports External or Internal I_{REF} Selection.

Default A[4] = ’0’, Select external I_{REF}.

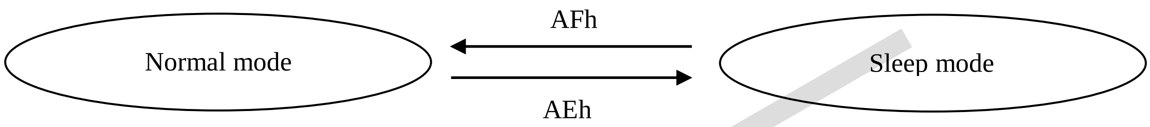
When A[4] = ’1’, Select internal I_{REF} during display ON.

2.1.13 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- AEh : Display OFF
- AFh : Display ON

Figure 2-8 : Transition between different modes



2.1.14 Set Page Start Address for Page Addressing Mode (B0h~B7h)

This command positions the page start address from 0 to 15 in GDDRAM under Page Addressing Mode. Please refer to Table 1-1 and Section 2.1.3 for details.

2.1.15 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately. Please refer to Table 2-3 for details.

2.1.16 Set Display Offset (D3h)

This is a double byte command. The second command specifies the mapping of the display start line to one of COM0~COM63 (assuming that COM0 is the display start line then the display start line register is equal to 0).

For example, to move the COM16 towards the COM0 direction by 16 lines the 6-bit data in the second byte should be given as 010000b. To move in the opposite direction by 16 lines the 6-bit data should be given by 64 – 16, so the second byte would be 110000b. The following two tables (Table 2-1 and Table 2-2) show the examples of setting the command C0h/C8h and D3h.

Table 2-1: Example of Set Display Offset and Display Start Line without Remap

	Output												
	64		64		64		56		56		56		Set MUX ratio(A8h)
	Normal		Normal		Normal		Normal		Normal		Normal		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		Display offset (D3h)
pin name	0		0		8		0		0		8		Display start line (40h - 7Fh)
COM0	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row0	RAM0	Row8	RAM8	Row0	RAM8	
COM1	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row1	RAM1	Row9	RAM9	Row1	RAM9	
COM2	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row2	RAM2	Row10	RAM10	Row2	RAM10	
COM3	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row3	RAM3	Row11	RAM11	Row3	RAM11	
COM4	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row4	RAM4	Row12	RAM12	Row4	RAM12	
COM5	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row5	RAM5	Row13	RAM13	Row5	RAM13	
COM6	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row6	RAM6	Row14	RAM14	Row6	RAM14	
COM7	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row7	RAM7	Row15	RAM15	Row7	RAM15	
COM8	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row8	RAM8	Row16	RAM16	Row8	RAM16	
COM9	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row9	RAM9	Row17	RAM17	Row9	RAM17	
COM10	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row10	RAM10	Row18	RAM18	Row10	RAM18	
COM11	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row11	RAM11	Row19	RAM19	Row11	RAM19	
COM12	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row12	RAM12	Row20	RAM20	Row12	RAM20	
COM13	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row13	RAM13	Row21	RAM21	Row13	RAM21	
COM14	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row14	RAM14	Row22	RAM22	Row14	RAM22	
COM15	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row15	RAM15	Row23	RAM23	Row15	RAM23	
COM16	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row16	RAM16	Row24	RAM24	Row16	RAM24	
COM17	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row17	RAM17	Row25	RAM25	Row17	RAM25	
COM18	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row18	RAM18	Row26	RAM26	Row18	RAM26	
COM19	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row19	RAM19	Row27	RAM27	Row19	RAM27	
COM20	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row20	RAM20	Row28	RAM28	Row20	RAM28	
COM21	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row21	RAM21	Row29	RAM29	Row21	RAM29	
COM22	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row22	RAM22	Row30	RAM30	Row22	RAM30	
COM23	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row23	RAM23	Row31	RAM31	Row23	RAM31	
COM24	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row24	RAM24	Row32	RAM32	Row24	RAM32	
COM25	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row25	RAM25	Row33	RAM33	Row25	RAM33	
COM26	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row26	RAM26	Row34	RAM34	Row26	RAM34	
COM27	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row27	RAM27	Row35	RAM35	Row27	RAM35	
COM28	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row28	RAM28	Row36	RAM36	Row28	RAM36	
COM29	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row29	RAM29	Row37	RAM37	Row29	RAM37	
COM30	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row30	RAM30	Row38	RAM38	Row30	RAM38	
COM31	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row31	RAM31	Row39	RAM39	Row31	RAM39	
COM32	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row32	RAM32	Row40	RAM40	Row32	RAM40	
COM33	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row33	RAM33	Row41	RAM41	Row33	RAM41	
COM34	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row34	RAM34	Row42	RAM42	Row34	RAM42	
COM35	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row35	RAM35	Row43	RAM43	Row35	RAM43	
COM36	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row36	RAM36	Row44	RAM44	Row36	RAM44	
COM37	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row37	RAM37	Row45	RAM45	Row37	RAM45	
COM38	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row38	RAM38	Row46	RAM46	Row38	RAM46	
COM39	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row39	RAM39	Row47	RAM47	Row39	RAM47	
COM40	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row40	RAM40	Row48	RAM48	Row40	RAM48	
COM41	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row41	RAM41	Row49	RAM49	Row41	RAM49	
COM42	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row42	RAM42	Row50	RAM50	Row42	RAM50	
COM43	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row43	RAM43	Row51	RAM51	Row43	RAM51	
COM44	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row44	RAM44	Row52	RAM52	Row44	RAM52	
COM45	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row45	RAM45	Row53	RAM53	Row45	RAM53	
COM46	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row46	RAM46	Row54	RAM54	Row46	RAM54	
COM47	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row47	RAM47	Row55	RAM55	Row47	RAM55	
COM48	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row48	RAM48	-	-	Row48	RAM56	
COM49	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row49	RAM49	-	-	Row49	RAM57	
COM50	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row50	RAM50	-	-	Row50	RAM58	
COM51	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row51	RAM51	-	-	Row51	RAM59	
COM52	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row52	RAM52	-	-	Row52	RAM60	
COM53	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row53	RAM53	-	-	Row53	RAM61	
COM54	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row54	RAM54	-	-	Row54	RAM62	
COM55	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row55	RAM55	-	-	Row55	RAM63	
COM56	Row56	RAM56	Row0	RAM0	Row56	RAM0	-	-	Row0	RAM0	-	-	
COM57	Row57	RAM57	Row1	RAM1	Row57	RAM1	-	-	Row1	RAM1	-	-	
COM58	Row58	RAM58	Row2	RAM2	Row58	RAM2	-	-	Row2	RAM2	-	-	
COM59	Row59	RAM59	Row3	RAM3	Row59	RAM3	-	-	Row3	RAM3	-	-	
COM60	Row60	RAM60	Row4	RAM4	Row60	RAM4	-	-	Row4	RAM4	-	-	
COM61	Row61	RAM61	Row5	RAM5	Row61	RAM5	-	-	Row5	RAM5	-	-	
COM62	Row62	RAM62	Row6	RAM6	Row62	RAM6	-	-	Row6	RAM6	-	-	
COM63	Row63	RAM63	Row7	RAM7	Row63	RAM7	-	-	Row7	RAM7	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		

(a)

(b)

(c)

(d)

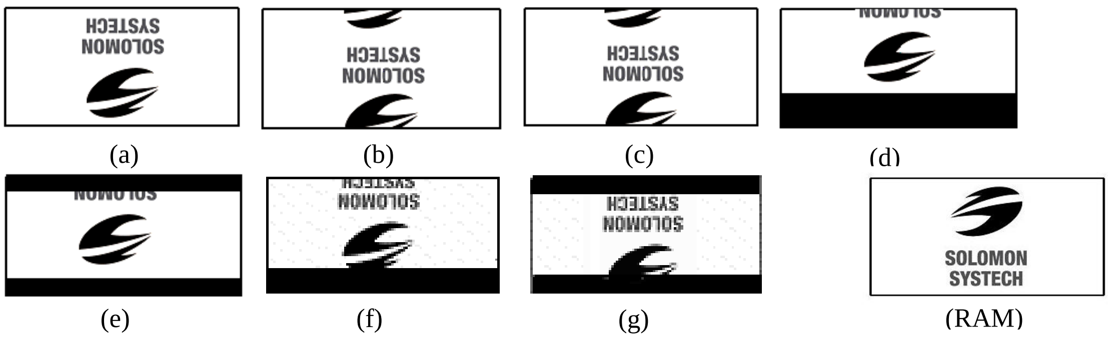
(e)

(f)

(RAM)

Table 2-2: Example of Set Display Offset and Display Start Line with Remap

	Output														
	64		64		64		48		48		48		48		Set MUX ratio(A8h)
	Remap		Remap		Remap		Remap		Remap		Remap		Remap		COM Normal / Remapped (C0h / C8h)
Hardware	0		8		0		0		8		0		8		Display offset (D3h)
pin name	0		0		8		0		0		8		16		Display start line (40h - 7Fh)
COM0	Row63	RAM63	Row7	RAM7	Row63	RAM7	Row47	RAM47	-	-	Row47	RAM55	-	-	
COM1	Row62	RAM62	Row6	RAM6	Row62	RAM6	Row46	RAM46	-	-	Row46	RAM54	-	-	
COM2	Row61	RAM61	Row5	RAM5	Row61	RAM5	Row45	RAM45	-	-	Row45	RAM53	-	-	
COM3	Row60	RAM60	Row4	RAM4	Row60	RAM4	Row44	RAM44	-	-	Row44	RAM52	-	-	
COM4	Row59	RAM59	Row3	RAM3	Row59	RAM3	Row43	RAM43	-	-	Row43	RAM51	-	-	
COM5	Row58	RAM58	Row2	RAM2	Row58	RAM2	Row42	RAM42	-	-	Row42	RAM50	-	-	
COM6	Row57	RAM57	Row1	RAM1	Row57	RAM1	Row41	RAM41	-	-	Row41	RAM49	-	-	
COM7	Row56	RAM56	Row0	RAM0	Row56	RAM0	Row40	RAM40	-	-	Row40	RAM48	-	-	
COM8	Row55	RAM55	Row63	RAM63	Row55	RAM63	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row47	RAM63	
COM9	Row54	RAM54	Row62	RAM62	Row54	RAM62	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row46	RAM62	
COM10	Row53	RAM53	Row61	RAM61	Row53	RAM61	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row45	RAM61	
COM11	Row52	RAM52	Row60	RAM60	Row52	RAM60	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row44	RAM60	
COM12	Row51	RAM51	Row59	RAM59	Row51	RAM59	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row43	RAM59	
COM13	Row50	RAM50	Row58	RAM58	Row50	RAM58	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row42	RAM58	
COM14	Row49	RAM49	Row57	RAM57	Row49	RAM57	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row41	RAM57	
COM15	Row48	RAM48	Row56	RAM56	Row48	RAM56	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row40	RAM56	
COM16	Row47	RAM47	Row55	RAM55	Row47	RAM55	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row39	RAM55	
COM17	Row46	RAM46	Row54	RAM54	Row46	RAM54	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row38	RAM54	
COM18	Row45	RAM45	Row53	RAM53	Row45	RAM53	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row37	RAM53	
COM19	Row44	RAM44	Row52	RAM52	Row44	RAM52	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row36	RAM52	
COM20	Row43	RAM43	Row51	RAM51	Row43	RAM51	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row35	RAM51	
COM21	Row42	RAM42	Row50	RAM50	Row42	RAM50	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row34	RAM50	
COM22	Row41	RAM41	Row49	RAM49	Row41	RAM49	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row33	RAM49	
COM23	Row40	RAM40	Row48	RAM48	Row40	RAM48	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row32	RAM48	
COM24	Row39	RAM39	Row47	RAM47	Row39	RAM47	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row31	RAM47	
COM25	Row38	RAM38	Row46	RAM46	Row38	RAM46	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row30	RAM46	
COM26	Row37	RAM37	Row45	RAM45	Row37	RAM45	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row29	RAM45	
COM27	Row36	RAM36	Row44	RAM44	Row36	RAM44	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row28	RAM44	
COM28	Row35	RAM35	Row43	RAM43	Row35	RAM43	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row27	RAM43	
COM29	Row34	RAM34	Row42	RAM42	Row34	RAM42	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row26	RAM42	
COM30	Row33	RAM33	Row41	RAM41	Row33	RAM41	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row25	RAM41	
COM31	Row32	RAM32	Row40	RAM40	Row32	RAM40	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row24	RAM40	
COM32	Row31	RAM31	Row39	RAM39	Row31	RAM39	Row15	RAM15	Row23	RAM23	Row15	RAM23	Row23	RAM39	
COM33	Row30	RAM30	Row38	RAM38	Row30	RAM38	Row14	RAM14	Row22	RAM22	Row14	RAM22	Row22	RAM38	
COM34	Row29	RAM29	Row37	RAM37	Row29	RAM37	Row13	RAM13	Row21	RAM21	Row13	RAM21	Row21	RAM37	
COM35	Row28	RAM28	Row36	RAM36	Row28	RAM36	Row12	RAM12	Row20	RAM20	Row12	RAM20	Row20	RAM36	
COM36	Row27	RAM27	Row35	RAM35	Row27	RAM35	Row11	RAM11	Row19	RAM19	Row11	RAM19	Row19	RAM35	
COM37	Row26	RAM26	Row34	RAM34	Row26	RAM34	Row10	RAM10	Row18	RAM18	Row10	RAM18	Row18	RAM34	
COM38	Row25	RAM25	Row33	RAM33	Row25	RAM33	Row9	RAM9	Row17	RAM17	Row9	RAM17	Row17	RAM33	
COM39	Row24	RAM24	Row32	RAM32	Row24	RAM32	Row8	RAM8	Row16	RAM16	Row8	RAM16	Row16	RAM32	
COM40	Row23	RAM23	Row31	RAM31	Row23	RAM31	Row7	RAM7	Row15	RAM15	Row7	RAM15	Row15	RAM31	
COM41	Row22	RAM22	Row30	RAM30	Row22	RAM30	Row6	RAM6	Row14	RAM14	Row6	RAM14	Row14	RAM30	
COM42	Row21	RAM21	Row29	RAM29	Row21	RAM29	Row5	RAM5	Row13	RAM13	Row5	RAM13	Row13	RAM29	
COM43	Row20	RAM20	Row28	RAM28	Row20	RAM28	Row4	RAM4	Row12	RAM12	Row4	RAM12	Row12	RAM28	
COM44	Row19	RAM19	Row27	RAM27	Row19	RAM27	Row3	RAM3	Row11	RAM11	Row3	RAM11	Row11	RAM27	
COM45	Row18	RAM18	Row26	RAM26	Row18	RAM26	Row2	RAM2	Row10	RAM10	Row2	RAM10	Row10	RAM26	
COM46	Row17	RAM17	Row25	RAM25	Row17	RAM25	Row1	RAM1	Row9	RAM9	Row1	RAM9	Row9	RAM25	
COM47	Row16	RAM16	Row24	RAM24	Row16	RAM24	Row0	RAM0	Row8	RAM8	Row0	RAM8	Row8	RAM24	
COM48	Row15	RAM15	Row23	RAM23	Row15	RAM23	-	-	Row7	RAM7	-	-	Row7	RAM23	
COM49	Row14	RAM14	Row22	RAM22	Row14	RAM22	-	-	Row6	RAM6	-	-	Row6	RAM22	
COM50	Row13	RAM13	Row21	RAM21	Row13	RAM21	-	-	Row5	RAM5	-	-	Row5	RAM21	
COM51	Row12	RAM12	Row20	RAM20	Row12	RAM20	-	-	Row4	RAM4	-	-	Row4	RAM20	
COM52	Row11	RAM11	Row19	RAM19	Row11	RAM19	-	-	Row3	RAM3	-	-	Row3	RAM19	
COM53	Row10	RAM10	Row18	RAM18	Row10	RAM18	-	-	Row2	RAM2	-	-	Row2	RAM18	
COM54	Row9	RAM9	Row17	RAM17	Row9	RAM17	-	-	Row1	RAM1	-	-	Row1	RAM17	
COM55	Row8	RAM8	Row16	RAM16	Row8	RAM16	-	-	Row0	RAM0	-	-	Row0	RAM16	
COM56	Row7	RAM7	Row15	RAM15	Row7	RAM15	-	-	-	-	-	-	-	-	
COM57	Row6	RAM6	Row14	RAM14	Row6	RAM14	-	-	-	-	-	-	-	-	
COM58	Row5	RAM5	Row13	RAM13	Row5	RAM13	-	-	-	-	-	-	-	-	
COM59	Row4	RAM4	Row12	RAM12	Row4	RAM12	-	-	-	-	-	-	-	-	
COM60	Row3	RAM3	Row11	RAM11	Row3	RAM11	-	-	-	-	-	-	-	-	
COM61	Row2	RAM2	Row10	RAM10	Row2	RAM10	-	-	-	-	-	-	-	-	
COM62	Row1	RAM1	Row9	RAM9	Row1	RAM9	-	-	-	-	-	-	-	-	
COM63	Row0	RAM0	Row8	RAM8	Row0	RAM8	-	-	-	-	-	-	-	-	
Display examples	(a)		(b)		(c)		(d)		(e)		(f)		(g)		



2.1.17 Set Display Clock Divide Ratio/ Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D) (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 0000b. Please refer to section 6.3 in SSD1312 datasheet for the details relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings available as shown below. The default setting is 1000b.

2.1.18 Set Pre-charge Period (D9h)

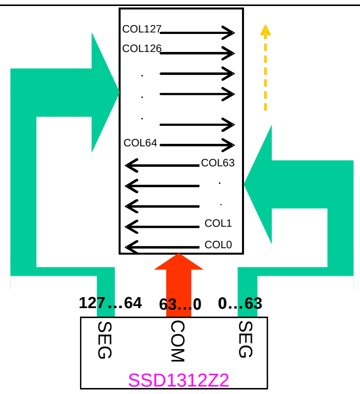
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK, where RESET equals to 2 DCLKs.

2.1.19 Set SEG Pins Hardware Configuration (DAh)

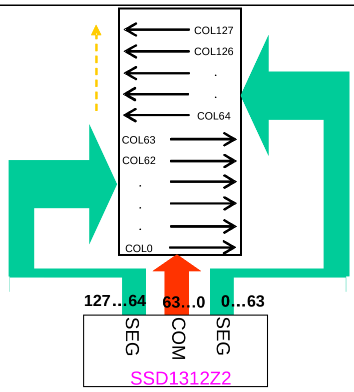
This command sets the SEG signals pin configuration to match the OLED panel hardware layout. SEG Odd / Even (Left / Right) and Top / Bottom connections are software selectable, thus there are total of 8 cases and they are shown on the followings:

Table 2-3 : SEG Pins Hardware Configuration

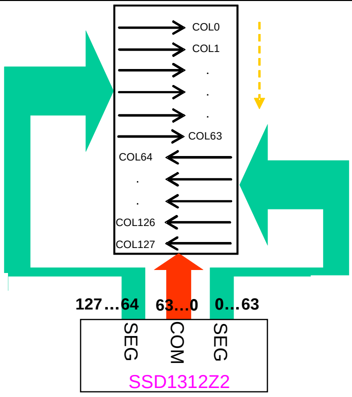
Case no.	Oddeven (1) / Sequential (0) Command : DAh -> A[4]	SEG Remap Command : A0h / A1h	Left / Right Swap Command : DAh -> A[5]	Remark
1	0	0	0	
2	0	0	1	
3	0	1	0	
4	0	1	1	
5	1	0	0	Default
6	1	0	1	
7	1	1	0	
8	1	1	1	



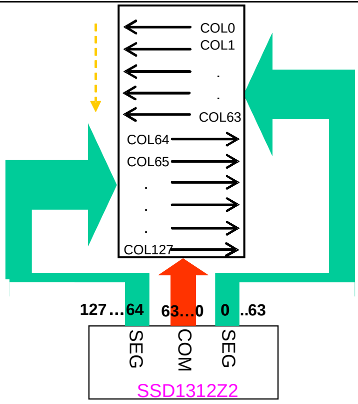
(1) Sequential SEG



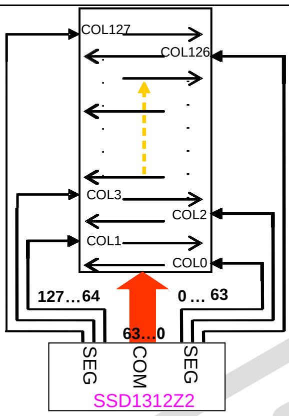
(2) Sequential SEG & left / right



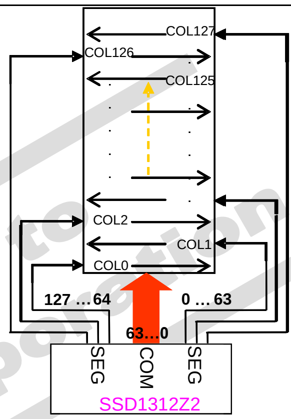
(3) Sequential SEG & SEG remap



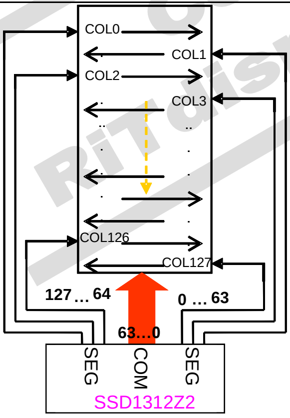
(4) Sequential SEG & SEG remap & left / right



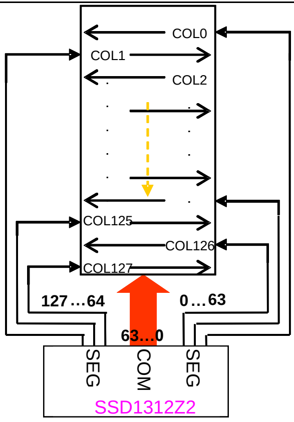
(5) Odd / even SEG



(6) Odd / even SEG & left / right



(7) Odd / even SEG & SEG remap



(8) Odd / even SEG & SEG remap & left / right

Note:

(1) The above eight figures are all with bump pads being faced up.

2.1.20 Set V_{COMH} Deselect Level (DBh)

This command adjusts the VCOMH regulator output. Please refer Table 1-1 for details.

2.1.21 NOP (E3h)

No Operation Command.

2.1.22 Charge Pump Setting (8Dh)

This command controls the ON/OFF of the Charge Pump. The Charge Pump must be enabled by the following command sequence:

8Dh;	Charge Pump Setting
12h / 52h / 72h / 92h;	Enable Charge Pump at different output mode
AFh;	Display ON

2.1.23 Set Command Lock (FDh)

This double byte command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is called "Lock" state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the "Lock" state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resumes from the "Lock" state, and the driver IC will then respond to the command and memory access.

2.1.24 Status register Read

This command is issued by setting D/C# ON LOW during a data read (See AC timing section for parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.