S6D05A1-X01

Mobile Display Driver IC

Revision 0.20

June 2010

Data Sheet

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S6D05A1-X01 Mobile Display Driver IC
Data Sheet, Revision 0.20

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Revision History

Revision No.	Date	Description	Author(s)
0.00	Dec. 2009	- Origin.	
0.10	May. 2010	- Refer to the Revision Descriptions	
0.20	June. 2010	- Refer to the Revision Descriptions	

Revision Descriptions for Revision 0.10

Chapter		Subjects (major changes comparing with previous version)
Chapter Name	Page	
2. ELECTRICAL SPECIFICATION	47~49	Modified MPU68 Interface AC characteristics
	60	Added the Table29.
3.INTERFACE	95~96	Modified the Read data format
	128~129	Delete the lagging mode
	149	Modified the Figure108 (STOP state description)
	154	Modified the Table72 (Reset trigger)
	161	Modified the Table73 (T_{LPX})
	165	Modified the Table74
4.FUNCTION DESCRIPTION	178	Modified the Figure134. Power-up pattern diagram
	179	Modified the Figure135.Setup Flow of Power
	180	Modified the Figure136.Deep Standby Sequence
	181	Modified the Figure138.Deep Standby Sequence
	234	Modified the Figure152. Model of LCD Module for the S6D05A1
	235	Modified the Table86. Cases of Panel Position Mounted IC
	248~250	Modified the MTP flow.(Figure158, Figure159, Figure160)
	257	Table94's note 2,3 is added.
5.COMMAND	261~263	Modified the Table95.(List of Level1 command)
	269	Modified the READ DISPLAY STATUS(09H)
	300, 302	Modified the default value of 2AH, 2BH
	327	Added the TEAR SCAN LINE(44H)
	334	Modified the READ BL CONTROL(54H)
	340	Modified the Read DDB Start(A1H)
	341	Modified the Read DDB Continue(A8H)
	345	Modified the Table96. (List of Level2 command)
	359	Modified the WRBLCTL(C3H)'s default value
	391	Modified the MTPRD(D3H)
	396, 399	Modified the DISCTL(F2H) 's default vale and adddedTE_INV
	402	Modified the MANPWRSEQ(F3H)
	407	Deleted the BOOST_CLK_SEL of PWRCTL(F4H)
	432	Modified the Figure198
	437	Modified the Table158.

Revision Descriptions for Revision 0.20

Chapter		Subjects (major changes comparing with previous version)
Chapter Name	Page	
2. ELECTRICAL SPECIFICATION	42	Sleep current item is added at MDDI, MIPI I/F
	69	Table 33's note is revised. (MDDI speed)
4.FUNCTION DESCRIPTION	181	Modified the Figure136.Deep Standby Sequence
	230	Frame frequency calculation example is added in self refresh mode
5.COMMAND	-	R06h, R07h, R08h is deleted in LEVEL1 command.
	396	Table 123's note is added.

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1 OVERVIEW

1.1 INTRODUCTION

S6D05A1 is a single-chip display driver IC for a TFT-LCD panel. Integrated on this chip are source drivers with built-in memory, gate drivers and power sources. S6D05A1 can support a TFT-LCD panel up to a resolution of 320-RGB x 480-dot or 360-RGB x 480-dot graphics with 16M-color. S6D05A1 also supports various types of peripheral interface such as 80/68-series MPU interface (8-/9-/16-/18-/24-bit data), 3-wire 9-bit and 4-wire 8-bit serial interface. S6D05A1 supports various types of RGB interface (6-/8-/16-/18-/24-bit data), MDDI and MIPI.

The Integrated on-chip functions that are described in this document include:

- Power saving: It reduces the overall power consumed in a TFT-LCD panel module.
- Internal GRAM:
- Internal DC/DC voltage converter
- MIE (Mobile Image Enhancement) functions

S6D05A1 features several power saving functions to reduce the overall power consumed in a TFT-LCD panel module: S6D05A1 operates at low voltage and has internal GRAMs that can store 320-RGB x 480-dot or 360-RGB x 480-dot 16M-color image data. In addition, it has an internal DC/DC voltage converter that generates various voltages needed for driving the TFT-LCD panel by using breeder resistors and the voltage followers.

S6D05A1 supports 320-RGB or 360-RGB Source Channel and it is possible to switch 320-RGB or 360-RGB Source Channel by setting register. This Spec is based on the assumption that the number of source channels is 320-RGB.

1.2 PRODUCT OPTIONS

S6D05A1 offers more than one option in order to meet customer-specific functions from the customers *Table 1* describes its functions.

Table 1 List of S6D05A1 Options

Options	Remarks
-X01	Reference design of S6D05A1 which supports various Host interfaces

1.3 FEATURES

S6D05A1 offers the following key features:

- A single-chip TFT-LCD Controller/gate driver/source driver with built-in Graphic RAM
- Supported Display panel resolution: 320xRGB (H) x 480 (V), 360xRGB (H) x 480 (V), NL = 240 to 480
- Integrated 4,147,200bit of graphic RAM (GRAM)
  - GRAM configuration: 360 x 480 x 24-bits = 4,147,200 bits
- Supported Interfaces
  - 3-wire 9-bit data and 4-wire 8-bit data serial interface (with RGB parallel Interface)
  - 8-/9-/16-/18-/24-bit interface with 80-/68-Series MPU (so called 80-/68-Series)
  - MDDI
  - MIPI
- Outputs
  - Common electrode output
  - Gate outputs
  - Source outputs
- Color Display mode
  - Full color mode (Idle mode off): 16M / 260k / 65k colors
  - Reduced color mode (Idle mode on): 8-colors (3-bit binary mode)
- Color modes on the display host interface
  - 16-bit/Pixel: RGB= (565) using the 4,147.2k bit frame memory
  - 18-bit/Pixel: RGB= (666) using the 4,147.2k bit frame memory
  - 24-bit/Pixel: RGB= (888) using the 4,147.2k bit frame memory
- Display features
  - Partial display mode
- Driving scheme: line inversion & frame inversion
- MIE (Mobile Image Enhancement) functions
  - Adaptive luminance/contrast enhancement function.
  - Reduce the power consumption of backlight.
- On-chip functions
  - Voltage Boosters
  - Adjustable VCOM voltage source generator
  - An oscillator for display clock generation & Timing generation
  - Factory default value (Contrast, Module ID, Module version, etc) can be stored inside IC
- MTP (Multi-time Programmable) Memory
  - MTP initialization & program voltages are generated automatically from the built-in power circuit.
  - Each 8-bit for product ID1/ID2/ID3
  - 6-bit for VCM, 5-bit for VML, 5-bit for GVD Offset adjustment
  - 1-bit for MTP writing protection
- Voltage Supplies

  - 2.3V – 3.3V for VCI, Supply voltage for Analog blocks
  - 1.65V – 3.3V for VDD3, Supply voltage for I/O
- Output voltage levels
  - 2.46V to 5.0V for GVDD, Source output voltage
  - AVDD1/2, Power supply for driver circuit (Note 1)
  - Maximum 6.0V for VCOM, Common electrode output voltage
  - 13.75V to 19.25V for VGH, Positive Gate output voltage (Note 2, Note 3)
  - -13.75V to - 8.25V for VGL, Negative Gate output voltage (Note 2)
- CMOS compatible inputs
- COG package
- Operating temperature range: -40°C to +85°C

NOTE:

1. Available AVDD1/2 Min=4.2V at VCI1=2.1V, Max=6V at VCI1=3V
   (AVDD1 is power supply for 2nd booster circuit and source driver. AVDD2 is power supply for VCOM driver, VCOMH and GVDD Amp.)
2. VCI1=2.75V, |VGH - VGL| Max = 30V
3. Maximum |VGH| should be lower than or equal to 19.25V in normal operating condition, regardless of VCI1 & BT settings.

1.4 BLOCK DIAGRAM

1.4.1 MODULE LEVEL

Figure 1 shows the block diagram of a mobile display panel module and related interface signals required by set makers and module makers. Level I interface signals represent the requirements by a set manufacturer that must be complied to by a module manufacturer. Level II interface signals, on the other hand, represent the requirements from the module manufacturer to that, typically, a driver IC manufacturer must comply.

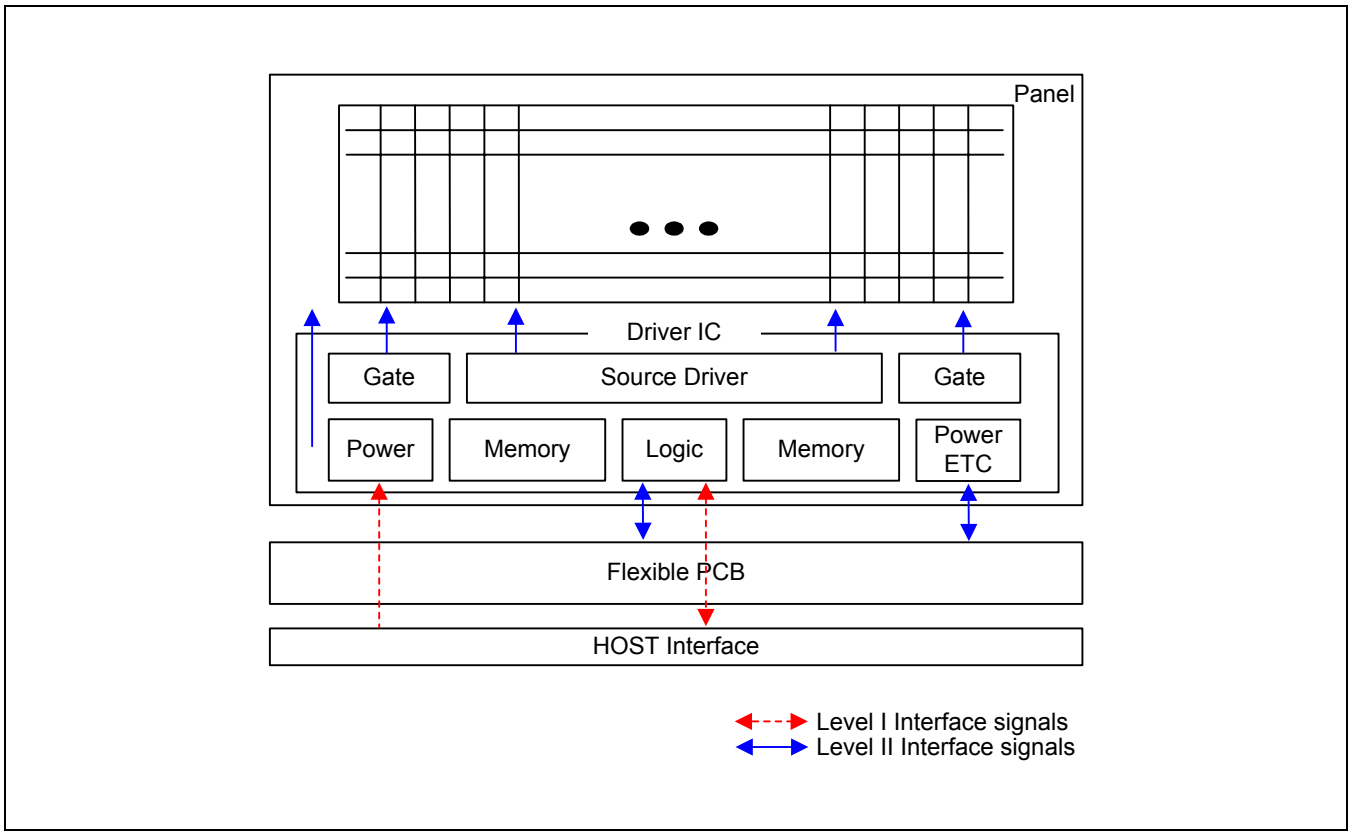


Figure 1 The Interface Signal Flow of a Mobile Display Panel Module.

There are also Level III signals which are for internal use only for the driver IC itself. These signals may not necessarily be released to the customer since they are designed for a specific manufacturing purpose and are supposed to be hidden features.

The reference specifications shown in this document serve only as guidelines to Level I and II interface signals only; the reason being that a specification related to Level I and II considers the parasitic and design requirements within the flexible PCB used by a display module maker. IC specification will offer related information among Level I/II on how each interface signals relates to each other.

1.4.2 FUNCTIONAL BLOCK DIAGRAM OF THE IC

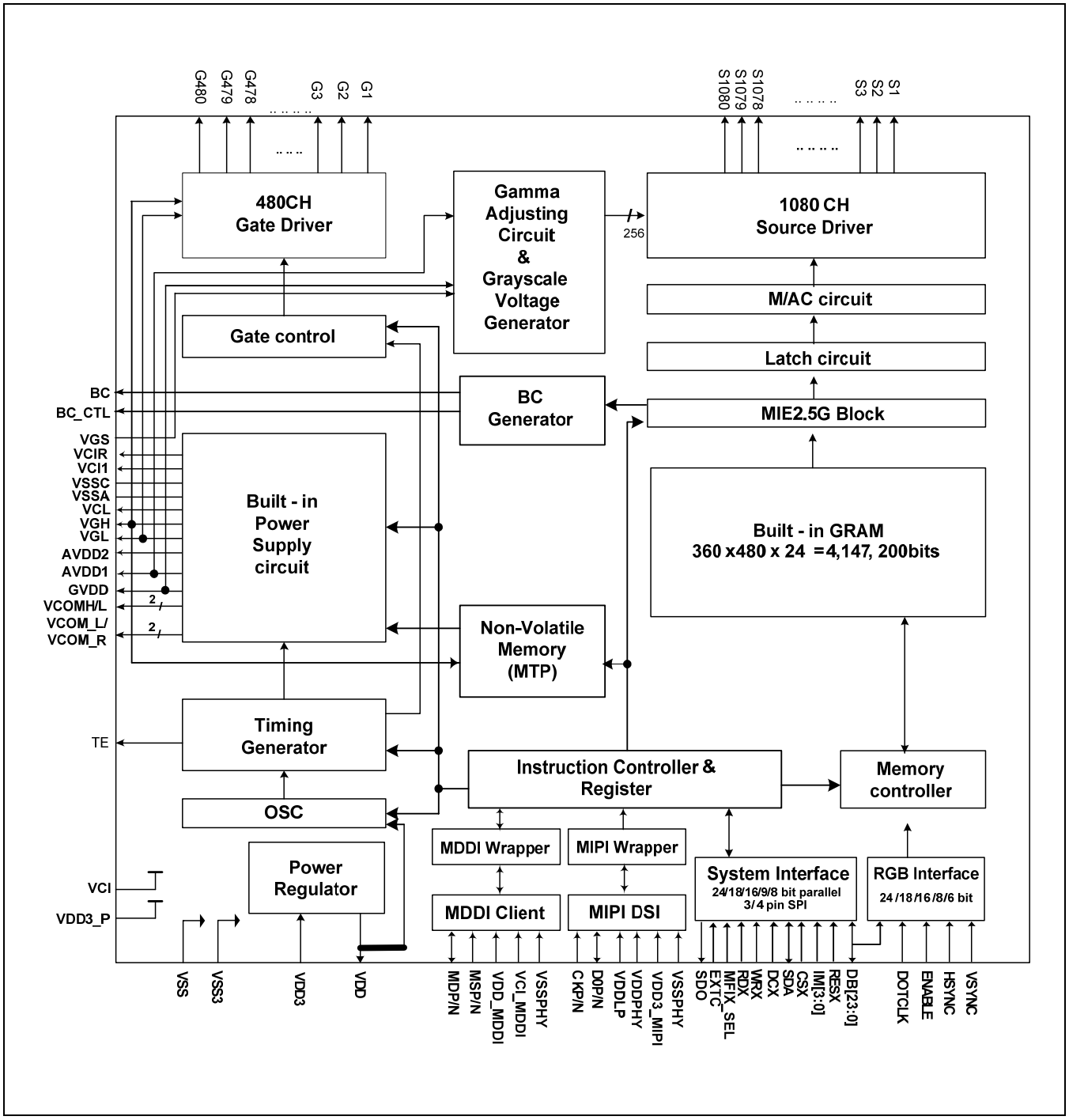


Figure 2 S6D05A1 Block Diagram

1.5 PAD INFORMATION

1.5.1 CONFIGURATION OF SIGNAL PADS

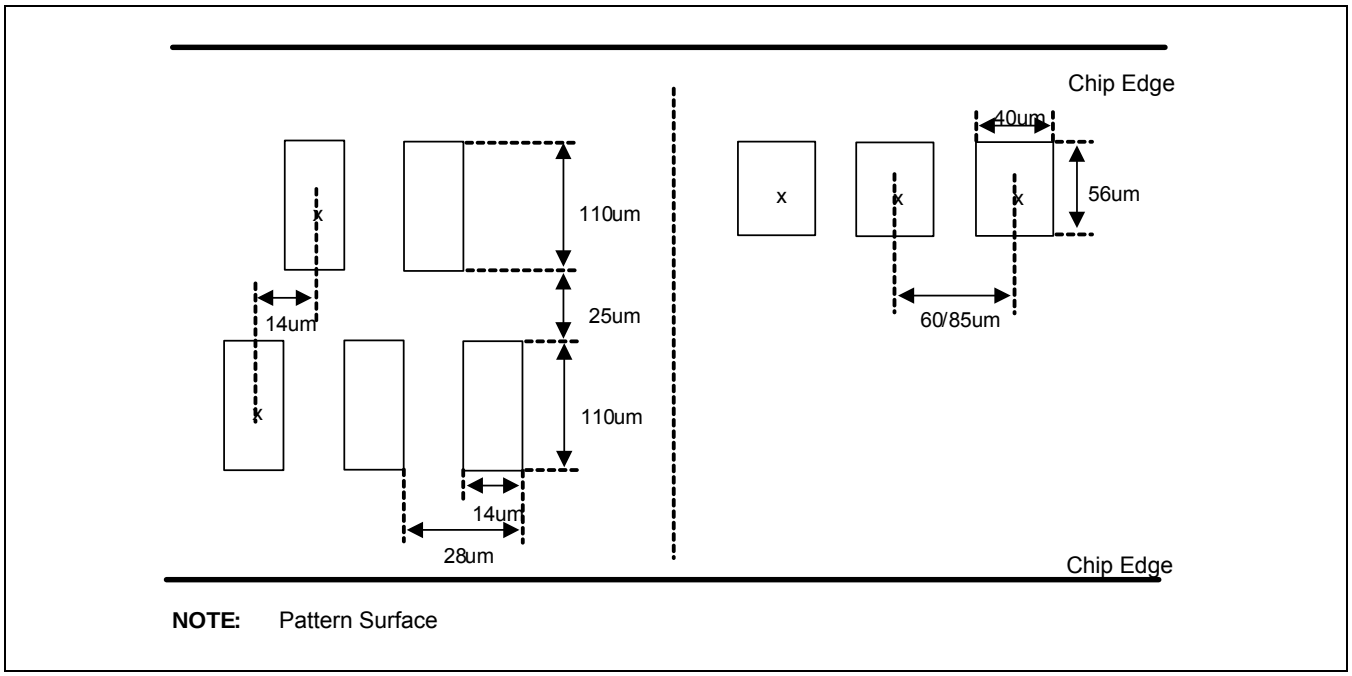


Figure 3 S6D05A1 PAD Configuration

1.5.2 BUMP

Table 2 S6D05A1 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip Size	-	23,160	1,150	μm
Bumped Pad Top Size	Input Side	40±2	56±2	
	Output Side	14±2	110±2	
Bumped Pad Height	Height	15±3 (in wafer)		
	Tolerance In Chip	Under 2		
	Dimple Height	Under 2		
Chip Thickness	-	300(note2)		

NOTE:
1. Scribe lane 80um included in this die size
2. Wafer thickness:
   – S6D05A1●●●–●●●9 : 280±10 um
   – S6D05A1●●●–●●●8 : 300±10 um
   – S6D05A1●●●–●●●Y : 470±10 um

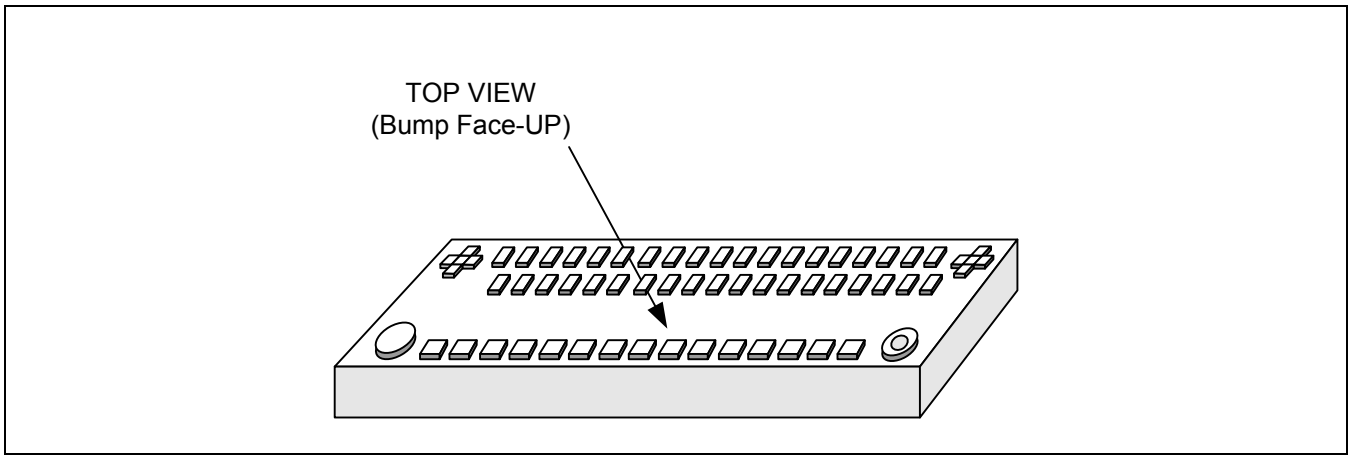


Figure 4 Pad Arrangement Layout

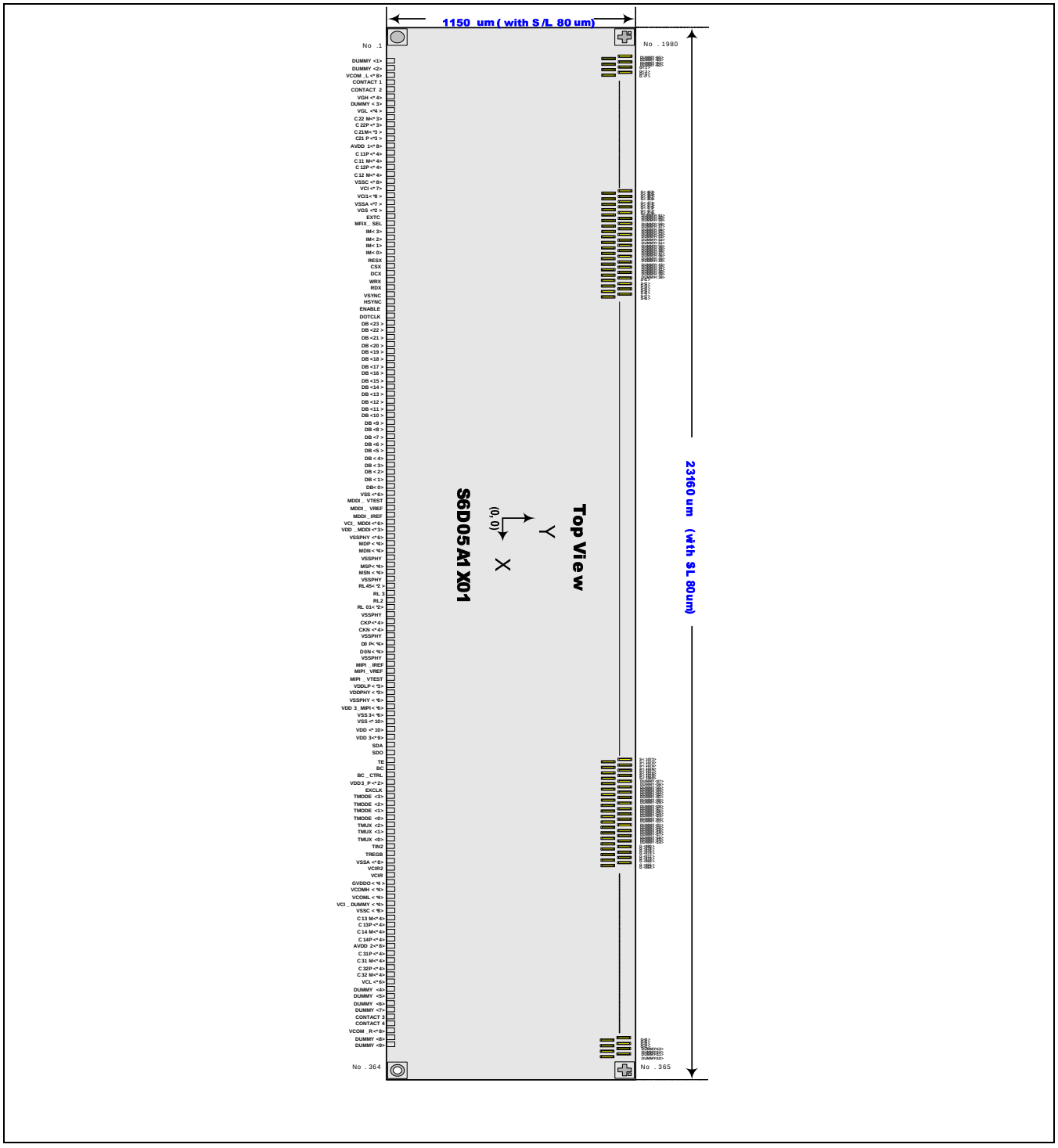


Figure 5 Chip Outline

1.5.3 ALIGN KEY

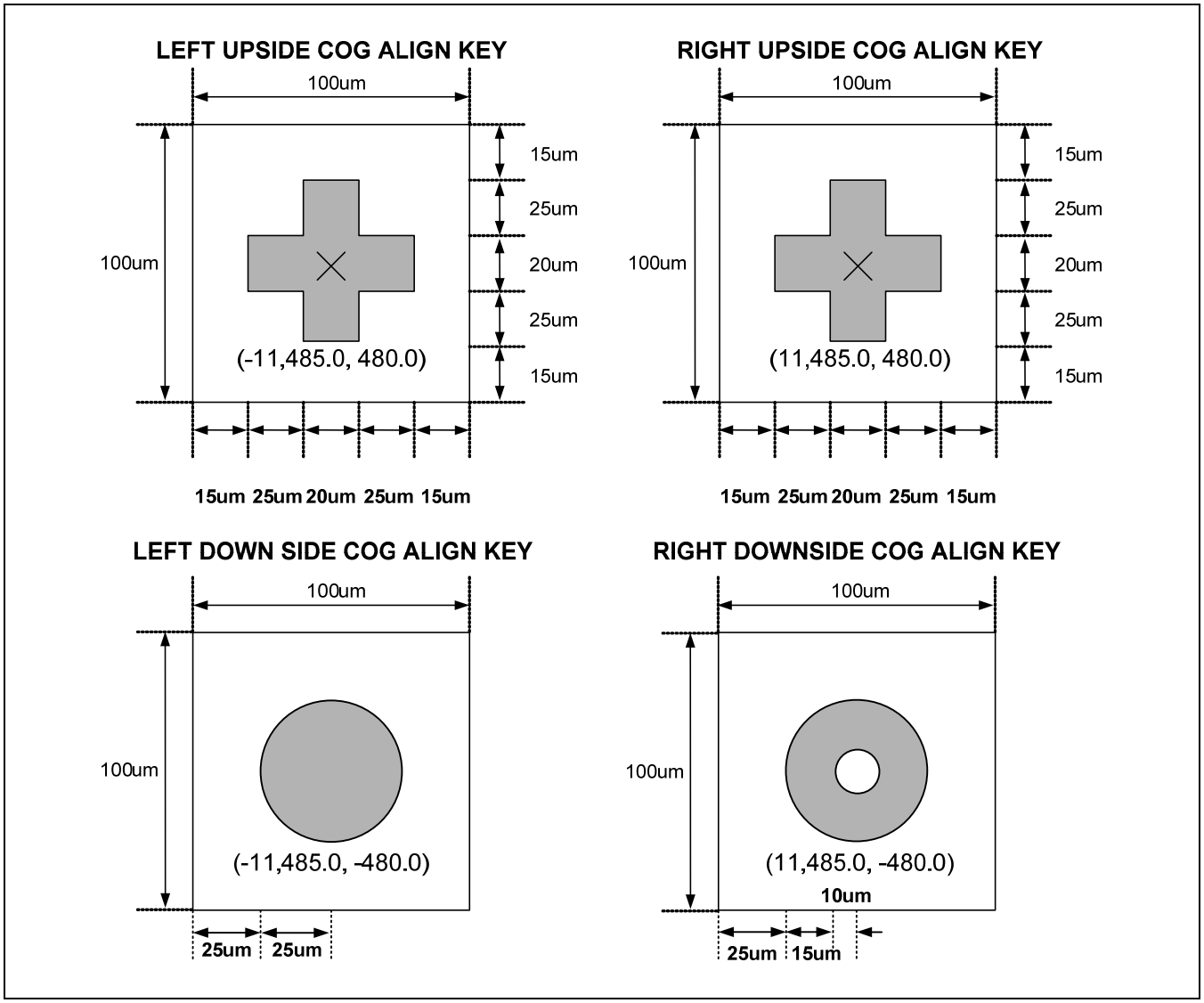


Figure 6 COG Align Key Configuration and Coordinate

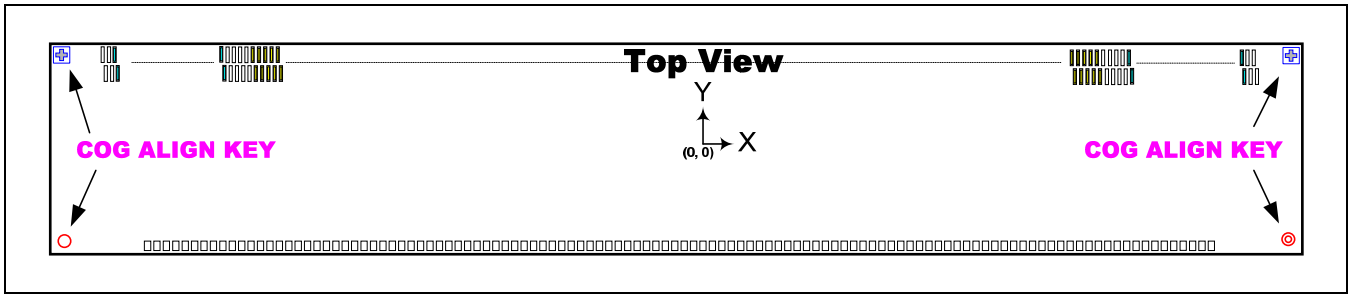


Figure 7 COG Align Key Arrangement Layout

1.6 DESCRIPTION OF SIGNAL PADS

1.6.1 PADS FOR POWER SUPPLIES

Table 3 Pads for Power Supplies

Name	I/O	Description
VCI	P	Power supply for analog and voltage booster block.
VCI_MDDI	P	Power supply for MDDI PHY. Must be connected to VCI level. When use MDDI, VCI minimum level is 2.5V.
VDD3	P	Power supply for I/O block provided from outside.
VDD3_MIPI	P	Power supply for MIPI DSI receiver. Must be connected to VDD3 level.
VDD3_P	P	Power supply for BC and BC_CTL output, which are for back light LED driver. Must be connected to VDD3 or VCI power compatible to the LED driver.
VCI_DUMMY	P	Power supply for analog and voltage booster block. This pad is internally connected to VCI power. For robuster analog operation, connect VCI to this pad. If not possible for any reason, just open this pad.
VSSA	P	GND for analog circuits.
VSSC	P	GND for voltage booster circuits.
VSS	P	GND for logic circuits.
VSS3	P	GND for I/O block
VSSPHY	P	Ground for MDDI / MIPI PHY.
VDD	O	Voltage regulator output for internal memory and logic circuit. Do not apply any external power to this pad. This pad needs an external capacitor.
VDD_MDDI	O	2.3V regulated power for analog circuit of the MDDI PHY. This pad needs an external capacitor. If not used, connect these pads to VSS.
VDDPHY	O	1.5V regulated power for analog circuit of the MIPI DSI receiver. This pad needs an external capacitor. If not used, connect these pads to VSS.
VDDLP	O	1.2V regulated power for LP mode operation of MIPI This pad needs an external capacitor. If not used, connect these pads to VSS.
VCIR	O	Reference voltage for VCI1/GVDD/VCOMH/VCOML voltage regulator. (typ. 2.0V) Normally floating. Optionally prepare space to connect an external capacitor.
VCI1	O	Reference input voltage for 1st/2nd booster circuit. This pad needs an external capacitor. <note 1> VCI1 cannot exceed 3V
AVDD1	O	Internally generated voltage output for 2nd booster/source driver. Output voltage of 1st booster circuit (=2 x VCI1) This pad needs an external capacitor.
AVDD2	O	Internally generated voltage output pad for GVDD/VCOMH amps. Output voltage of 1st booster circuit (=2 x VCI1) This pad needs an external capacitor.
VGH	O	Positive power output of the 2nd booster circuit. Gate “ON” level voltage. This pad needs an external capacitor.

Name	I/O	Description
VGL	O	Negative power output of the 2nd booster circuit. Gate “OFF” level voltage. This pad needs an external capacitor.
VCL	O	3rd booster output voltage. Reference voltage for VCOML voltage regulator. This pad needs an external capacitor.
VGS	I	Reference voltage input for grayscale voltage generator. Connect an external resistor or to system ground.
GVDD	O	Reference voltage input for grayscale voltage generator. An internal register can be used to adjust the GVDD voltage. This pad needs an external capacitor.
VCOMH	O	High level output voltage of VCOM. An internal register can be used to adjust the VCOMH voltage. This pad needs an external capacitor.
VCOML	O	Low level output voltage of VCOM. An internal register can be used to adjust the difference voltage between VCOMH and VCOML. This pad needs an external capacitor.
VCOM_L	O	Power supply pad for the TFT- display common electrode in left side. Charge recycling method is used with VCI voltage. Connect this pad to the TFT-display common electrode
VCOM_R	O	Power supply pad for the TFT- display common electrode in right side. Charge recycling method is used with VCI voltage. Connect this pad to the TFT-display common electrode
C11P, C11M C12P, C12M	-	Connect the charge-pumping capacitor for generating AVDD1 level.
C13P, C13M C14P, C14M	-	Connect the charge-pumping capacitor for generating AVDD2 level.
C21P, C21M C22P, C22M	-	Connect the charge-pumping capacitor for generating VGH, VGL level.
C31P, C31M, C32P, C32M	-	Connect the charge-pumping capacitor for generating VCL level.

1.6.2 SIGNAL PADS FOR LOGIC INTERFACE

Table 4 Signal Pads for Logic Interface

<table>
<tr><th>Name</th><th>I/O</th><th colspan="6">Description</th></tr>
<tr><td>MDP/MDN</td><td>I/O</td><td colspan="6">Differential Data input/output pins for MDDI interface. When the forward link activates, MDP/MDN receive data from host. When the reverse link activates, MDP/MDN transmit data to host. Connect a termination resistor between MDP and MDN. If not used, these pads should be unconnected.</td></tr>
<tr><td>MSP/MSN</td><td>I</td><td colspan="6">Differential Strobe input pins for MDDI interface. These pins always receive strobe data regardless of link direction. Also these pins are output pins for MDDI failsafe function. Connect a termination resistor between MSP and MSN. If not used, these pads should be unconnedted.</td></tr>
<tr><td>D0P/N</td><td>I/O</td><td colspan="6">First differential data input/output pins. When forward link activates, these pins receive data from host. When reverse link activates, these pins transmit data to host. If not used, connect these pads to VSS.</td></tr>
<tr><td>CKP/N</td><td>I</td><td colspan="6">Differential clock input pins for MIPI interface. These pins always receive high speed clock when MIPI activates in high speed data transmission mode. If not used, connect these pads to VSS.</td></tr>
<tr><td rowspan="18">IM[3:0]</td><td rowspan="18">I</td><td colspan="6">Selects the MPU interface mode</td></tr>
<tr><td>IM3</td><td>IM2</td><td>IM1</td><td>IM0</td><td>Interface mode</td><td>DB pad</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>80 MPU 24-bit Parallel I/F</td><td>DB[23:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MPU 18-bit Parallel I/F</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MPU 16-bit Parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MPU 9-bit Parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MPU 8-bit Parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>×</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data Serial interface & RGB Interface</td><td>Refer to DB Description</td></tr>
<tr><td>×</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data Serial interface & RGB Interface</td><td>Refer to DB Description</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>MDDI</td><td>Refer to DB Description</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>68 MPU 24-bit Parallel I/F</td><td>DB[23:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>68 MPU 18-bit Parallel I/F</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>68 MPU 16-bit Parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>68 MPU 9-bit Parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>68 MPU 8-bit Parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>MIPI</td><td>Refer to DB Description</td></tr>
<tr><td>RESX</td><td>I</td><td colspan="6">Active low. This signal is used to reset the device and must be applied to initialize the chip properly.</td></tr>
<tr><td>CSX</td><td>I</td><td colspan="6">Chip select signal. Activate MPU interface mode by setting this to ‘low’. This pad can be permanently connected to “Low” in MPU interface mode only.
If not used, connect this pad to either VSS or VDD3.</td></tr>
<tr><td>DCX</td><td>I</td><td colspan="6">Display Data/Command selection signal in parallel interface
DCX=’1’: Display Data or Command parameter.</td></tr>
</table>

<table>
<tr><th>Name</th><th>I/O</th><th colspan="6">Description</th></tr>
<tr><td></td><td></td><td colspan="6">DCX=’0’: Command Index.
If not used, connect this pad to either VSS or VDD3.</td></tr>
<tr><td>RDX</td><td>I</td><td colspan="6">Read Enable in 80-parallel interface
Read /Write operation enable signal (E) in 68-parallel interface
If not used, connect this pad to VDD3.</td></tr>
<tr><td>WRX</td><td>I</td><td colspan="6">Write Enable in 80-parallel interface.
Read/Write operation selection signal(RW) in 68-parallel interface(Low: write, High: read)
Serial interface clock in Serial Interface
If not used, connect this pad to either VSS or VDD3.</td></tr>
<tr><td rowspan="24">DB[23:0]</td><td rowspan="24">I/O</td><td colspan="6">Data Bus.</td></tr>
<tr><td colspan="4">Interface Mode</td><td colspan="2">Description</td></tr>
<tr><td>IM</td><td>RIM</td><td>VFPF (Note)</td><td>Interface Mode</td><td>Index</td><td>Data</td></tr>
<tr><td>0100</td><td>×</td><td>×</td><td>80 MPU 24-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[23:0]</td></tr>
<tr><td>0011</td><td>×</td><td>×</td><td>80 MPU 18-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[17:0]</td></tr>
<tr><td>0000</td><td>×</td><td>×</td><td>80 MPU 16-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[15:0]</td></tr>
<tr><td>0001</td><td>×</td><td>×</td><td>80 MPU 9-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[8:0]</td></tr>
<tr><td>0010</td><td>×</td><td>×</td><td>80 MPU 8-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[7:0]</td></tr>
<tr><td rowspan="5">×101</td><td>0</td><td>111</td><td>3-wire 9-bit data Serial Interface & RGB 24-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[23:0]</td></tr>
<tr><td>0</td><td>110</td><td>3-wire 9-bit data Serial Interface & RGB 18-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>101</td><td>3-wire 9-bit data Serial Interface & RGB 16-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[15:0]</td></tr>
<tr><td>1</td><td>111</td><td>3-wire 9-bit data Serial Interface & RGB 8-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>110</td><td>3-wire 9-bit data Serial Interface & RGB 6-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[5:0]</td></tr>
<tr><td rowspan="5">×110</td><td>0</td><td>111</td><td>4-wire 8-bit data Serial Interface & RGB 24-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[23:0]</td></tr>
<tr><td>0</td><td>110</td><td>4-wire 8-bit data Serial Interface & RGB 18-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>101</td><td>4-wire 8-bit data Serial Interface & RGB 16-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[15:0]</td></tr>
<tr><td>1</td><td>111</td><td>4-wire 8-bit data Serial Interface & RGB 8-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>110</td><td>4-wire 8-bit data Serial Interface & RGB 6-bit I/F</td><td>SDA Or DB[1:0]</td><td>DB[5:0]</td></tr>
<tr><td>0111</td><td>×</td><td>×</td><td>MDDI</td><td>-</td><td>-</td></tr>
<tr><td>1100</td><td>×</td><td>×</td><td>68 MPU 24-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[23:0]</td></tr>
<tr><td>1011</td><td>×</td><td>×</td><td>68 MPU 18-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[17:0]</td></tr>
</table>

<table>
<tr><th>Name</th><th>I/O</th><th colspan="6">Description</th></tr>
<tr><td rowspan="7"></td><td rowspan="7"></td><td colspan="4">Interface Mode</td><td colspan="2">Description</td></tr>
<tr><td>IM</td><td>RIM</td><td>VFPF (Note)</td><td>Interface Mode</td><td>Index</td><td>Data</td></tr>
<tr><td>1000</td><td>×</td><td>×</td><td>68 MPU 16-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[15:0]</td></tr>
<tr><td>1001</td><td>×</td><td>×</td><td>68 MPU 9-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[8:0]</td></tr>
<tr><td>1010</td><td>×</td><td>×</td><td>68 MPU 8-bit Parallel I/F</td><td>DB[7:0]</td><td>DB[7:0]</td></tr>
<tr><td>1111</td><td>×</td><td>×</td><td>MIPI</td><td>-</td><td>-</td></tr>
<tr><td colspan="6">NOTE:
1. "denotes “Don’t care"
2. VFPF = COLMOD [6:4] (Refer to 3Ah Command)
Must be connected to VDD3 or VSS level when not used.</td></tr>
<tr><td>SDA</td><td>I/O</td><td colspan="6">Serial data bus. If not used, connect this pad to either VDD3 or VSS</td></tr>
<tr><td>SDO</td><td>O</td><td colspan="6">Serial data output when set SDO_EN=1 if MFIX_SEL is low. If not used, leave this pad unconnected</td></tr>
<tr><td>MFIX_SEL</td><td>I</td><td colspan="6">When use SDA in Serial I/F for instruction, connect this pad to VSS.
When use DB[1:0] in Serial I/F for instruction , If MFIX_SEL is high, DB[1:0] is used to transfer instruction, If MFIX_SEL is low, DB[1:0] is used to transfer DISPLAY DATA.
Refer to the 1.7 INTERFACE PAD CONFIGURATION.</td></tr>
<tr><td>TE</td><td>O</td><td colspan="6">Tearing effect output pad to synchronize MPU to frame writing, activated by S/W command. When this pad is not activated, this signal stays low.
If not used, leave this pad unconnected.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td colspan="6">Pixel clock signal in RGB I/F mode.
If not used, connect this pad to either VDD3 or VSS.</td></tr>
<tr><td>VSYNC</td><td>I</td><td colspan="6">Vertical Sync signal in RGB I/F mode.
If not used, connect this pad to either VDD3 or VSS.</td></tr>
<tr><td>HSYNC</td><td>I</td><td colspan="6">Horizontal Sync signal in RGB I/F mode.
If not used, connect this pad to either VDD3 or VSS.</td></tr>
<tr><td>ENABLE</td><td>I</td><td colspan="6">Data Enable signal in RGB I/F mode.
If not used, connect this pad to either VDD3 or VSS.</td></tr>
</table>

NOTE: If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there should be no influence to the Power Consumption of the display module. When CSX=’1’, there is no influence to the parallel interface.

Table 5 Pads for Source/Gate Driver Output Signal

Name	I/O	Description
S1 to S1080	O	Signal pads for Source driver output.
G1 to G480	O	Signal pads for Gate driver output.

Table 6 MIE Pins

Name	I/O	Description
BC	O	This pin is used to PWM output for back light control of LED driver. In normal operation, leave this pad unconnected.
BC_CTL	O	This pin is used to enable the back light LED driver (active high). In normal operation, leave this pad unconnected.

Table 7 Miscellaneous Signal Pads

Name	I/O	Description
EXTC	I	Input pads used only for test purpose at IC-side. In normal operation, connect this pad to VSS.
CONTACT1 CONTACT2 CONTACT3 CONTACT4		Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at VSS level. When measuring an ohmic resisstance of the contact, do not apply any power.

Table 8 Test Signal Pads

Name	I/O	Description
TMODE [3:0]	I	Input pads used only for test purpose at IC-side. During normal operation, connect these pads to VSS.
EXCLK	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TMUX [2:0]	I	Input pads used only for test purpose at IC-side. During normal operation, connect these pads to VSS.
TIN2	I	Input pads used only for test purpose at IC-side. During normal operation, connect these pads to VSS.
TREGB	I	Input pads used only for test purpose at IC-side. During normal operation, connect these pads to VSS.
VCIR2	I	Input pads used only for test purpose at IC-side. During normal operation, connect these pads to VSS.
RL01,RL2, RL3,RL45	I	Input pads used only for test purpose at IC-side. During normal operation, this pad should be floating.
MDDI_IREF	I	Input pads used only for test purpose at IC-side. During normal operation, this pad should be floating.
MDDI_VREF	I	Input pads used only for test purpose at IC-side. During normal operation, this pad should be floating.
MDDI_VTEST	I	Input pads used only for test purpose at IC-side. During normal operation, this pad should be floating.
MIPI_IREF	I	Input pads used only for test purpose at IC-side. During normal operation, this pad should be floating.
MIPI_VREF	I	Input pads used only for test purpose at IC-side. During normal operation, this pad should be floating.
MIPI_VTEST	I	Input pads used only for test purpose at IC-side. During normal operation, this pad should be floating.

1.7 INTERFACE PAD CONFIGURATION

Table 9 Interface Pad Configuration1 (MPU)

PIN NAME/ IF MODE	80/68 MPU					MDDI	MIPI
	24bit	18bit	16bit	9bit	8bit		
TMODE[3:0]	VSS	VSS	VSS	VSS	VSS	VSS	VSS
MFIX_SEL	VSS	VSS	VSS	VSS	VSS	VSS/VDD3	VSS/VDD3
IM[3]	VSS/VDD3	VSS/VDD3	VSS/VDD3	VSS/VDD3	VSS/VDD3	VSS	VDD3
IM[2]	VDD3	VSS/	VSS	VSS	VSS	VDD3	VDD3
IM[1]	VSS	VDD3	VSS	VSS	VDD3	VDD3	VDD3
IM[0]	VSS	VDD3	VSS	VDD3	VSS	VDD3	VDD3
MDP/MDN	Floating	Floating	Floating	Floating	Floating	MDP/MDN	Floating
MSP/MSN	Floating	Floating	Floating	Floating	Floating	MSP/MSN	Floating
D0P/N	VSS	VSS	VSS	VSS	VSS	VSS	D0P/N
CKP/N	VSS	VSS	VSS	VSS	VSS	VSS	CKP/N
RESX	RESX	RESX	RESX	RESX	RESX	RESX	RESX
CSX	CSX	CSX	CSX	CSX	CSX	VDD3/VSS	VDD3/VSS
DCX	DCX	DCX	DCX	DCX	DCX	VDD3/VSS	VDD3/VSS
WRX	WRX	WRX	WRX	WRX	WRX	VDD3/VSS	VDD3/VSS
RDX	RDX	RDX	RDX	RDX	RDX	VDD3	VDD3
VSYNC	(VSYNC)	(VSYNC)	(VSYNC)	(VSYNC)	(VSYNC)	VDD3/VSS	VDD3/VSS
HSYNC	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
ENABLE	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
DOTCLK	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
SDA	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
SDO	Floating	Floating	Floating	Floating	Floating	Floating	Floating
DB[23:18]	DB[23:18]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[17:16]	DB[17:16]	DB[17:16]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[15:9]	DB[15:9]	DB[15:9]	DB[15:9]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[8]	DB[8]	DB[8]	DB[8]	DB[8]	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[7:0]	DB[7:0]	DB[7:0]	DB[7:0]	DB[7:0]	DB[7:0]	VDD3/VSS	VDD3/VSS

Table 10 Interface Pad Configuration2 (SPI 3wire/RGB, When use SDA for Instruction)

PIN NAME/ IF MODE	RGB(SPI 3wire)				
	24bit	18bit	16bit	8bit	6bit
TMODE[3:0]	VSS	VSS	VSS	VSS	VSS
MFIX_SEL	VSS	VSS	VSS	VSS	VSS
IM[3]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
IM[2]	VDD3	VDD3	VDD3	VDD3	VDD3
IM[1]	VSS	VSS	VSS	VSS	VSS
IM[0]	VDD3	VDD3	VDD3	VDD3	VDD3
MDP/MDN	Floating	Floating	Floating	Floating	Floating
MSP/MSN	Floating	Floating	Floating	Floating	Floating
D0P/N	VSS	VSS	VSS	VSS	VSS
CKP/N	VSS	VSS	VSS	VSS	VSS
RESX	RESX	RESX	RESX	RESX	RESX
CSX	CSX	CSX	CSX	CSX	CSX
DCX	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
WRX	SCL	SCL	SCL	SCL	SCL
RDX	VDD3	VDD3	VDD3	VDD3	VDD3
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
DOTCLK	DOTCLK	DOTCLK	DOTCLK	DOTCLK	DOTCLK
SDA	SDA	SDA	SDA	SDA	SDA
SDO	SDO	SDO	SDO	SDO	SDO
DB[23:18]	DB[23:18]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[17:16]	DB[17:16]	DB[17:16]	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[15:8]	DB[15:8]	DB[15:8]	DB[15:8]	VDD3/VSS	VDD3/VSS
DB[7:6]	DB[7:6]	DB[7:6]	DB[7:6]	DB[7:6]	VDD3/VSS
DB[5:0]	DB[5:0]	DB[5:0]	DB[5:0]	DB[5:0]	DB[5:0]

NOTE:

1. SDA is used to transfer/read Instruction, and DB[23:0] are used to transfer DISPLAY Data according to the I/F Type
2. When SDO_EN is set, SDA is used to transfer instruction, and SDO is used to read instruction from IC

Table 11 Interface Pad Configuration3 (SPI 4wire/RGB, When use SDA for Instruction)

PIN NAME/ IF MODE	RGB(SPI 4wire)				
	24bit	18bit	16bit	8bit	6bit
TMODE[3:0]	VSS	VSS	VSS	VSS	VSS
MFIX_SEL	VSS	VSS	VSS	VSS	VSS
IM[3]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
IM[2]	VDD3	VDD3	VDD3	VDD3	VDD3
IM[1]	VDD3	VDD3	VDD3	VDD3	VDD3
IM[0]	VSS	VSS	VSS	VSS	VSS
MDP/MDN	Floating	Floating	Floating	Floating	Floating
MSP/MSN	Floating	Floating	Floating	Floating	Floating
D0P/N	VSS	VSS	VSS	VSS	VSS
CKP/N	VSS	VSS	VSS	VSS	VSS
RESX	RESX	RESX	RESX	RESX	RESX
CSX	CSX	CSX	CSX	CSX	CSX
DCX	DCX	DCX	DCX	DCX	DCX
WRX	SCL	SCL	SCL	SCL	SCL
RDX	VDD3	VDD3	VDD3	VDD3	VDD3
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
DOTCLK	DOTCLK	DOTCLK	DOTCLK	DOTCLK	DOTCLK
SDA	SDA	SDA	SDA	SDA	SDA
SDO	SDO	SDO	SDO	SDO	SDO
DB[23:18]	DB[23:18]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[17:16]	DB[17:16]	DB[17:16]	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[15:8]	DB[15:8]	DB[15:8]	DB[15:8]	VDD3/VSS	VDD3/VSS
DB[7:6]	DB[7:6]	DB[7:6]	DB[7:6]	DB[7:6]	VDD3/VSS
DB[5:0]	DB[5:0]	DB[5:0]	DB[5:0]	DB[5:0]	DB[5:0]

NOTE:

1. SDA is used to transfer Instruction, and DB[23:0] are used to transfer DISPLAY Data according to the I/F Type.
2. When SDO_EN is set, SDA is used to transfer instruction, and SDO is used to read instruction from IC

Table 12 Interface Pad Configuration5 (SPI 3wire/RGB, When use DB[1:0] for Instruction)

PIN NAME/ IF MODE	RGB(SPI 3wire)				
	24bit	18bit	16bit	8bit	6bit
TMODE[3:0]	VSS	VSS	VSS	VSS	VSS
MFIX_SEL	VSS/VDD3	VSS/VDD3	VSS/VDD3	VSS/VDD3	VSS/VDD3
IM[3]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
IM[2]	VDD3	VDD3	VDD3	VDD3	VDD3
IM[1]	VSS	VSS	VSS	VSS	VSS
IM[0]	VDD3	VDD3	VDD3	VDD3	VDD3
MDP/MDN	Floating	Floating	Floating	Floating	Floating
MSP/MSN	Floating	Floating	Floating	Floating	Floating
D0P/N	VSS	VSS	VSS	VSS	VSS
CKP/N	VSS	VSS	VSS	VSS	VSS
RESX	RESX	RESX	RESX	RESX	RESX
CSX	CSX	CSX	CSX	CSX	CSX
DCX	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
WRX	SCL	SCL	SCL	SCL	SCL
RDX	VDD3	VDD3	VDD3	VDD3	VDD3
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
DOTCLK	DOTCLK	DOTCLK	DOTCLK	DOTCLK	DOTCLK
SDA	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
SDO	Floating	Floating	Floating	Floating	Floating
DB[23:18]	DB[23:18]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[17:16]	DB[17:16]	DB[17:16]	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[15:8]	DB[15:8]	DB[15:8]	DB[15:8]	VDD3/VSS	VDD3/VSS
DB[7:6]	DB[7:6]	DB[7:6]	DB[7:6]	DB[7:6]	VDD3/VSS
DB[5:2]	DB[5:2]	DB[5:2]	DB[5:2]	DB[5:2]	DB[5:2]
DB[1]	DB[1]/SDO	DB[1]/SDO	DB[1]/SDO	DB[1]/SDO	DB[1]/SDO
DB[0]	DB[0]/SDI	DB[0]/SDI	DB[0]/SDI	DB[0]/SDI	DB[0]/SDI

NOTE: When MFIX_SEL is high, DB[0] is used to transfer instruction, and DB[1] is used to read instruction from IC. When MFIX_SEL is Low, DB[23:0] are used to transfer DISPLAY data according to the I/F Type

Table 13 Interface Pad Configuration4 (SPI 4wire/RGB, When use DB[1:0] for Instruction)

PIN NAME/ IF MODE	RGB(SPI 4wire)				
	24bit	18bit	16bit	8bit	6bit
TMODE[3:0]	VSS	VSS	VSS	VSS	VSS
MFIX_SEL	VSS/VDD3	VSS/VDD3	VSS/VDD3	VSS/VDD3	VSS/VDD3
IM[3]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
IM[2]	VDD3	VDD3	VDD3	VDD3	VDD3
IM[1]	VDD3	VDD3	VDD3	VDD3	VDD3
IM[0]	VSS	VSS	VSS	VSS	VSS
MDP/MDN	Floating	Floating	Floating	Floating	Floating
MSP/MSN	Floating	Floating	Floating	Floating	Floating
D0P/N	VSS	VSS	VSS	VSS	VSS
CKP/N	VSS	VSS	VSS	VSS	VSS
RESX	RESX	RESX	RESX	RESX	RESX
CSX	CSX	CSX	CSX	CSX	CSX
DCX	DCX	DCX	DCX	DCX	DCX
WRX	SCL	SCL	SCL	SCL	SCL
RDX	VDD3	VDD3	VDD3	VDD3	VDD3
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
DOTCLK	DOTCLK	DOTCLK	DOTCLK	DOTCLK	DOTCLK
SDA	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
SDO	Floating	Floating	Floating	Floating	Floating
DB[23:18]	DB[23:18]	VDD3/VSS	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[17:16]	DB[17:16]	DB[17:16]	VDD3/VSS	VDD3/VSS	VDD3/VSS
DB[15:8]	DB[15:8]	DB[15:8]	DB[15:8]	VDD3/VSS	VDD3/VSS
DB[7:6]	DB[7:6]	DB[7:6]	DB[7:6]	DB[7:6]	VDD3/VSS
DB[5:2]	DB[5:2]	DB[5:2]	DB[5:2]	DB[5:2]	DB[5:2]
DB[1]	DB[1]/SDO	DB[1]/SDO	DB[1]/SDO	DB[1]/SDO	DB[1]/SDO
DB[0]	DB[0]/SDI	DB[0]/SDI	DB[0]/SDI	DB[0]/SDI	DB[0]/SDI

NOTE: When MFIX_SEL is high, DB[0] is used to transfer instruction, and DB[1] is used to read instruction from IC. When MFIX_SEL is Low, DB[23:0] are used to transfer DISPLAY data according to the I/F Type

2 ELECTRICAL SPECIFICATIONS

2.1 ABSOLUTE MAXIMUM RATINGS

Table 14 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage for logic block	VDD - VSS	-0.3 to 3.3	V
Supply voltage for I/O block	VDD3 - VSS	-0.3 to +5.0	V
Supply voltage for step-up circuit	VCI - VSS	-0.3 to +5.0	V
LCD Supply Voltage range	AVDD - VSS	-0.3 to +6.5	V
	VGH - VSS	-0.3 to +22.0	V
	VSS - VGL	-0.3 to +22.0	V
	VSS - VCL	-0.3 to +5.0	V
	| VGH - VGL |	-0.3 to +33	V
Input Voltage range	Vin	-0.3 to VDD3 +0.5	V
Operating temperature	Topr	-40 to + 85	°C
Storage temperature	Tstg	-55 to +110	°C

NOTE:

1. The absolute maximum rating is the limit value. When the IC is exposed to the operating environment beyond this range the IC does not assure normal operations and may be damaged permanently, not be able to be recovered.
2. The operating temperature is the range of device-operating temperature. They do not guarantee chip performance.

Caution: Stresses above these absolute maximum ratings may cause permanent damage.
These are stress ratings only and functional operation at these conditions is not implied.
Exposure to maximum rating conditions for extended periods may reduce device reliability.

2.2 DC ELECTRICAL CHARACTERISTICS

2.2.1 BASIC CHARACTERISTICS

Table 15 DC Electrical Characteristics.

(Ta = 25°C)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Power supply for I/O	VDD3		1.65	-	3.3	V	
Power supply, for Internal reference	VCI		2.3	-	3.3	V	
LCD driving voltage	VGH		13.75		19.25		*1
	VGL		–13.75		–8.25		*1
	VCL		–3.0		–2.1		
	AVDD1		4.2		6.0		
	AVDD2		4.2		6.0		
	GVDD		2.46		5.0		
Logic Input voltage, high	V_{IH}		0.7* VDD3	-	VDD3	V	*2
Logic Input voltage, low	V_{IL}		0	-	0.3* VDD3	V	*2
Logic output voltage, high	V_{OH}	IOH = –0.5mA	0.8* VDD3	-	VDD3	V	*3
Logic output voltage, low	V_{OL}	IOL = 0.5mA	0.0	-	0.2* VDD3	V	*3
Leakage current, input	I_{IL}	VIN = VSS or VDD3	–1.0		1.0	μA	*2
Leakage current, output	I_{OL}	VIN = VSS or VDD3	–3.0		3.0	μA	*3
Operating frequency	Fosc	Frame(f) = 60Hz Display line = 480 Ta = 25°C	0.95* TYP	20	1.05* TYP	MHz	
Input voltage to the 1st Booster	VCI1		2.1		3.0	V	*4
Power efficiency of the 1st Booster	η_{AVDD1}	ILOAD = 4mA	90	95	-	%	
Power efficiency of the 1st Booster	η_{AVDD2}	ILOAD = 3mA	90	95	-	%	
Power efficiency of the 2nd Booster	η_{VGH}	ILOAD = 100uA	90	95	-	%	
Power efficiency of the 3rd Booster	η_{VGL}	ILOAD = 100uA	90	95	-	%	
Power efficiency of the 4th Booster	η_{VCL}	ILOAD = 300uA	90	95	-	%	
Current consumption during normal operation	IVDD3	VCI=3V, VDD3=3V Frame(f) = 60Hz MPU I/F White pattern MIE function off	-	-	5	mA	-

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
	IVCI	VCI=3V, VDD3=3V Frame(f) = 60Hz	-	-	20	mA	
Current consumption during Sleep mode (MPU I/F)	IVDD3	VDD3 = 3.3V	-	-	30	μA	
	IVCI	VCI = 3.3V	-	-	5	μA	
Current consumption during Sleep mode (MDDI I/F)	IVDD3	INIT_HIBER	-	-	50	μA	
	IVCI		-	-	160	μA	
Current consumption during Sleep mode (MIPI I/F)	IVDD3	LP-11	-	-	120	μA	
	IVCI		-	-	30	μA	
Current consumption during Deep Standby mode	IVDD3	VDD3 = 3.3V Ta = 25°C	-	-	1.0	μA	
	IVCI	VCI = 3.3V Ta = 25°C	-	-	1.0	μA	

NOTE:

1. VCI1=2.75V, |VGH-VGL| Max=30V
2. Signals under consideration; CSX, RDX, WRX, DB0 to DB23, RESX, SDA, IM, DCX, VSYNC, HSYNC, ENABLE, DOTCLK
3. Signals under consideration; DB0 to DB23, TE, SDA, SDO, BC, BC_CTL, TE
4. Practical VCI1 range is over 2.1V. VCI1 under 2.1V is used only for power-up period.

Table 16 DC Characteristics for LCD Driver Outputs

(TYP: VCI=VDD3=3.0V, Ta=25°C)

Characteristic	Symbol	Condition	MIN	TYP	MAX	Unit	Note
On resistance of Gate driver output	R_{onvgh}	VGH = 8.4V VGL = – 6.3V	-	-	7	kΩ	-
	R_{onvgl}		-	-	7	kΩ	-
On resistance of source driver output	R_{onp}	AVDD = 4.5V AVSS = 0V	-	-	20	kΩ	-
	R_{onn}		-	-	20	kΩ	-
On resistance of binary driver Output	R_{onpb}	GVDD = 4.5V AVSS = 0V	-	-	300	kΩ	-
	R_{onnb}		-	-	300	kΩ	-
Output voltage deviation (Mean value) AVDD=5.0V, GVDD=4.5V	ΔV_O	AVDD – 0.8V ≤ VSO	-	-	±20	mV	*1
		0.8V < VSO < AVDD – 0.8V	-	-	±10	mV	*1
		VSO ≤ 0.8V	-	-	±20	mV	*1
Delay, source driver	t_{SD}	AVDD = 5.5V VDD = 5.0V SAP = 1000	-	-	8.1	μs	*2
Delay, VCOM driver	t_{CD}	VCOM amplitude = 4.5V (VCOMH = 3.85V, VCOML = – 0.65V)	-	-	27.2	μs	*3
Delay, Gate driver	t_{GD}	VGH = 18.0V VGL = – 10.0V			5.4	μs	*4

NOTE:

1. VSO is the output voltage of analog output pads: S1 through S1080. GVDD=4.5V & AVDD=5.0V. When offset cancellation mode is enable. Refer to OCM[1:0]
2. tSD: LCD Source driver delay.(AVDD=5.5V, Input swing range = 1.1V to 4.5V, target voltage = input voltage +/–10mV). Panel load (typical case): R=8.8kohm, C=45pF.
3. tCD: LCD VCOM driver delay. (VCOM amplitude=4.5V, Input swing range = –0.65V to 3.85V, target voltage = input voltage +/–10mV) . Panel load (typical case): R=93.5ohm, C=31nF, CL1=33.3us
4. tGD: LCD Gate driver delay. (Input swing range = -10V to 18V, Rising & Falling target voltage = |VGH–VGL| × 0.05 ~ |VGH-VGL|x0.95), Panel load (typical case): R=15.7kohm, C=92pF.

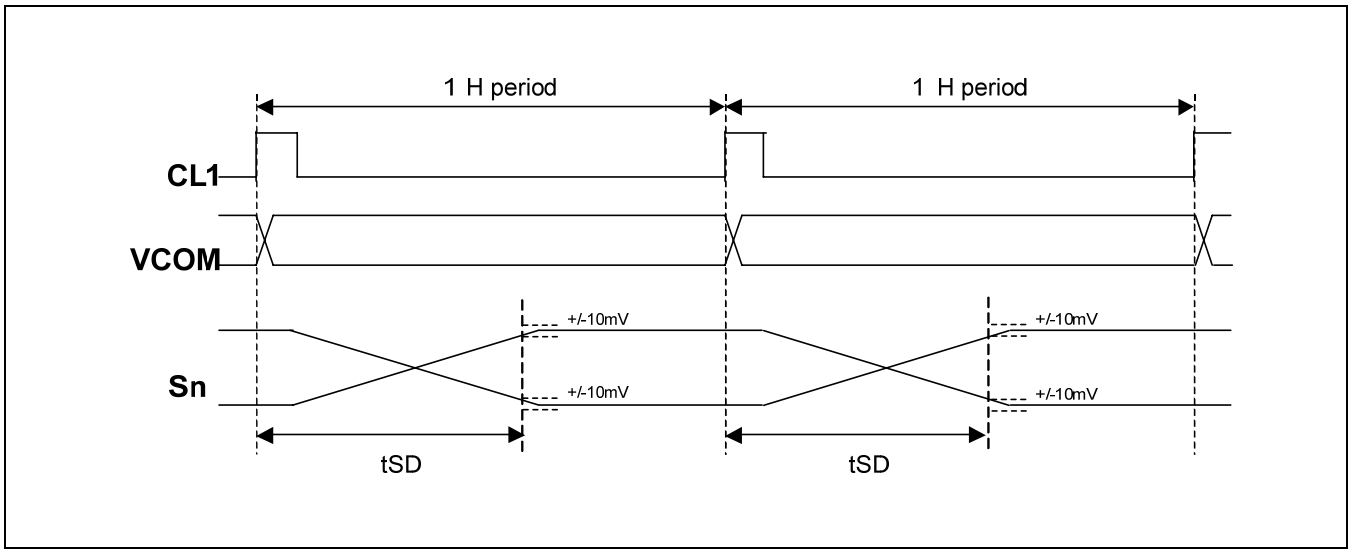


Figure 8 LCD Source Driver Delay

2.3 AC CHARACTERISTEICS

2.3.1 PARALLEL INTERFACE CHARACTERISTICS (80-SERIES MPU)

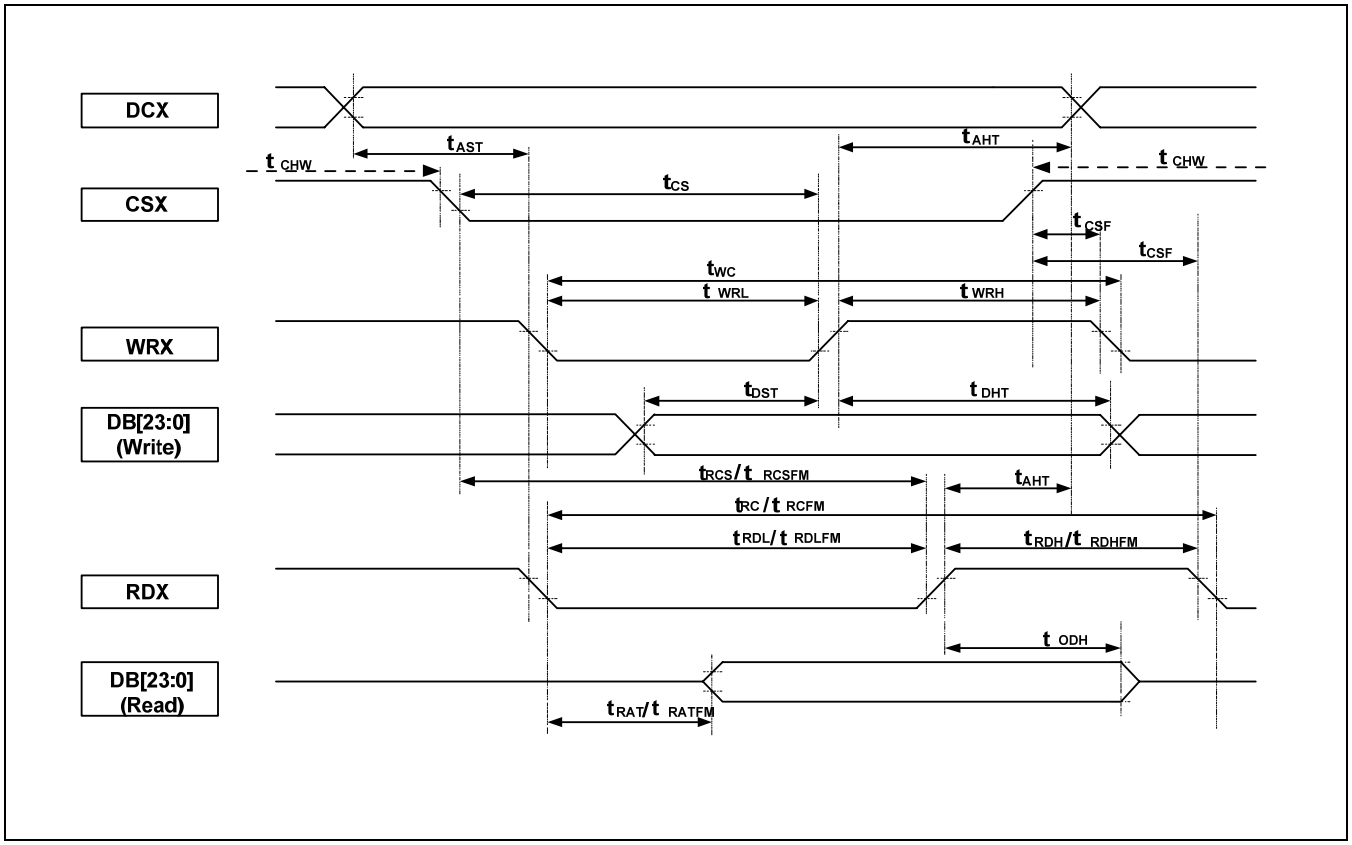


Figure 9 MPU 80 Interface AC Characteristics

Table 17 MPU 80 Interface AC Characteristics (1/2 Transfer)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DCX	tAST	Address setup time	0	-	ns	
	tAHT	Address hold time (Write/Read)	10	-	ns	
CSX	tCHW	Chip select “H” pulse width	0	-	ns	
	tCS	Chip select setup time (Write)	15	-	ns	
	tRCS	Chip select setup time (Read ID)	45	-	ns	
	tRCSFM	Chip select setup time (Read FM)	355	-	ns	
	tCSF	Chip select wait time (Write/Read)	10	-	ns	
WRX	tWC	Write cycle	44	-	ns	
	tWRH	Control pulse “H” duration	15	-	ns	
	tWRL	Control pulse “L” duration	15	-	ns	
RDX(ID)	tRC	Read cycle (ID)	160	-	ns	When read ID data
	tRDH	Control pulse “H” duration (ID)	90	-	ns	
	tRDL	Control pulse “L” duration (ID)	45	-	ns	
RDX(FM)	tRCFM	Read cycle (FM)	450	-	ns	When read from the frame memory
	tRDHFM	Control pulse “H” duration (FM)	90	-	ns	
	tRDLFM	Control pulse “L” duration (FM)	355	-	ns	
DB[23:0]	tDST	Data setup time	10	-	ns	For the maximum CL = 30pF, For the minimum CL = 8pF
	tDHT	Data hold time	10	-	ns	
	tRAT	Read access time (ID)	-	40	ns	
	tRATFM	Read access time (FM)	-	340	ns	
	tODH	Output disable time	20	80	ns	

NOTE:

1. Above table’s values are values of when supposed tr & tf by 7ns. If tr & tf change, above table’s values can change.
2. tRAT and tODH timings are based on 20% to 80 % of VDD3-GND.
3. Other timings are based on 30% to 70% of VDD3-GND.
4. tWRL and tRDL are related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.
5. DCX timing is related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.

Table 18 MPU 80 Interface AC Characteristics (3 Transfer)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DCX	tAST	Address setup time	0	-	ns	
	tAHT	Address hold time (Write/Read)	10	-	ns	
CSX	tCHW	Chip select “H” pulse width	0	-	ns	
	tCS	Chip select setup time (Write)	15	-	ns	
	tRCS	Chip select setup time (Read ID)	45	-	ns	
	tRCSFM	Chip select setup time (Read FM)	355	-	ns	
	tCSF	Chip select wait time (Write/Read)	10	-	ns	
WRX	tWC	Write cycle	25	-	ns	
	tWRH	Control pulse “H” duration	10	-	ns	
	tWRL	Control pulse “L” duration	10	-	ns	
RDX(ID)	tRC	Read cycle (ID)	160	-	ns	When read ID data
	tRDH	Control pulse “H” duration (ID)	90	-	ns	
	tRDL	Control pulse “L” duration (ID)	45	-	ns	
RDX(FM)	tRCFM	Read cycle (FM)	450	-	ns	When read from the frame memory
	tRDHFM	Control pulse “H” duration (FM)	90	-	ns	
	tRDLFM	Control pulse “L” duration (FM)	355	-	ns	
DB[23:0]	tDST	Data setup time	10	-	ns	For the maximum CL=30pF, For the minimum CL=8pF
	tDHT	Data hold time	10	-	ns	
	tRAT	Read access time (ID)	-	40	ns	
	tRATFM	Read access time (FM)	-	340	ns	
	tODH	Output disable time	20	80	ns	

NOTE:

1. Above table’s values are values of when supposed tr & tf by 7ns. If tr & tf change, above table’s values can change.
2. tRAT and tODH timings are based on 20% to 80 % of VDD3-GND.
3. Other timings are based on 30% to 70% of VDD3-GND.
4. tWRL and tRDL are related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.
5. DCX timing is related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.

2.3.2 PARALLEL INTERFACE CHARACTERISTICS (68-SERIES MPU)

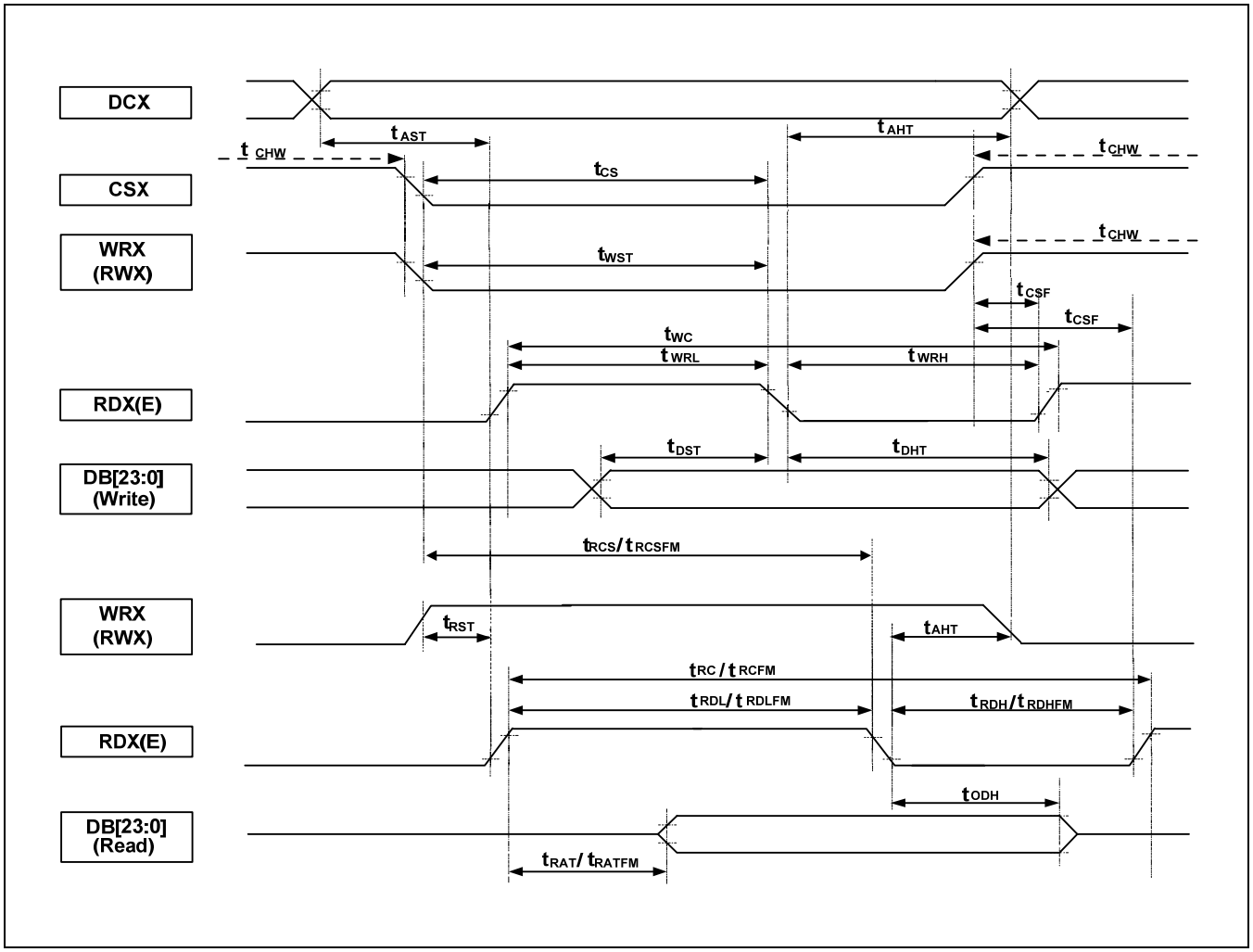


Figure 10 MPU 68 Interface AC Characteristics

Table 19 MPU 68 Interface AC Characteristics (1/2 Transfer)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DCX	tAST	Address setup time	0	-	ns	
	tAHT	Address hold time (Write/Read)	10	-	ns	
CSX	tCHW	Chip select “H” pulse width	0	-	ns	
	tCS	Chip select setup time (Write)	15	-	ns	
	tRCS	Chip select setup time (Read ID)	45	-	ns	
	tRCSFM	Chip select setup time (Read FM)	355	-	ns	
	tCSF	Chip select wait time (Write/Read)	10	-	ns	
RWX	tWST	Write setup time (Write)	15	-	ns	
	tRST	Read setup time (Read)	5	-	ns	
E	tWC	Write cycle	44	-	ns	
	tWRH	Control pulse “H” duration	15	-	ns	
	tWRL	Control pulse “L” duration	15	-	ns	
E(ID)	tRC	Read cycle (ID)	160	-	ns	When read ID data
	tRDH	Control pulse “H” duration (ID)	45	-	ns	
	tRDL	Control pulse “L” duration (ID)	90	-	ns	
E(FM)	tRCFM	Read cycle (FM)	450	-	ns	When read from the frame memory
	tRDHFM	Control pulse “H” duration (FM)	355	-	ns	
	tRDLFM	Control pulse “L” duration (FM)	90	-	ns	
DB[23:0]	tDST	Data setup time	10	-	ns	For the maximum CL=30pF, For the minimum CL=8pF
	tDHT	Data hold time	10	-	ns	
	tRAT	Read access time (ID)	-	40	ns	
	tRATFM	Read access time (FM)	-	340	ns	
	tODH	Output disable time	20	80	ns	

NOTE:

1. Above table’s values are values of when supposed tr & tf by 7ns. If tr & tf change, above table’s values can change.
2. tRAT and tODH timings are based on 20% to 80 % of VDD3–GND.
3. Other timings are based on 30% to 70% of VDD3-GND.
4. tWRL and tRDL are related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.
5. DCX timing is related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.

Table 20 MPU 68 Interface AC Characteristics (3 Transfer)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DCX	tAST	Address setup time	0	-	ns	
	tAHT	Address hold time (Write/Read)	10	-	ns	
CSX	tCHW	Chip select “H” pulse width	0	-	ns	
	tCS	Chip select setup time (Write)	15	-	ns	
	tRCS	Chip select setup time (Read ID)	45	-	ns	
	tRCSFM	Chip select setup time (Read FM)	355	-	ns	
	tCSF	Chip select wait time (Write/Read)	10	-	ns	
RWX	tWST	Write setup time (Write)	15	-	ns	
	tRST	Read setup time (Read)	5	-	ns	
E	tWC	Write cycle	25	-	ns	
	tWRH	Control pulse “H” duration	10	-	ns	
	tWRL	Control pulse “L” duration	10	-	ns	
E(ID)	tRC	Read cycle (ID)	160	-	ns	When read ID data
	tRDH	Control pulse “H” duration (ID)	45	-	ns	
	tRDL	Control pulse “L” duration (ID)	90	-	ns	
E(FM)	tRCFM	Read cycle (FM)	450	-	ns	When read from the frame memory
	tRDHFM	Control pulse “H” duration (FM)	355	-	ns	
	tRDLFM	Control pulse “L” duration (FM)	90	-	ns	
DB[23:0]	tDST	Data setup time	10	-	ns	For the maximum CL=30pF, For the minimum CL=8pF
	tDHT	Data hold time	10	-	ns	
	tRAT	Read access time (ID)	-	40	ns	
	tRATFM	Read access time (FM)	-	340	ns	
	tODH	Output disable time	20	80	ns	

NOTE:

1. Above table’s values are values of when supposed tr & tf by 7ns. If tr & tf change, above table’s values can change.
2. tRAT and tODH timings are based on 20% to 80 % of VDD3-GND.
3. Other timings are based on 30% to 70% of VDD3-GND.
4. tWRL and tRDL are related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.
5. DCX timing is related with an interval in which CSX=”L” and WRX, RDX=”L” overlap.

2.3.3 SERIAL INTERFACE CHARACTERISTICS, WHEN MFIX_SEL=0 (3-WIRE/ 9-BIT SERIAL INTERFACE)

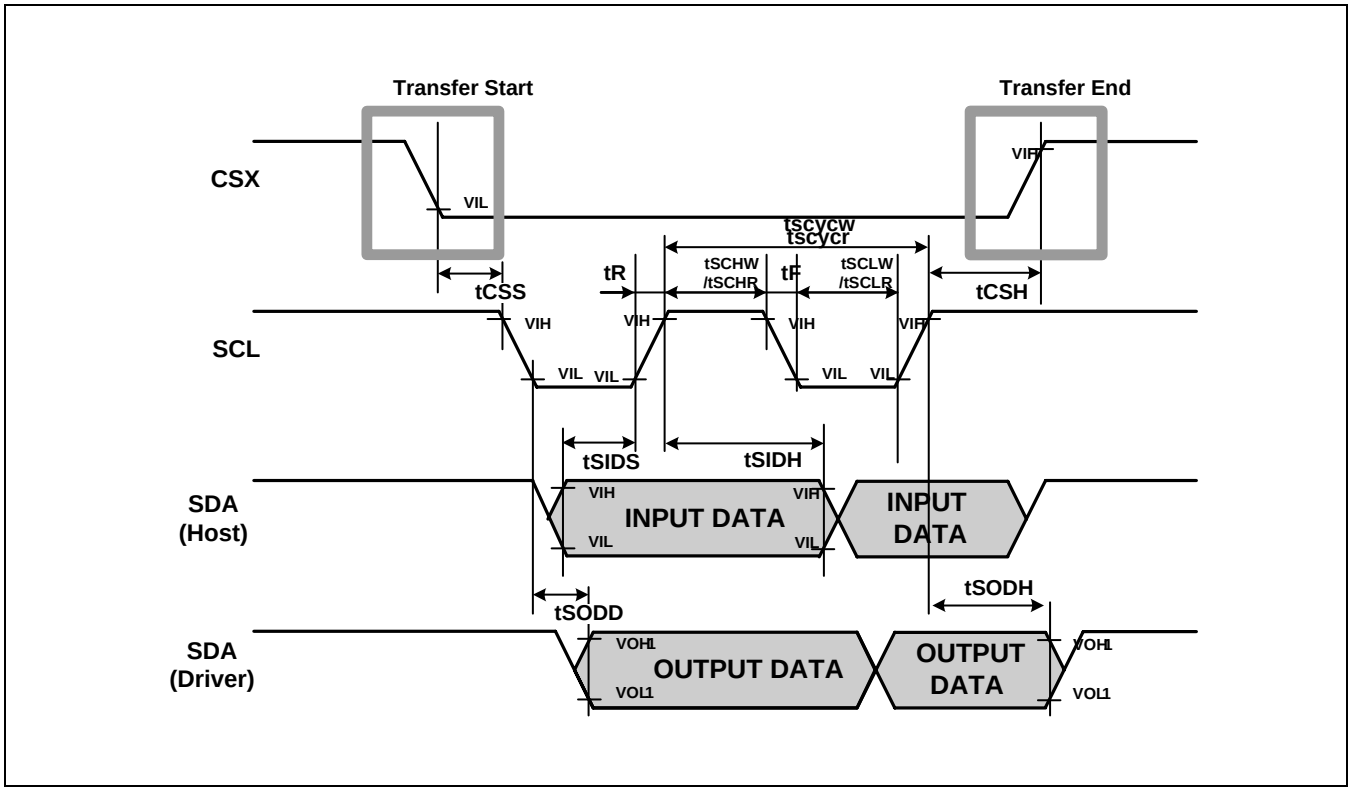


Figure 11 3- wire 9bit Serial Interface Characteristics, When MFIX_SEL=0

Table 21 Serial Interface AC Characteristics, When MFIX_SEL=0 (3-wire 9bit)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscycw	66	-	ns
Serial clock read cycle time	tscycr	150	-	ns
Serial clock rise / fall time	tR, tF	-	Note	ns
Pulse width high for write	tSCHW	15	-	ns
Pulse width high for read	tSCHR	60	-	ns
Pulse width low for write	tSCLW	15	-	ns
Pulse width low for read	tSCLR	60	-	ns
Chip Select setup time	tCSS	15	-	ns
Chip Select hold time	tCSH	15	-	ns
Serial input data setup time	tSIDS	15	-	ns
Serial input data hold time	tSIDH	15	-	ns
Serial output data delay time	tSODD	5	50	ns
Serial output data hold time	tSODH	15	75	ns

NOTE: Above table's values are values of when supposed tr & tf by 2ns. If tr & tf change, above table's values can change.

2.3.4 SERIAL INTERFACE CHARACTERISTICS, WHEN MFIX_SEL=1 (3-WIRE/ 9-BIT SERIAL INTERFACE)

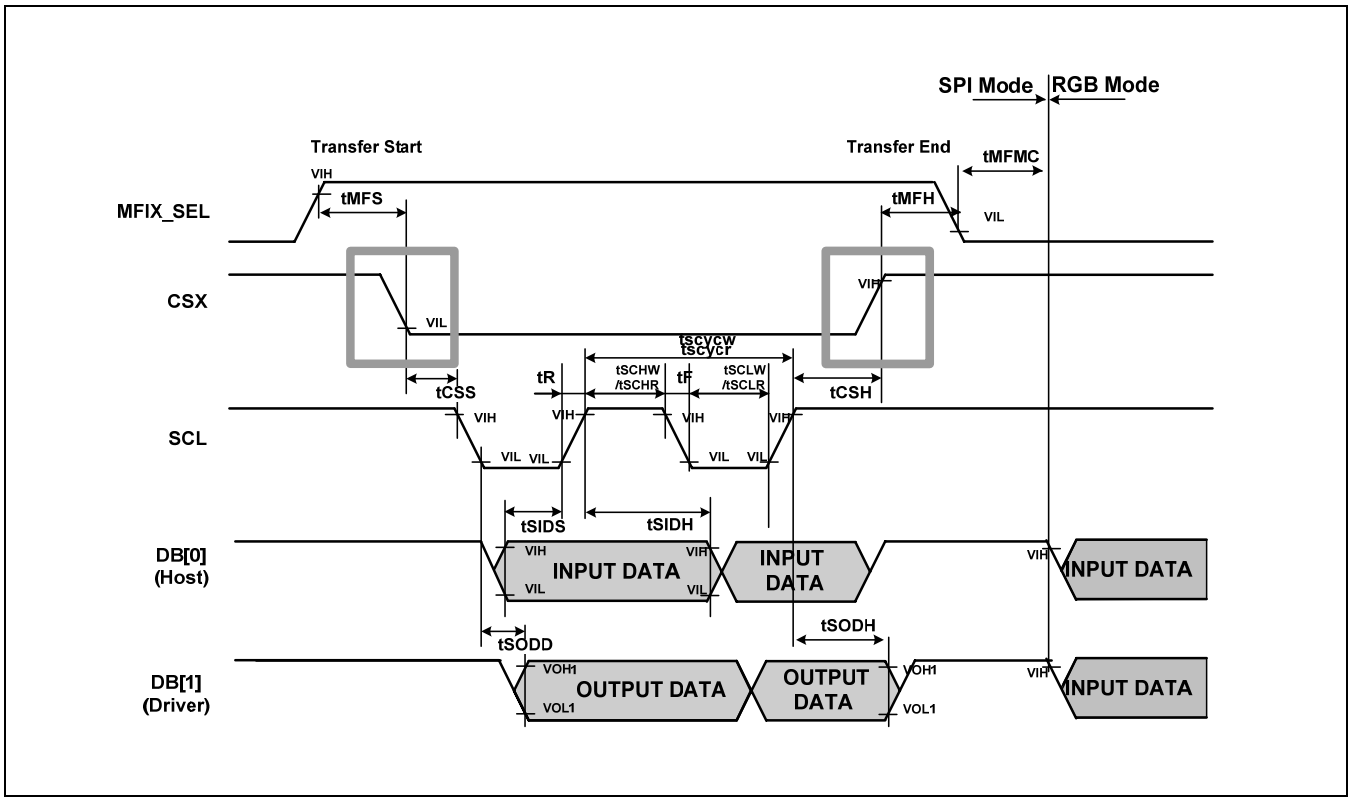


Figure 12 3- wire 9bit Serial Interface Characteristics, When MFIX_SEL=1

Table 22 Serial interface AC Characteristics, When MFIX_SEL=1 (3-wire 9bit)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscycw	66	-	ns
Serial clock read cycle time	tscycr	150	-	ns
Serial clock rise / fall time	tR, tF	-	Note	ns
Pulse width high for write	tSCHW	15	-	ns
Pulse width high for read	tSCHR	60	-	ns
Pulse width low for write	tSCLW	15	-	ns
Pulse width low for read	tSCLR	60	-	ns
Chip Select setup time	tCSS	15	-	ns
Chip Select hold time	tCSH	15	-	ns
Serial input data setup time	tSIDS	15	-	ns
Serial input data hold time	tSIDH	15	-	ns
Serial output data delay time	tSODD	5	50	ns
Serial output data hold time	tSODH	15	75	ns
Command setup time	tMFS	10	-	ns
Command Hold time	tMFH	10	-	ns
MFIX_SEL Mode Change time	tMFMC	20	-	ns

NOTE: Above table's values are values of when supposed tr & tf by 2ns. If tr & tf change, above table's values can change.

2.3.5 SERIAL INTERFACE CHARACTERISTICS, WHEN MFIX_SEL=0 (4-WIRE/ 8-BIT SERIAL INTERFACE)

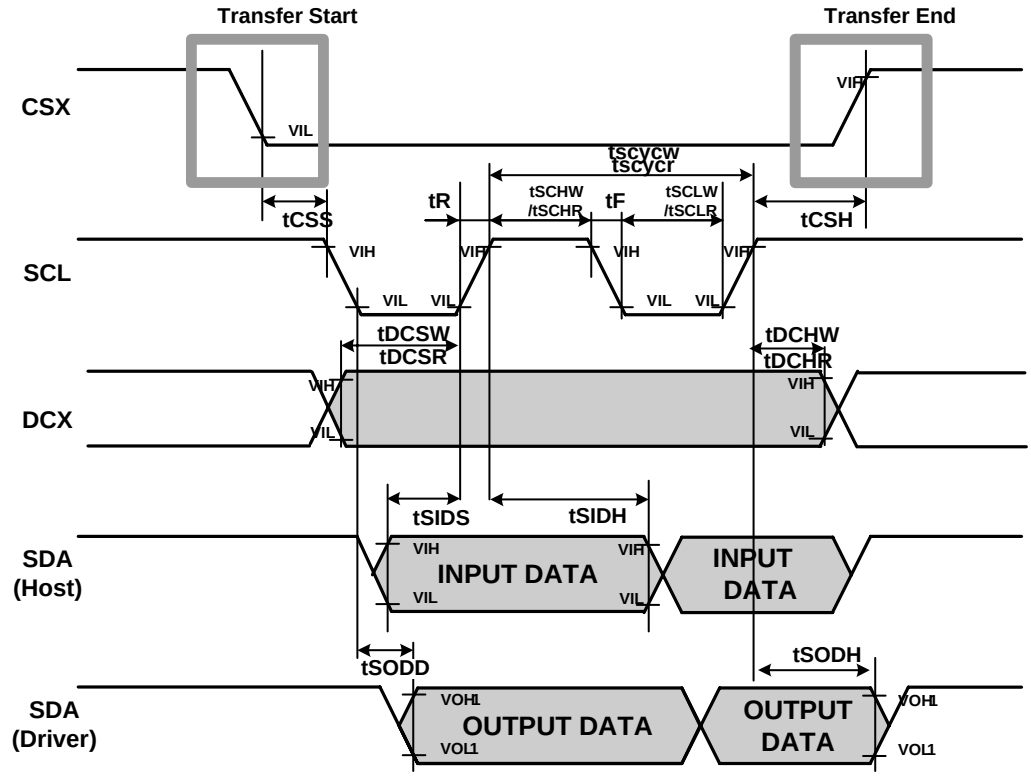


Figure 13 4-wire 8bit Serial Interface Characteristics, When MFIX_SEL=0

Table 23 Serial Interface AC Characteristics, When MFIX_SEL=0(4-wire 8bit)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscycw	66		ns
Serial clock read cycle time	tscycr	150		ns
Serial clock rise / fall time	tR, tF		Note	ns
Pulse width high for write	tSCHW	30		ns
Pulse width high for read	tSCHR	60		ns
Pulse width low for write	tSCLW	30		ns
Pulse width low for read	tSCLR	60		ns
Chip Select setup time	tCSS	15		ns
Chip Select hold time	tCSH	15		ns
DCX Setup time for write	tDCSW	15		ns
DCX Setup time for read	tDCSR	60		ns
DCX hold time for write	tDCHW	20		ns
DCX hold time for read	tDCHR	60		ns
Serial input data setup time	tSIDS	15		ns
Serial input data hold time	tSIDH	15		ns
Serial output data delay time	tSODD	5	50	ns
Serial output data hold time	tSODH	15	75	ns

NOTE: Above table's values are values of when supposed tr & tf by 2ns. If tr & tf change, above table's values can change.

2.3.6 SERIAL INTERFACE CHARACTERISTICS, WHEN MFIX_SEL=1 (4-WIRE/ 8-BIT SERIAL INTERFACE)

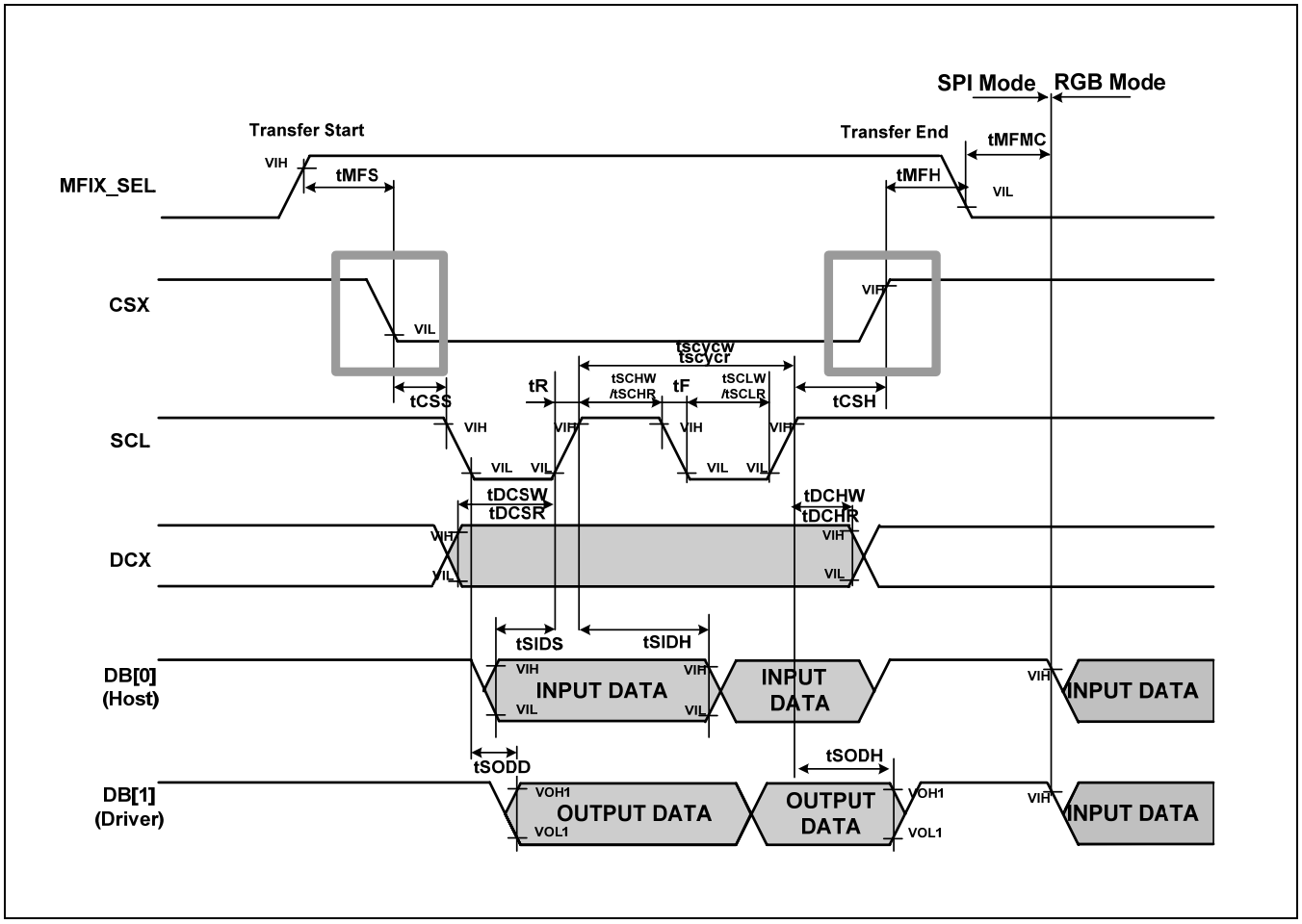


Figure 14 4-wire 8bit Serial Interface Characteristics, When MFIX_SEL=1

Table 24 Serial Interface AC Characteristics, When MFIX_SEL=1 (4-wire 8bit)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscycw	66		ns
Serial clock read cycle time	tscycr	150		ns
Serial clock rise / fall time	tR, tF		Note	ns
Pulse width high for write	tSCHW	30		ns
Pulse width high for read	tSCHR	60		ns
Pulse width low for write	tSCLW	30		ns
Pulse width low for read	tSCLR	60		ns
Chip Select setup time	tCSS	15		ns
Chip Select hold time	tCSH	15		ns
DCX Setup time for write	tDCSW	15		ns
DCX Setup time for read	tDCSR	60		ns
DCX hold time for write	tDCHW	20		ns
DCX hold time for read	tDCHR	60		ns
Serial input data setup time	tSIDS	15		ns
Serial input data hold time	tSIDH	15		ns
Serial output data delay time	tSODD	5	50	ns
Serial output data hold time	tSODH	15	75	ns
Command setup time	tMFS	10	-	ns
Command hold time	tMFH	10	-	ns
MFIX_SEL Mode Change time	tMFMC	20	-	ns

NOTE: Above table's values are values of when supposed tr & tf by 2ns. If tr & tf change, above table's values can change.

2.3.7 RGB INTERFACE CHARACTERISTICS

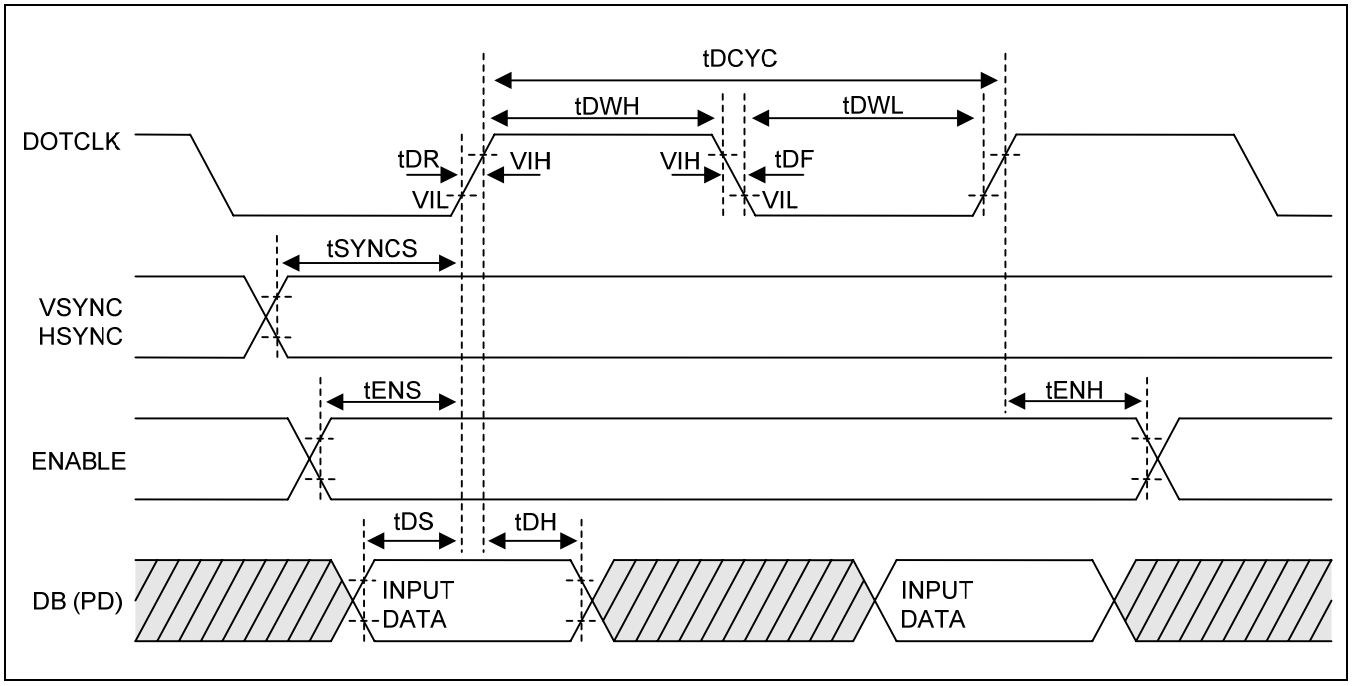


Figure 15 RGB Interface Characteristics

Table 25 RGB Interface AC Characteristics (1 Transfer)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Parameter	Description	Min	Max	Unit
tDCYC	DOTCLK period	47	-	ns
tDWL	DOTCLK pulse width low	15	-	ns
tDWH	DOTCLK pulse width high	15	-	ns
tDR / tDF	DOTCLK rising / falling time		Note	ns
tSYNCS	VSYNC, HSYNC setup	13	-	ns
tENS	ENABLE setup	13	-	ns
tENH	ENABLE hold	13	-	ns
tDS	Input Data setup	13	-	ns
tDH	Input Data hold	13	-	ns

NOTE:
1. Above table's values are values of when supposed tr & tf by 7ns. If tr & tf change, above table's values can change.
2. VSYNC Low Pulse Width ≥2H
3. HSYNC Low Pulse Width ≥ 2 DOTCLK (24/18/16 bit I/F)

Table 26 RGB interface AC Characteristics (3 Transfer)

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Parameter	Description	Min	Max	Unit
tDCYC	DOTCLK period	30	-	ns
tDWL	DOTCLK pulse width low	12	-	ns
tDWH	DOTCLK pulse width high	12	-	ns
tDR / tDF	DOTCLK rising / falling time		Note	ns
tSYNCS	VSYNC, HSYNC setup	10	-	ns
tENS	ENABLE setup	10	-	ns
tENH	ENABLE hold	10	-	ns
tDS	Input Data setup	10	-	ns
tDH	Input Data hold	10	-	ns

NOTE:

1 Above table's values are values of when supposed tr & tf by 7ns. If tr & tf change, above table's values can change.

2. VSYNC Low Pulse Width ≥2H

3. HSYNC Low Pulse Width ≥ 6 DOTCLK (8/6 bit I/F)

2.3.8 RESX SIGNAL

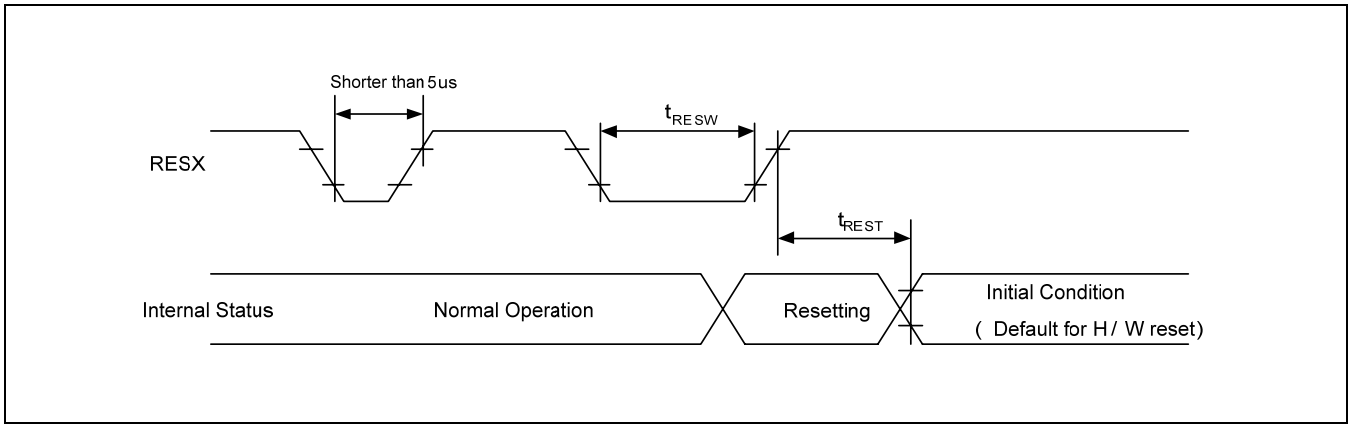


Figure 16 Reset Input Timing

Table 27 Reset Input Timing When APON=1

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Symbol	Parameter	Pad	Min	Typ	Max	Unit	Note
tRESW	Reset low pulse width	RESX	10	-	-	µs	-
tREST	Reset completion time	RESX	-	-	5	ms	Reset during Sleep In mode
		RESX		-	120	ms	Reset during Sleep Out mode

Table 28 Reset Input Timing When APON=0

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Symbol	Parameter	Pad	Min	Typ	Max	Unit	Note
tRESW	Reset low pulse width	RESX	10	-	-	µs	-
tREST	Reset completion time	RESX	-	-	5	ms	Reset during Sleep In mode
		RESX		-	5	ms	Reset during Sleep Out mode

Table 29 Reset Input Timing When Deep Standby

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Symbol	Parameter	Pad	Min	Typ	Max	Unit	Note
tRESW	Reset low pulse width	RESX	50	-	-	µs	-
tREST	Reset completion time	RESX	-	-	5	ms	Reset during Deep standby mode

Table 30 RESX Pulse

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

NOTE:

1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.
2. During the reset period, the display will be blanked (The display is entering blanking sequence, for which the maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains in the blank state in Sleep In–mode) and then return to Default condition for H/W reset.
3. During Reset Completion Time, ID1, ID2, ID3 and VCM, VML, GVD Offset value in MTP will be latched to the internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
4. Spike Rejection also applies during a valid reset pulse as shown below:.

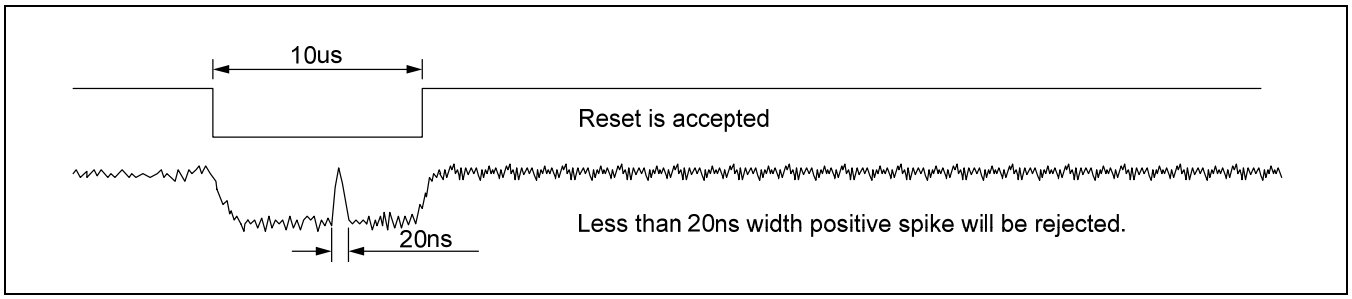


Figure 17 RESX Pulse Width

5. It is necessary to wait for 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

2.3.9 MEASUREMENT CONDITIONS

The measurement conditions shown in this section is provided for a reference purpose to the module makers. The condition for the actual IC measurement will be determined after the consideration of a practical manufacturing environment of mass production.

2.3.9.1 tRATFM, tODH Measurement Condition

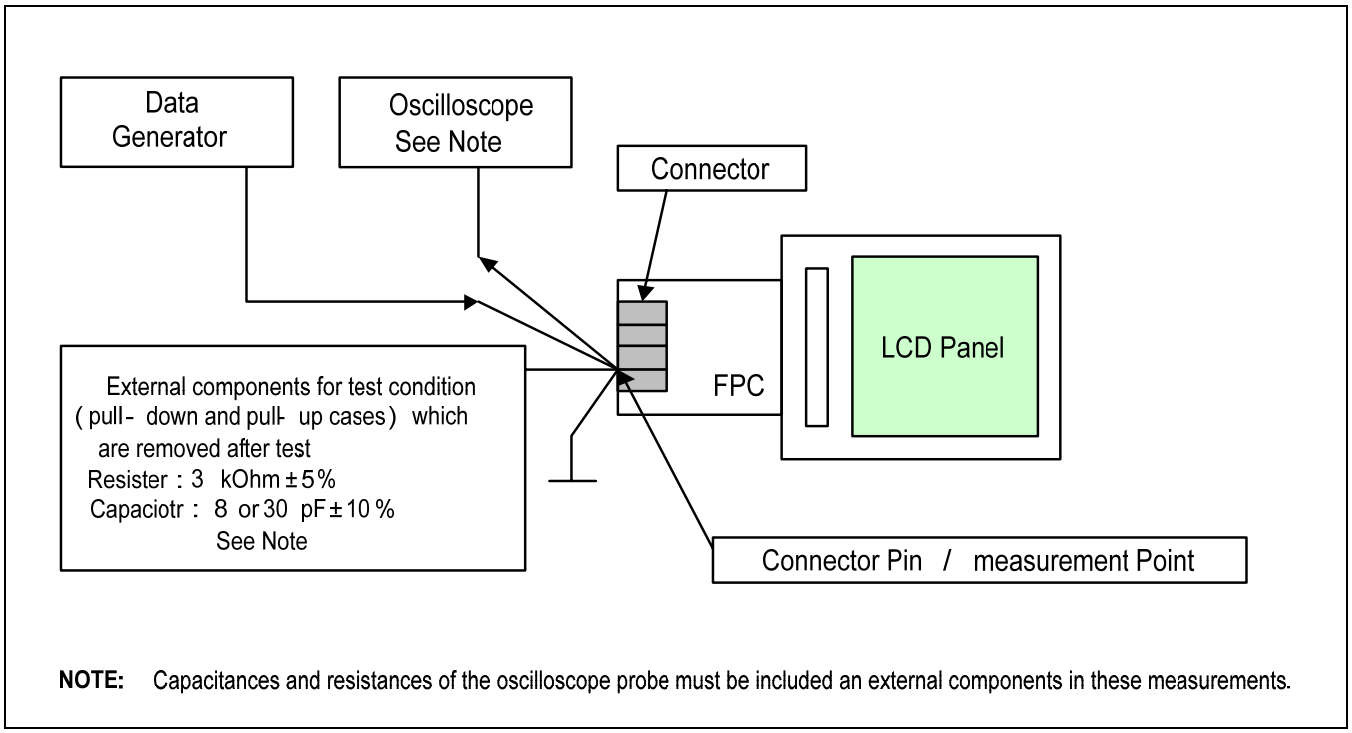


Figure 18 Measurement Condition Set-up of MPU Interface at a Module Level

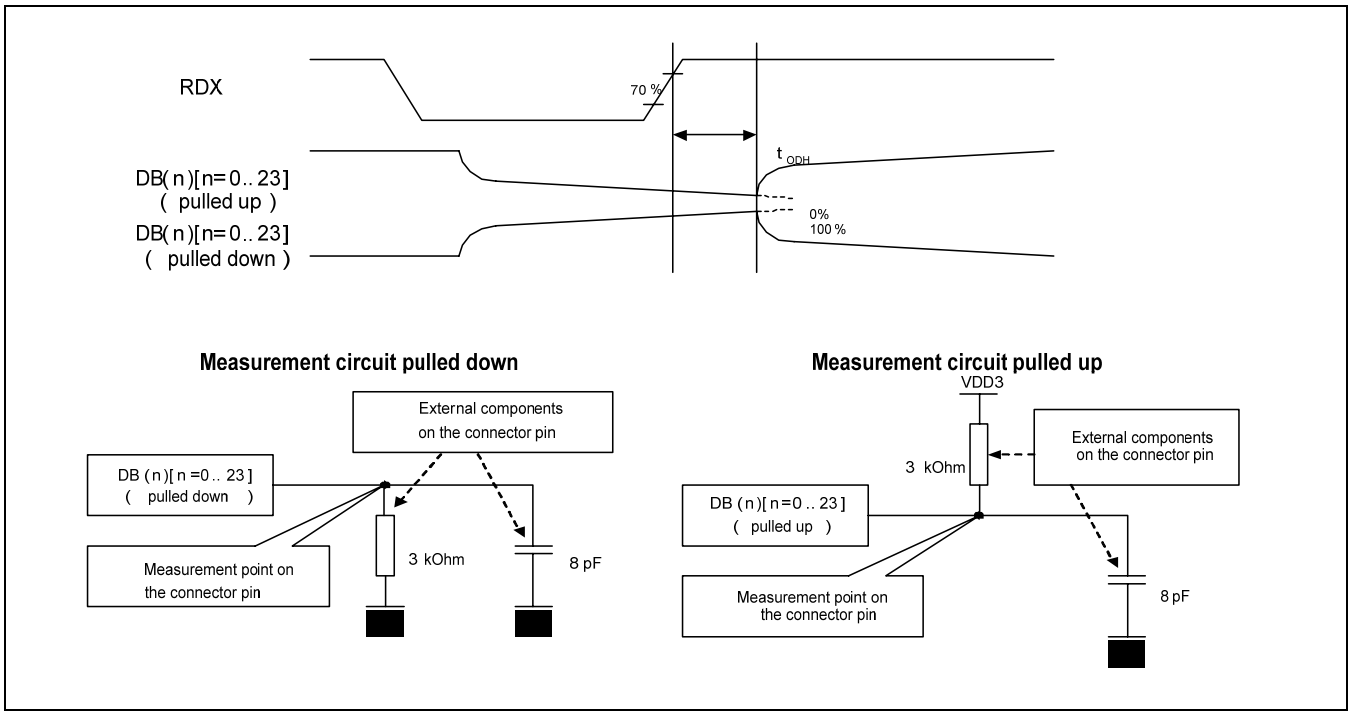


Figure 19 Minimum Value Measurement of MPU Interface

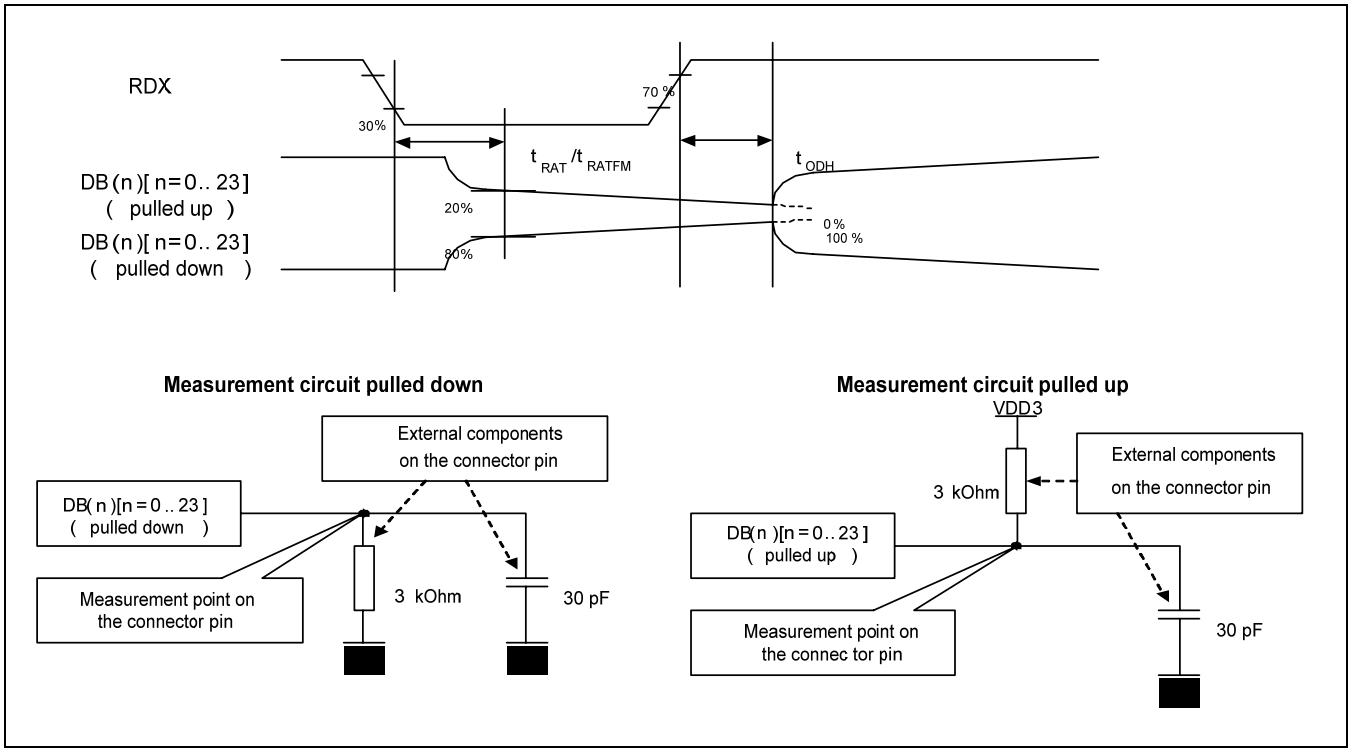


Figure 20 Maximum Value Measurement of MPU Interface

2.3.9.2 tSODD, tSODH Measurement Condition

Measurement Condition Set-up

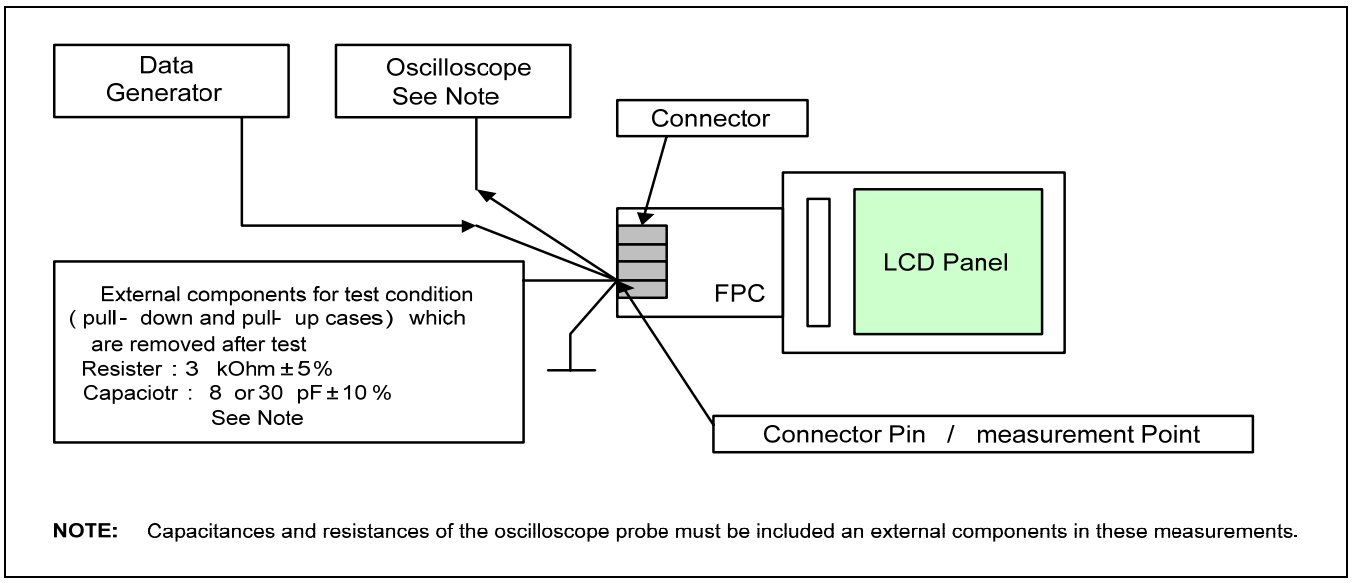


Figure 21 Measurement Condition Set-up of SPI at a Module Level

Minimum Value Measurement

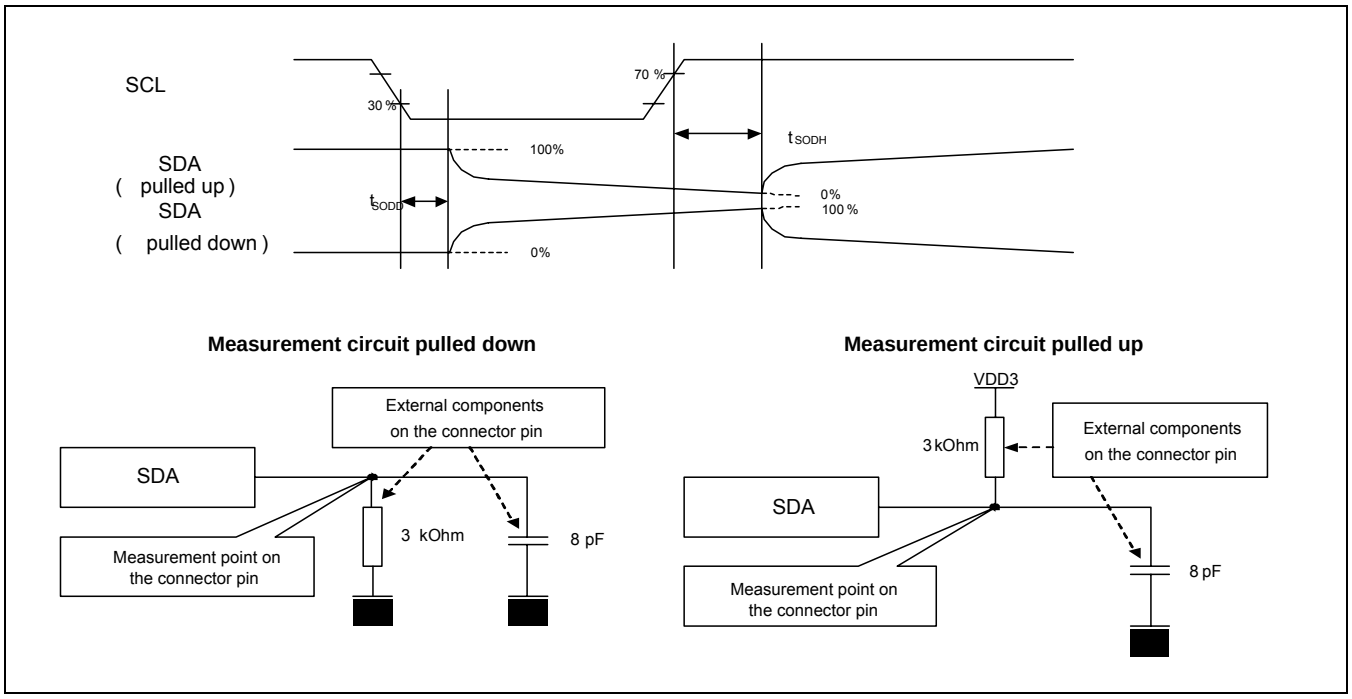


Figure 22 Minimum Value Measurement of SPI

Maximum Value Measurement

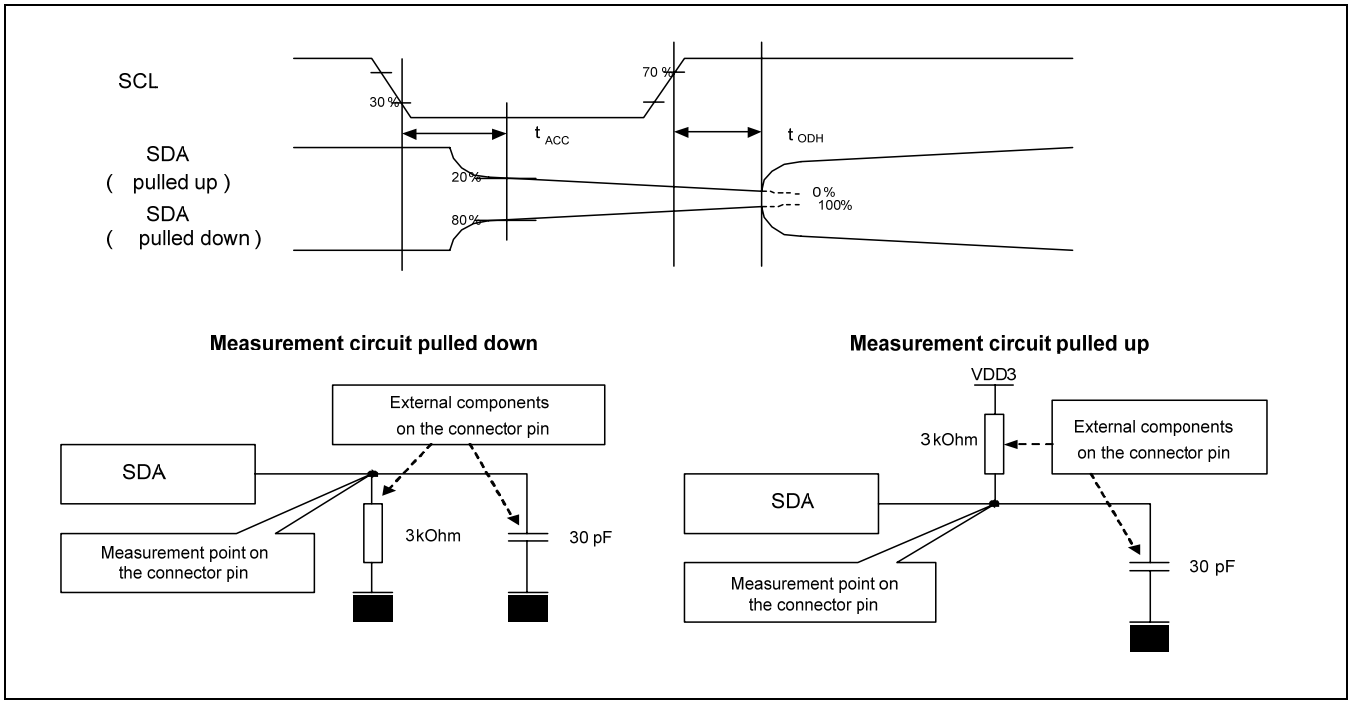


Figure 23 Maximum Value Measurement of SPI

2.4 MDDI DC/AC CHARACTERISTICS

Table 31 Data/Strobe Rx DC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal shall be interpreted as a logic-one level.			50	mV	
V_{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as logic-zero level.	–50			mV	
V_{IT+}	Receiver differential input high threshold voltage (offset for hibernation wake-up).Above this differential voltage the input signal shall be interpreted as a logic-one level.		125	175	mV	
V_{IT-}	Receiver differential input low threshold voltage (offset for hibernation wake-up).Below this differential voltage the input signal shall be interpreted as logic-zero level.	75	125		mV	
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0		1.65	V	
R_{term}	Parallel termination resistance value	98	100	102	Ω	

Table 32 Driver Electrical DC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit	Note
$I_{diffabs}$	Absolute driver differential output current range (Current through the termination resistor)	2.5		4.5	mA	Rterm = 100Ω
$V_{out-rng-int}$	Single-ended driver output voltage range with respect to ground, internal mode	0.35		1.60	V	Under all conditions, including double-drive

Please refer to VESA specification Ver 1.0

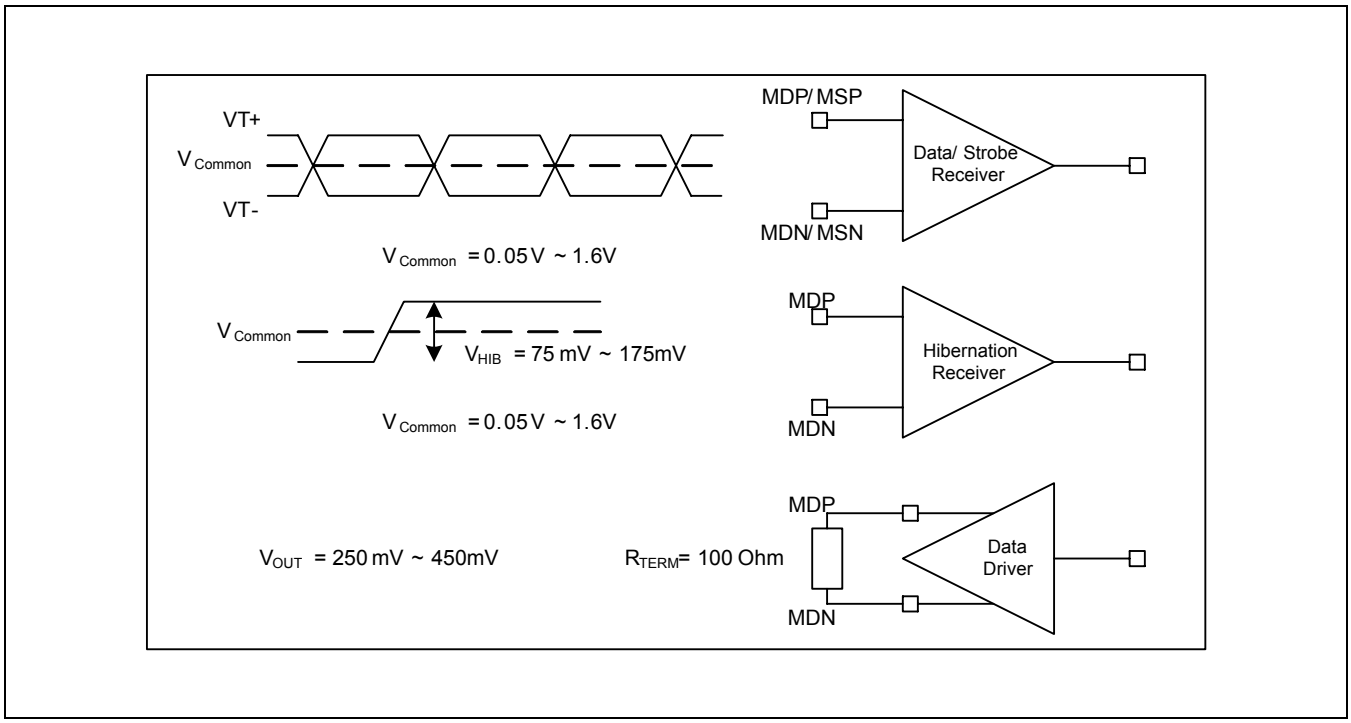


Figure 24 MDDI Receiver, Driver Electrical Diagram

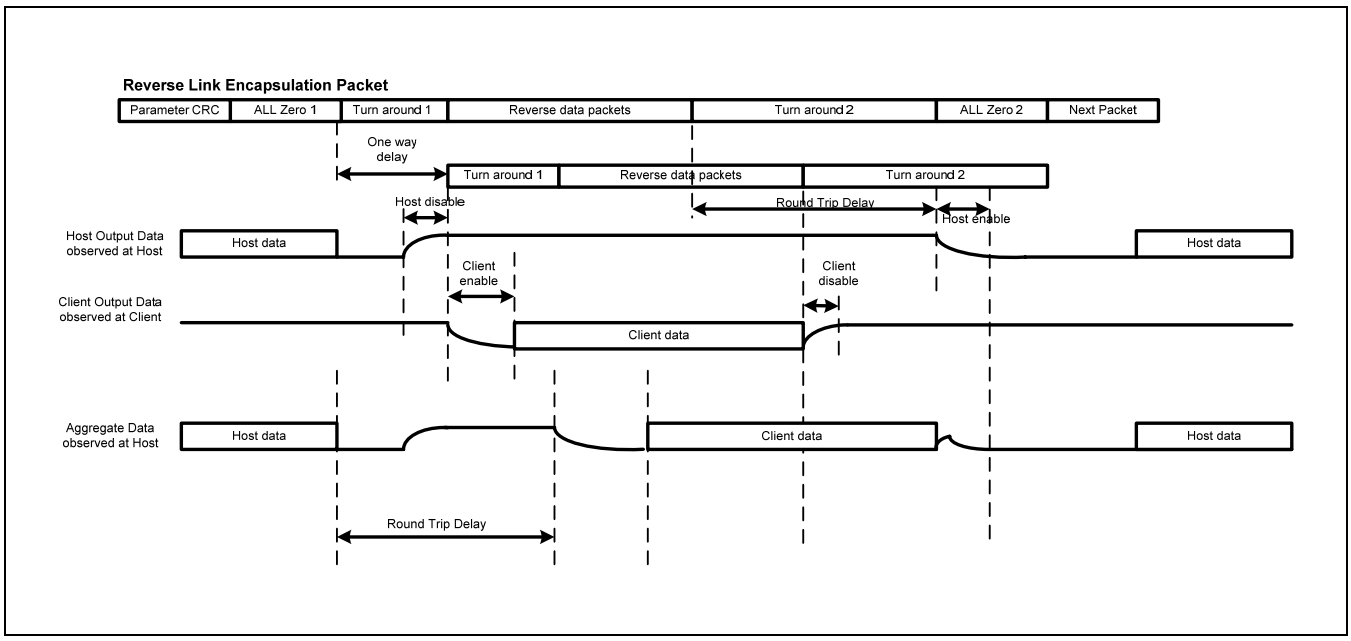


Figure 25 Host Enable/Disable Time and Client Enable/Disable Time Diagram

Table 33 Receiver AC Characteristics

Parameter	Description	MIN	TYP	MAX	Unit
t_{BIT}	Forward link data bit rate.	2.666		-	ns
$T_{host\text{-}enable}$	Host output enable time	0		24*tBIT	ns
$T_{host\text{-}disable}$	Host output disable time, entire length of the Turn-Around 1 field	0		24*tBIT	ns
$T_{client\text{-}enable}$	Client output enable time, entire length of the Turn-Around 1 field	0		24*tBIT	ns
$T_{client\text{-}disable}$	Client output disable time, measured from the end of the last bit of the Turn-Around 2 field	0		24*tBIT	ns

NOTE: tBIT= 1 / Link_Data_Rate, where Link_Data_Rate is the bit rate of a single data pair
(For example, if the average forward link bit rate is 375Mbps, then tBIT= 1 / 375Mbps = 2.666ns)
These specifications are from VESA specification Ver 1.1

2.5 MIPI CHARACTERISTICS

2.5.1 DC CHARACTERISTICS

Table 34 MIPI DC Characteristics

Items		Parameter	Min	Nom	Max	Unit	Notes
LP_TX	Thevenin output high level	V_{OH}	1.1	1.2	1.3	V	
	Thevenin output low level	V_{OL}	–50		50	mV	
	Output impedance of LP transmitter	Z_{OLP}	110			Ω	1
HS_RX	Common-mode voltage HS receive mode	$V_{CMRX(DC)}$	70		330	mV	2,3
	Differential input high threshold	V_{IDTH}			70	mV	
	Differential input low threshold	V_{IDTL}	–70			mV	
	Single-ended input high voltage	V_{IHHS}			460	mV	2
	Single-ended input low voltage	V_{ILHS}	–40			mV	2
	Single-ended threshold for HS termination enable	$V_{TERM-EN}$			450	mV	
	Differential input impedance	Z_{ID}	80	100	125	Ω	
LP_RX	Logic 1 input voltage	V_{IH}	880			mV	
	Logic 0 input voltage, not in ULP State	V_{IL}			550	mV	
	Input hysteresis	V_{HYST}	25			mV	
LP_CD	Logic 1 contention threshold	V_{IHCD}	450			mV	
	Logic 0 contention threshold	V_{ILCD}			200	mV	

NOTE:

1. Even though the maximum value for ZOLP is not specified, the output impedance of LP transmitter ensures that the TRLP/TFLP specification is met
2. Excluding additional RF interference of 100mV peak sine wave beyond 450MHz
3. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

2.5.2 HIGH SPEED DATA-CLOCK TIMING

The Host sends a differential clock signal to S6D05A1 for data sampling. This signal is a DDR (half-rate) clock having one transition per data bit time. The timing relationship of DDR clock differential signal to the Data differential signal is shown in *Figure 26*.

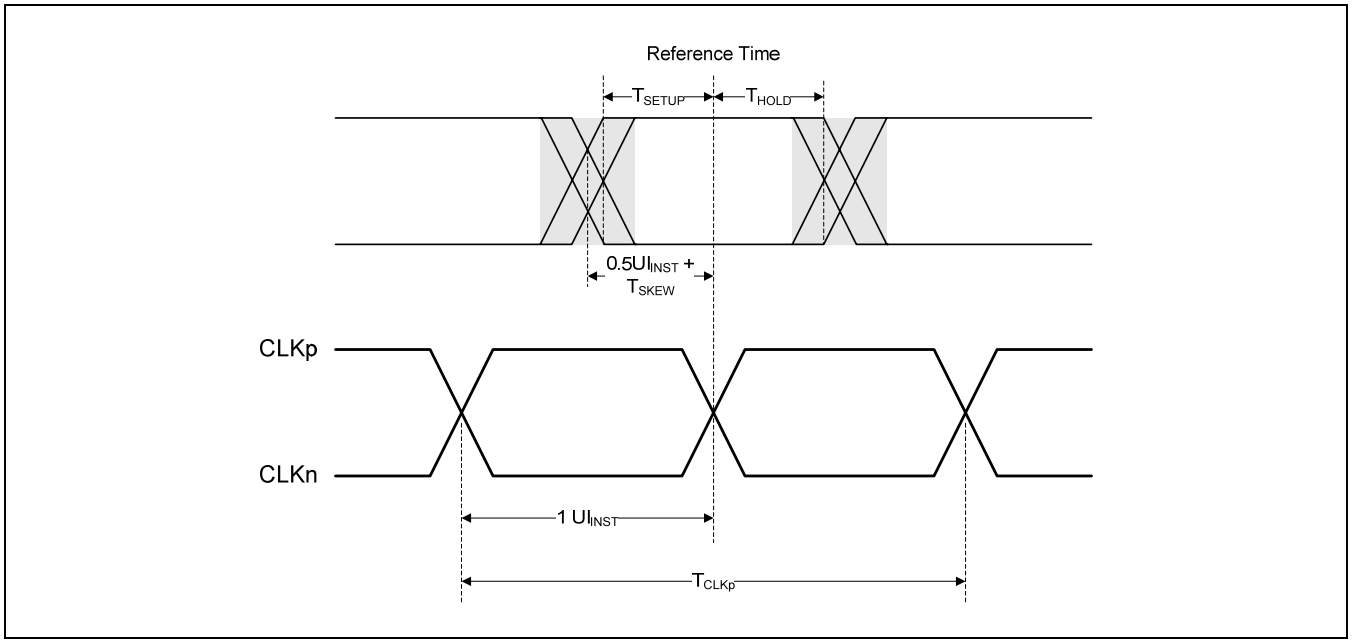


Figure 26 MIPI Data to Clock Timing Definitions

Table 35 MIPI Pin Characteristic Specifications

Clock Parameter	Symbol	#of d-lane	Min	Typ	Max	Unit	Notes
UI Instantaneous	UIINST	1	2		12.5	ns	1,2

NOTE:
1. This value corresponds to a minimum 80 Mbps data rate.
2 Minimum UI shall not be violated for any single bit period, that is any DDR half cycle within a data burst.

Table 36 MIPI Data-Clock Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data to Clock Skew [Measured at transmitter]	$T_{SKEW[TX]}$	–0.15		0.15	U_{IINST}	1
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15			U_{IINST}	2
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15			U_{IINST}	2

NOTE:
1. Total silicon and package delay budget of 0.3* UIINST
2. Total setup and hold window for receiver of 0.3* UIINST

3 INTERFACE

3.1 MPU INTERFACE

3.1.1 INTERFACE TYPE SELECTION

While the driver IC is used to parallel interface, it transfers commands, parameters and display data between the driver IC and MPU using a bi-directional data line up to 24 bits of bus width. The interface which communicates with MPU is selected by using a combination of IM [3:0] pins.

Table 37 Interface Type Selection

Mode	IM3	IM2	IM1	IM0
80 MPU 24-bit Parallel I/F	0	1	0	0
80 MPU 18-bit Parallel I/F	0	0	1	1
80 MPU 16-bit Parallel I/F	0	0	0	0
80 MPU 9-bit Parallel I/F	0	0	0	1
80 MPU 8-bit Parallel I/F	0	0	1	0
3-wire 9bit Data Serial I/F	x	1	0	1
4-wire 8bit Data Serial I/F	x	1	1	0
MDDI	0	1	1	1
68 MPU 24-bit Parallel I/F	1	1	0	0
68 MPU 18-bit Parallel I/F	1	0	1	1
68 MPU 16-bit Parallel I/F	1	0	0	0
68 MPU 9-bit Parallel I/F	1	0	0	1
68 MPU 8-bit Parallel I/F	1	0	1	0
MIPI	1	1	1	1

3.1.2 PAD DESCRIPTION OF MPU INTERFACE

MPU interface of the S6D05A1 is changed according to the bus width used. The pin assignments are listed in the table below. When CSX is inactive as high, DB23 to DB0 are placed in the high-impedance state internally.

3.1.2.1 80/68-series MPU Parallel Interface

Table 38 Interface Signal Description in Case of MPU I/F

<table>
<tr><th>Pin Name</th><th colspan="2">Description</th></tr>
<tr><td>CSX</td><td colspan="2">Chip select control signal</td></tr>
<tr><td>DCX</td><td colspan="2">Data bus transfers a command when DCX is low.
Data bus transfers parameters or display data when DCX is high.</td></tr>
<tr><td>RDX</td><td colspan="2">Read control signal
When RDX is low, the data bus is held on output state.</td></tr>
<tr><td>WRX</td><td colspan="2">Write control signal
Data is latched on the rising edge of WRX.</td></tr>
<tr><td rowspan="7">DB23 to DB0</td><td colspan="2">Data bus</td></tr>
<tr><td>Mode</td><td>DB pads</td></tr>
<tr><td>80/68 MPU 24-bit Parallel I/F</td><td>DB23-DB0 : 24-bit data</td></tr>
<tr><td>80/68 MPU 18-bit Parallel I/F</td><td>DB23-DB18 : unused
DB17-DB0 : 18-bit data</td></tr>
<tr><td>80/68 MPU 16-bit Parallel I/F</td><td>DB23-DB16 : unused
DB15-DB0 : 16-bit data</td></tr>
<tr><td>80/68 MPU 9-bit Parallel I/F</td><td>DB23-DB9 : unused
DB8-DB0 : 9-bit data</td></tr>
<tr><td>80/68 MPU 8-bit Parallel I/F</td><td>DB23-DB8 : unused
DB7-DB0 : 8-bit data</td></tr>
<tr><td colspan="2">If not used, connect these pads to VDD3 or VSS.</td></tr>
</table>

3.1.2.2 3-wire/9-bit Serial Interface

Table 39 Interface Signals in Case of 3-wire/9-bit Serial Interface.

Pad signal	Description
CSX	Chip select signal
SCL (WRX)	Clock signal During write mode, the data is latched on the rising edge of SCL signal.
SDA	When use bidirection(MFIX_SEL=0) for transfering instruction, SDA is Serial Data in/output pin
DB[1:0]	When use unidirection(MFIX_SEL=1) for transfering instruction, DB[1] is Serial Data outut pin, DB[0] is Serial Data input pin, Refer to the 1.7 INTERFACE PAD CONFIGURATION.

3.1.2.3 4-wire/8-bit Serial Interface

Table 40 Interface Signals in Case of 4-wire/8-bit Serial Interface.

Pad signal	Description
CSX	Chip select signal
DCX	Data bus is regarded as a command when DCX is low. Data bus is regarded as a parameter when DCX is high.
SCL (WRX)	Clock signal During write mode, the data is latched on the rising edge of SCL signal.
SDA	When use bidirection(MFIX_SEL=0) for transfering instruction, SDA is Serial Data in/output pin
DB[1:0]	When use unidirection(MFIX_SEL=1) for transfering instruction, DB[1] is Serial Data outut pin, DB[0] is Serial Data input pin, Refer to the 1.7 INTERFACE PAD CONFIGURATION.

3.1.3 SEQUENCE OF MPU INTERFACE

In 80 MPU 24-bit parallel interfaces, the chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write signal, RDX is the parallel data read signal and DB[23:0] is parallel data. The MPU reads the data at the rising edge of RDX signal. The DCX is the data/command flag. When DCX='1', DB[23:0] bits are display RAM data or command parameters. When DCX='0', DB[7:0] bits are commands. The 80/68-Series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected with IM[1:0].

Table 41 The Function of 80/68-series Parallel Interface

DCX	RDX	WRX	Function
L	1	↑	Write 8-bit command
H	1	↑	Write 8-bit parameter or [80/68 MPU 24-bit Parallel I/F] Write 24-bit display data (DB23 to DB0) [80/68 MPU 18-bit Parallel I/F] Write 18-bit display data (DB17 to DB0) [80/68 MPU 16-bit Parallel I/FI] Write 16-bit display data (DB15 to DB0) [80/68 MPU 9-bit Parallel I/F] Write 9-bit display data (DB8 to DB0) [80/68 MPU 8-bit Parallel I/F] Write 8-bit display data (DB7 to DB0)
H	↑	1	[80/68 MPU 24-bit Parallel I/F] Read 24-bit display data (DB23 to DB0) [80/68 MPU 18-bit Parallel I/F] Read 18-bit display data (DB17 to DB0) [80/68 MPU 16-bit Parallel I/F] Read 16-bit display data (DB15 to DB0) [80/68 MPU 9-bit Parallel I/F] Read 9-bit display data (DB8 to DB0) [80/68 MPU 8-bit Parallel I/F] Read 8-bit display data (DB7 to DB0)
H	↑	1	Read 8-bit parameter

↑ = Rising Edge

3.1.3.1 Write Sequence of MPU Interface

The write cycle means that the host writes information (command or/and data) to the driver IC via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, and WRX) and data signals (DB[23:0]). DCX bit is a control signal, which represents the data is a command or a data. The data signals represent command if the control signal is low (=’0’) and represent data if the control signal is high (=’1’).

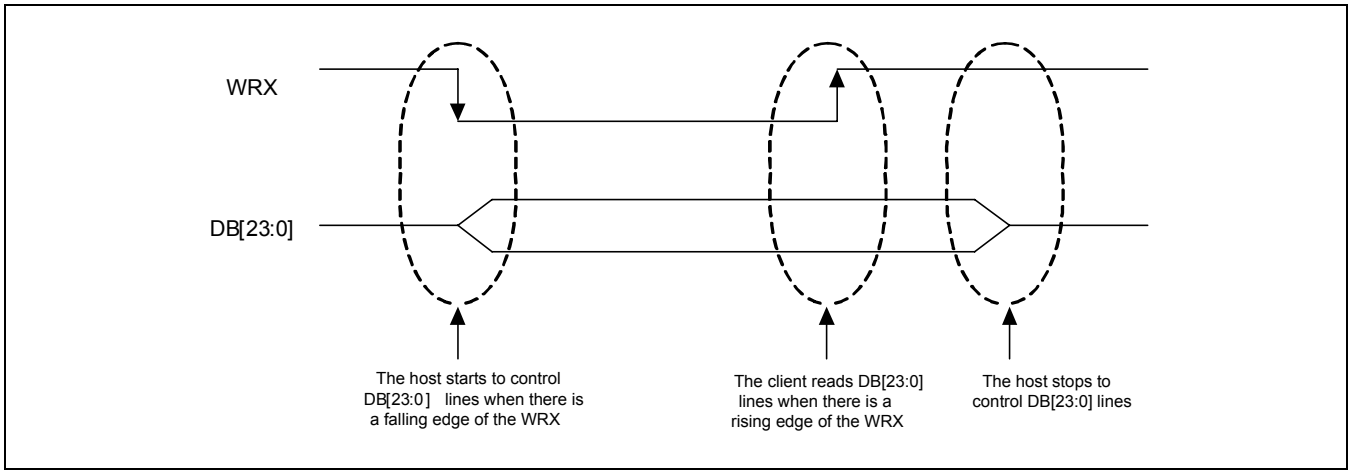


Figure 27 80-series WRX Protocol

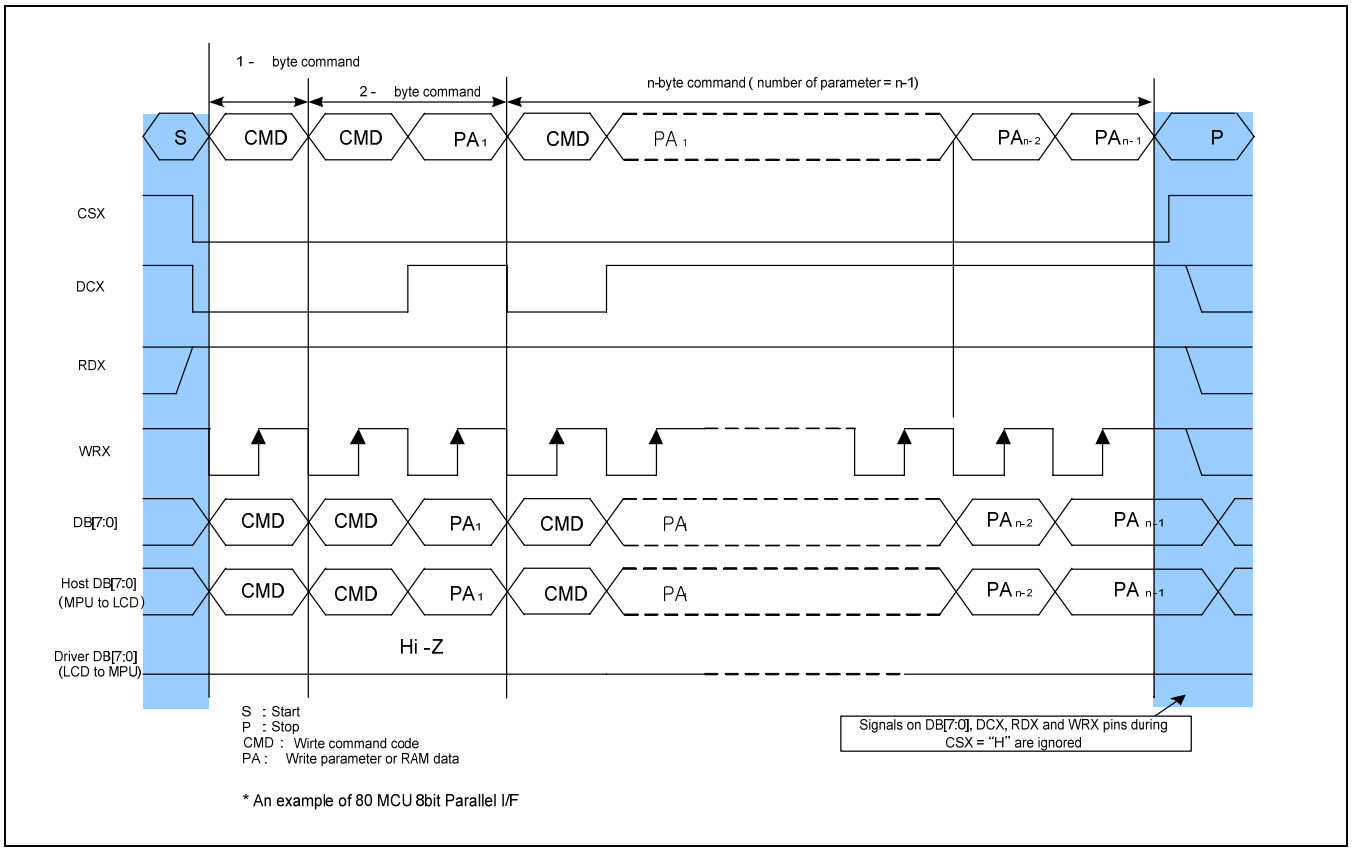


Figure 28 80-series PARALLEL Bus Protocol, Write to Register or Display RAM

3.1.3.2 READ Sequence of MPU Interface

The read cycle (RDX high-low-high sequence) means that the host reads information from driver IC via the interface. The IC sends data (DB [23:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

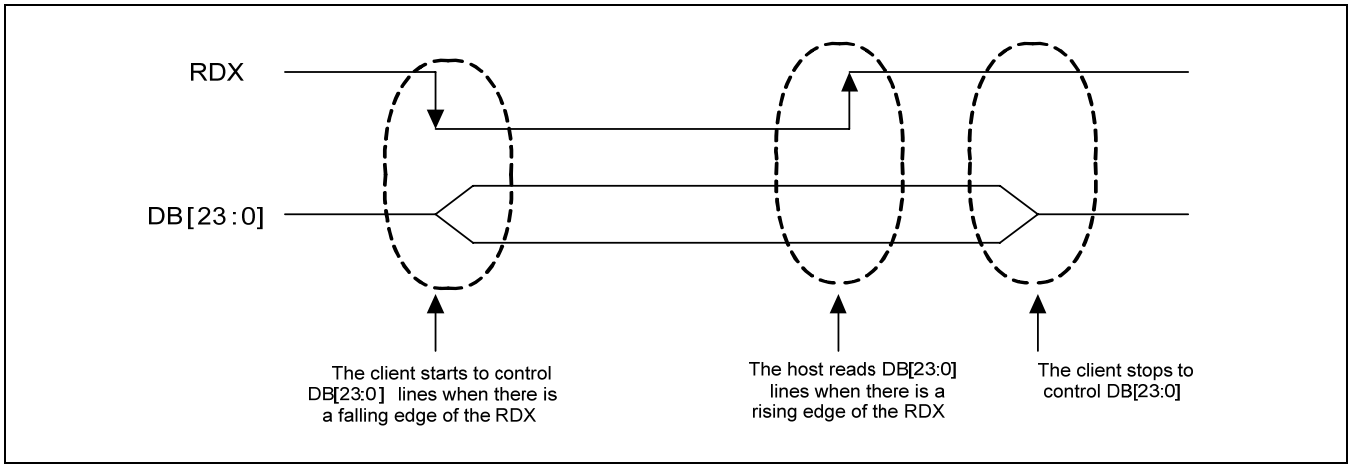


Figure 29 80-series RDX Protocol

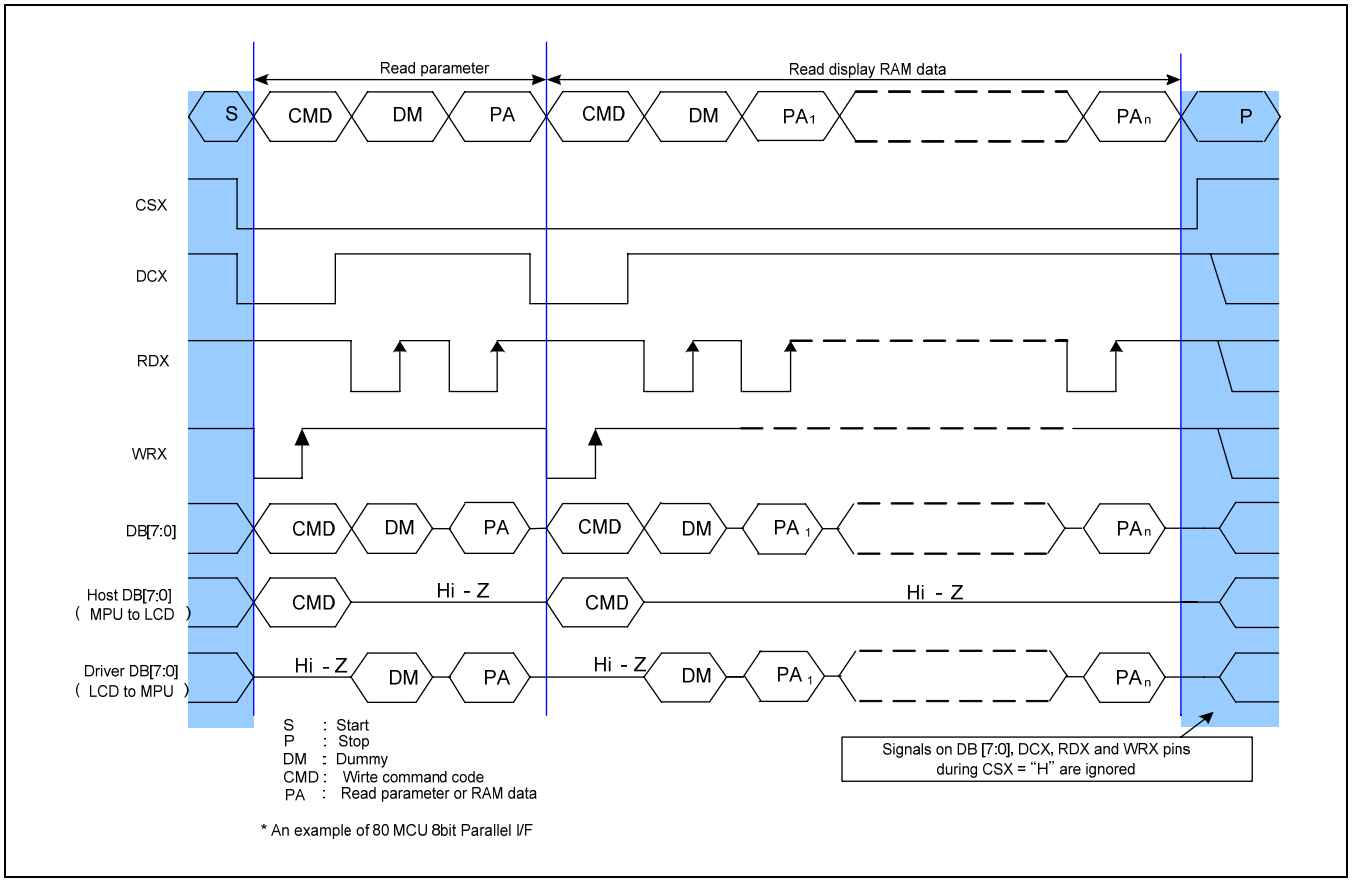


Figure 30 80-series Parallel Bus Protocol, Read From Register or Display RAM

3.1.4 SEQUENCE OF 4-WIRE/8-BIT SERIAL INTERFACE

The serial interface is 4-wire/8-bit interface for communication between the micro controller and the LCD driver chip. The 4-wire serial use: CSX (chip enable), DCX (Command/Parameter selection pad), SCL (WRX) and SDA or SDO are used for interface with MPU only, so it can be stopped when no communication is necessary.

3.1.4.1 Write Sequence of 4-wire/8-bit Serial Interface

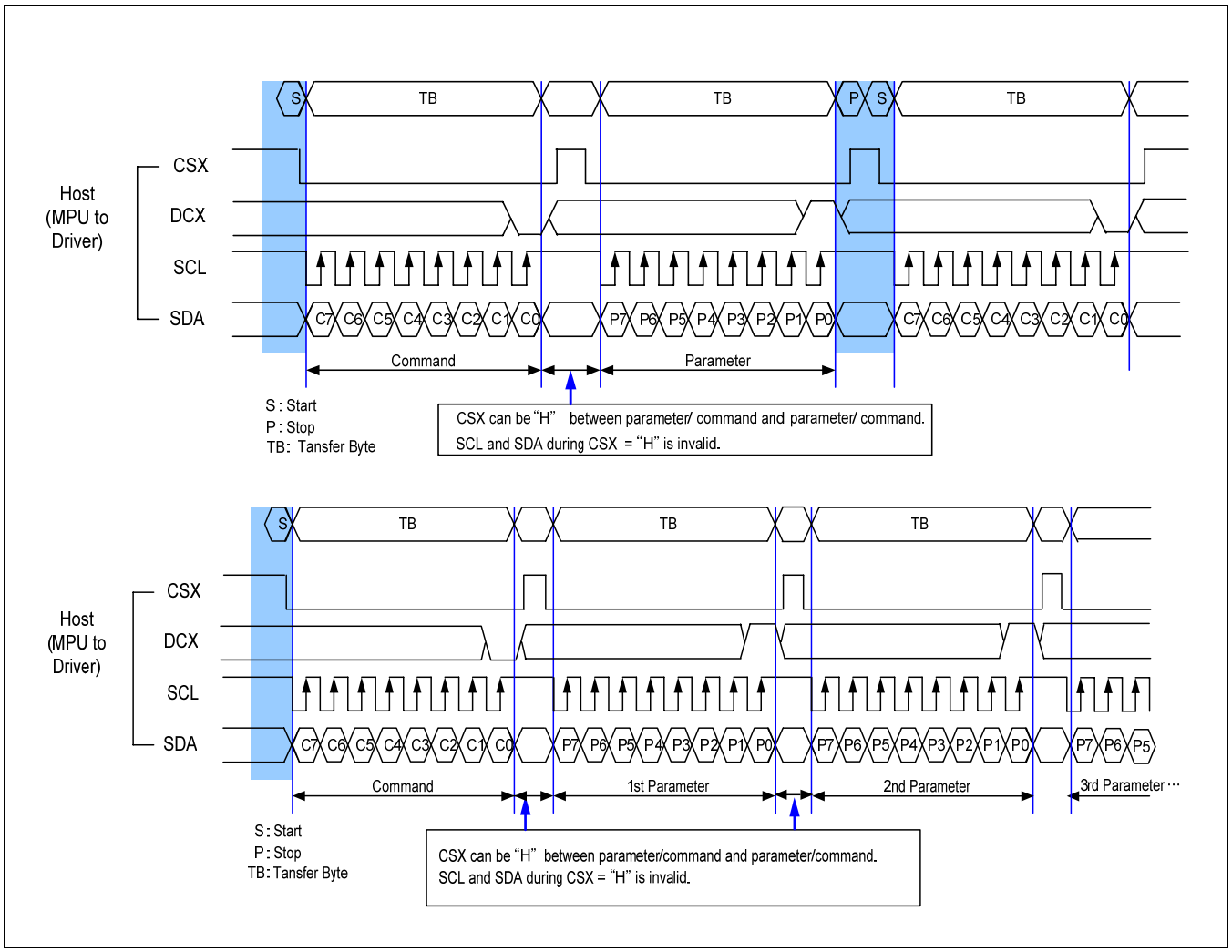


Figure 31 4-wire/8-bit Data Serial Interface Write Mode, When MFIX_SEL=0

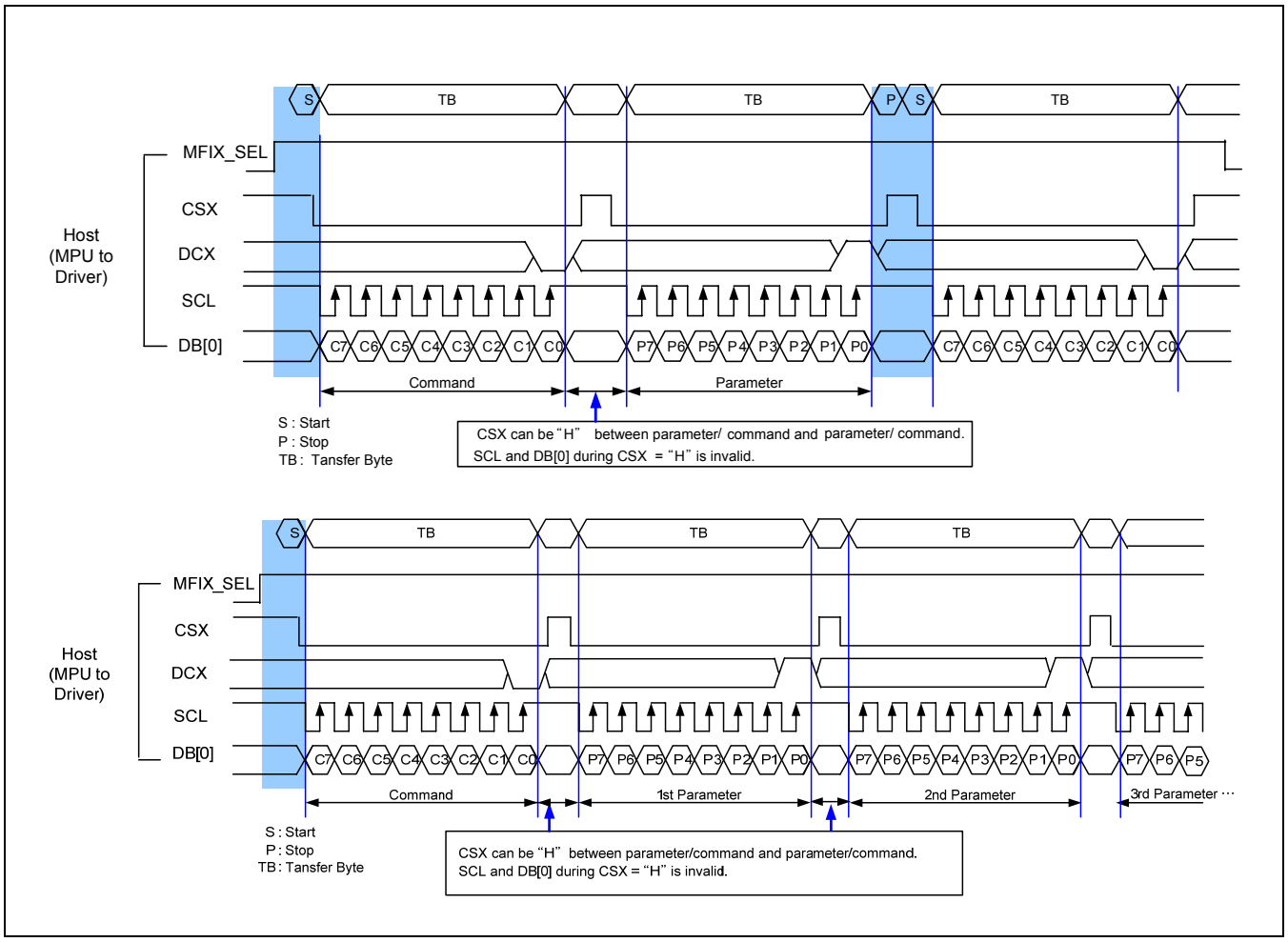


Figure 32 4-wire/8-bit Data Serial Interface Write Mode, When MFIX_SEL=1

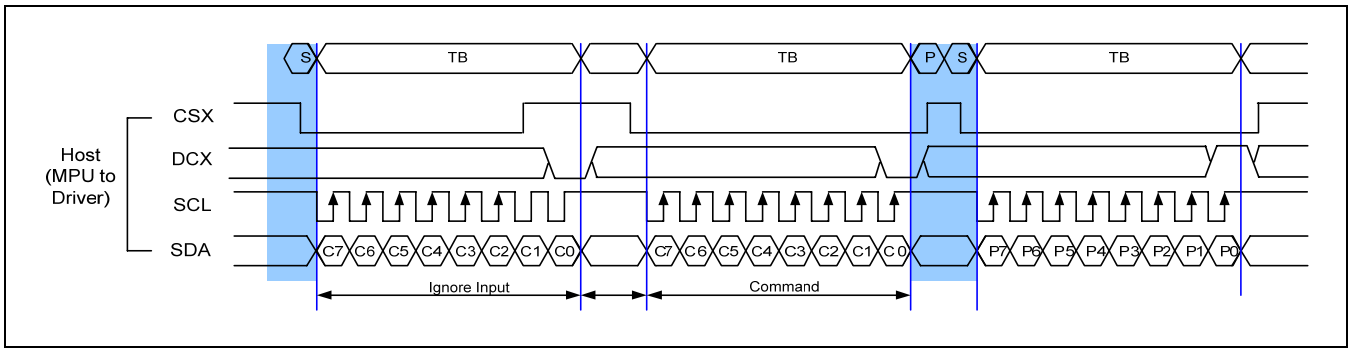


Figure 33 4-wire/8-bit Serial Interface Write Mode, When MFIX_SEL=0 (CSX="H" During Transmission)

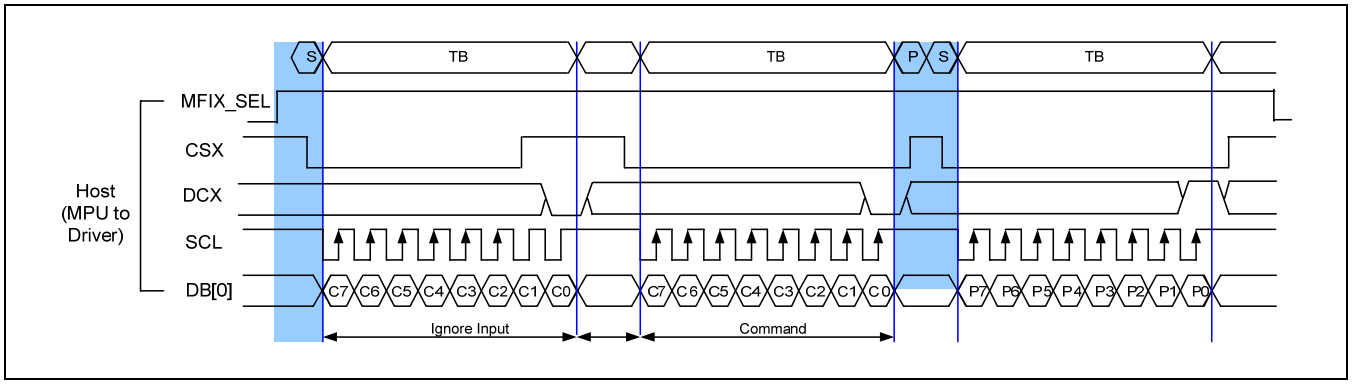


Figure 34 4-wire/8-bit Serial Interface Write Mode, When MFIX_SEL=1 (CSX="H" During Transmission)

3.1.4.2 Read Sequence of 4-wire/8-bit Serial Interface

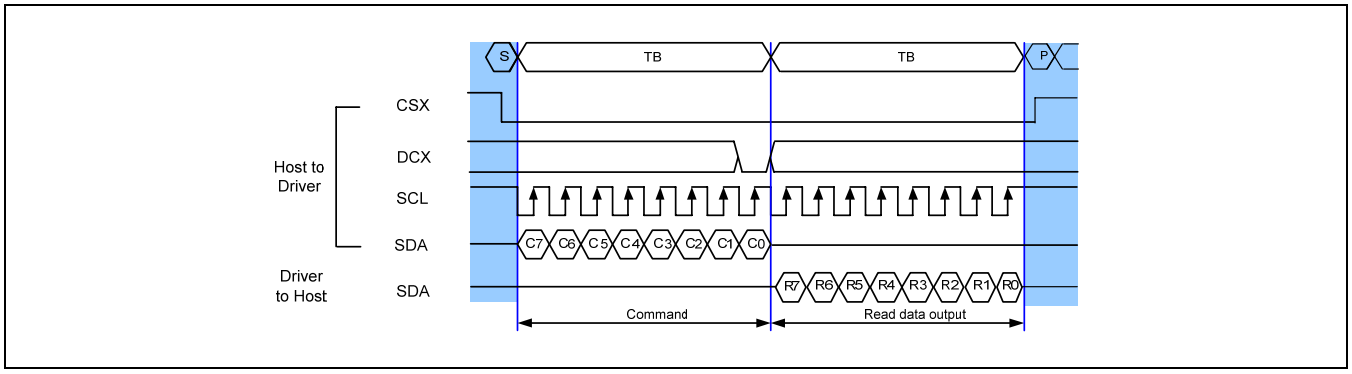


Figure 35 4-wire/8-bit Data Serial Interface Read 1-byte Mode, When MFIX_SEL=0

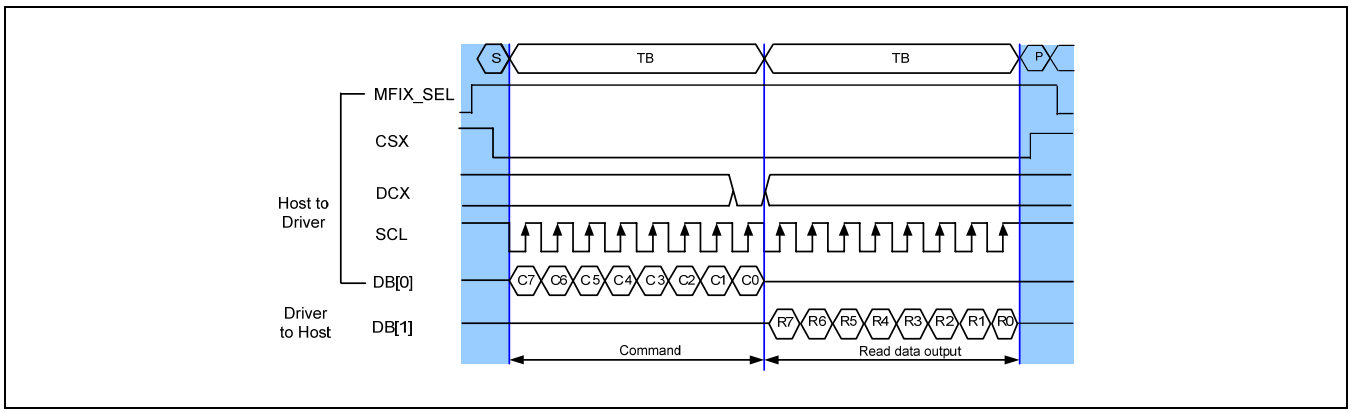


Figure 36 4-wire/8-bit Data Serial Interface Read 1-byte Mode, When MFIX_SEL=1

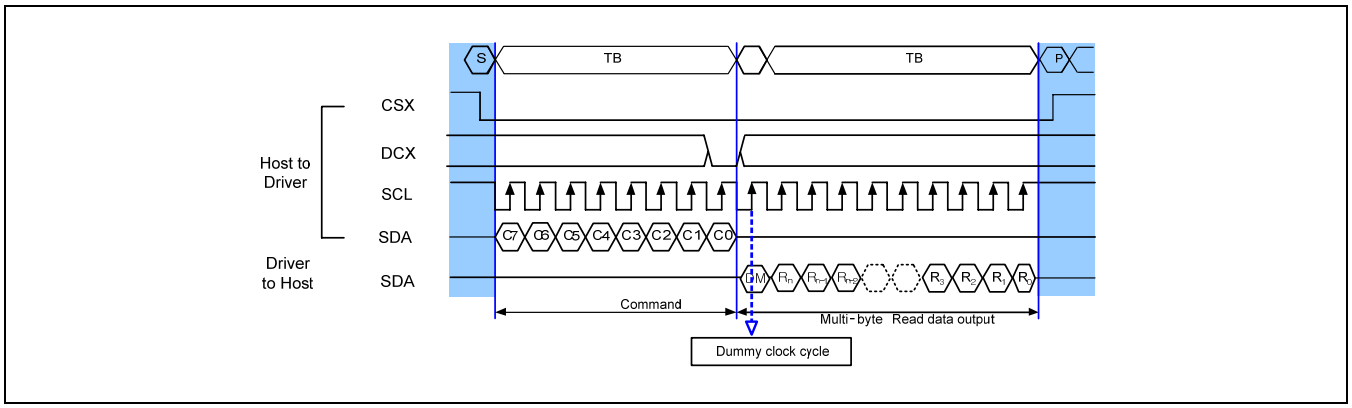


Figure 37 4-wire/8-bit Data Serial Interface Read Multi-byte Mode, When MFIX_SEL=0

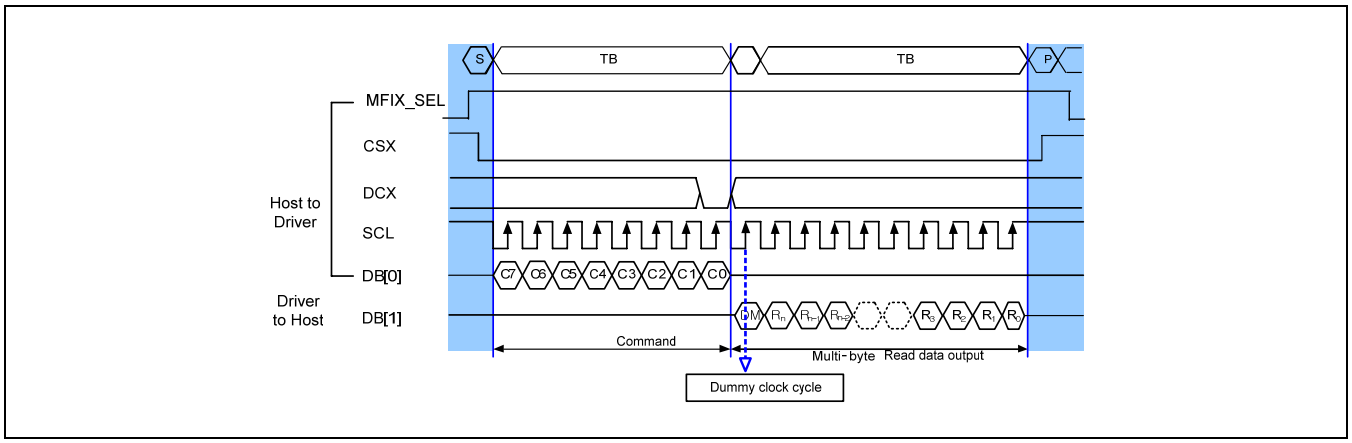


Figure 38 4-wire/8-bit Data Serial Interface Read Multi-byte Mode, When MFIX_SEL=1

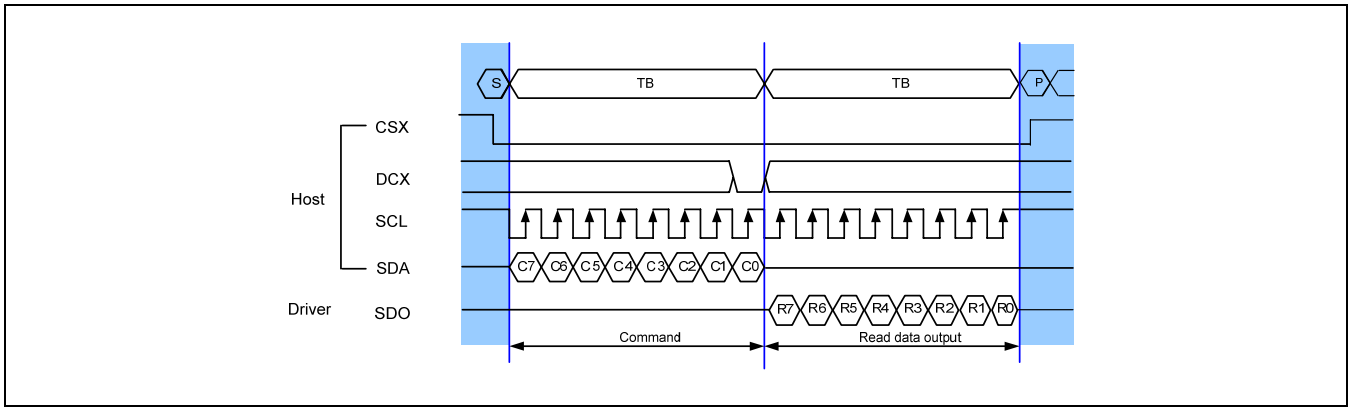


Figure 39 4-wire/8-bit Data Serial Interface Read 1-byte Mode, When MFIX_SEL=0 & SDO_EN=1

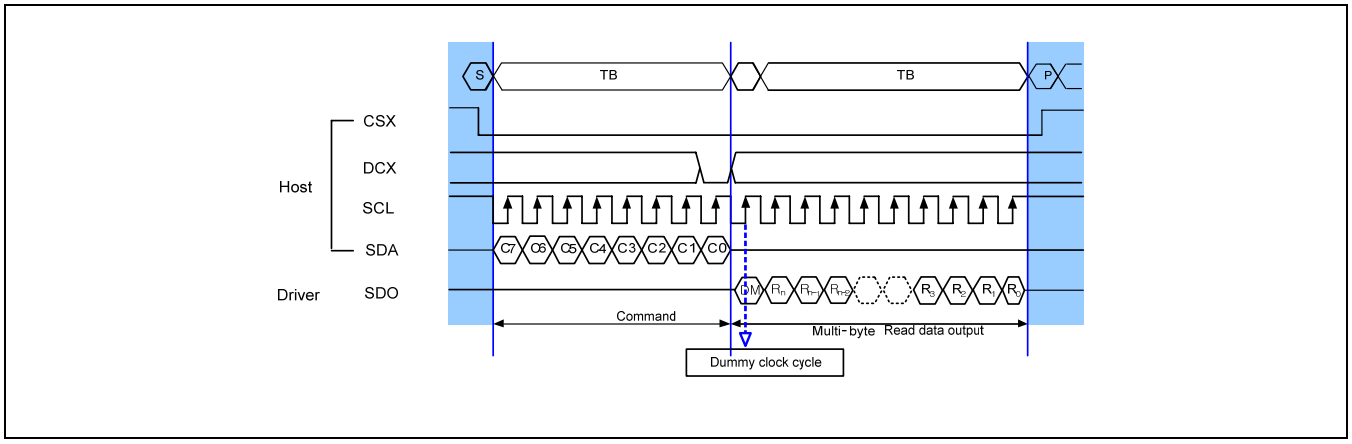


Figure 40 4-wire/8-bit Data Serial Interface Read Multi-byte Mode, When MFIX_SEL=0 & SDO_EN=1

3.1.5 SEQUENCE OF 3-WIRE/9-BIT SERIAL INTERFACE

The serial interface is 3-wire/9-bit interface for communication between the micro controller and the LCD driver chip. The 3-wire serial use: CSX, SCL (WRX) and SDA or DB[1:0] are used for interface with MPU only, so it can be stopped when no communication is necessary.

3.1.5.1 Write Sequence of 3-wire/9-bit Serial Interface

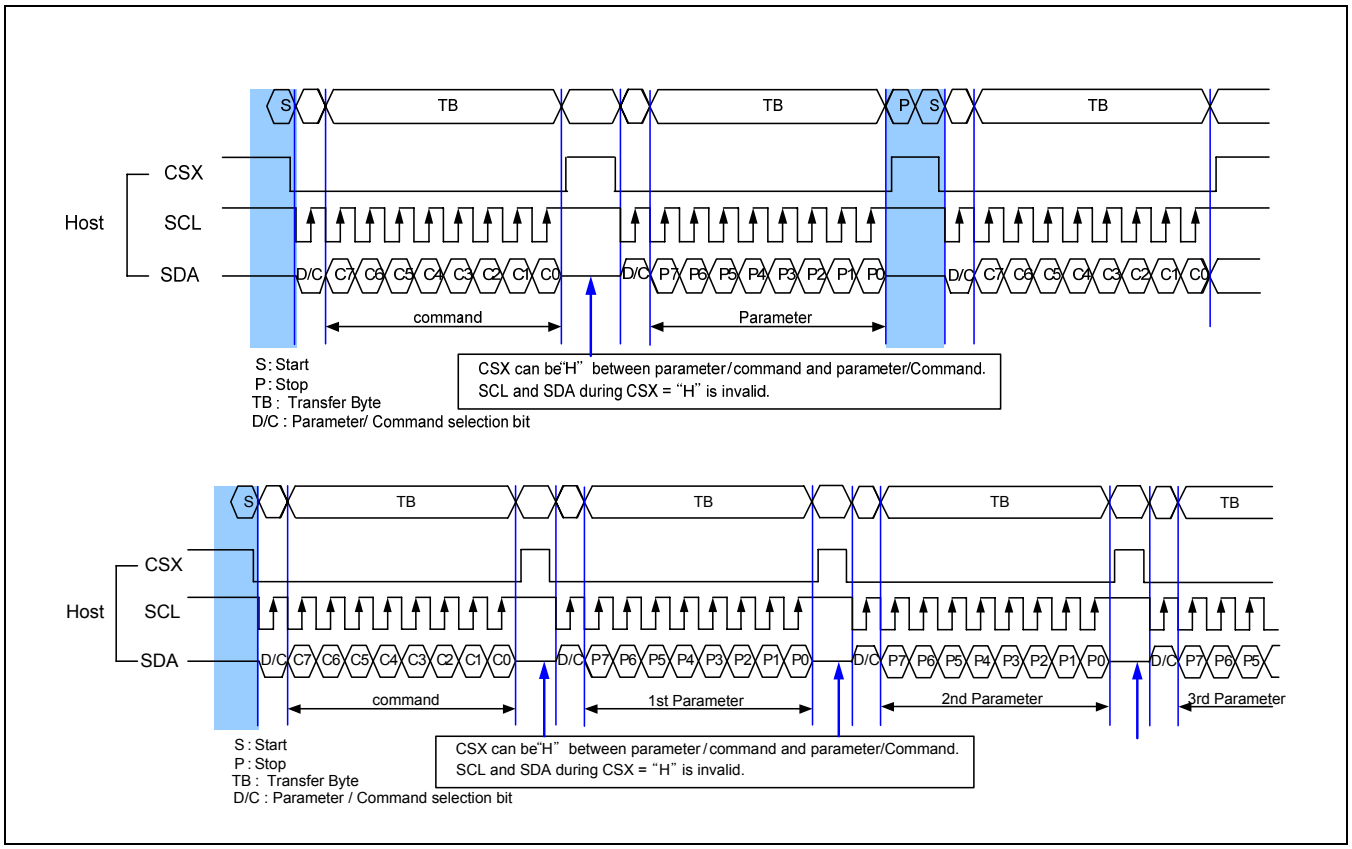


Figure 41 3-wire/9-bit Data Serial Interface Write Mode, When MFIX_SEL=0

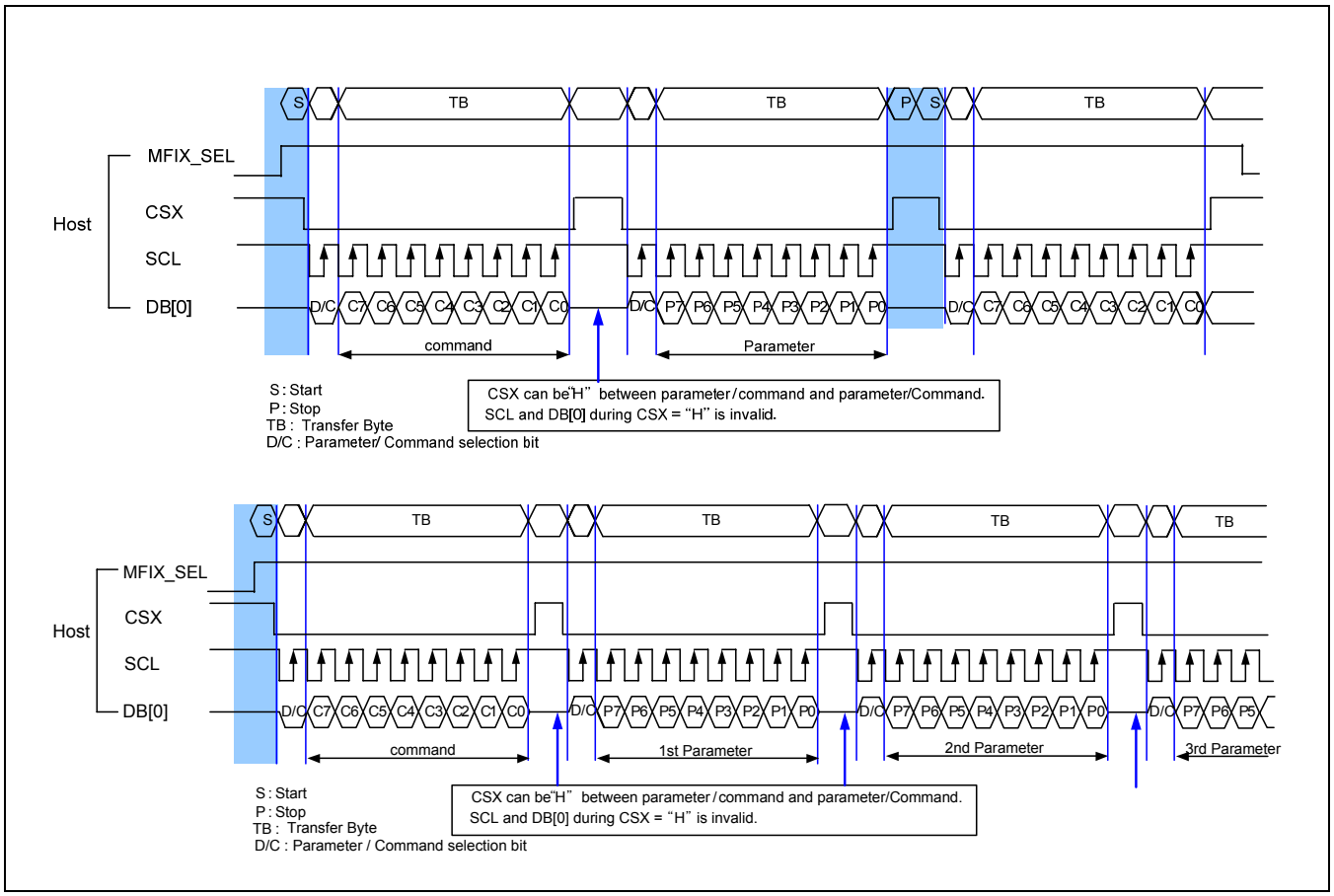


Figure 42 3-wire/9-bit Data Serial Interface Write Mode, When MFIX_SEL=1

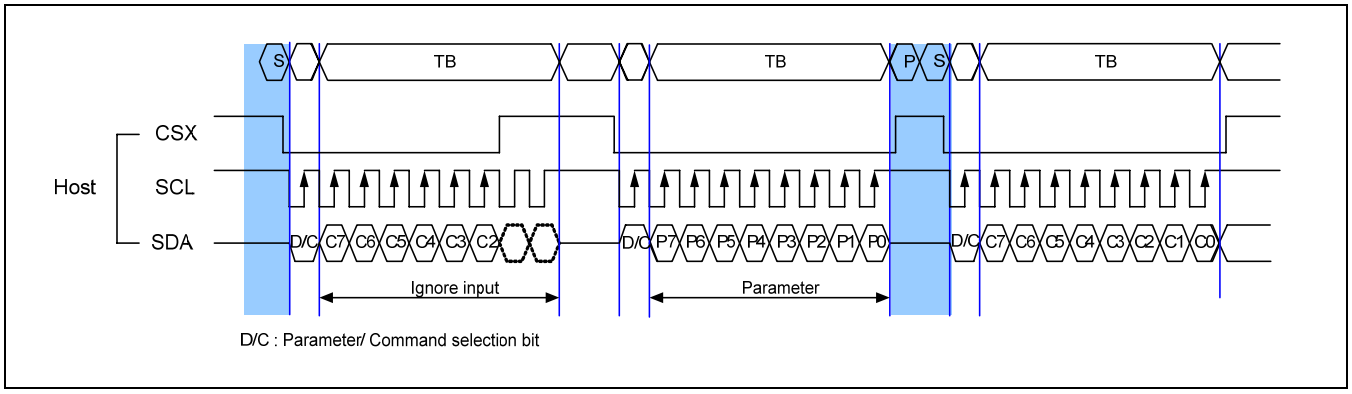


Figure 43 3-wire/9-bit Data Serial Interface Write Mode, When MFIX_SEL=0 (CSX=”H” During Transmission)

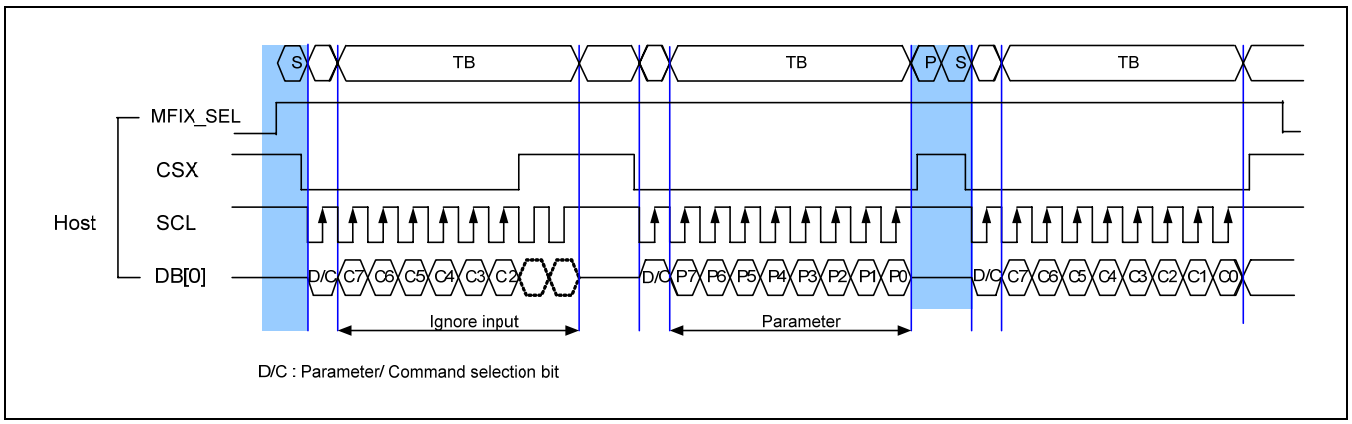


Figure 44 3-wire/9-bit Data Serial Interface Write Mode, When MFIX_SEL=1 (CSX=”H” During Transmission)

3.1.5.2 Read Sequence of 3-wire/9-bit Serial Interface

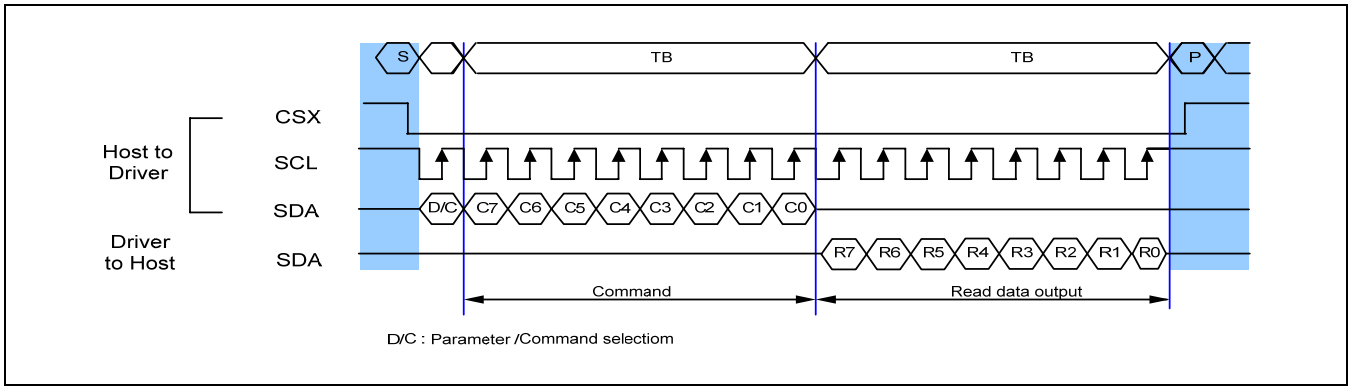


Figure 45 3-wire/9-bit Data Serial Interface Read 1-byte Mode, When MFIX_SEL=0

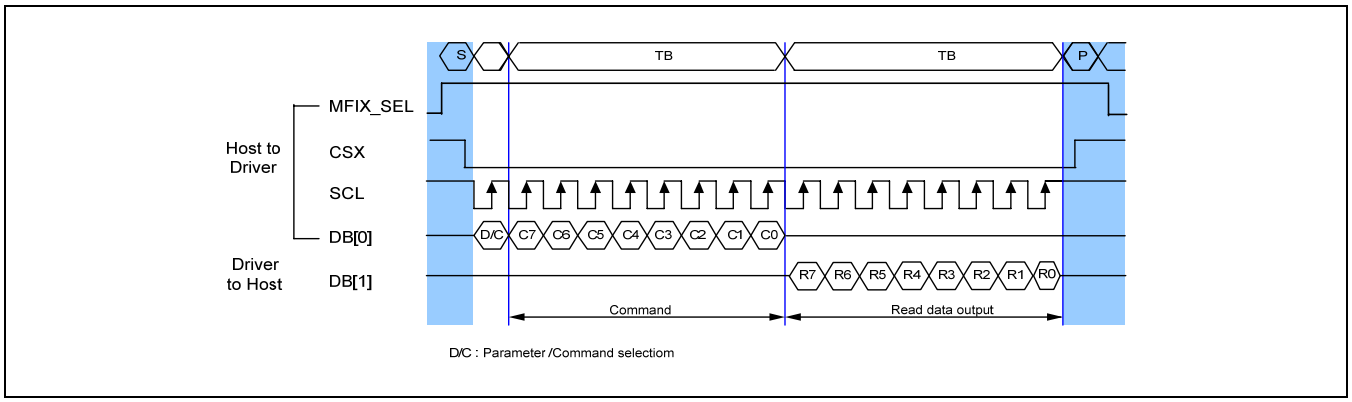


Figure 46 3-wire/9-bit Data Serial Interface Read 1-byte Mode, When MFIX_SEL=1

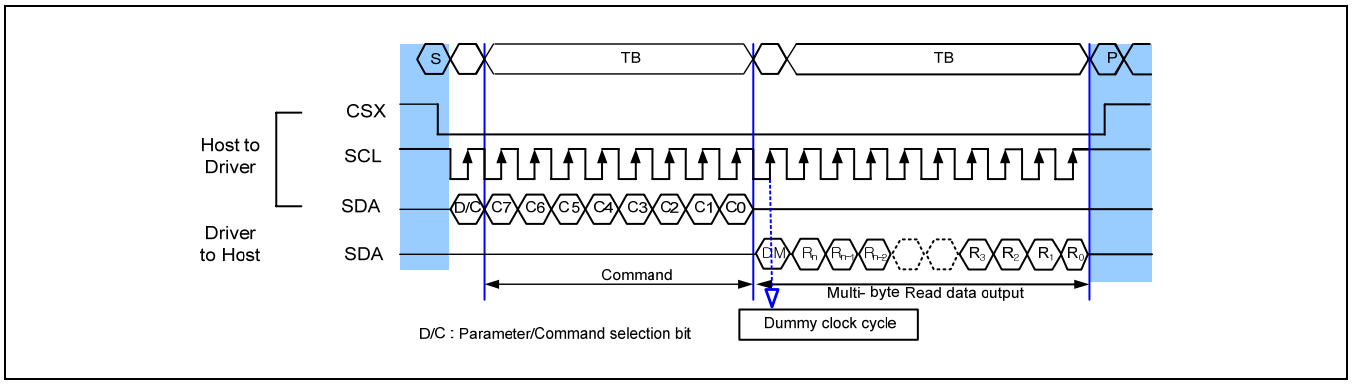


Figure 47 3-wire/9-bit Data Serial Interface Read Multi-byte Mode, When MFIX_SEL=0

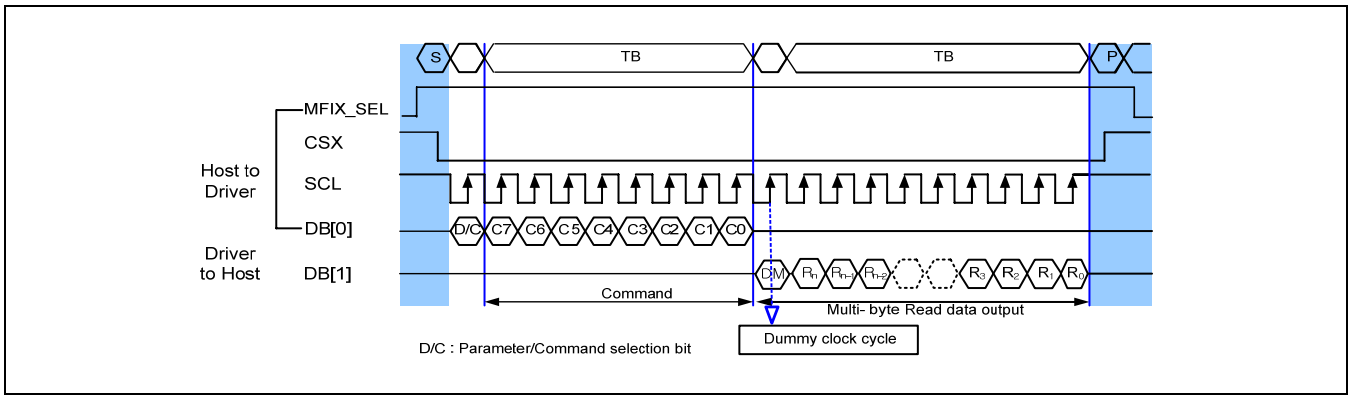


Figure 48 3-wire/9-bit Data Serial Interface Read Multi-byte Mode, When MFIX_SEL=1

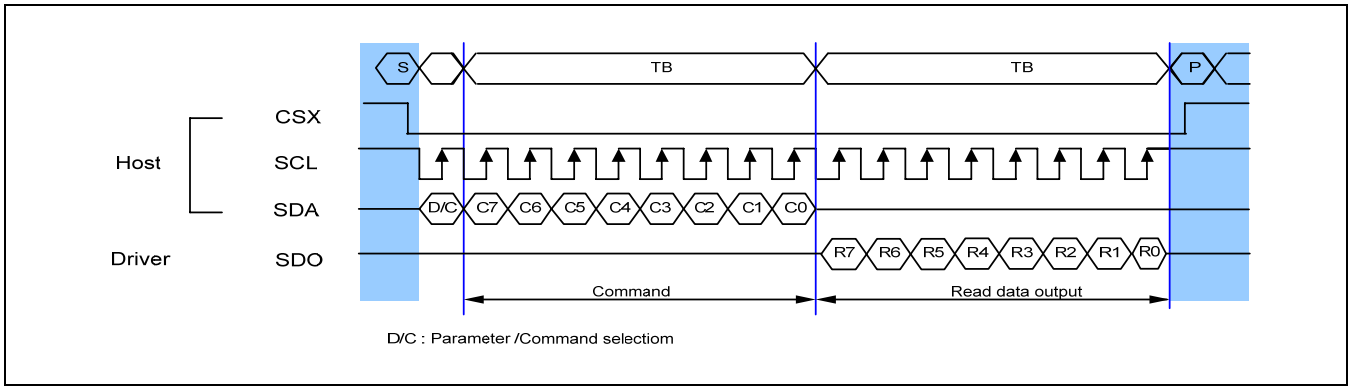


Figure 49 3-wire/9-bit Data Serial Interface Read 1-byte Mode, When MFIX_SEL=0 & SDO_EN=1

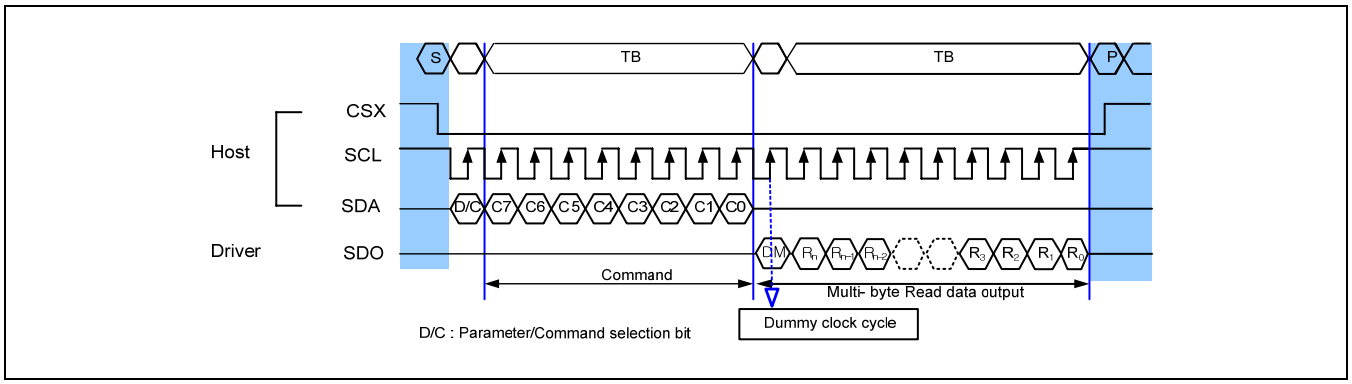


Figure 50 3-wire/9-bit Data Serial Interface Read Multi-byte Mode, When MFIX_SEL=0 & SDO_EN=1

3.1.6 DESCRIPTION OF MPU INTERFACE

The parallel interface of the S6D05A1 can communicated with the MPU using 24 bit bidirectional data bus (DB23 to DB0) to transfer command, parameter and display data.

3.1.6.1 Bidirectional Data Bus

The purpose of MPU interface in the S6D05A1 is to communicate with the MPU in a direct connection. If the driver IC is not selected as CSX = L, the data bus (data line) is placed in the high-impedance state to prevent the other driver IC's from adverse effects. When the driver IC is not selected, inputs through the MPU interface (DCX, RDX, and WRX) have no effect. The example below represents the 80/68 MPU 24bit Parallel interfaces.

Table 42 Bidirectional Data Bus Description of MPU 24bit

DCX	WRX	RDX	Description
L	↑	1	Command write Commands are input to DB7 to DB0
H	↑	1	Parameter and display data write Parameters and display data are respectively input to DB7 to DB0 and DB23 to DB0.
H	1	↑	Parameter and display data read Parameters and display data are respectively output to DB7 to DB0 and DB23 to DB0.
H	1	↑	Dummy data is output

3.1.6.2 Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then S6D05A1 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

1. Command-Pause-Command

2. Command-Pause-Parameter

3. Parameter-Pause-Command

4. Parameter-Pause-Parameter

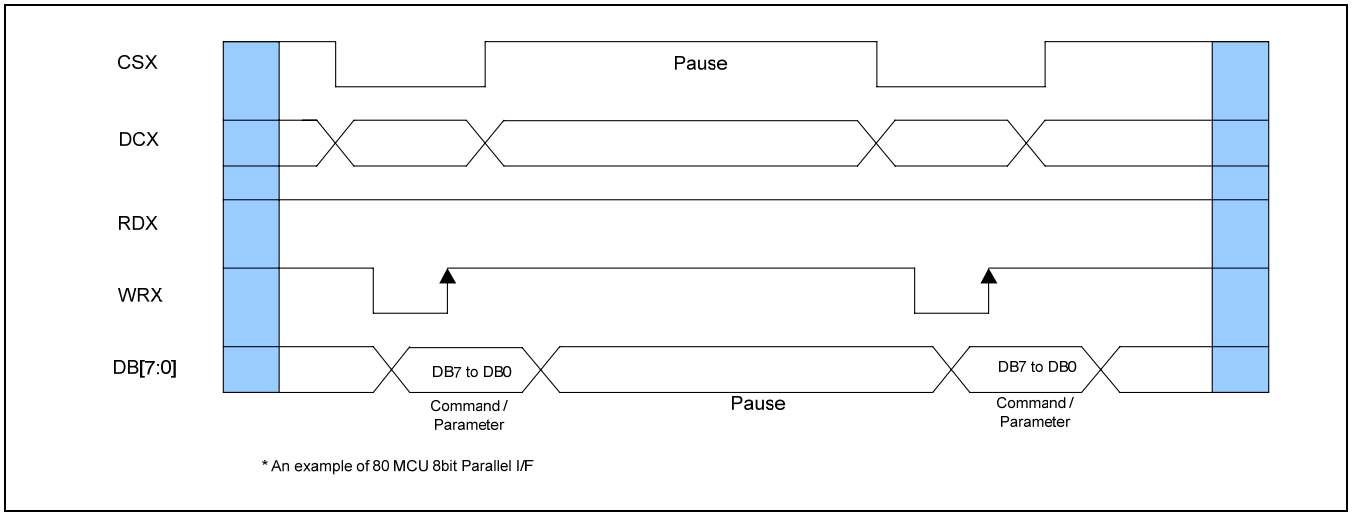


Figure 51 Parallel Interface Pause

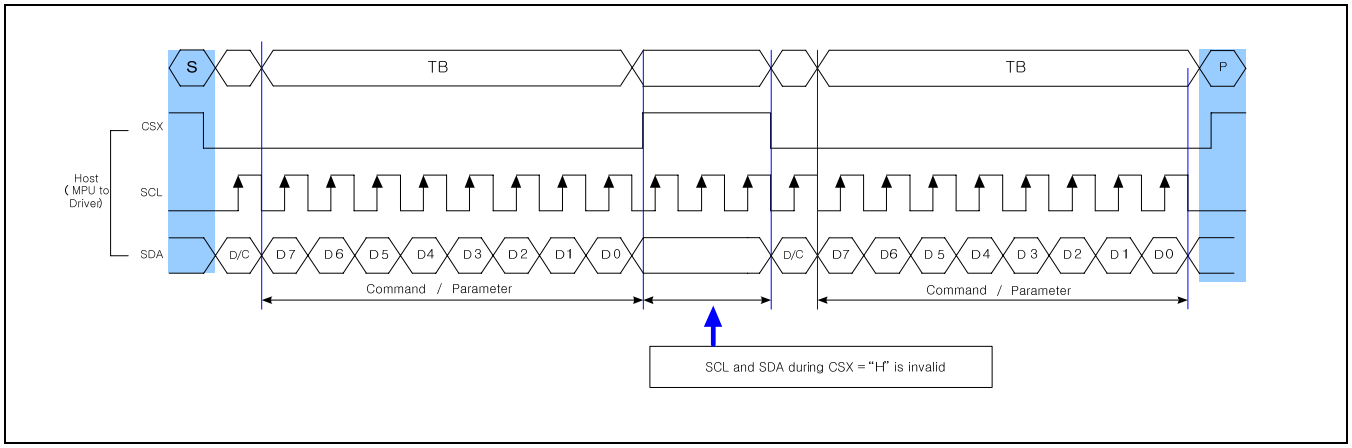


Figure 52 Serial Interface Pause

3.1.6.3 Data Transfer Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before SDA of the byte has been completed, then S6D05A1 will reject the previous bits have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX has reached the High state.

If there is a break in data transmission by CSX pulse, while transferring a Command or Multiple Parameter command Data, before SDA of the byte has been completed, then S6D05A1 will reject the previous bits and reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

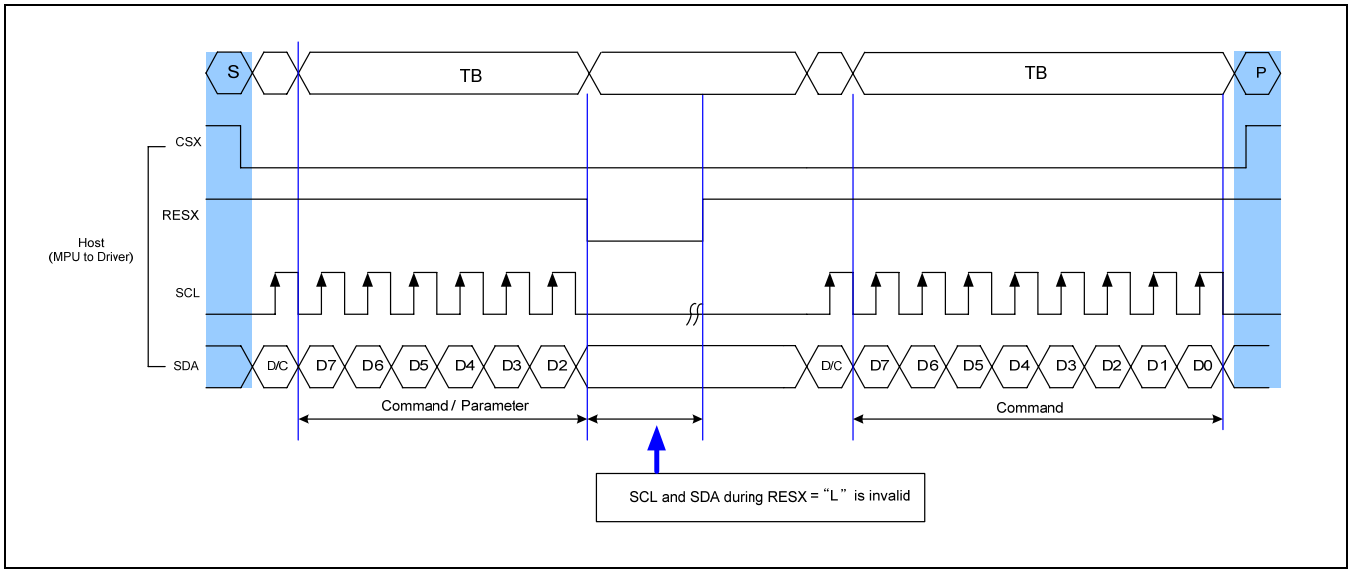


Figure 53 Serial Bus Protocol, Write Mode – Interrupted by RESX

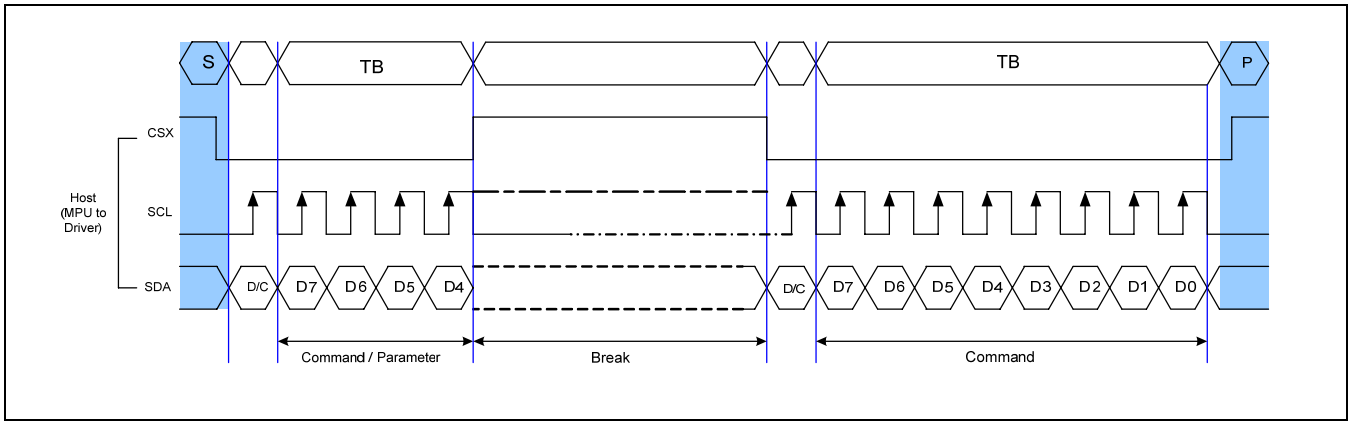


Figure 54 Serial Bus Protocol, Write Mode – Interrupted by CSX

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown in following Figure.

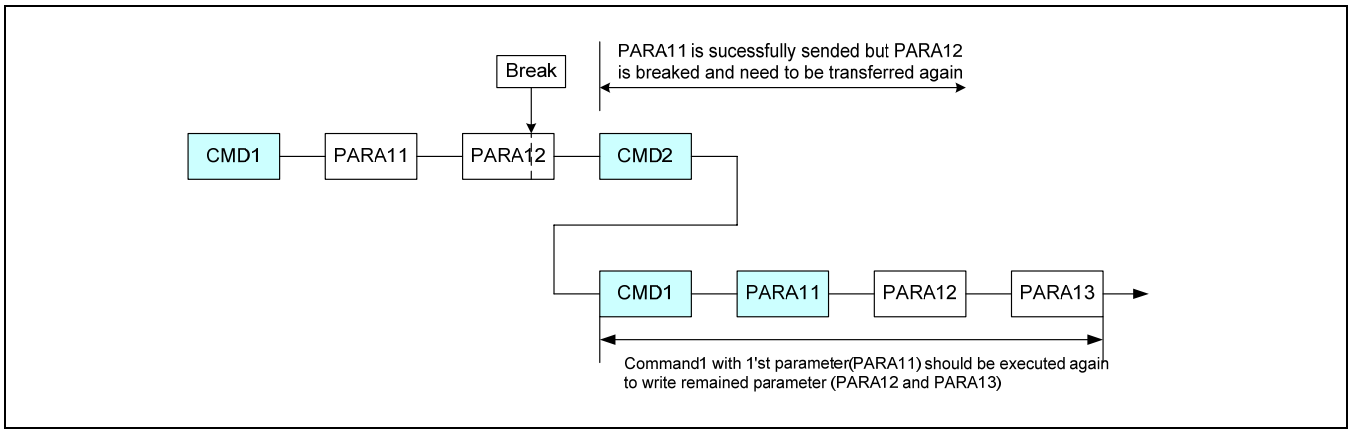


Figure 55 Write Interrupt Recovery (Serial Interface)

If 2 or more parameter command are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains in the previous value.

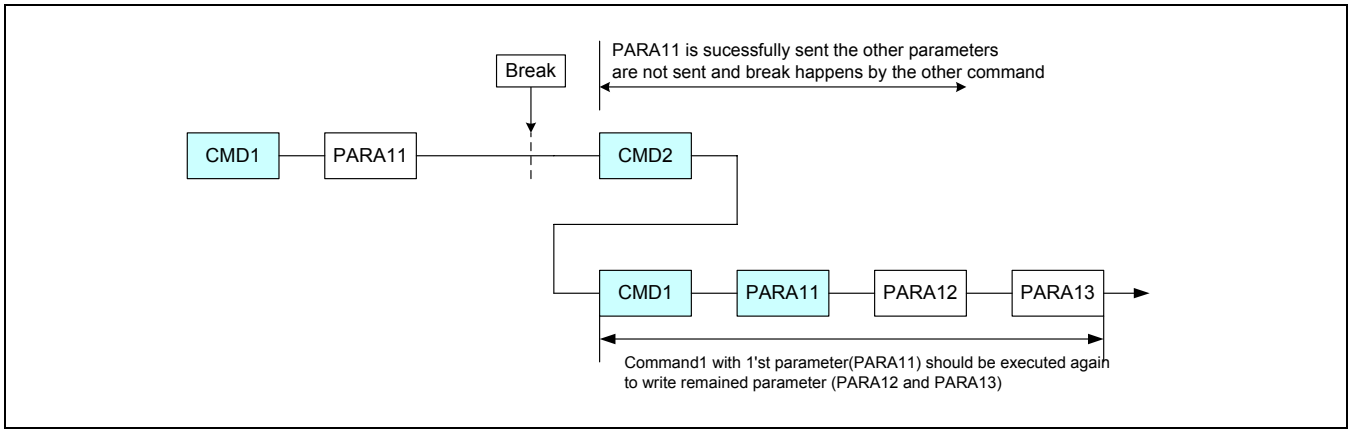


Figure 56 Write Interrupt Recovery (Both Serial and Parallel Interface)

3.1.6.4 Display Module Data Transfer Modes

The Module has 2 color modes for transferring data to the display RAM. Data can be downloaded to the Frame Memory by 2 methods.

Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

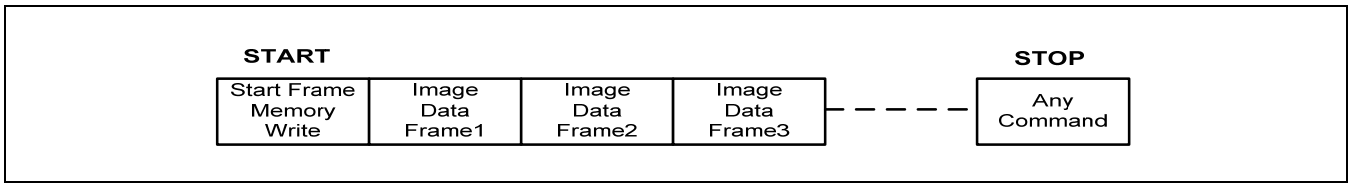


Figure 57 Image Data Writing Method 1

Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Frame Memory Write command is sent, and a new Frame is downloaded.

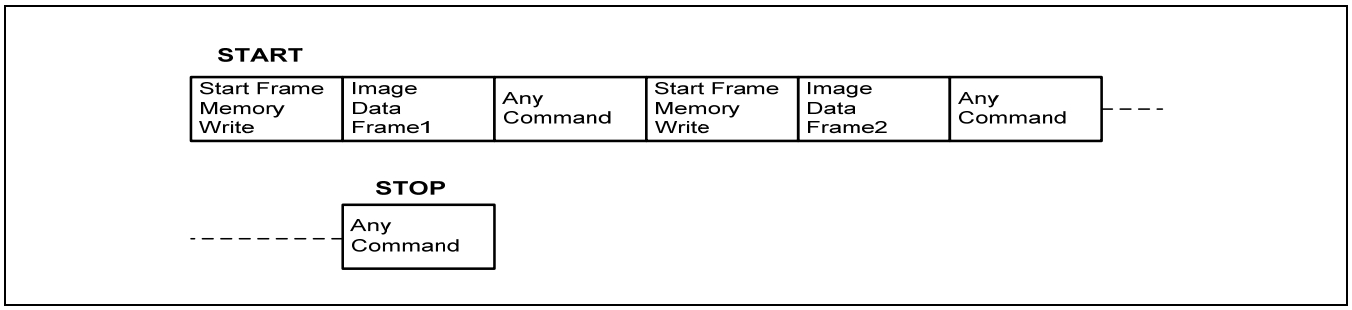


Figure 58 Image Data Writing Method 2

NOTE: These methods apply to all Data Transfer Color modes on any interfaces.
The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

3.2 DISPLAY MODULE DATA COLOR CODING

Various data formats are available in which display data can be written to the display data RAM. It is possible to choose a format suitable for the purpose of use. The data format is determined by a combination of COLMOD and MDT commands.

3.2.1 DISPLAY DATA FORMAT FOR WRITE

Table 43 Display Data Format for Write

Color mode	Interface (IM[3:0])				
	24bit	18bit	16bit	9bit	8bit
	0100	0011	0000	0001	0010
16M Color (COLMOD[2:0] = 111)	24bit 888 1/1 (MDT=00)	16bit 888 2/3 (MDT=00)	16bit 888 2/3 (MDT=00)	8bit 888 1/3 (MDT=00)	8bit 888 1/3 (MDT=00)
		16bit 888 1/2 (MDT=01)	16bit 888 1/2 (MDT=01)		
262k Color (COLMOD[2:0] = 110)	18bit 666 1/1 (MDT=00)	18bit 666 1/1 (MDT=00)	16bit 666 2/3 (MDT=00)	9bit 666 1/2 (MDT=00)	6bit 666 1/3 (MDT=00) 6bit 666 1/3 (MDT=01)
			12bit 666 1/2 (MDT=01) 16bit 666 1/2 (MDT=10) 16bit 666 1/2 (MDT=11)	6bit 666 1/3 (MDT=01)	
65k Color (COLMOD[2:0] = 101)	16bit 565 1/1 (MDT=00)	16bit 565 1/1 (MDT=00)	16bit 565 1/1 (MDT=00)	8bit 565 1/2 (MDT=00)	8bit 565 1/2 (MDT=00)

NOTE:
1. Display data expand (666 → 888 or 565 → 888) method is decided by IPM command (IPM's default condition = "100")
2. Register sets related to data format (IPM, MDT,..) are on the F7H command (Level 2)

In 65k color mode (16-bit data) data bit should be expanded to 24-bit like below. It will be used “IPM=100”

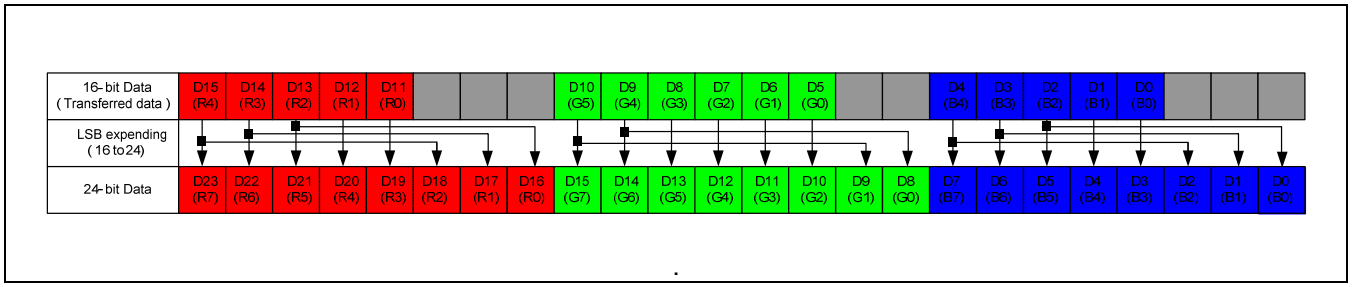


Figure 59 Data Expand Method (65K Color Mode)

In 262k color mode (18-bit data) data bit should be expanded to 24-bit like below. It will be used “IPM=100”

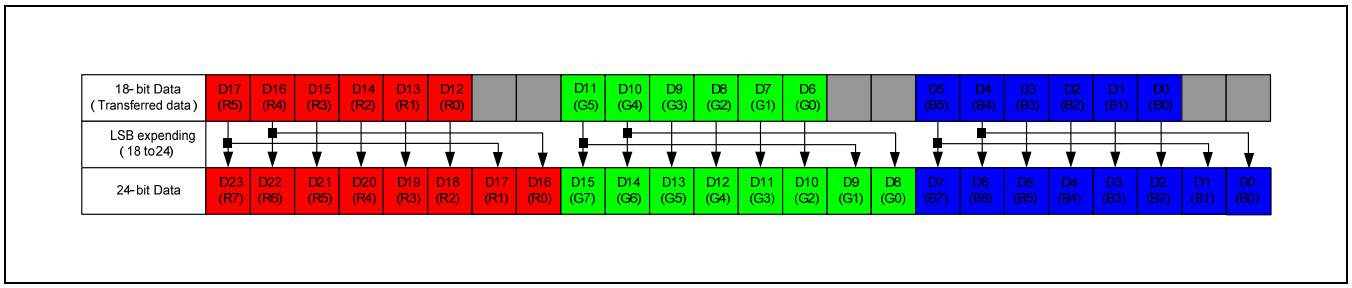


Figure 60 Data Expand Method (262K Color Mode)

3.2.2 DISPLAY DATA FORMAT FOR READ

3.2.2.1 Read Data Format

In every color mode, output display data is 24bit.

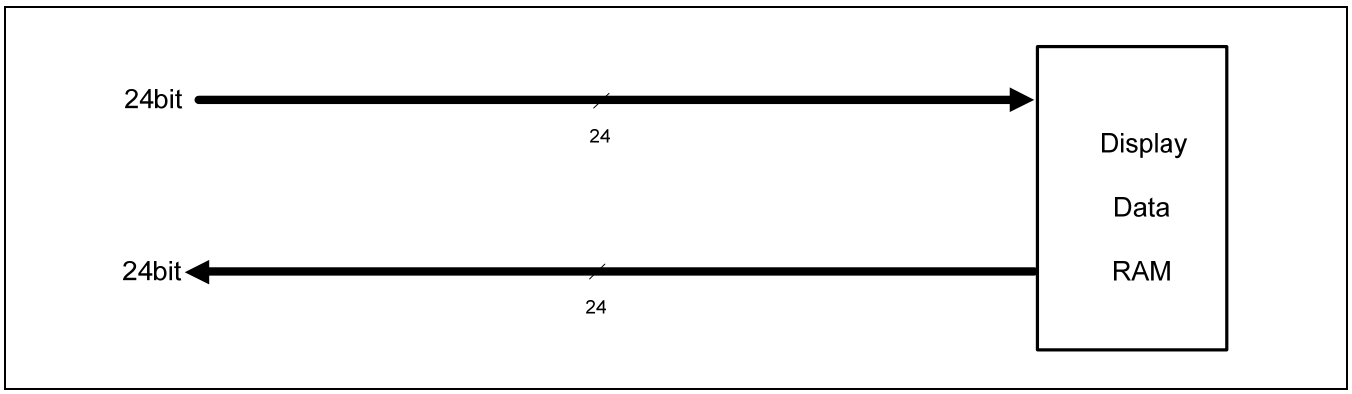


Figure 61 Case of 16M Color Mode

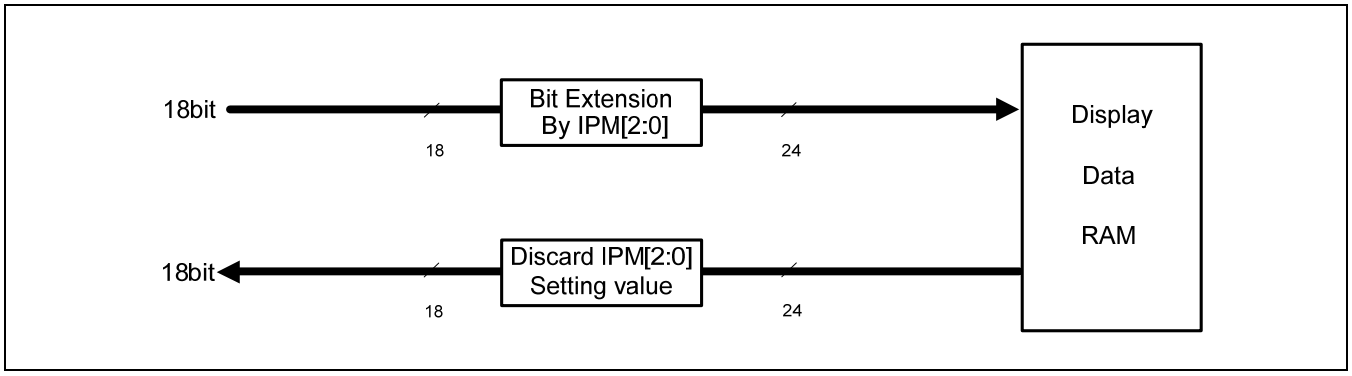


Figure 62 Case of 262K Color Mode

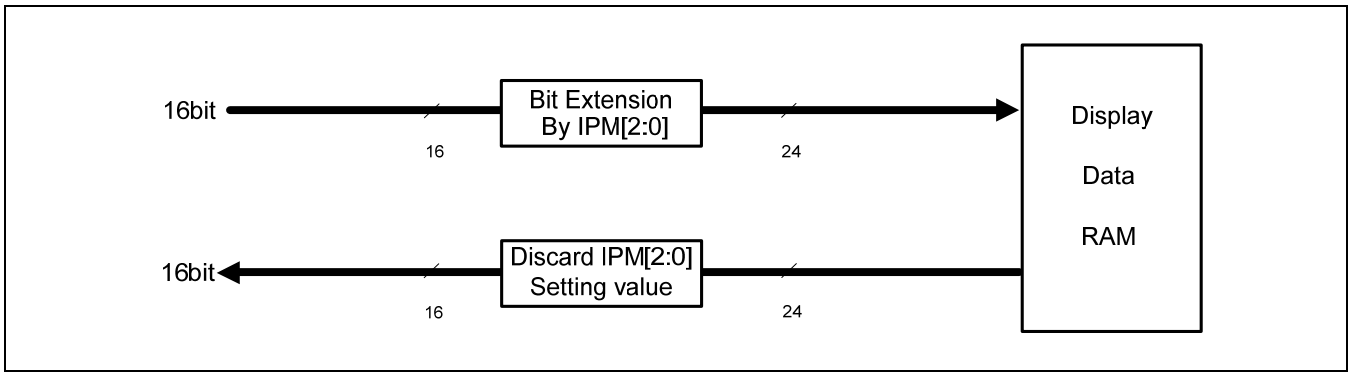


Figure 63 Case of 65K Color Mode

3.2.2.2 Display Data Read Sequence

Fort the 24bit read operation, set the COLMOD (3Ah) in 24-bits/pixel. So there are some limits on setting MDT [1:0] register in read mode.

1) 24bit Interface

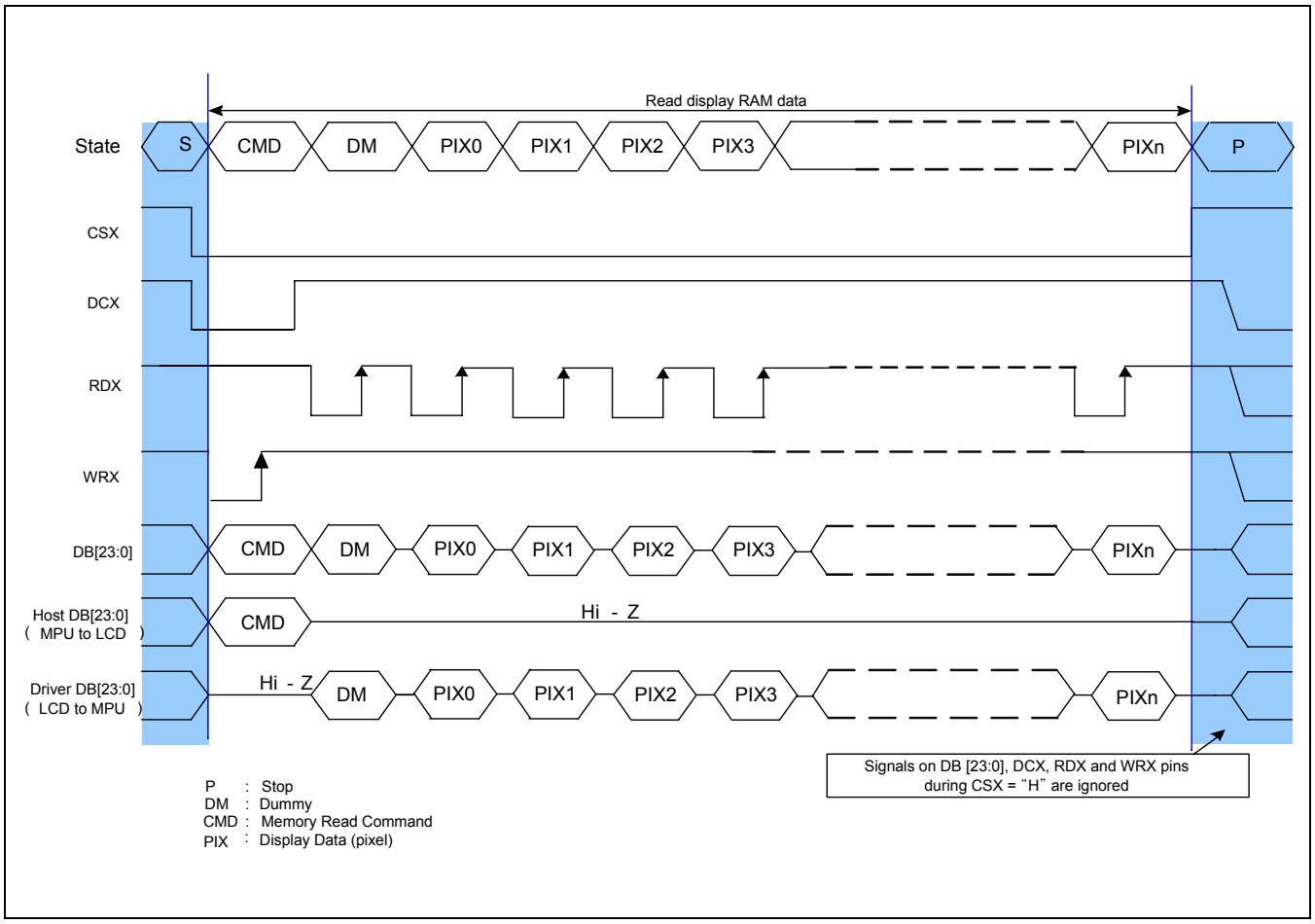


Figure 64 Display Data Read (24bit Interface Type)

2) 18bit Interface

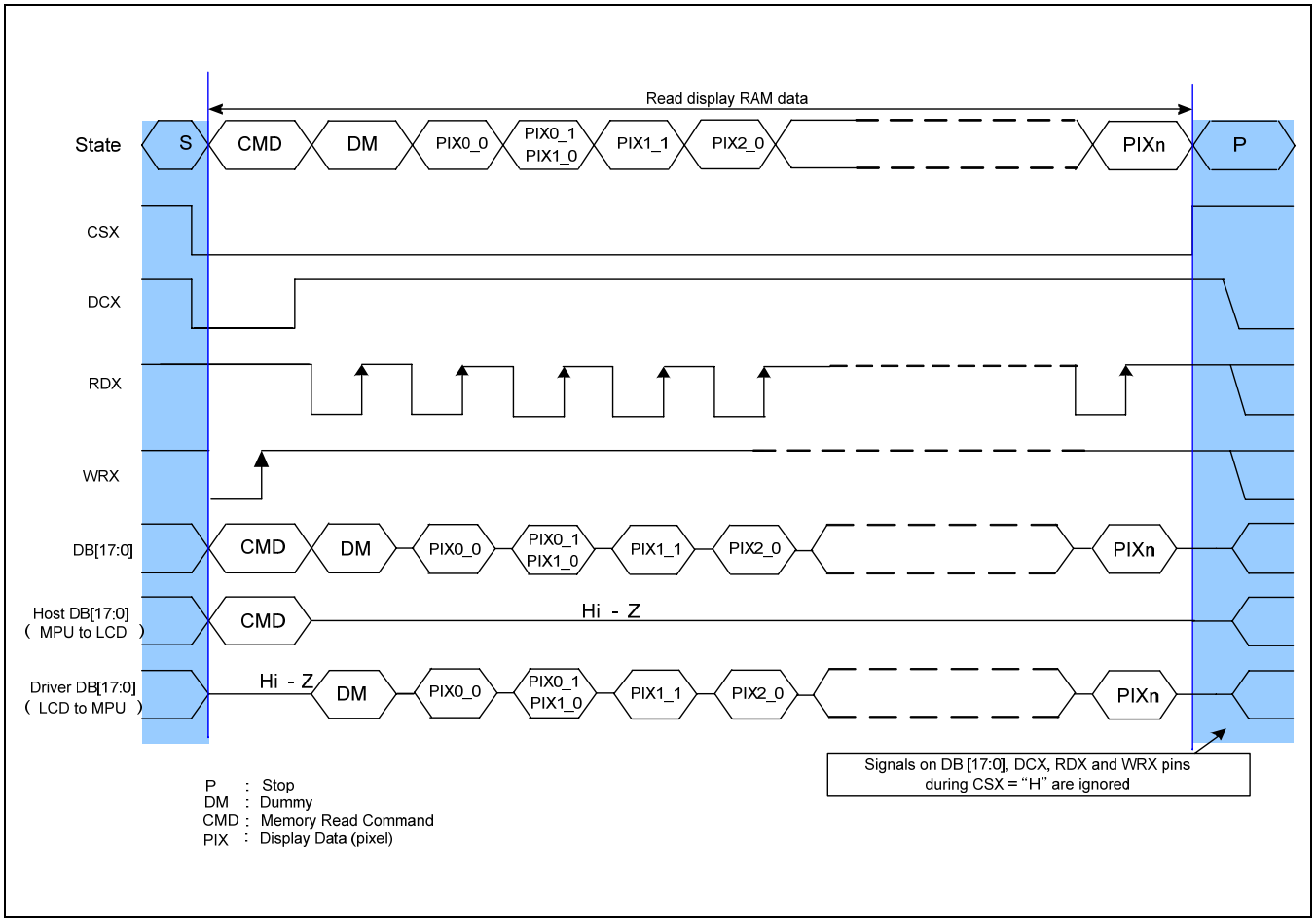
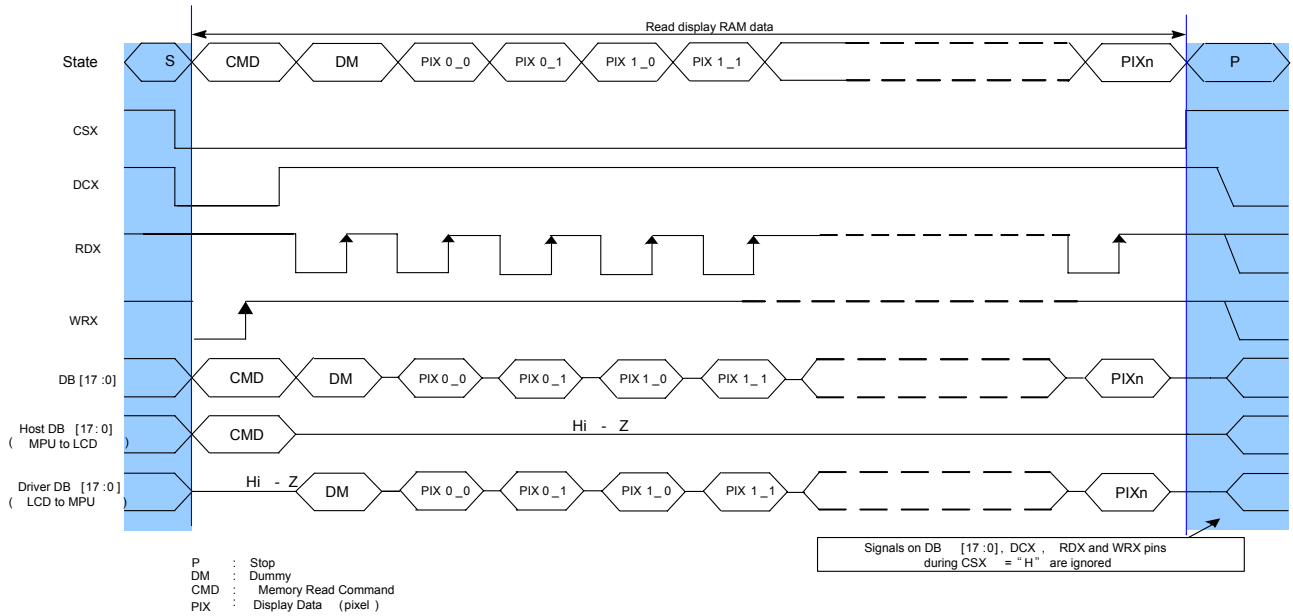


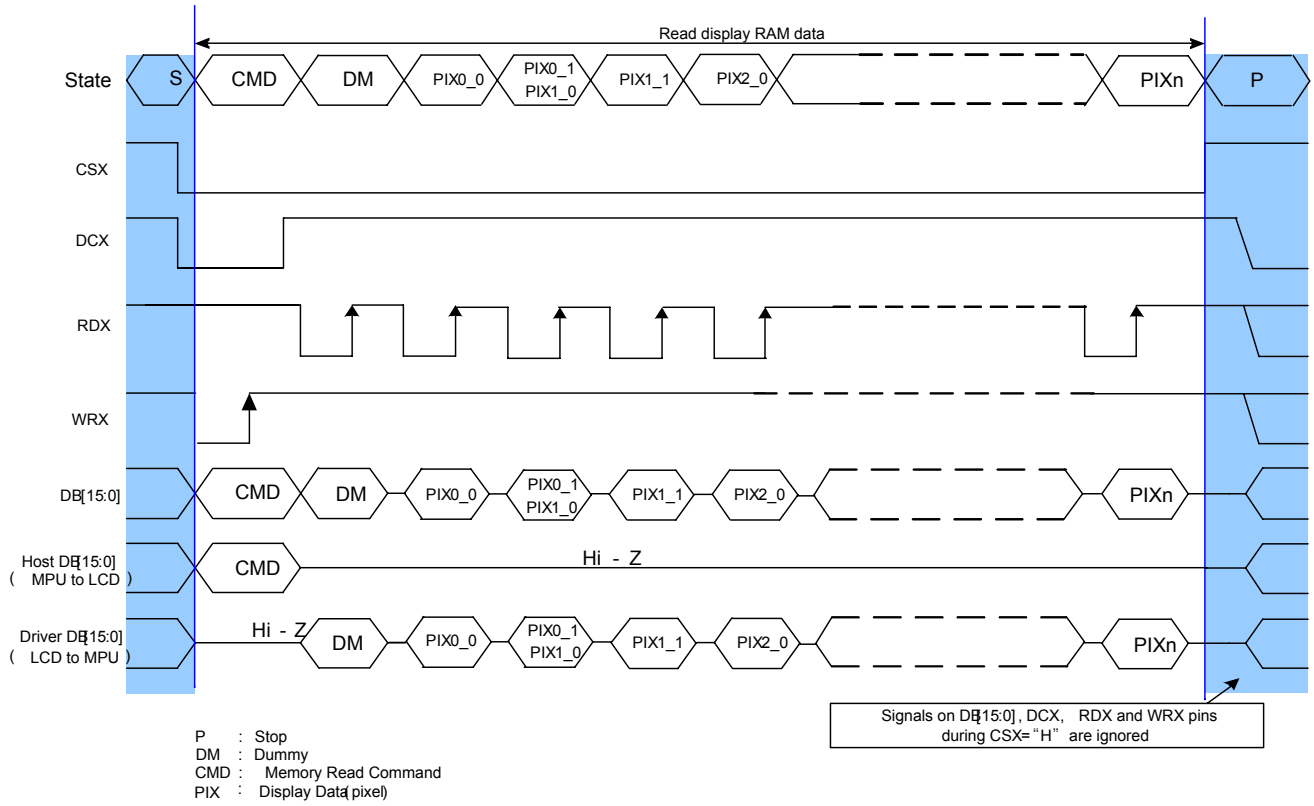
Figure 65 Display Data Read (18bit Interface: MDT=00)



NOTE: MDT[1:0]=”10" or “11” are setting disable in MPU 18bit Interface

Figure 66 Display Data Read (18bit Interface: MDT=01)

3) 16bit Interface



NOTE: If MDT[1:0] register set to "10" or "11", data read sequence operate as MDT=00.

Figure 67 Display Data Read (16bit Interface : MDT=00)

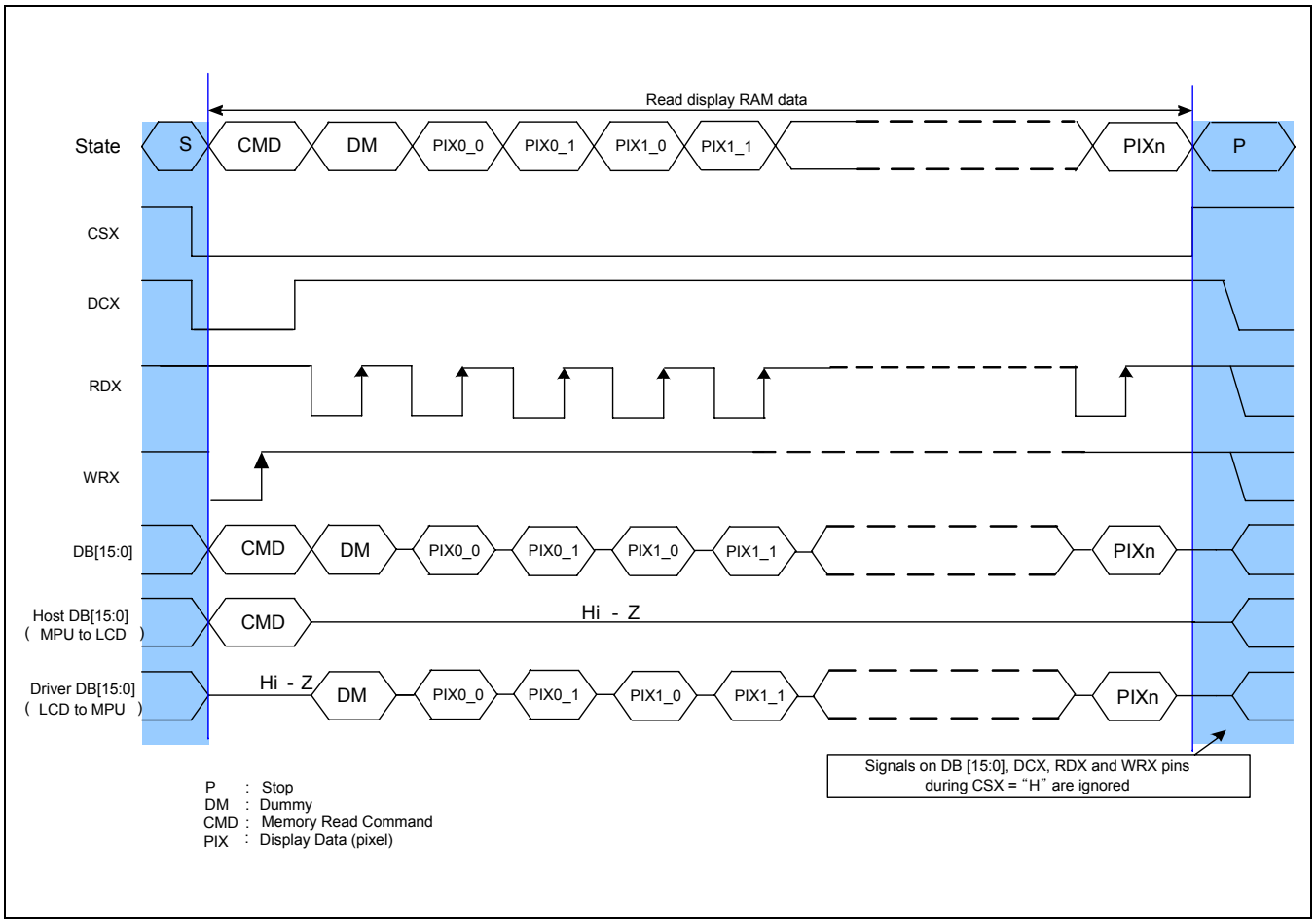
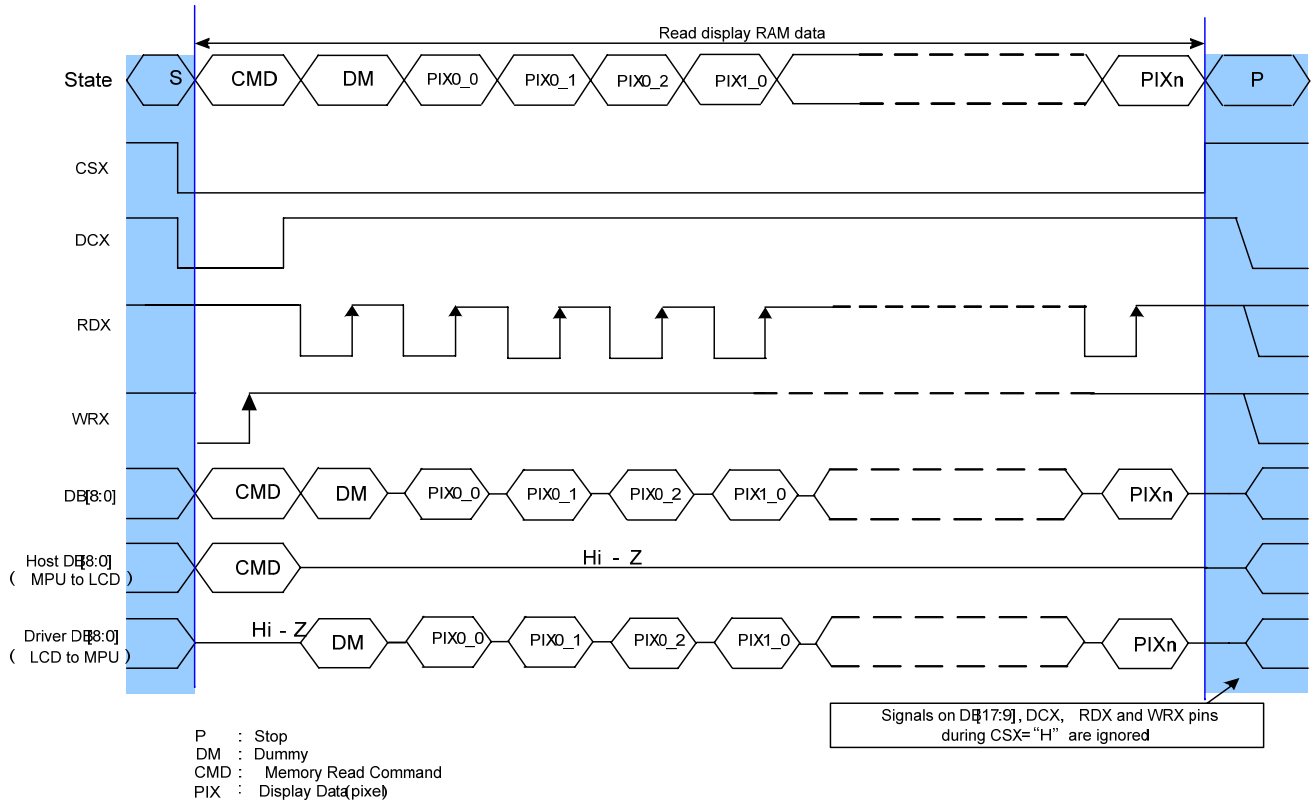


Figure 68 Display Data Read (16bit Interface : MDT=01)

4) 9bit Interface



NOTE:

1. MDT[1:0]="10" or "11" are setting disable in MPU 9bit Interface.
2. If MDT[1:0] register set to "01", data read sequence operate as MDT = 00.

Figure 69 Display Data Read (9bit Interface: MDT=00)

5) 8bit Interface

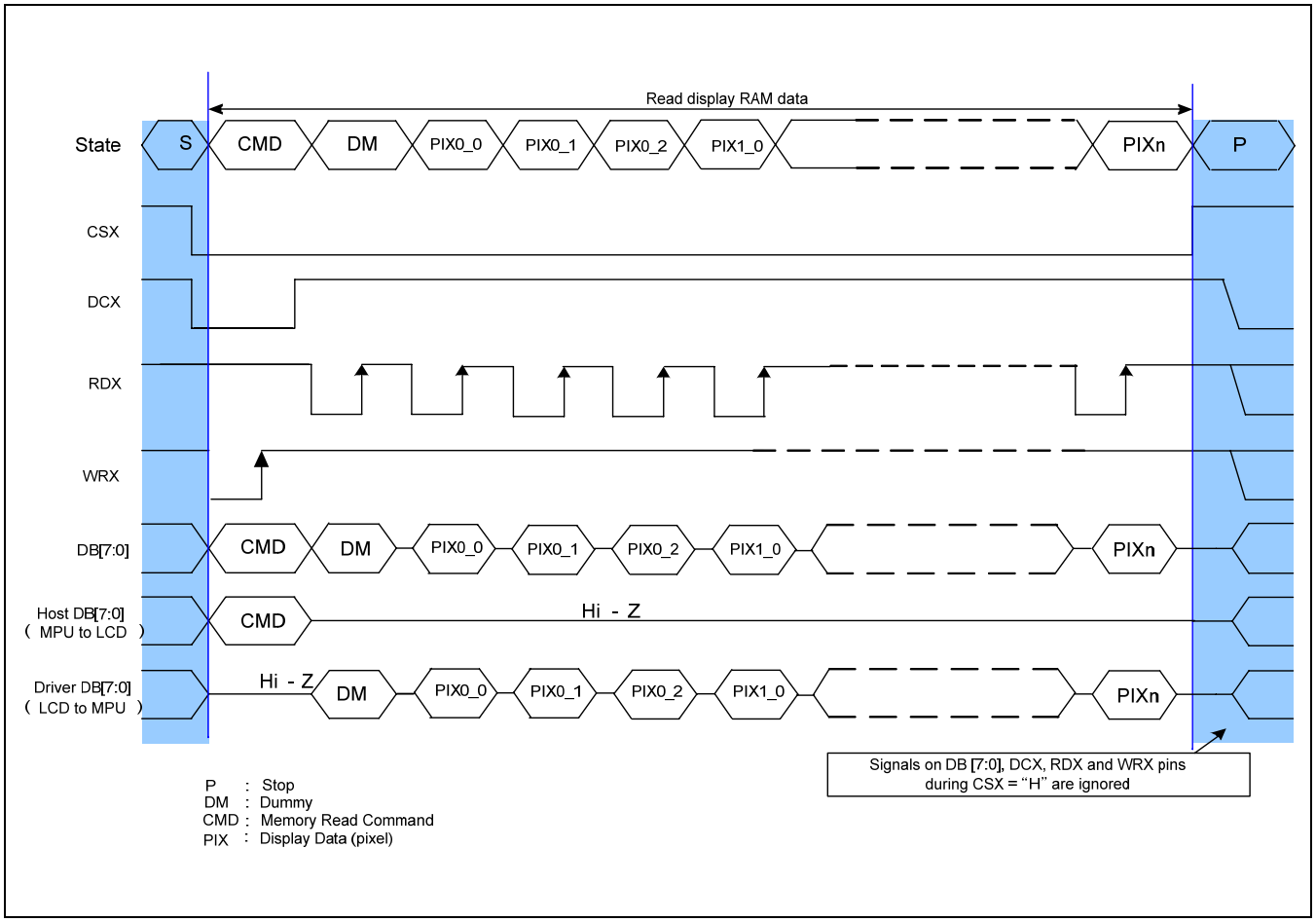


Figure 70 Display Data Read (8bit Interface type)

3.2.3 16M COLOR MODE

For the display data to be accessed in 16M color mode, it is necessary that 16M color mode be selected (B2 to B0: 111) using COLMOD command before writing/reading to or from the display data RAM. In this mode, the display data per pixel comprised of 8 bits for R, 8 bits for G and 8 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MPU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed.

This Chapter is based on the assumption that the number of 360-RGB source channels.

Table 44 24-bit Parallel Interface for 888 1/1 Formats (MDT = 00)

Count	0	1	2	…	359	360
D/CX	0	1	1	…	1	1
D23		0R7	1R7	…	358R7	359R7
D22		0R6	1R6	…	358R6	359R6
D21		0R5	1R5	…	358R5	359R5
D20		0R4	1R4	…	358R4	359R4
D19		0R3	1R3	…	358R3	359R3
D18		0R2	1R2	…	358R2	359R2
D17		0R1	1R1	…	358R1	359R1
D16		0R0	1R0	…	358R0	359R0
D15		0G7	1G7	…	358G7	359G7
D14		0G6	1G6	…	358G6	359G6
D13		0G5	1G5	…	358G5	359G5
D12		0G4	1G4	…	358G4	359G4
D11		0G3	1G3	…	358G3	359G3
D10		0G2	1G2	…	358G2	359G2
D9		0G1	1G1	…	358G1	359G1
D8		0G0	1G0	…	358G0	359G0
D7	**C7**	0B7	1B7	…	358B7	359B7
D6	**C6**	0B6	1B6	…	358B6	359B6
D5	**C5**	0B5	1B5	…	358B5	359B5
D4	**C4**	0B4	1B4	…	358B4	359B4
D3	**C3**	0B3	1B3	…	358B3	359B3
D2	**C2**	0B2	1B2	…	358B2	359B2
D1	**C1**	0B1	1B1	…	358B1	359B1
D0	**C0**	0B0	1B0	…	358B0	359B0

Table 45 18-bit Parallel Interface for 888 2/3 Formats (MDT = 00)

Count	0	1	2	3	…	538	539	540
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R7	0B7	1G7	…	358R7	358B7	359G7
D14		0R6	0B6	1G6	…	358R6	358B6	359G6
D13		0R5	0B5	1G5	…	358R5	358B5	359G5
D12		0R4	0B4	1G4	…	358R4	358B4	359G4
D11		0R3	0B3	1G3	…	358R3	358B3	359G3
D10		0R2	0B2	1G2	…	358R2	358B2	359G2
D9		0R1	0B1	1G1	…	358R1	358B1	359G1
D8		0R0	0B0	1G0	…	358R0	358B0	359G0
D7	C7	0G7	1R7	1B7	…	358G7	359R7	359B7
D6	C6	0G6	1R6	1B6	…	358G6	359R6	359B6
D5	C5	0G5	1R5	1B5	…	358G5	359R5	359B5
D4	C4	0G4	1R4	1B4	…	358G4	359R4	359B4
D3	C3	0G3	1R3	1B3	…	358G3	359R3	359B3
D2	C2	0G2	1R2	1B2	…	358G2	359R2	359B2
D1	C1	0G1	1R1	1B1	…	358G1	359R1	359B1
D0	C0	0G0	1R0	1B0	…	358G0	359R0	359B0

Table 46 18-bit Parallel Interface for 888 1/2 Formats (MDT = 01)

Count	0	1	2	3	4	…	719	720
D/CX	0	1	1	1	1	…	1	1
D17								
D16								
D15		0R7	0B7	1R7	1B7	…	359R7	359B7
D14		0R6	0B6	1R6	1B6	…	359R6	359B6
D13		0R5	0B5	1R5	1B5	…	359R5	359B5
D12		0R4	0B4	1R4	1B4	…	359R4	359B4
D11		0R3	0B3	1R3	1B3	…	359R3	359B3
D10		0R2	0B2	1R2	1B2	…	359R2	359B2
D9		0R1	0B1	1R1	1B1	…	359R1	359B1
D8		0R0	0B0	1R0	1B0	…	359R0	359B0
D7	C7	0G7		1G7		…	359G7	
D6	C6	0G6		1G6		…	359G6	
D5	C5	0G5		1G5		…	359G5	
D4	C4	0G4		1G4		…	359G4	
D3	C3	0G3		1G3		…	359G3	
D2	C2	0G2		1G2		…	359G2	
D1	C1	0G1		1G1		…	359G1	
D0	C0	0G0		1G0		…	359G0	

Table 47 16-bit Parallel Interface for 888 2/3 Formats (MDT = 00)

Count	0	1	2	3	…	538	539	540
D/CX	0	1	1	1	…	1	1	1
D15		0R7	0B7	1G7	…	358R7	358B7	359G7
D14		0R6	0B6	1G6	…	358R6	358B6	359G6
D13		0R5	0B5	1G5	…	358R5	358B5	359G5
D12		0R4	0B4	1G4	…	358R4	358B4	359G4
D11		0R3	0B3	1G3	…	358R3	358B3	359G3
D10		0R2	0B2	1G2	…	358R2	358B2	359G2
D9		0R1	0B1	1G1	…	358R1	358B1	359G1
D8		0R0	0B0	1G0	…	358R0	358B0	359G0
D7	C7	0G7	1R7	1B7	…	358G7	359R7	359B7
D6	C6	0G6	1R6	1B6	…	358G6	359R6	359B6
D5	C5	0G5	1R5	1B5	…	358G5	359R5	359B5
D4	C4	0G4	1R4	1B4	…	358G4	359R4	359B4
D3	C3	0G3	1R3	1B3	…	358G3	359R3	359B3
D2	C2	0G2	1R2	1B2	…	358G2	359R2	359B2
D1	C1	0G1	1R1	1B1	…	358G1	359R1	359B1
D0	C0	0G0	1R0	1B0	…	358G0	359R0	359B0

Table 48 16-bit Parallel Interface for 888 1/2 Formats (MDT = 01)

Count	0	1	2	3	4	…	719	720
D/cx	0	1	1	1	1	…	1	1
D15		0R7	0B7	1R7	1B7	…	359R7	359B7
D14		0R6	0B6	1R6	1B6	…	359R6	359B6
D13		0R5	0B5	1R5	1B5	…	359R5	359B5
D12		0R4	0B4	1R4	1B4	…	359R4	359B4
D11		0R3	0B3	1R3	1B3	…	359R3	359B3
D10		0R2	0B2	1R2	1B2	…	359R2	359B2
D9		0R1	0B1	1R1	1B1	…	359R1	359B1
D8		0R0	0B0	1R0	1B0	…	359R0	359B0
D7	C7	0G7		1G7		…	359G7	
D6	C6	0G6		1G6		…	359G6	
D5	C5	0G5		1G5		…	359G5	
D4	C4	0G4		1G4		…	359G4	
D3	C3	0G3		1G3		…	359G3	
D2	C2	0G2		1G2		…	359G2	
D1	C1	0G1		1G1		…	359G1	
D0	C0	0G0		1G0		…	359G0	

Table 49 9-bit Parallel Interface for 888 1/3 Formats (MDT = 00)

Count	0	1	2	3	…	1078	1079	1080
D/CX	0	1	1	1	…	1	1	1
D8								
D7	C7	0R7	0G7	0B7	…	359R7	359G7	359B7
D6	C6	0R6	0G6	0B6	…	359R6	359G6	359B6
D5	C5	0R5	0G5	0B5	…	359R5	359G5	359B5
D4	C4	0R4	0G4	0B4	…	359R4	359G4	359B4
D3	C3	0R3	0G3	0B3	…	359R3	359G3	359B3
D2	C2	0R2	0G2	0B2	…	359R2	359G2	359B2
D1	C1	0R1	0G1	0B1	…	359R1	359G1	359B1
D0	C0	0R0	0G0	0B0	…	359R0	359G0	359B0

Table 50 8-bit Parallel Interface for 888 1/3 Formats (MDT = 00)

Count	0	1	2	3	…	1078	1079	1080
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R7	0G7	0B7	…	359R7	359G7	359B7
D6	C6	0R6	0G6	0B6	…	359R6	359G6	359B6
D5	C5	0R5	0G5	0B5	…	359R5	359G5	359B5
D4	C4	0R4	0G4	0B4	…	359R4	359G4	359B4
D3	C3	0R3	0G3	0B3	…	359R3	359G3	359B3
D2	C2	0R2	0G2	0B2	…	359R2	359G2	359B2
D1	C1	0R1	0G1	0B1	…	359R1	359G1	359B1
D0	C0	0R0	0G0	0B0	…	359R0	359G0	359B0

3.2.4 262K COLOR MODE

For the display data to be accessed in 262k color mode, it is necessary that 262k color mode be selected (B2 to B0: 110) using COLMOD command before writing/reading to or from the display data RAM. In this mode, the display data per pixel comprised of 6 bits for R, 6 bits for G and 6 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MPU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed.

This Chapter is based on the assumption that the number of 360-RGB source channels.

Table 51 24-bit Parallel interface for 666 1/1 formats (MDT = 00)

Count	0	1	2	…	359	360
D/CX	0	1	1	…	1	1
D23				…		
D22				…		
D21				…		
D20				…		
D19				…		
D18				…		
D17		0R5	1R5	…	358R5	359R5
D16		0R4	1R4	…	358R4	359R4
D15		0R3	1R3	…	358R3	359R3
D14		0R2	1R2	…	358R2	359R2
D13		0R1	1R1	…	358R1	359R1
D12		0R0	1R0	…	358R0	359R0
D11		0G5	1G5	…	358G5	359G5
D10		0G4	1G4	…	358G4	359G4
D9		0G3	1G3	…	358G3	359G3
D8		0G2	1G2	…	358G2	359G2
D7	C7	0G1	1G1	…	358G1	359G1
D6	C6	0G0	1G0	…	358G0	359G0
D5	C5	0B5	1B5	…	358B5	359B5
D4	C4	0B4	1B4		358B4	359B4
D3	C3	0B3	1B3		358B3	359B3
D2	C2	0B2	1B2	…	358B2	359B2
D1	C1	0B1	1B1	…	358B1	359B1
D0	C0	0B0	1B0	…	358B0	359B0

Table 52 18-bit Parallel Interface for 666 1/1 Formats (MDT = 00)

Count	0	1	2	…	359	360
D/CX	0	1	1	…	1	1
D17		0R5	1R5	…	358R5	359R5
D16		0R4	1R4	…	358R4	359R4
D15		0R3	1R3	…	358R3	359R3
D14		0R2	1R2	…	358R2	359R2
D13		0R1	1R1	…	358R1	359R1
D12		0R0	1R0	…	358R0	359R0
D11		0G5	1G5	…	358G5	359G5
D10		0G4	1G4	…	358G4	359G4
D9		0G3	1G3	…	358G3	359G3
D8		0G2	1G2	…	358G2	359G2
D7	C7	0G1	1G1	…	358G1	359G1
D6	C6	0G0	1G0	…	358G0	359G0
D5	C5	0B5	1B5	…	358B5	359B5
D4	C4	0B4	1B4	…	358B4	359B4
D3	C3	0B3	1B3	…	358B3	359B3
D2	C2	0B2	1B2	…	358B2	359B2
D1	C1	0B1	1B1	…	358B1	359B1
D0	C0	0B0	1B0	…	358B0	359B0

Table 53 16-bit Parallel Interface for 666 2/3 Formats (MDT = 00)

Count	0	1	2		…	538	539	540
D/CX	0	1	1		…	1	1	1
D15								
D14								
D13								
D12								
D11		0R5	0B5	1G5	…	358R5	358B5	359G5
D10		0R4	0B4	1G4	…	358R4	358B4	359G4
D9		0R3	0B3	1G3	…	358R3	358B3	359G3
D8		0R2	0B2	1G2	…	358R2	358B2	359G2
D7	C7	0R1	0B1	1G1	…	358R1	358B1	359G1
D6	C6	0R0	0B0	1G0	…	358R0	358B0	359G0
D5	C5	0G5	1R5	1B5	…	358G5	359R5	359B5
D4	C4	0G4	1R4	1B4	…	358G4	359R4	359B4
D3	C3	0G3	1R3	1B3	…	358G3	359R3	359B3
D2	C2	0G2	1R2	1B2	…	358G2	359R2	359B2
D1	C1	0G1	1R1	1B1	…	358G1	359R1	359B1
D0	C0	0G0	1R0	1B0	…	358G0	359R0	359B0

Table 54 16-bit Parallel Interface for 666 1/2 Formats (MDT = 01)

Count	0	1	2	3	4	…	719	720
D/CX	0	1	1	1	1	…	1	1
D15								
D14								
D13								
D12								
D11		0R5	0B5	1R5	1B5	…	359R5	359B5
D10		0R4	0B4	1R4	1B4	…	359R4	359B4
D9		0R3	0B3	1R3	1B3	…	359R3	359B3
D8		0R2	0B2	1R2	1B2	…	359R2	359B2
D7	C7	0R1	0B1	1R1	1B1	…	359R1	359B1
D6	C6	0R0	0B0	1R0	1B0	…	359R0	359B0
D5	C5	0G5		1G5		…	359G5	
D4	C4	0G4		1G4		…	359G4	
D3	C3	0G3		1G3		…	359G3	
D2	C2	0G2		1G2		…	359G2	
D1	C1	0G1		1G1		…	359G1	
D0	C0	0G0		1G0		…	359G0	

Table 55 16-bit Parallel interface for 666 1/2 formats (MDT = 10)

Count	0	1	2	3	4	…	719	720
D/CX	0	1	1	1	1	…	1	1
D15		0R5	0B1	1R5	1B1	…	359R5	359B1
D14		0R4	0B0	1R4	1B0	…	359R4	359B0
D13		0R3		1R3		…	359R3	
D12		0R2		1R2		…	359R2	
D11		0R1		1R1		…	359R1	
D10		0R0		1R0		…	359R0	
D9		0G5		1G5		…	359G5	
D8		0G4		1G4		…	359G4	
D7	C7	0G3		1G3		…	359G3	
D6	C6	0G2		1G2		…	359G2	
D5	C5	0G1		1G1		…	359G1	
D4	C4	0G0		1G0		…	359G0	
D3	C3	0B5		1B5		…	359B5	
D2	C2	0B4		1B4		…	359B4	
D1	C1	0B3		1B3		…	359B3	
D0	C0	0B2		1B2		…	359B2	

Table 56 16-bit Parallel Interface for 666 1/2 Formats (MDT = 11)

Count	0	1	2	3	4	…	719	720
D/CX	0	1	1	1	1	…	1	1
D15			0R3		1R3	…		359R3
D14			0R2		1R2	…		359R2
D13			0R1		1R1	…		359R1
D12			0R0		1R0	…		359R0
D11			0G5		1G5	…		359G5
D10			0G4		1G4	…		359G4
D9			0G3		1G3	…		359G3
D8			0G2		1G2	…		359G2
D7	C7		0G1		1G1	…		359G1
D6	C6		0G0		1G0	…		359G0
D5	C5		0B5		1B5	…		359B5
D4	C4		0B4		1B4	…		359B4
D3	C3		0B3		1B3	…		359B3
D2	C2		0B2		1B2	…		359B2
D1	C1	0R5	0B1	1R5	1B1	…	359R5	359B1
D0	C0	0R4	0B0	1R4	1B0	…	359R4	359B0

Table 57 9-bit Parallel Interface for 666 1/2 Formats (MDT = 00)

Count	0	1	2	3	4	…	719	720
D/CX	0	1	1	1	1	…	1	1
D8		0R5	0G2	1R5	1G2	…	359R5	359G2
D7	C7	0R4	0G1	1R4	1G1	…	359R4	359G1
D6	C6	0R3	0G0	1R3	1G0	…	359R3	359G0
D5	C5	0R2	0B5	1R2	1B5	…	359R2	359B5
D4	C4	0R1	0B4	1R1	1B4	…	359R1	359B4
D3	C3	0R0	0B3	1R0	1B3	…	359R0	359B3
D2	C2	0G5	0B2	1G5	1B2	…	359G5	359B2
D1	C1	0G4	0B1	1G4	1B1	…	359G4	359B1
D0	C0	0G3	0B0	1G3	1B0	…	359G3	359B0

Table 58 9-bit Parallel Interface for 666 1/3 Formats (MDT = 01)

Count	0	1	2	3	…	1078	1079	1080
D/CX	0	1	1	1	…	1	1	1
D8								
D7	C7							
D6	C6							
D5	C5	0R5	0G5	0B5	…	359R5	359G5	359B5
D4	C4	0R4	0G4	0B4	…	359R4	359G4	359B4
D3	C3	0R3	0G3	0B3	…	359R3	359G3	359B3
D2	C2	0R2	0G2	0B2	…	359R2	359G2	359B2
D1	C1	0R1	0G1	0B1	…	359R1	359G1	359B1
D0	C0	0R0	0G0	0B0	…	359R0	359G0	359B0

Table 59 8-bit Parallel Interface for 666 1/3 Formats (MDT = 00)

Count	0	1	2	3	…	1078	1079	1080
D/CX	0	1	1	1	…	1	1	1
D7	C7							
D6	C6							
D5	C5	0R5	0G5	0B5	…	359R5	359G5	359B5
D4	C4	0R4	0G4	0B4	…	359R4	359G4	359B4
D3	C3	0R3	0G3	0B3	…	359R3	359G3	359B3
D2	C2	0R2	0G2	0B2	…	359R2	359G2	359B2
D1	C1	0R1	0G1	0B1	…	359R1	359G1	359B1
D0	C0	0R0	0G0	0B0	…	359R0	359G0	359B0

Table 60 8-bit Parallel Interface for 666 1/3 Formats (MDT = 01)

Count	0	1	2	3	…	1078	1079	1080
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	359R5	359G5	359B5
D6	C6	0R4	0G4	0B4	…	359R4	359G4	359B4
D5	C5	0R3	0G3	0B3	…	359R3	359G3	359B3
D4	C4	0R2	0G2	0B2	…	359R2	359G2	359B2
D3	C3	0R1	0G1	0B1	…	359R1	359G1	359B1
D2	C2	0R0	0G0	0B0	…	359R0	359G0	359B0
D1	C1							
D0	C0							

3.2.5 65K COLOR MODE

For the display data to be accessed in 65k color mode, it is necessary that 65k color mode be selected (B2 to B0: 101) using COLMOD command before writing or reading to or from the display data RAM. In this mode, the display data per pixel comprised of 5 bits for R, 6 bits for G and 5 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MPU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed.

This Chapter is based on the assumption that the number of 360-RGB source channels.

Table 61 24-bit Parallel Interface for 565 1/1 Formats (MDT = 00)

Count	0	1	2	…	359	360
D/CX	0	1	1	…	1	1
D23						
D22						
D21						
D20						
D19						
D18						
D17						
D16						
D15		0R4	1R4	…	358R4	359R4
D14		0R3	1R3	…	358R3	359R3
D13		0R2	1R2	…	358R2	359R2
D12		0R1	1R1	…	358R1	359R1
D11		0R0	1R0	…	358R0	359R0
D10		0G5	1G5	…	358G5	359G5
D9		0G4	1G4	…	358G4	359G4
D8		0G3	1G3	…	358G3	359G3
D7	C7	0G2	1G2	…	358G2	359G2
D6	C6	0G1	1G1	…	358G1	359G1
D5	C5	0G0	1G0	…	358G0	359G0
D4	C4	0B4	1B4	…	358B4	359B4
D3	C3	0B3	1B3	…	358B3	359B3
D2	C2	0B2	1B2	…	358B2	359B2
D1	C1	0B1	1B1	…	358B1	359B1
D0	C0	0B0	1B0	…	358B0	359B0

Table 62 18-bit Parallel Interface for 565 1/1 Formats (MDT = 00)

Count	0	1	2	…	359	360
D/CX	0	1	1	…	1	1
D17						
D16						
D15		0R4	1R4		358R4	359R4
D14		0R3	1R3		358R3	359R3
D13		0R2	1R2	…	358R2	359R2
D12		0R1	1R1	…	358R1	359R1
D11		0R0	1R0	…	358R0	359R0
D10		0G5	1G5	…	358G5	359G5
D9		0G4	1G4	…	358G4	359G4
D8		0G3	1G3	…	358G3	359G3
D7	C7	0G2	1G2	…	358G2	359G2
D6	C6	0G1	1G1	…	358G1	359G1
D5	C5	0G0	1G0	…	358G0	359G0
D4	C4	0B4	1B4	…	358B4	359B4
D3	C3	0B3	1B3	…	358B3	359B3
D2	C2	0B2	1B2	…	358B2	359B2
D1	C1	0B1	1B1	…	358B1	359B1
D0	C0	0B0	1B0	…	358B0	359B0

Table 63 16-bit Parallel Interface for 565 1/2 Formats (MDT = 00)

Count	0	1	2	…	359	360
D/CX	0	1	1	…	1	1
D15		0R4	1R4	…	358R4	359R4
D14		0R3	1R3	…	358R3	359R3
D13		0R2	1R2	…	358R2	359R2
D12		0R1	1R1	…	358R1	359R1
D11		0R0	1R0	…	358R0	359R0
D10		0G5	1G5	…	358G5	359G5
D9		0G4	1G4	…	358G4	359G4
D8		0G3	1G3	…	358G3	359G3
D7	C7	0G2	1G2	…	358G2	359G2
D6	C6	0G1	1G1	…	358G1	359G1
D5	C5	0G0	1G0	…	358G0	359G0
D4	C4	0B4	1B4	…	358B4	359B4
D3	C3	0B3	1B3	…	358B3	359B3
D2	C2	0B2	1B2	…	358B2	359B2
D1	C1	0B1	1B1	…	358B1	359B1
D0	C0	0B0	1B0	…	358B0	359B0

Table 64 9-bit Parallel Interface for 565 1/2 Formats (MDT = 00)

Count	0	1	2	3	4	…	719	720
D/CX	0	1	1	1	1	…	1	1
D8								
D7	C7	0R4	0G2	1R4	1G2	…	359R4	359G2
D6	C6	0R3	0G1	1R3	1G1	…	359R3	359G1
D5	C5	0R2	0G0	1R2	1G0	…	359R2	359G0
D4	C4	0R1	0B4	1R1	1B4	…	359R1	359B4
D3	C3	0R0	0B3	1R0	1B3	…	359R0	359B3
D2	C2	0G5	0B2	1G5	1B2	…	359G5	359B2
D1	C1	0G4	0B1	1G4	1B1	…	359G4	359B1
D0	C0	0G3	0B0	1G3	1B0	…	359G3	359B0

Table 65 8-bit Parallel Interface for 565 1/2 Formats (MDT = 00)

Count	0	1	2	3	4	…	719	720
D/CX	0	1	1	1	1	…	1	1
D7	C7	0R4	0G2	1R4	1G2	…	359R4	359G2
D6	C6	0R3	0G1	1R3	1G1	…	359R3	359G1
D5	C5	0R2	0G0	1R2	1G0	…	359R2	359G0
D4	C4	0R1	0B4	1R1	1B4	…	359R1	359B4
D3	C3	0R0	0B3	1R0	1B3	…	359R0	359B3
D2	C2	0G5	0B2	1G5	1B2	…	359G5	359B2
D1	C1	0G4	0B1	1G4	1B1	…	359G4	359B1
D0	C0	0G3	0B0	1G3	1B0	…	359G3	359B0

3.3 RGB INTERFACE

3.3.1 MOTION PICTURE DISPLAY

S6D05A1 incorporates RGB interface to display motion pictures and GRAM to store data for display.
The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK.

In the period between the completion of displaying one frame data and the next VSYNC signal, the display status will remain in front porch period.

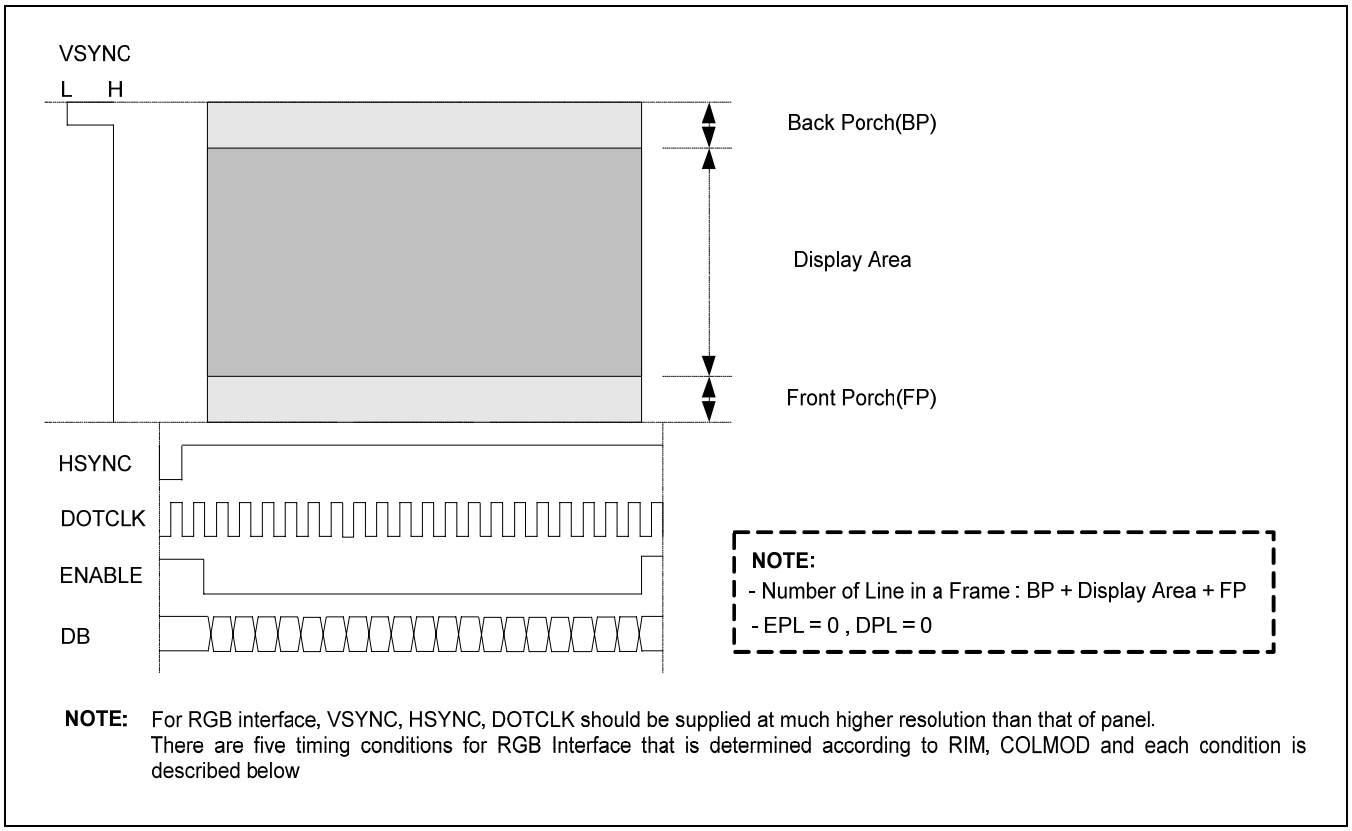


Figure 71 RGB Interface

Table 66 RGB Interface Mode Selection

RIM	COLMOD[6:4]	RGB Interface Mode
0	111 (16M color)	24-bit RGB interface (1 transfer/pixel)
	110 (262k color)	18-bit RGB interface (1 transfer/pixel)
	101 (65k color)	16-bit RGB interface (1 transfer/pixel)
1	111 (16M color)	8-bit RGB interface (3 transfer/pixel)
	110 (262k color)	6-bit RGB interface (3 transfer/pixel)

3.3.2 24-BIT RGB INTERFACE

3.3.2.1 Bit Assignment

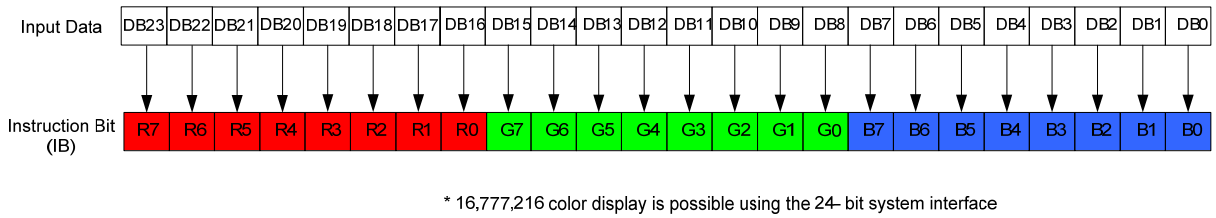
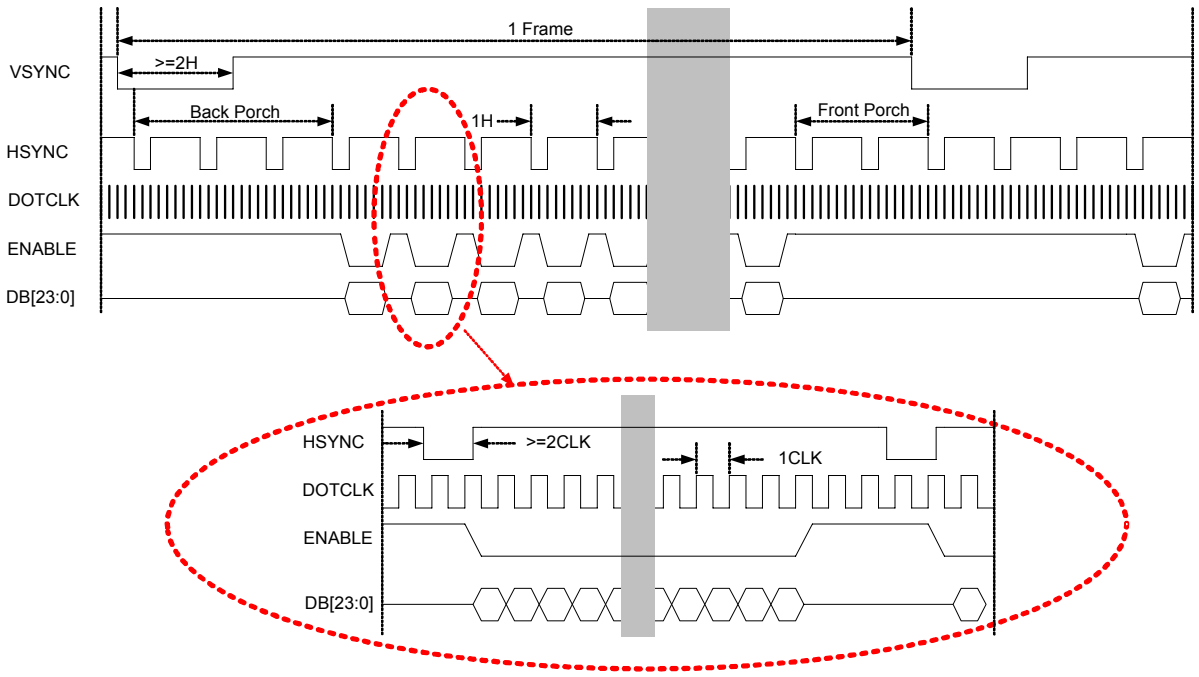


Figure 72 Bit Assignment of GRAM Data on 24bit RGB Interface

3.3.2.2 Timing Diagram



NOTE: The number of DOTCLK for 1H period must be bigger than Horizontal Pixel + 30 (ex, 360RGB : DOTCLK >390)

Figure 73 Timing Diagram of 24bit RGB Interface

3.3.3 18-BIT RGB INTERFACE

3.3.3.1 Bit Assignment

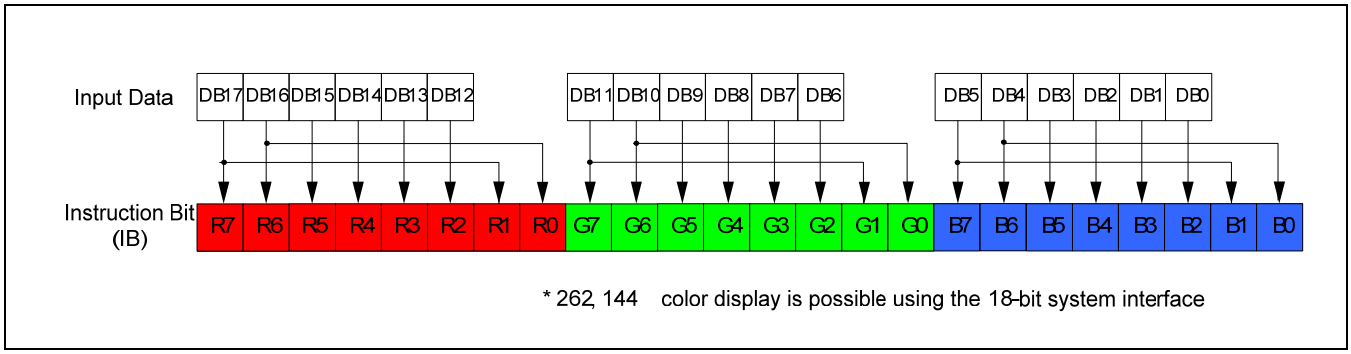
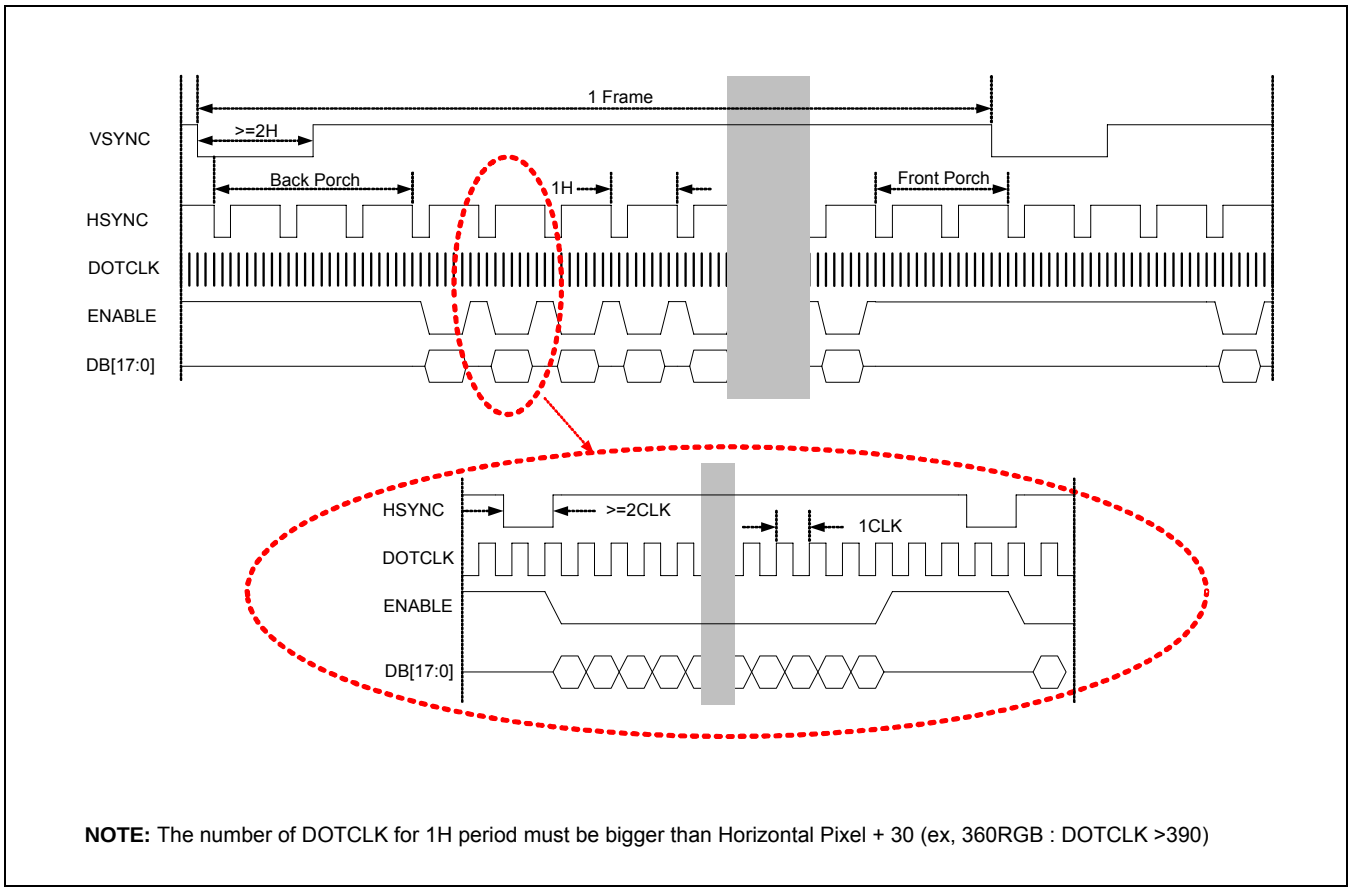


Figure 74 Bit Assignment of GRAM Data on 18bit RGB Interface(IPM=”100”)

3.3.3.2 Timing Diagram



NOTE: The number of DOTCLK for 1H period must be bigger than Horizontal Pixel + 30 (ex, 360RGB : DOTCLK >390)

Figure 75 Timing Diagram of 18bit RGB Interface

3.3.4 16-BIT RGB INTERFACE

3.3.4.1 Bit Assignment

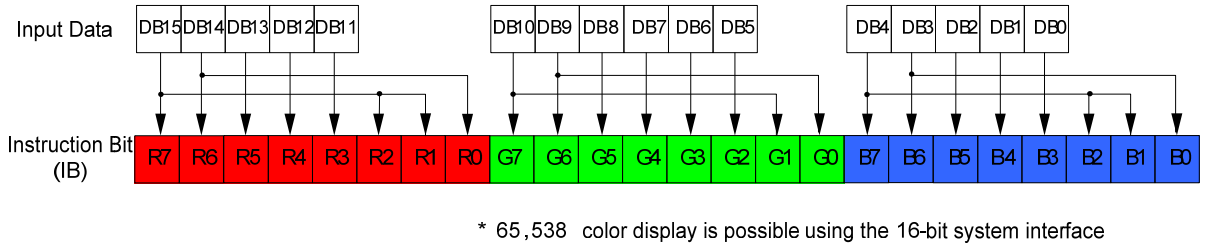
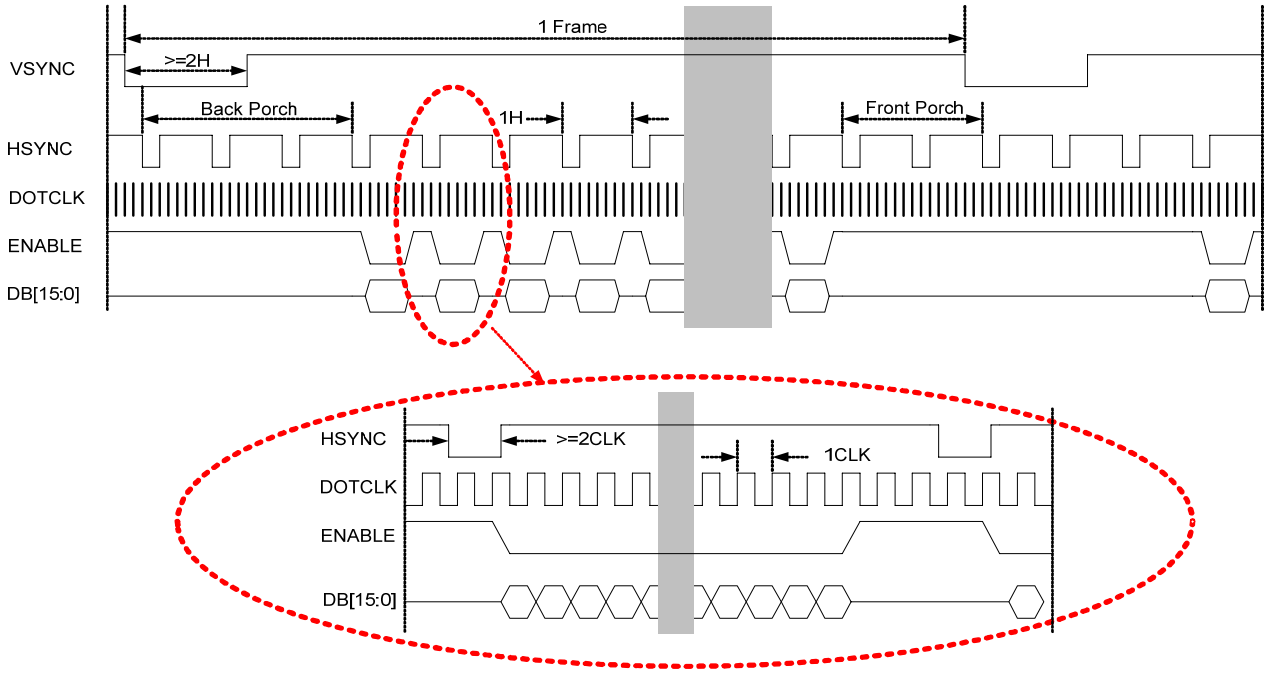


Figure 76 Bit Assignment of GRAM Data on 16bit RGB Interface(IPM=”100”)

3.3.4.2 Timing Diagram



NOTE: The number of DOTCLK for 1H period must be bigger than Horizontal Pixel + 30 (ex, 360RGB : DOTCLK >390)

Figure 77 Timing Diagram of 16bit RGB Interface

3.3.5 8-BIT RGB INTERFACE

In order to transfer data on 8bit RGB Interface there should be three transfers.

3.3.5.1 Bit Assignment

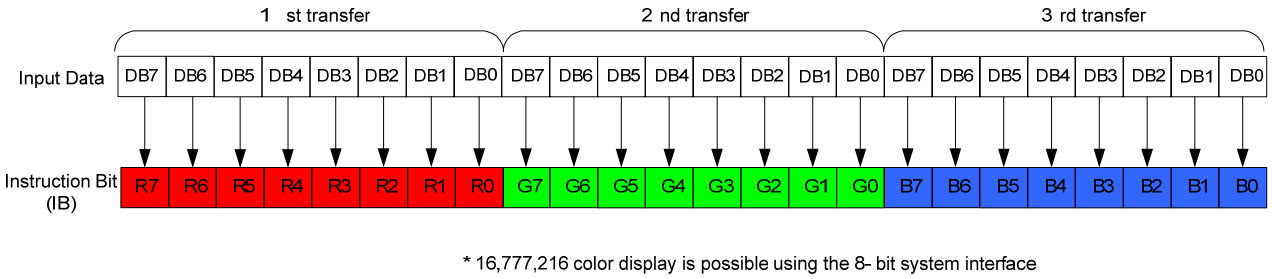
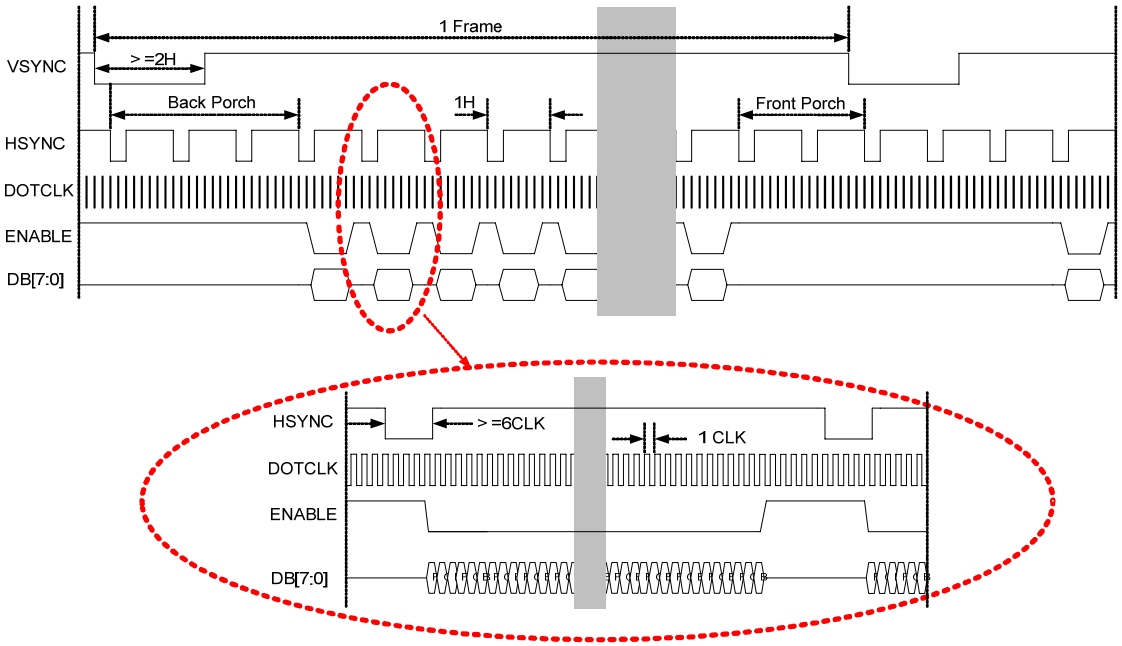


Figure 78 Bit Assignment of GRAM Data on 8bit RGB Interface

3.3.5.2 Timing Diagram

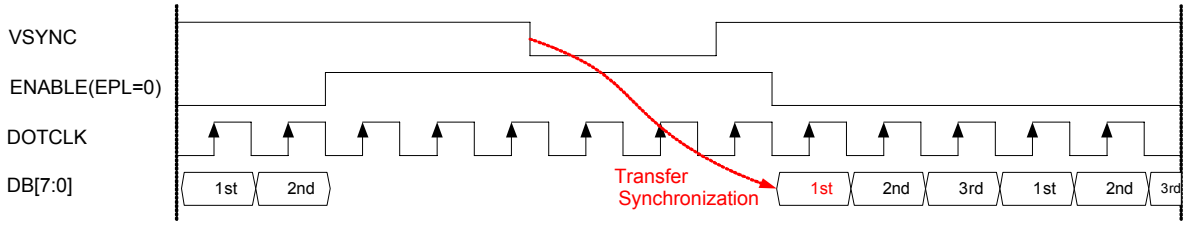


NOTE:

1. Three clocks are regarded as one clock for transfer when data is transferred in 8-bit interface. VSYNC,HSYNC,ENABLE,DOTCLK, and DB[7:0] should be transferred in units of three clocks.
2. The number of DOTCLK for 1H period must be bigger than ((Horizontal Pixel + 30)x3). (ex, 320RGB: DOTCLK>350X3)

Figure 79 Timing Diagram of 8bit RGB Interface

3.3.5.3 Transfer Synchronization



NOTE: The figure above shows Transfer Synchronization functions for 8bit RGB Interface. S6D05A1 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 8bit RGB Interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data Transmission state. Transfer mismatch can Be corrected at every VSYNC signal assertion. In this method, when data is consecutively transferred in for Displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation. The display is operated in units of three DOTCLKs. When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

Figure 80 Transfer Synchronization Function in 8-bit RGB Interface Mode

3.3.6 6-BIT RGB INTERFACE

In order to transfer data on 6bit RGB Interface there should be three transfers.

3.3.6.1 Bit Assignment

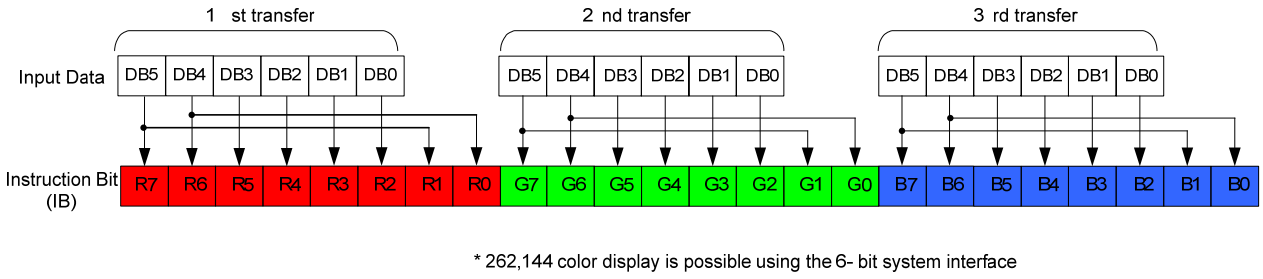
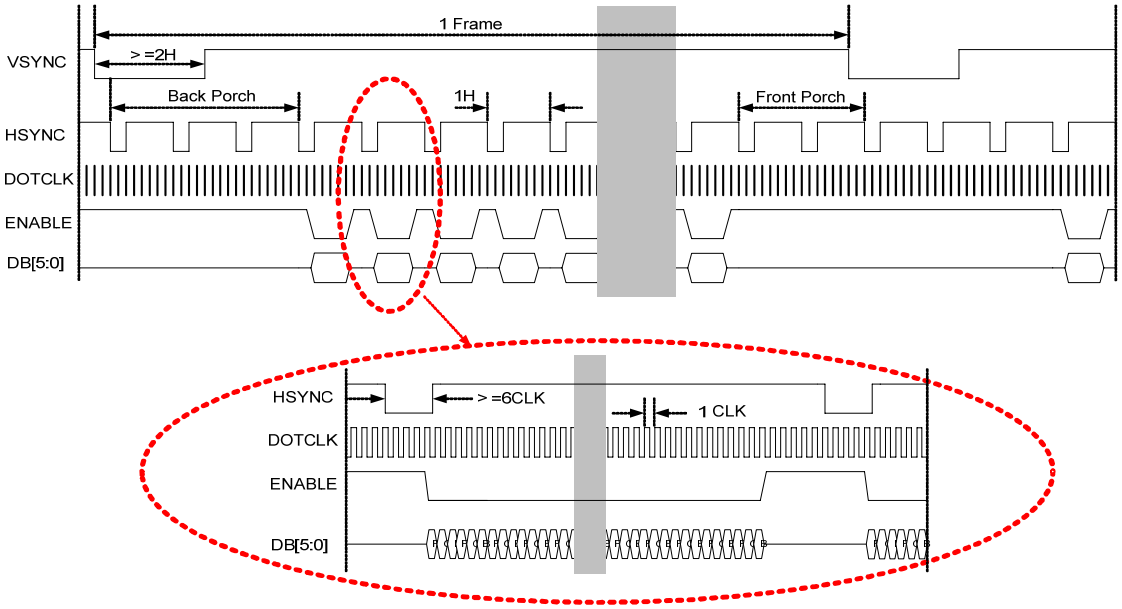


Figure 81 Bit Assignment of GRAM Data on 6bit RGB Interface(IPM="100")

3.3.6.2 Timing Diagram

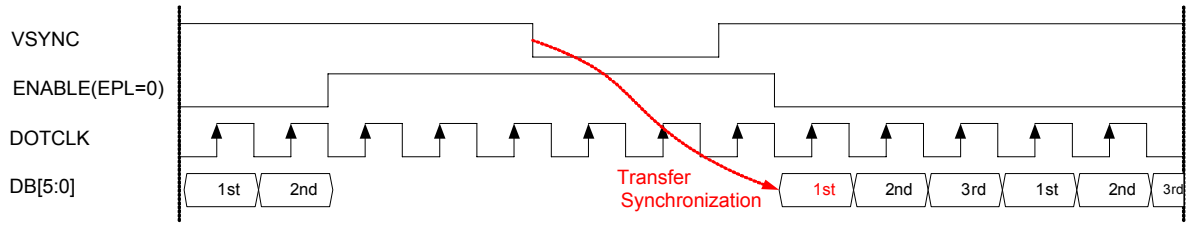


NOTE:

1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface. VSYNC,HSYNC,ENABLE,DOTCLK, and DB[5:0] should be transferred in units of three clocks.
2. The number of DOTCLK for 1H period must be bigger than ((Horizontal Pixel + 30)x3). (ex, 360RGB: DOTCLK>390X3)

Figure 82 Timing Diagram of 6bit RGB Interface

3.3.6.3 Transfer Synchronization



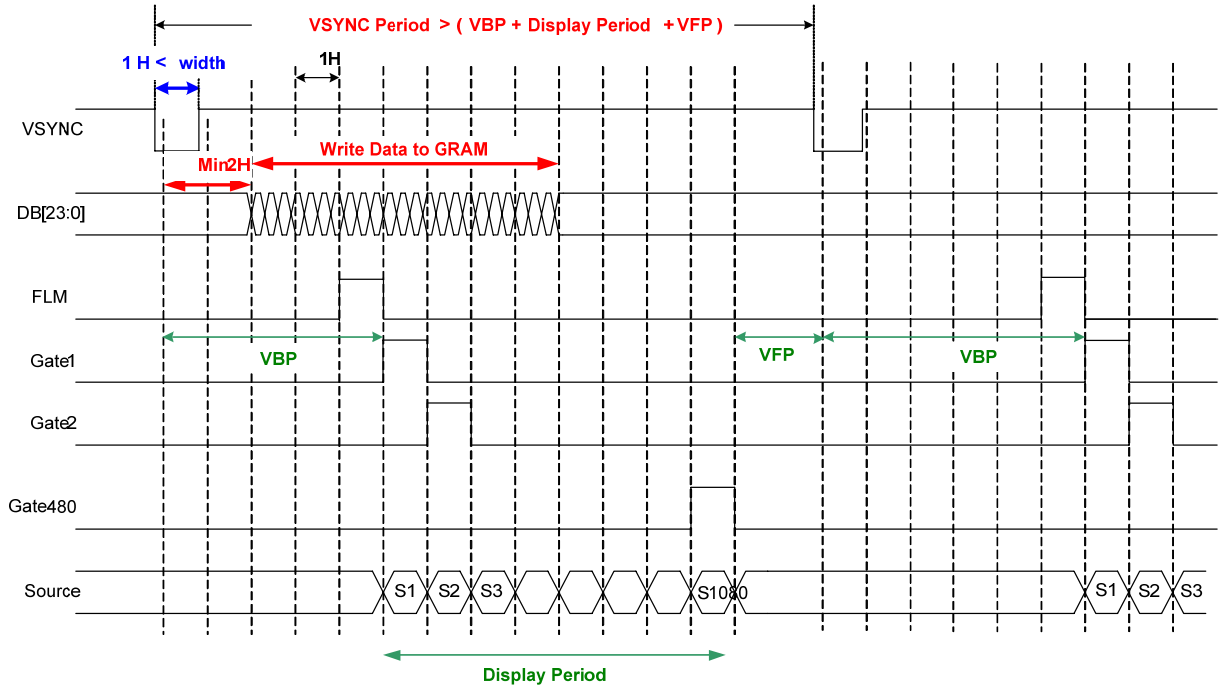
NOTE: The figure above shows Transfer Synchronization functions for 6bit RGB Interface. S6D05A1 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 6bit RGB Interface.
The transfer countEr is reset on the falling edge of VSYNC and enters the 1st data Transmission state.
Transfer mismatch can Be corrected at every VSYNC signal assertion.
In this method, when data is consecutively transferred in for Displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation. The display is operated in units of three DOTCLKs.
When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

Figure 83 Transfer Synchronization Function in 6-bit RGB Interface Mode

3.4 VSYNC INTERFACE

3.4.1 DEFINITION

The S6D05A1 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.
When DM1-0=”10”, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables tearing-free display of motion pictures with the conventional interface.
Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.



NOTE:
1. VSYNC period should always be constant.
   If not, some degradation of display such as flicker may occur in LCD system.
2. Display data don’t need to be written for every VSYNC period.
   For example, any system is working under 60Hz frame Rate and 30-fps motion picture condition.
   So being written display data for every other frame would be enough.

Figure 84 Timing Diagram of VSYNC I/F

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. The internal memory writing address counter is reset by VSYNC. So, insure interval time between VSYNC falling and GRAM data writing.

3.4.2 VSYNC INTERFACE MODE

3.4.2.1 Leading Mode

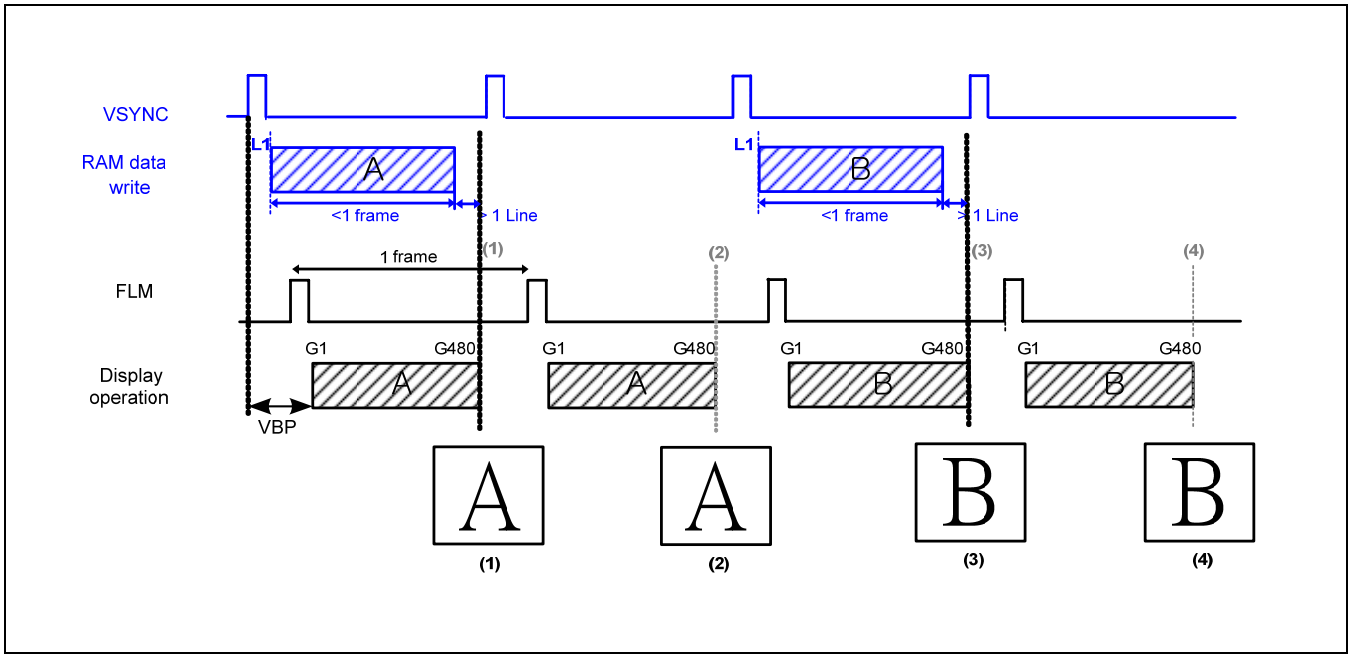


Figure 85 Operation for Leading Mode of VSYNC Interface (VPL = 1)

3.5 SPI TO RAM INTERFACE

3.5.1 DISPLAY DATA ACCESS FOR SPI

Table 67 Memory Access Mode Selection

IM3	IM2	IM1	IM0	Mode	SELF-REF(register)	
x	1	0	1	3-wire 9bit Data Serial I/F&RGB I/F	0	RGB I/F
					1	SPI
x	1	1	0	4-wire 8bit Data Serial I/F&RGB I/F	0	RGB I/F
					1	SPI

Table 68 SPI Display Data Format for Write

Color mode	MDT [1:0]	# of Transfer	# of Parameters							
			P7	P6	P5	P4	P3	P2	P1	P0
16M Color (COLMOD[2:0] = 111)	XX (1/3)	1	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]
		2	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]
		3	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
262k Color (COLMOD[2:0] = 110)	00 (1/3)	1	X	X	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]
		2	X	X	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]
		3	X	X	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
	01 (1/3)	1	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	X	X
		2	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	X	X
		3	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	X	X
65k Color (COLMOD[2:0] = 101)	XX (1/2)	1	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]
		2	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

NOTE:

1. Display data expand (666 → 888 or 565 → 888) method is decided by IPM command (IPM's default condition = "100")
2. Register sets related to data format (IPM, MDT,..) are on the F7H command (Level 2)

In 65k color mode (16-bit data) data bit should be expanded to 24-bit like below. It will be used “IPM=100”

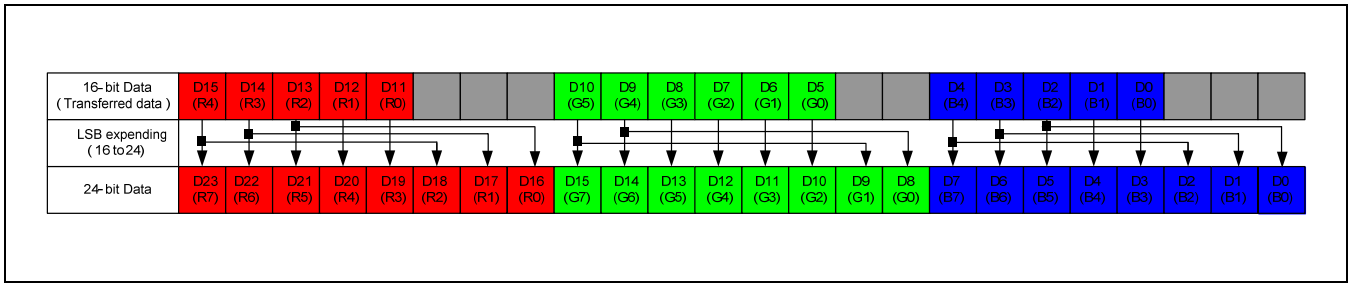


Figure 86 Data Expand Method (65K Color Mode)

In 262k color mode (18-bit data) data bit should be expanded to 24-bit like below. It will be used “IPM=100”

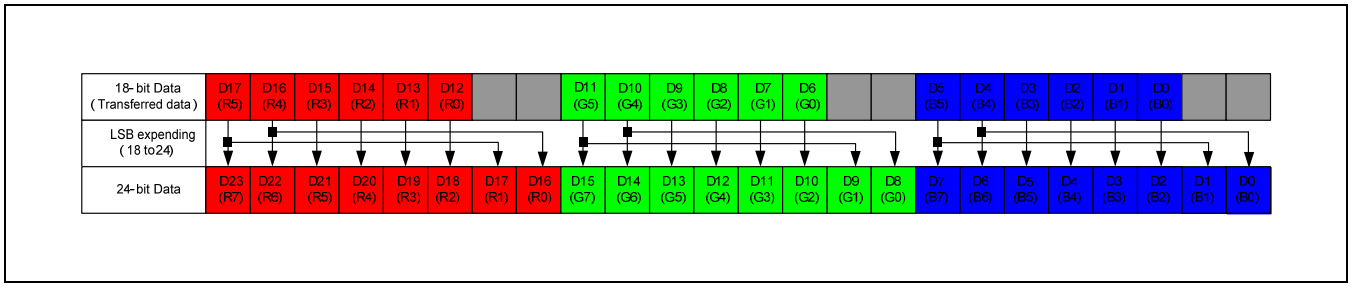


Figure 87 Data Expand Method (262K Color Mode)

3.6 MDDI

3.6.1 INTRODUCTION TO MDDI

The S6D05A1 supports MDDI, mobile display driver interface. The physical layer of MDDI is based on a high-speed, differential serial interface. Both command and image data transfer can be achieved with MDDI.
MDDI host & client are linked by Data and STB line. Through Data line, either command or image data is transferred from MDDI host to MDDI client, and vice versa. Data is transferred by packet unit.
Through STB line, strobe signal is transferred. When the link is in “FORWARD direction,” data is transferred from host to client; in “REVERSE direction,” client transfers data to MDDI host.

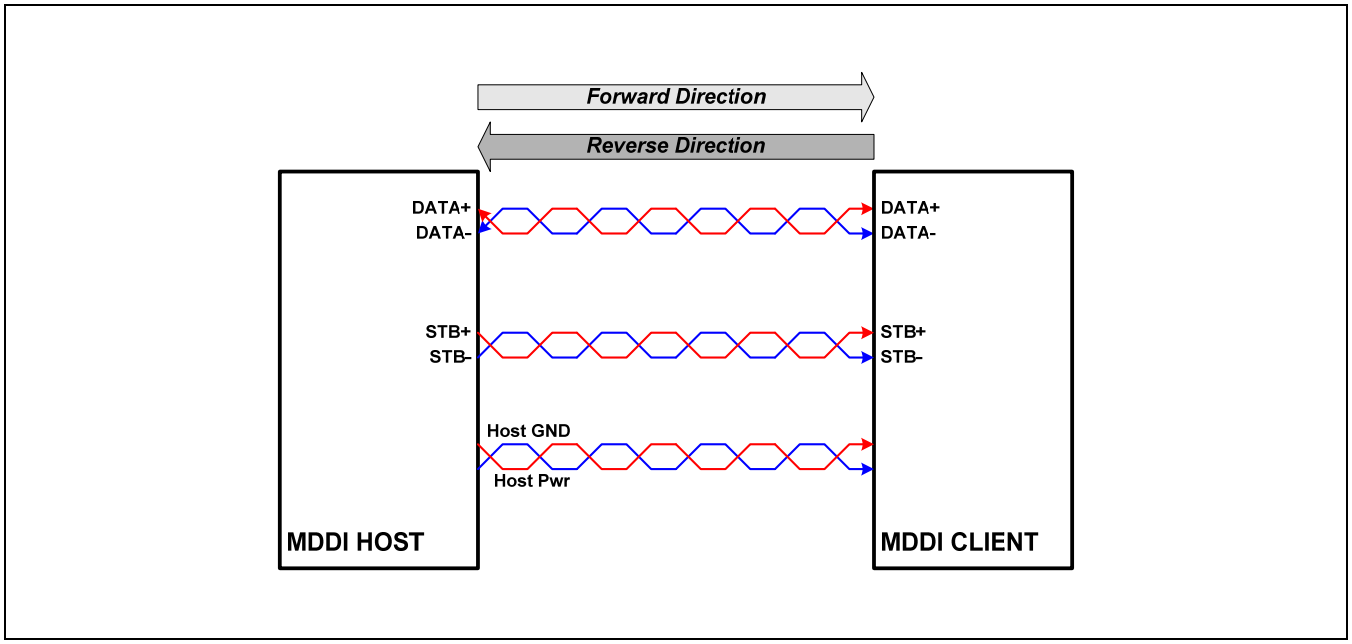


Figure 88 Physical Connection of MDDI Host and Client

3.6.2 DATA-STB ENCODING

Data is encoded using a DATA-STB method. Data signal is bi-directional over a pair of differential cable while STB signal is unidirectional over a pair of differential cable driven by a host as shown in following Figure. Figure below illustrates how the data sequence “1110001011” is transmitted using DATA-STB encoding.

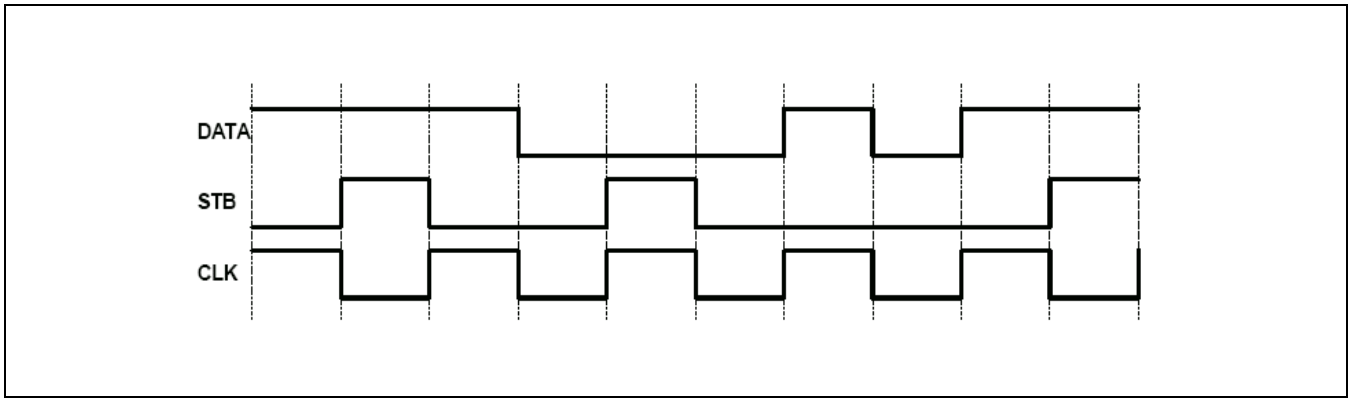


Figure 89 Data-STB Encoding

The Following figure shows a sample circuit to generate DATA and STB from input data, and then recover the input data from DATA and STB.

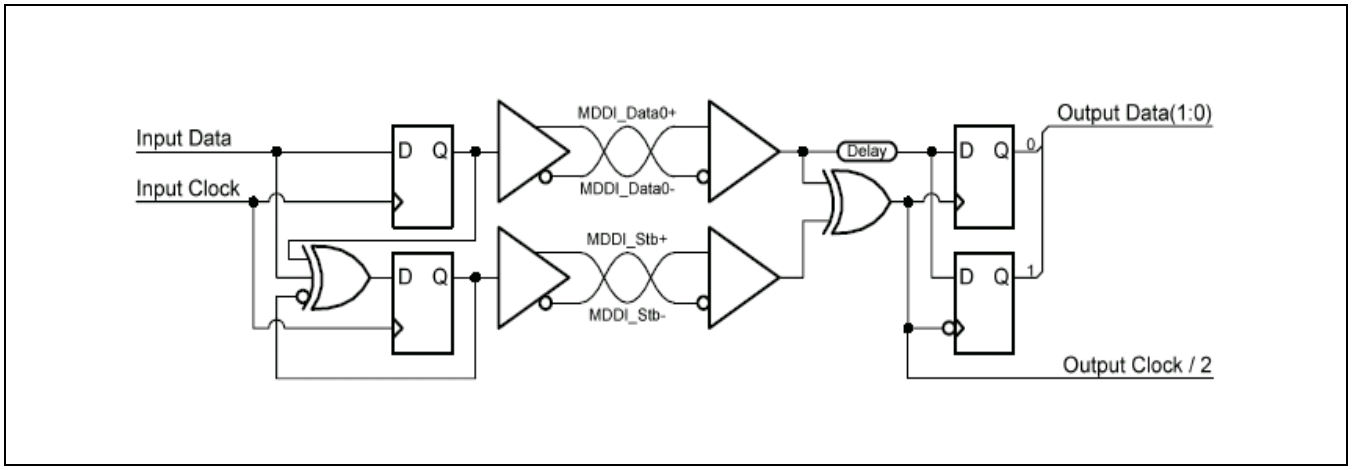


Figure 90 Data / STB Generation & Recovery Circuit

3.6.3 MDDI DATA & STB

The Data (MDP/MDN) and STB (MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets. The MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state, the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation, a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

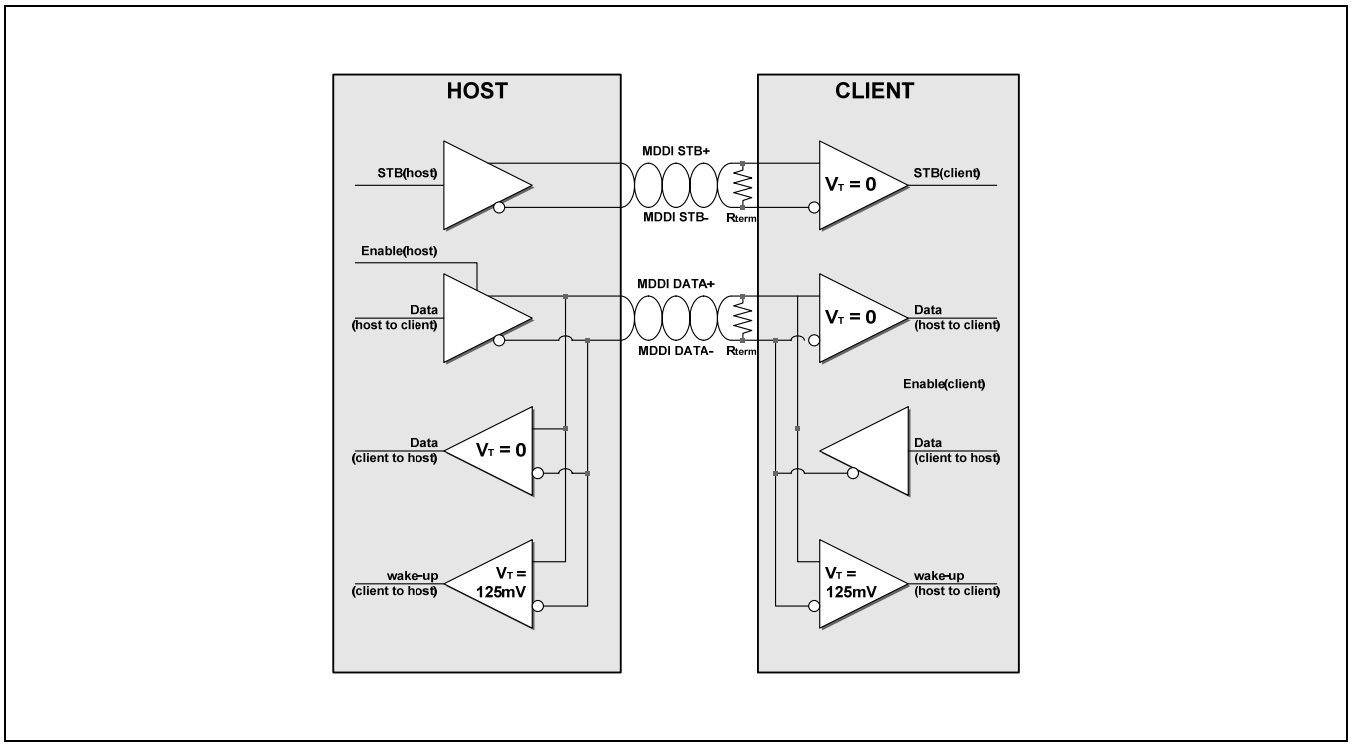


Figure 91 Differential Connection Between Host and Client

3.6.4 MDDI PACKET

MDDI transfer data in a packet format. MDDI host can generate and send packets.
In S6D05A1, several packet formats are supported. Packets are transferred from MDDI host to client (forward direction); but reverse encapsulation packet is transferred from MDDI client to host (reverse direction).
A number of packets, started by sub-frame header packet, construct 1 sub frame.

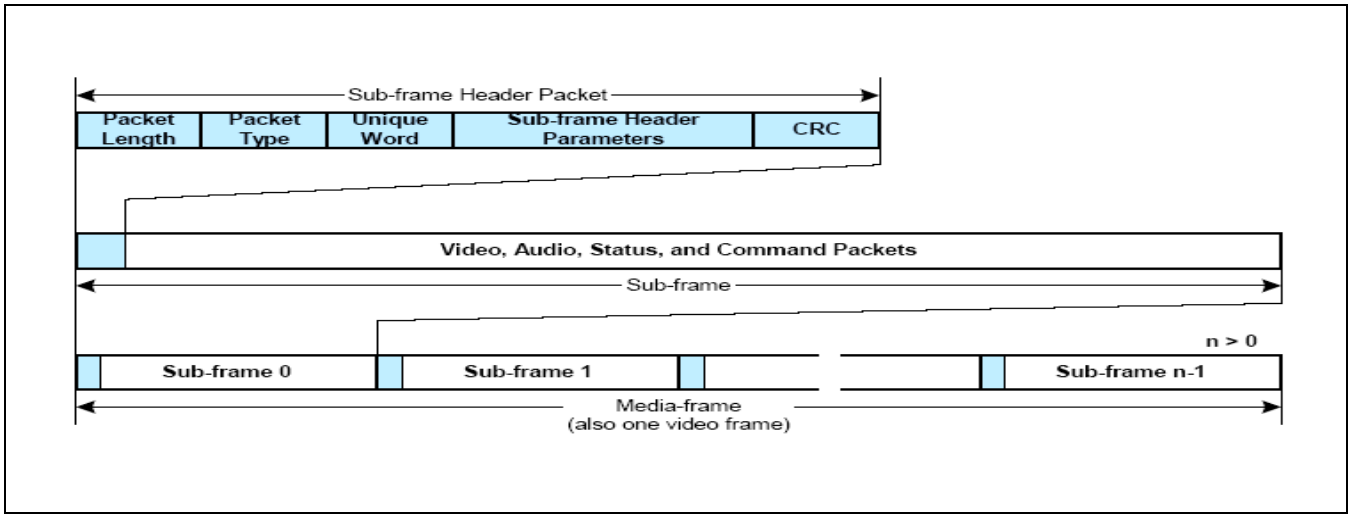


Figure 92 MDDI Packet Structure

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frame construct media-frame together.
The following table describes 9 types of packets which are supported in S6D05A1.

PACKET	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

3.6.4.1 Sub-Frame Header Packet

packet length	packet type = 3bffh	unique word = 005ah	reserved1	sub-frame length	protocol version	sub-frame conut	media frame count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (sub-frame header packet is 3bffh)
unique word : Identify "This packet is sub-frame header packet"
reserved1 : not used (set zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packets
mddi frame count : specifies number of media frames
CRC : error check

Figure 93 Sub-Frame Header Packet Structure

3.6.4.2 Register Access Packet

Basis of Register Data List is 4byte unit. Therefore, when write 1parameter, remainders must fill by 0.

packet length	packet type = 146	bClient ID	Read / Write Info	Register Address	Paramter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	Packet Length -14byte	2 bytes

packet length : packet length not including packet length block
packet type : packet type (Register Access packet is 146 (decimal))
bClient ID : set to all zero
Read / Write Info : to write register value , bits [15:14] = " 00 "
to request register value , bits [15: 14] = " 10 "
bits [13 : 0] refer to VESA SPEC
Register Address : Register address is written here
Parameter CRC : To check error from packet length to register address
Register Data List : A list of 4byte register data values to be written to LDI
CRC : To error check register data list
※ Basis of Register Data List is 4-byte unit. Therefore, When Register Parameter is not Multiply of 4, Remainder bits must fill by 0

000000FFh
Register Data list

Figure 94 Register Access Packet Structure

3.6.4.3 Video Stream Packet

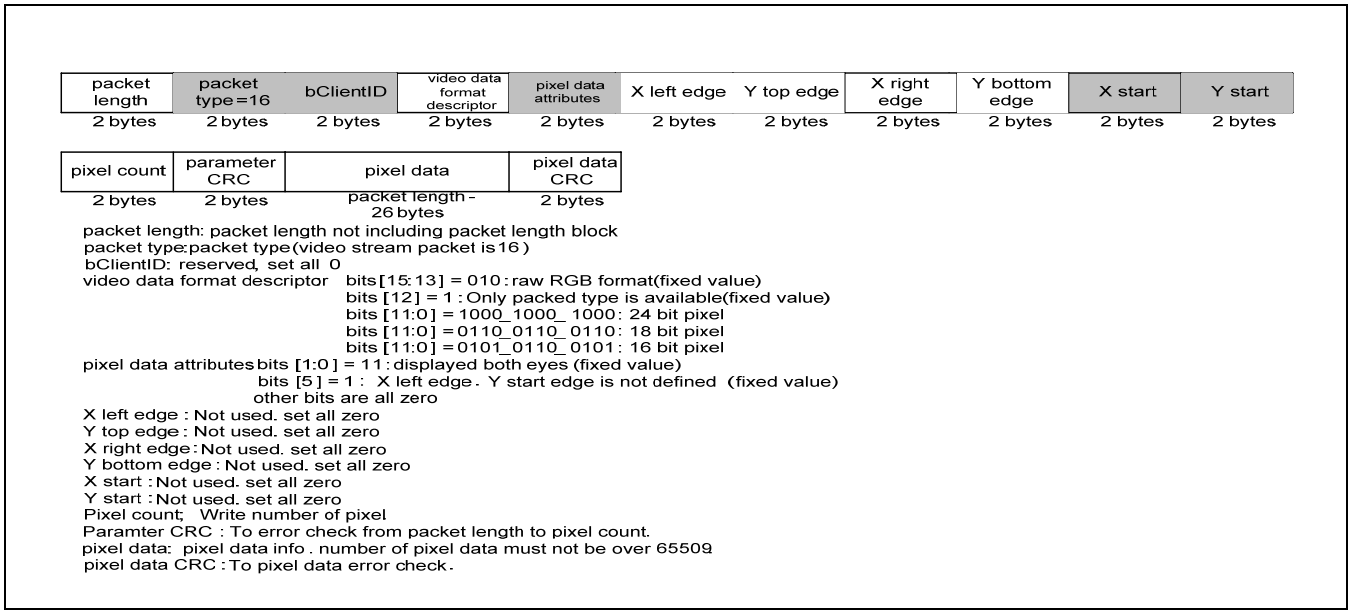
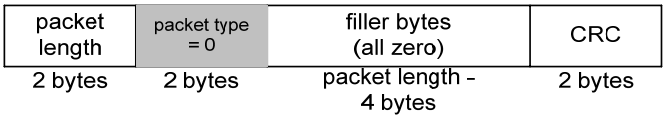


Figure 95 Video Stream Packet Structure

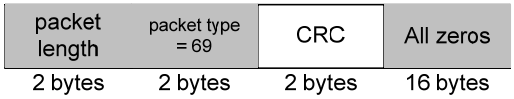
3.6.4.4 Filler Packet



packet length : packet length not including packet length block
packet type : packet type(Filler packet is 0(decimal))
filler bytes : set to all zero(The size is under packet length availabe)
CRC : To error check

Figure 96 Filler Packet Structure

3.6.4.5 Link Shutdown Packet



packet length : packet length not including packet length block
packet type : packet type(Link shutdown packet is 69(decimal))
CRC : To error check
All zeros : write all zero (size is 16 bytes)

Figure 97 Link Shutdown Packet Structure

: fixed value
For More information about MDDI packet, refer to VESA MDDI spec.

3.6.5 PANEL CONTROL

S6D05A1 supports video stream packet for memory write and register access packet for register write/read. Followings are some examples of memory and register write/read sequence.

3.6.5.1 Writing Video Data to Memory Sequence

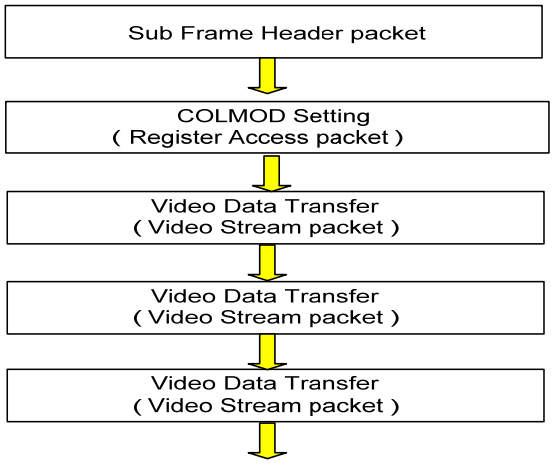


Figure 98 Writing Video Data To Memory Sequence

Table 69 COLMOD Setting in MDDI

Video data format descriptor[11:0]	COLMOD[2:0]
1000_1000_1000	111 (16M color)
0110_0110_0110	110 (262k color)
0101_0110_0101	101 (65k color)

NOTE: If user want to transfer 888(24bit) video data, Set COLMOD[2:0]=”111” prior to Video Stream Packet

3.6.5.2 Writing Register Sequence

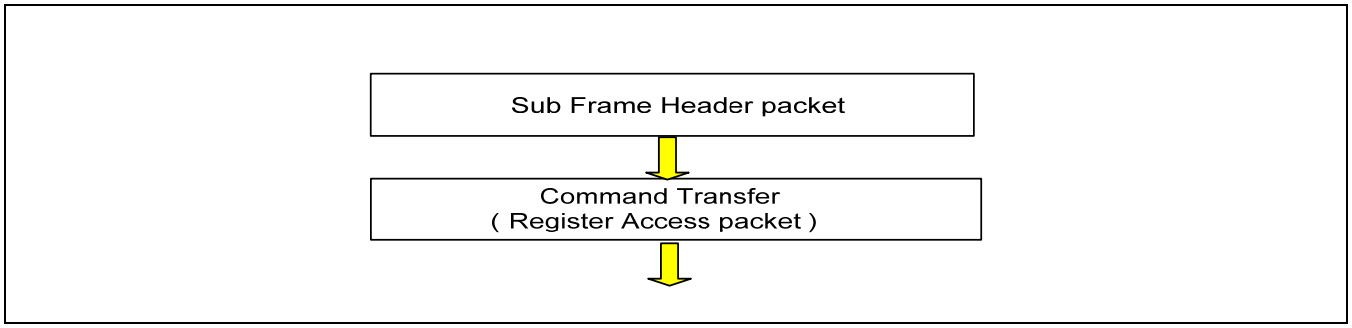


Figure 99 Writing Register Sequence

3.6.5.3 Reading Video Data from Memory Sequence

In order to read a pixel data from memory (readable one pixel only), the following sequence should be programmed. Memory read command (2EH) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

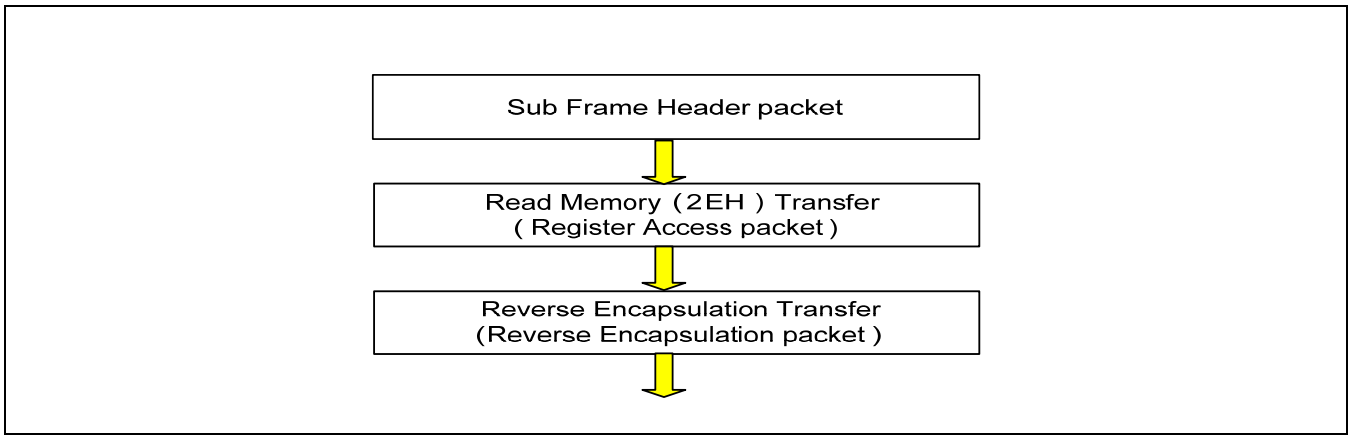
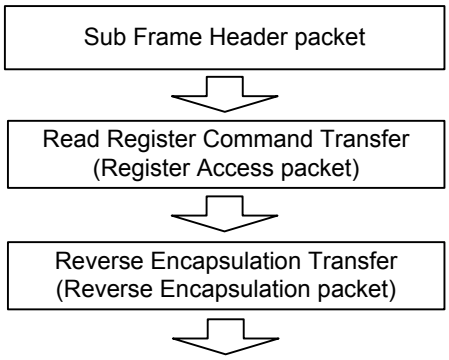


Figure 100 Reading Video Data from Memory Sequence

3.6.5.4 Reading Register Sequence

In order to read registers, the following sequence should be programmed. Register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.



NOTE: Only Level 1 Registers are readable in MDDI.

Figure 101 Reading Register Sequence

3.6.6 TEARING-LESS DISPLAY

In S6D05A1, the matching between data writes timing and written data display timing is important. If timing is mismatched, tearing effect can occur.
To avoid display tearing effect, two possible ways are suggested.
First case is that data write is slower than speed of displaying written data. In this case, data write speed is not critical, but current consumption in interface will be increased because data transfer time is long. Data write time is selected widely in this case.
Other case is that data write is faster than speed of displaying written data. In this case, data update speed is very high so that transfer time is short. So current consumption in interface can be minimized, but it requires fast data transfer. The most important thing is to avoid data scan conflicts with data update.
The following figures describe some examples to avoid display tearing phenomenon.

A. Display speed is slower than data write.

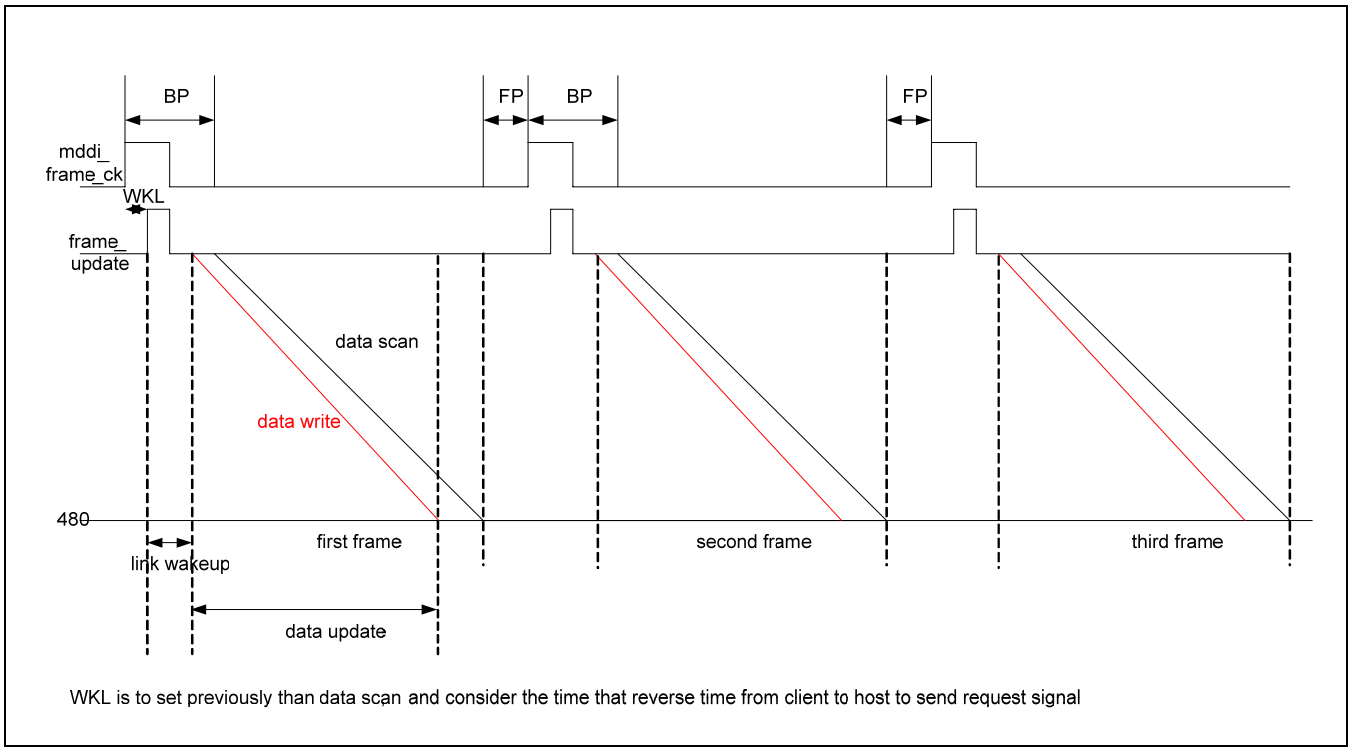


Figure 102 Tearing-Less Display: Data Write Speed is Slower Than Display

B. display speed is faster than data write.

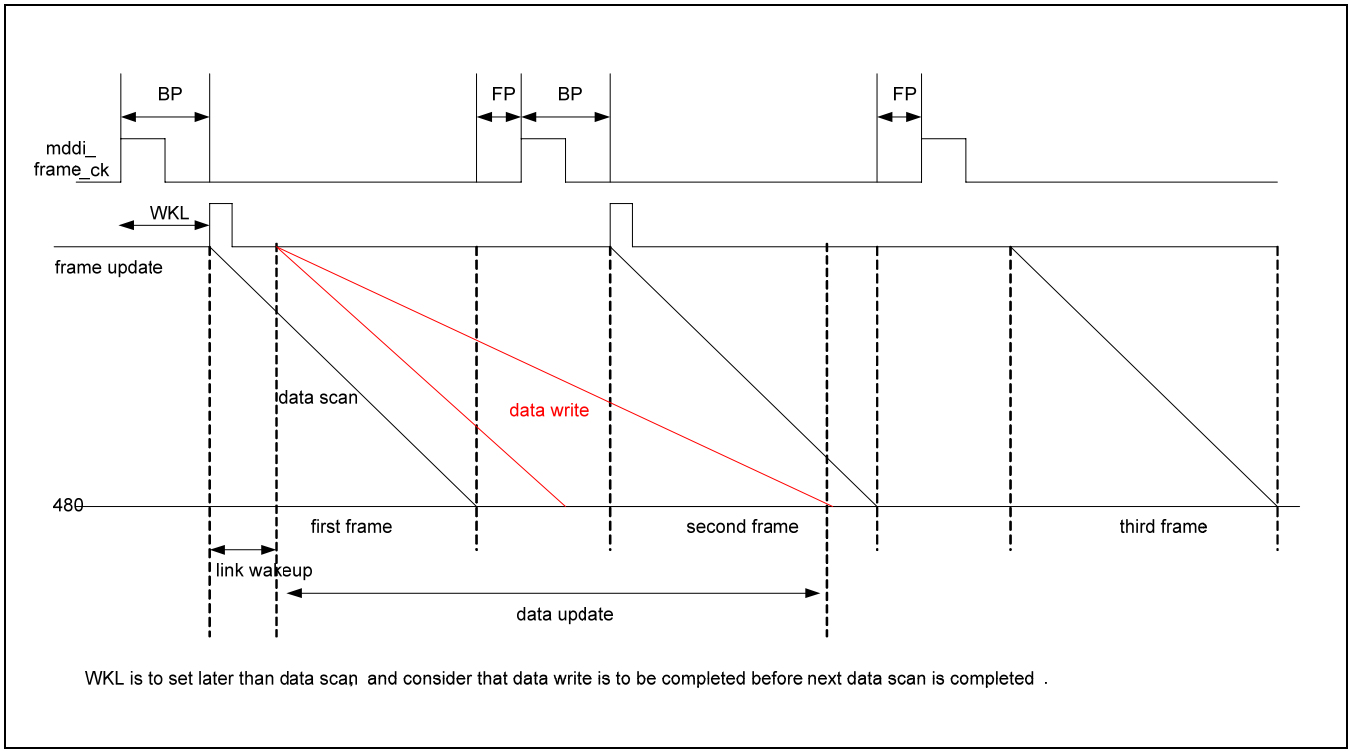


Figure 103 Tearing-Less Display: Display Speed is Faster Than Data Write

3.6.7 HIBERNATION / WAKE-UP

S6D05A1 support hibernation mode to save interface power consumption. MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force MDDI link into hibernation frequently to save power consumption.

During hibernation mode, the hi-speed transmitters and receivers are disabled and the low-speed & low-power receivers are enabled in order to detect wake-up sequence.

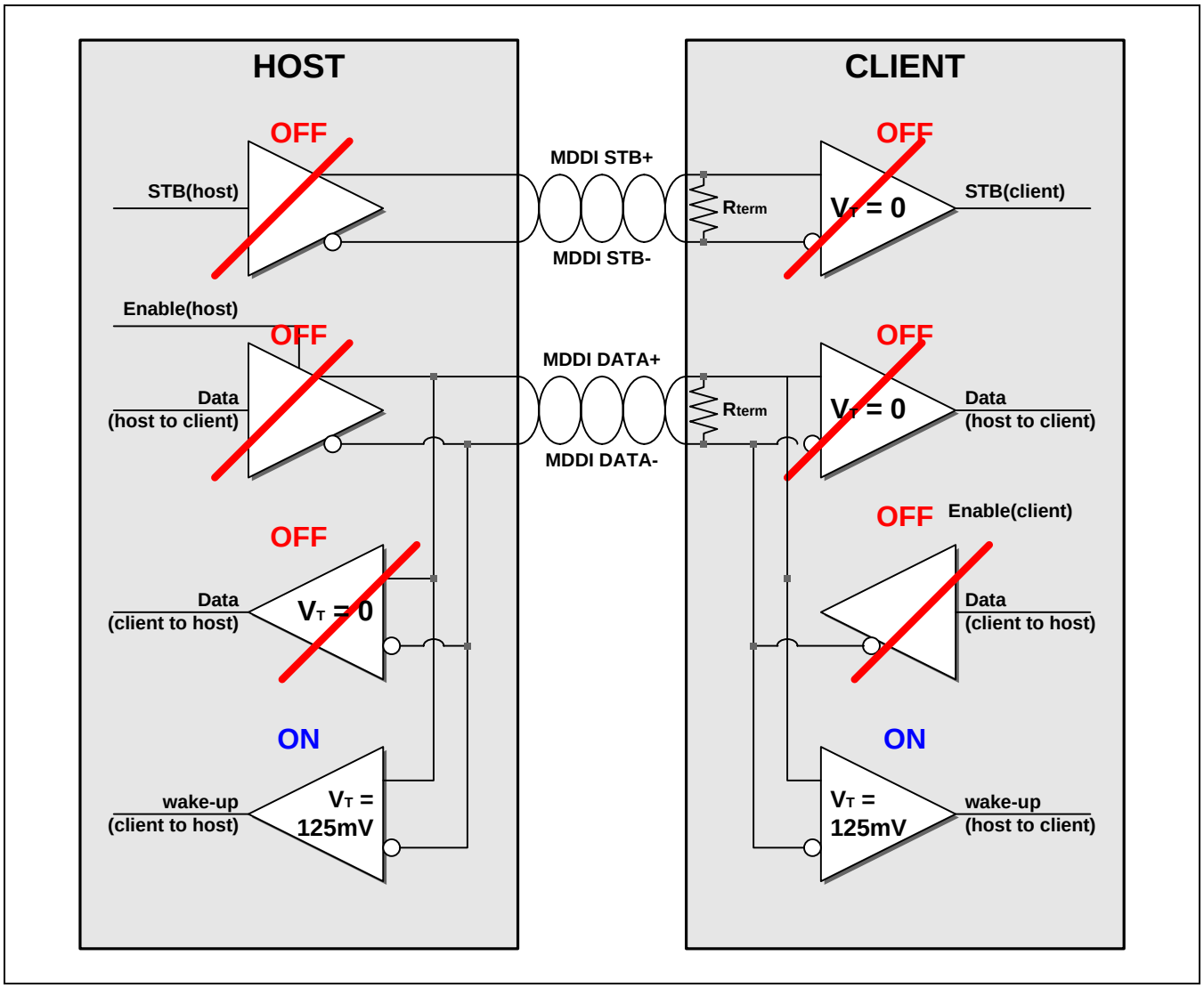


Figure 104 MDDI Transceiver / Receiver State In Hibernation

When the link wakes up from hibernation, the host and client exchange a sequence of pulses. These pulses can be detected using low-speed, low-power receivers that consume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operating speed.

Either the client or the host can wake up the link; Host-initiated link wakeup and Client-initiated link wakeup.

3.6.8 MDDI LINK WAKE-UP PROCEDURE

A. Host-initiated Link Wake-up Procedure

The simple case of a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.

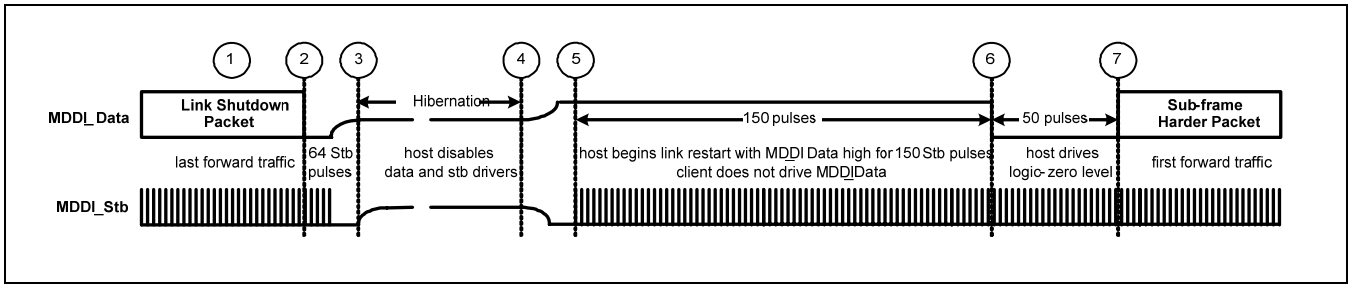


Figure 105 Host-Initiated Link Wake-Up Sequence

The Detailed descriptions for labeled events are as follows:

1. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.
2. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data to a logic-zero level, and then disables the MDDI_Data output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point 3.
3. The host enters the low-power hibernation state by disabling the MDDI_Data and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state.
It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation.
The client is also in the low-power hibernation state.
4. After a while, the host begins the link restart sequence by enabling the MDDI_Data and MDDI_Stb driver outputs. The host drives MDDI_Data to a logic-one level and MDDI_Stb to logic-zero level for at least the time it takes for the drivers to fully enable their outputs.
The host shall wait at least 200n sec after MDDI_Data reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.
5. The host drivers are fully enabled and MDDI_Data is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having logic-zero level on MDDI_Data for duration of 150 MDDI_Stb cycles.
6. The host drives MDDI_Data to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.
7. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point The MDDI host generates MDDI_Stb based on the logic level on MDDI_Data so that proper data-strobe encoding commences from point 7.

B. Client-initiated Link Wake-up Procedure

An example of a typical client-initiated service request event with no contention is illustrated in the following figure.

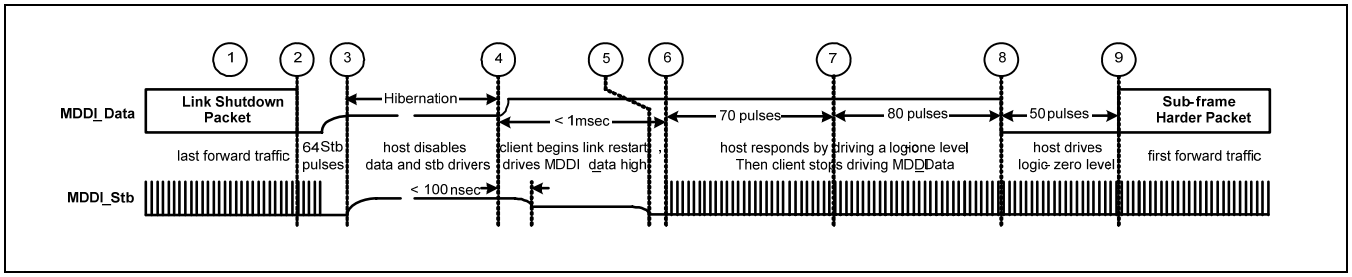


Figure 106 Client-Initiated Link Wake-Up Sequence

The Detailed descriptions for labeled events are as follows:

1. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.
2. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data to a logic-zero level, and then disables the MDDI_Data output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point 3.
3. The host enters the low-power hibernation state by disabling its MDDI_Data and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.
4. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logical-zero level in the client before the host enables its MDDI_Stb driver. The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client. After that, the client enables its MDDI_Data driver while driving MDDI_Data to a logic-one level. It is allowed for MDDI_Data and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200n sec.
5.Within 1m sec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_Data and MDDI_Stb driver outputs. The host drives MDDI_Data to a logic-one level and MDDI_Stb to a logical-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200n sec after MDDI_Data reaches a valid logic-one level and MDDI_Stb reaches a valid fully-

driven logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

6. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data at a logic-one level for a total duration of 150 MDDI_Stb pulses through point 8. The host generates MDDI_Stb in a manner consistent with sending a logical-zero level on MDDI_Data. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.

7. The client continues to drive MDDI_Data to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data driver at point 7. The host continues to drive MDDI_Data to a logic-one level for duration of 80 additional MDDI_Stb pulses, and at point 8 drives MDDI_Data to logic-zero level.

8. The host drives MDDI_Data to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

9. After asserting MDDI_Data to logic-zero level and driving MDDI_Stb for duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point 9 by sending a Sub-frame Header Packet.

The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

3.6.9 CLIENT-INITIATED LINK WAKE-UP

S6D05A1 supports VSYNC based client-initiated link wake-up. As client-initiated wake-up action is executed in hibernation state only, the register setting for wake-up have to be set before link shut-down.

A. VSYNC Based Link Wake-up

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register (EAh: VWAKE_EN) is set, client initiated wake-up is executed in synchronization with the vertical-sync signal which generated in S6D05A1. Using VSYNC based link wake-up, tearing-less display can be accomplished if interface speed and wake-up time is well known.

The following figure shows detailed timing for VSYNC based link wake-up.

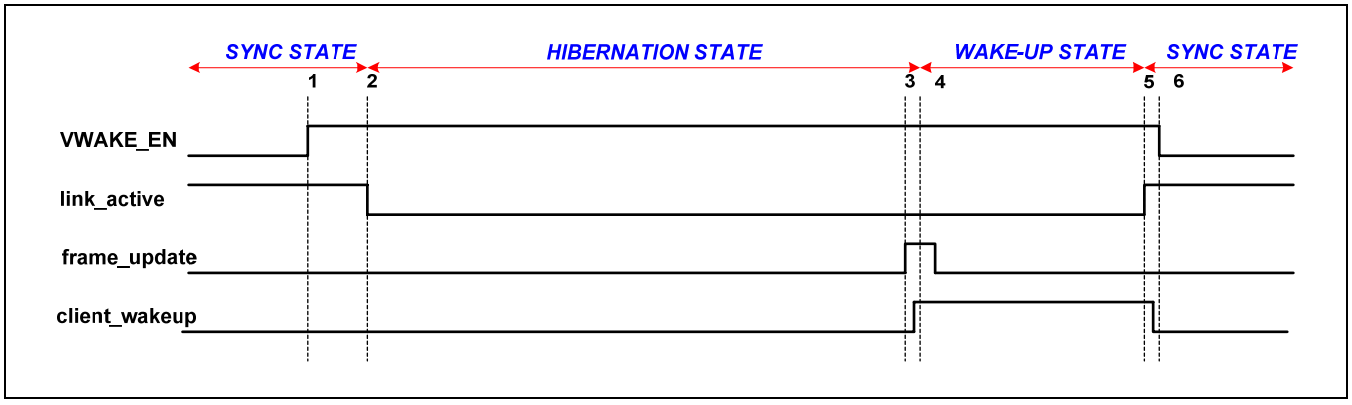


Figure 107 VSYNC Based Link Wake-Up Procedure

The Detailed descriptions for labeled events are as follows:

1. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.
2. Link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the S6D05A1.
3. Frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up can be set using WKF and WKL (E1h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.
4. Client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.
5. Link_active goes high after the host brings the link out of hibernation.
6. After link wake-up, client_wakeup signal and the VWAKE_EN register are cleared automatically.

3.6.10 MDDI OPERATION

In MDDI, six operation modes are available. The following table describes six modes.

Table 70 MDDI Opreration State

STATE	OSC	Booster circuit	Internal logic status	MDDI I/O	Wake-up by
INIT_HIBER	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link hibernation	Hibernation driver ON	Host – Initiated
WAIT	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
NORMAL	ON	Enabled	Display ON /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
SLEEP	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link in SYNC	standard driver ON	-
HIBER	ON	Enabled	Display ON /Internal Logic ON MDDI Link hibernation	Hibernation driver ON	Host – Initiated Client –Initiated (VSYNC)
STOP	OFF	Disabled	Display OFF /Internal Logic ON MDDI Link OFF	Driver All OFF	RESET

INIT_HIBER: Initial status when external power is connected to the IC. In this state, internal oscillator is OFF, and MDDI link is in hibernation state. As no command or signal is applied to the IC except RESET input and booster circuit is OFF, and internal logic is ON.

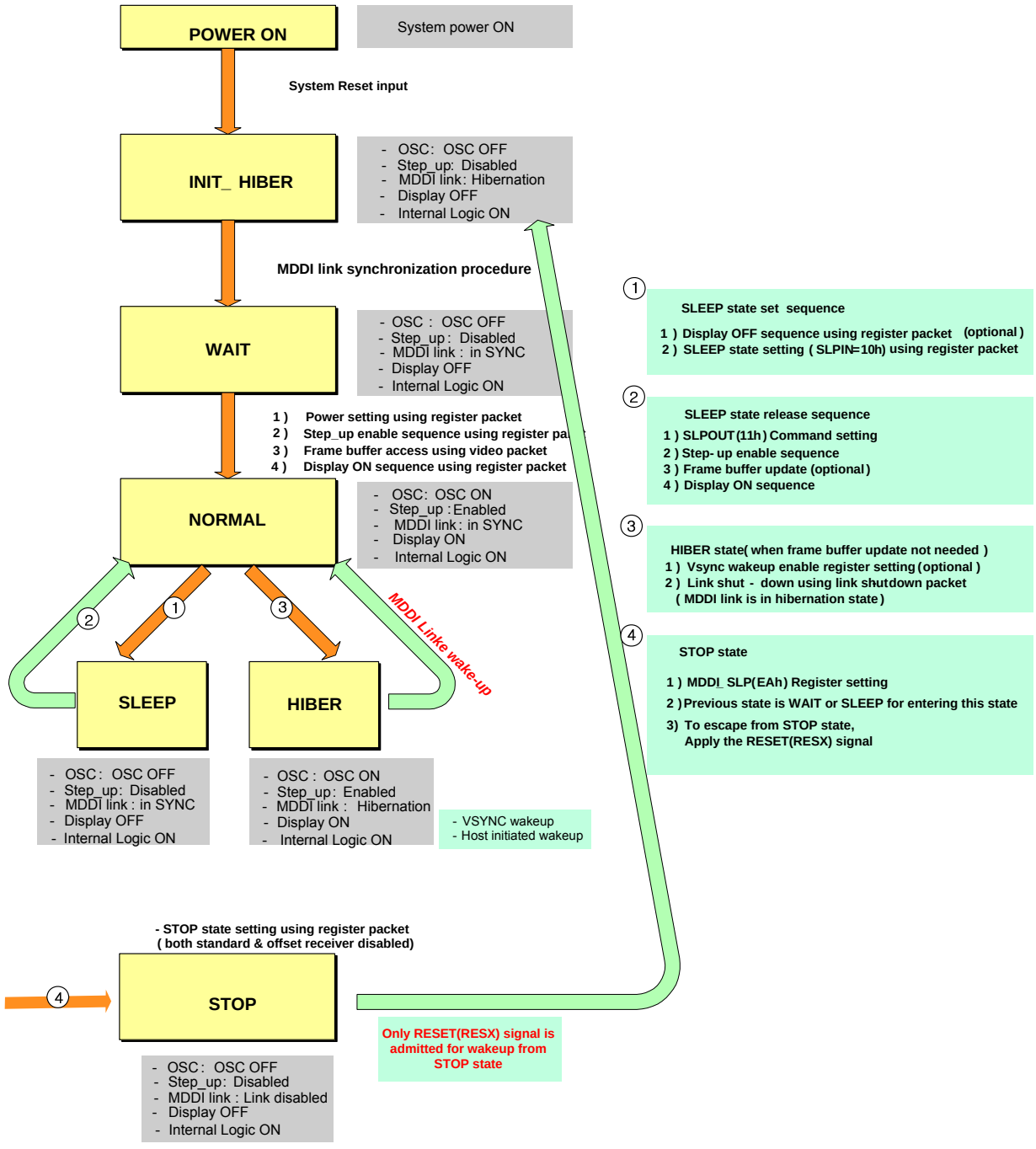
WAIT: After the wake-up sequence, the IC is in WAIT state. MDDI link is in SYNC, and internal logic is ON, and booster is still OFF because no other register access or video stream packet is transferred to the IC.

NORMAL: MDDI link, booster circuit, and internal logic circuit are ON. Register access or Video data transfer is available in NORMAL state.

HIBER: When no more video data update is needed, MDDI link is in hibernation so that interface power can be reduced. Internal booster & logic circuits are still operating. MDDI link wakeup will be accomplished when VSYNC wakeup register is set before hibernation

SLEEP: This state is set by register access. Booster is OFF, but MDDI link is ON. MDDI link and internal logic have to be in SYNC because the IC must receive commands for power save or normal operation

STOP: STOP state is set by MDDI_SLP register access (EAh). In this state, MDDI link, internal oscillator, Boosters are all OFF. But internal logic is still ON. To release STOP state, input reset signal. After reset, status is INIT_HIBER state.



NOTE: Deep Standby Mode -> MDDI mode enter "STOP" mode and Logic Power is off

Figure 108 Operating State in MDDI Mode

3.7 MIPI D-PHY

3.7.1 FEATURES

- ***Data Lanes***
  - HS(High Speed) Transmission (Unidirectional) : up to 500Mbps/lane under one data lane mode
  - LP(Low Power) Transmission (Bidirectional) : up to 10Mbps
  - Both Video and Command modes are supported
  - TE(Tearing Effect) Signaling is supported
  - Diagnostic function – checksum and two bit ECC error monitoring
  - Functionality supported by Escape mode
  - Clock Lane supports ULPS
  - Packet-Based Protocol
  - D-PHY version 0.90
  - DSI version 1.01 r11

3.7.2 GLOBAL OPERATION

MIPI PHY Global Operation*Figure 109* shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround and Initialization

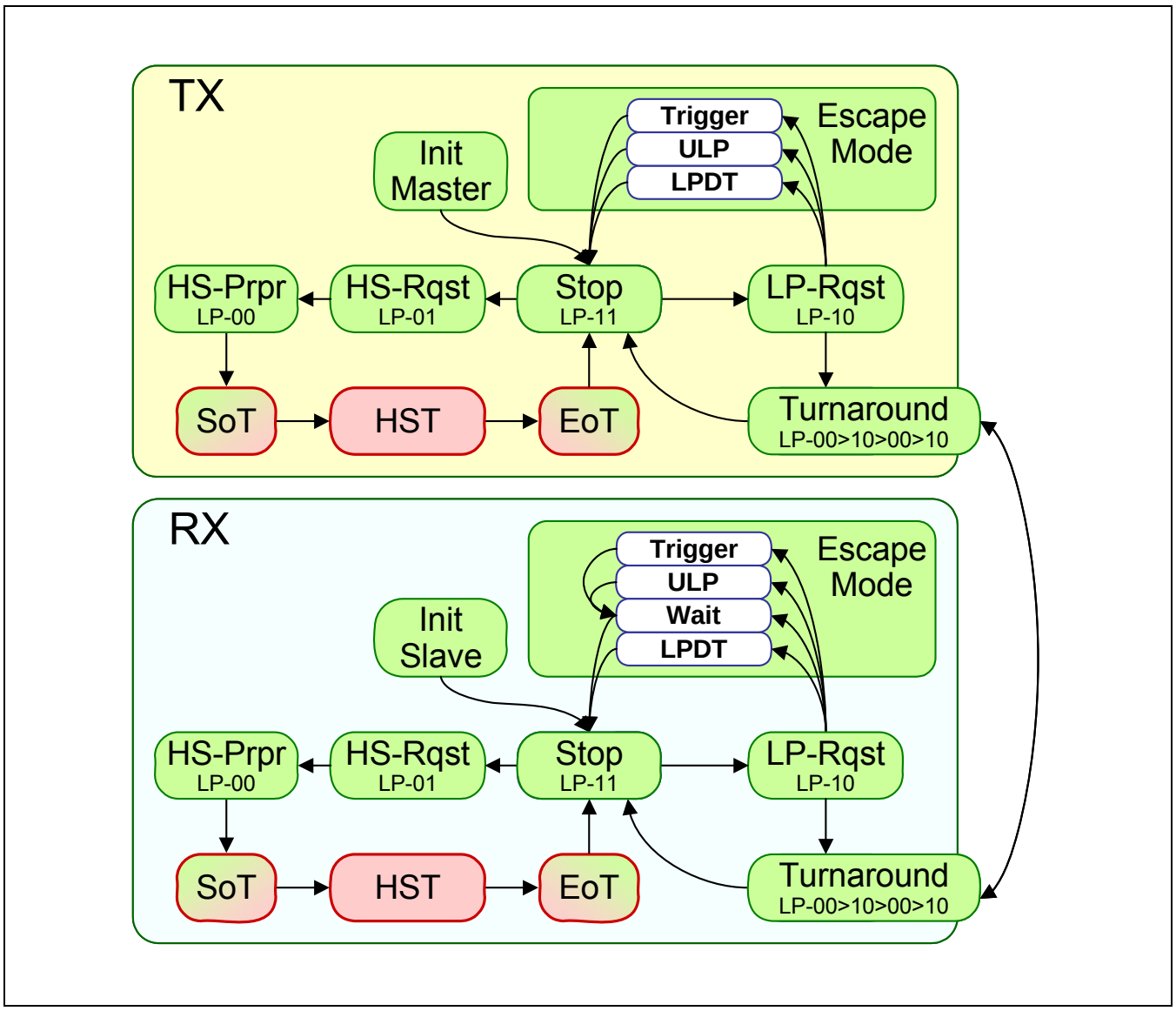


Figure 109 MIPI PHY Global Operation

3.7.3 LANE STATE

Table 71 MIPI Lane State Table

State Code	Line Voltage Levels		High-Speed Burst Mode	Low-Power	
	Dp-Line	Dn-Line		Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

3.7.4 CLOCK LANE FLOW DIAGRAM

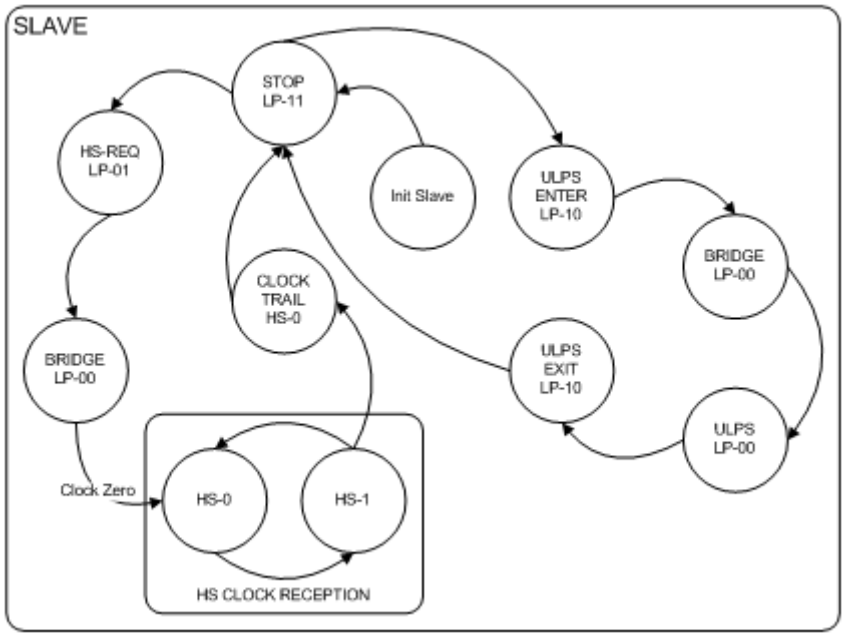


Figure 110 Clock Lane Module Flow Diagram

3.7.5 HIGH SPEED DATA TRANSMISSION

The following figure shows the sequence of the high speed data transmission including SoT data.

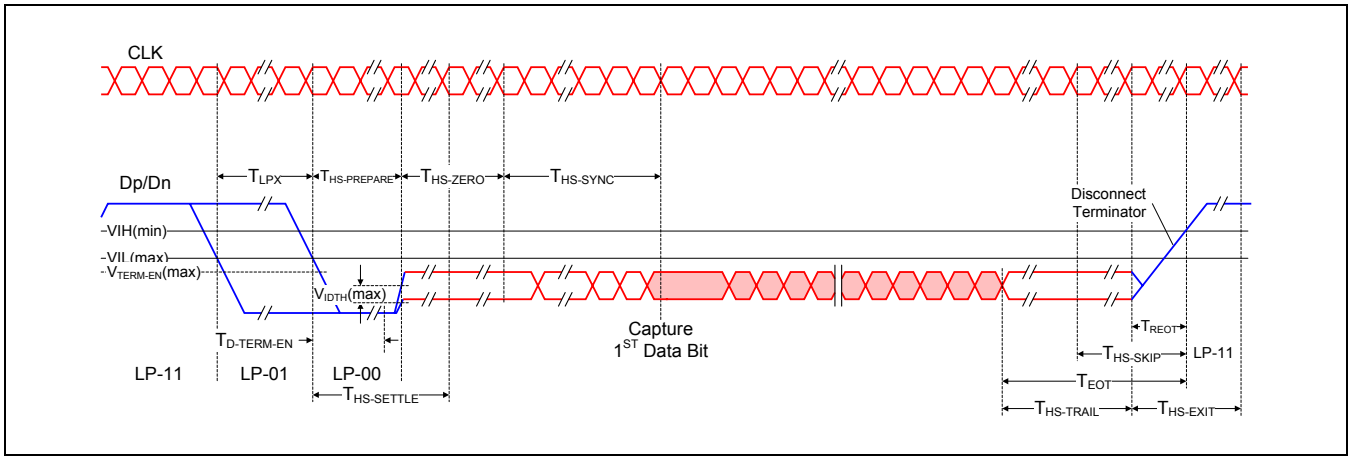


Figure 111 High-Speed Data Transmission in Bursts

3.7.6 HIGH SPEED CLOCK TRANSMISSION

The following figure shows the sequence of the high speed clock transmission. In high speed mode the clock lane provides a low-swing differential DDR clock signal from Master to Slave for high speed data transmission.

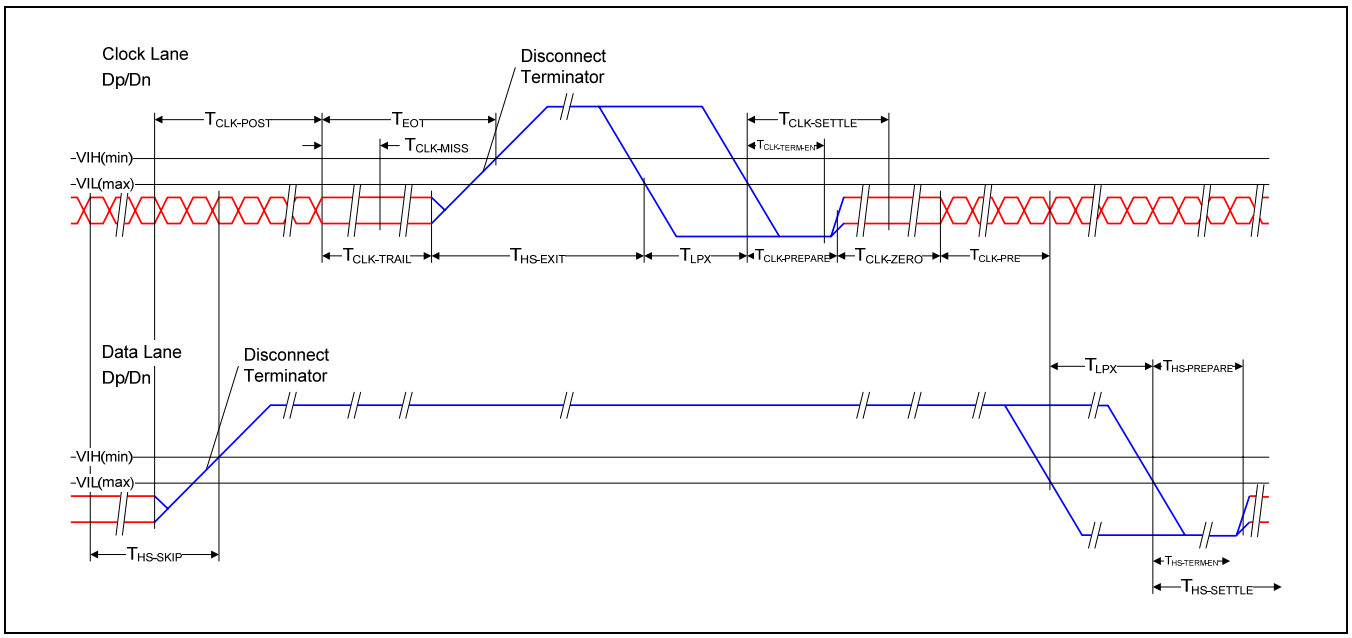


Figure 112 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

3.7.7 ESCAPE MODE

Escape Mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Though Escape Mode operation is optional in D-PHY, the host processor and peripheral in which Command Mode operation is supported shall implement reverse-direction Escape Mode as well as forward direction Escape Mode.
A Data Lane shall enter Escape Mode via an Escape Mode Entry procedure (LP-11,LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape Mode in Space state (LP-00). If an LP-10 is detected after the first Bridge state or an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape Mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.
Once Escape Mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. 0 lists all currently available Escape Mode commands and actions. All unassigned commands are reserved for future expansion

Table 72 MIPI Escape Mode Entry Code

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)	S6D05A1	
			LP–RX	LP–TX
Low-Power Data Transmission	Mode	11100001	O	O
Ultra-Low Power State	Mode	00011110	O	-
Undefined-1	Mode	10011111	-	-
Undefined-2	Mode	11011110	-	-
Reset-Trigger [Remote Application]	Trigger	01100010	-	-
Unknown-3 [TE Trigger]	Trigger	01011101	-	O
Unknown-4 [Acknowledge Trigger]	Trigger	00100001	-	O
Unknown-5	Trigger	10100000	-	-

3.7.8 LOWER POWER DATA LANE OPERATION

The following figure shows the sequence of the low power data transmission. The Escape mode uses the spaced one hot bit encoding for asynchronous communication.

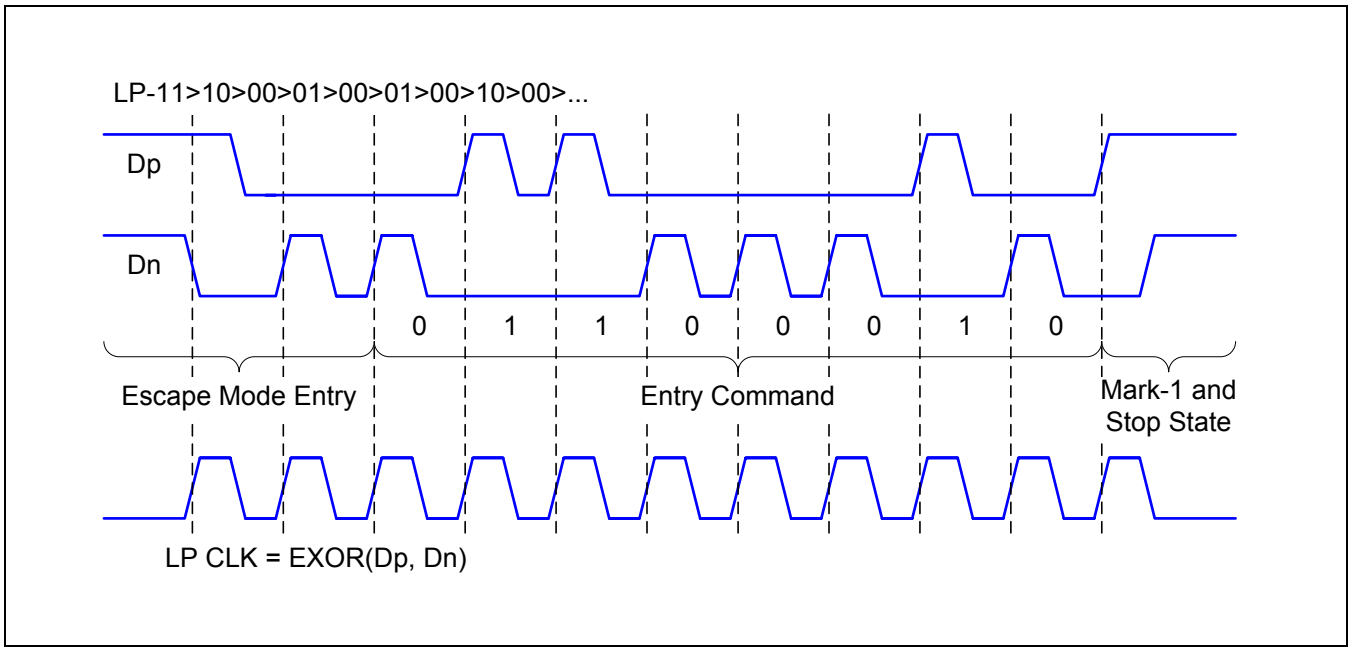


Figure 113 Trigger-Reset Command in Escape Mode

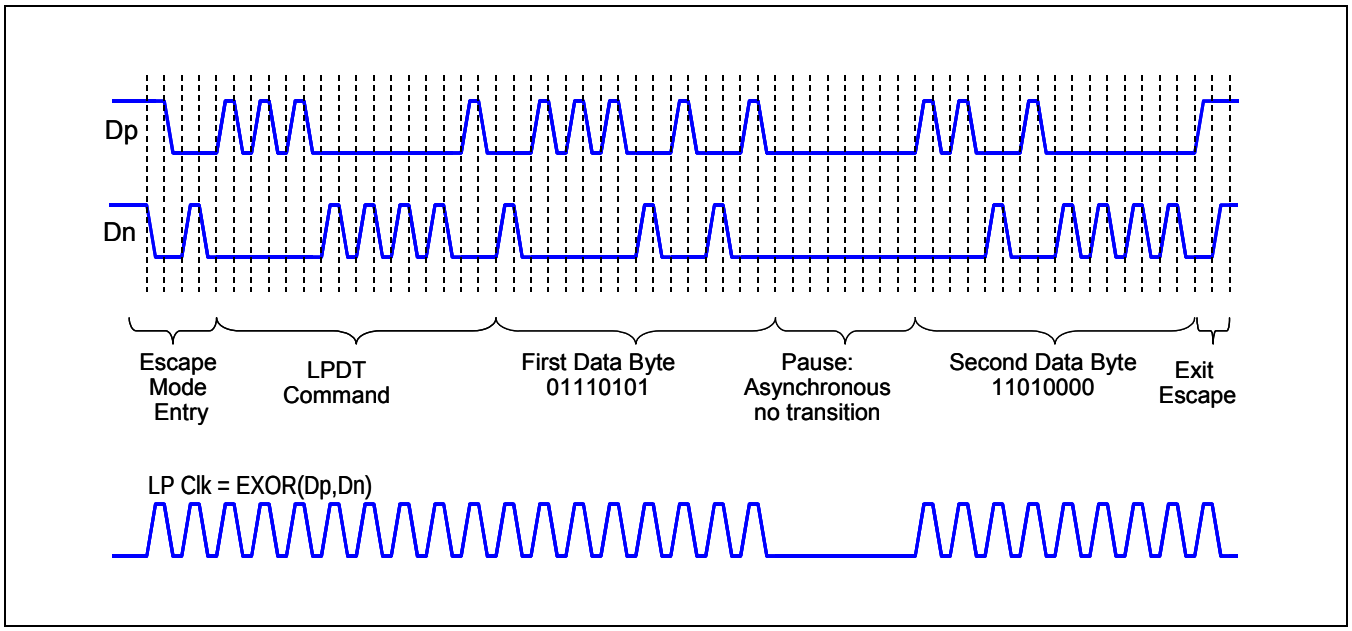


Figure 114 Low Power Data Transmission

3.7.9 ULTRA-LOW POWER STATE

If the Ultra Low Power Entry Command is sent after an Escape Mode Entry command, the Lane shall enter the Ultra Low Power State (ULP). This Command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop State. *Figure 115* shows an Ultra Low Power Entry and Exit example.

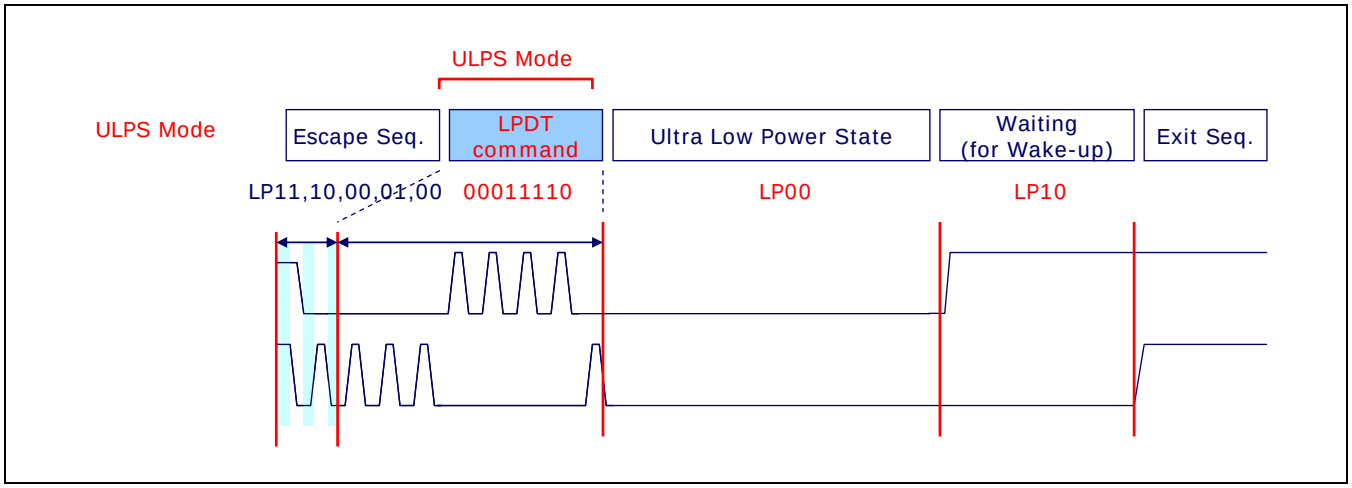


Figure 115 Ultra Low Power State Mode

The Host processor provides LP10 state before Exit to wait for the MIPI SLAVE's stabilization. ULPS packet turn off the PHY_IO HS_RX. The ULPS turn off the bias current of HS_RX. The LP10 wakeup state is a trigger to turn on the HS_RX before normal STOP state.

3.7.10 REMOTE APPLICATION RESET

Remote Application Reset Command is used in case of transmission from the host processor to the peripheral. If the Entry Command Pattern matches the Remote Application Reset Command a Trigger is flagged to the protocol at the peripheral side via the logical PPI.

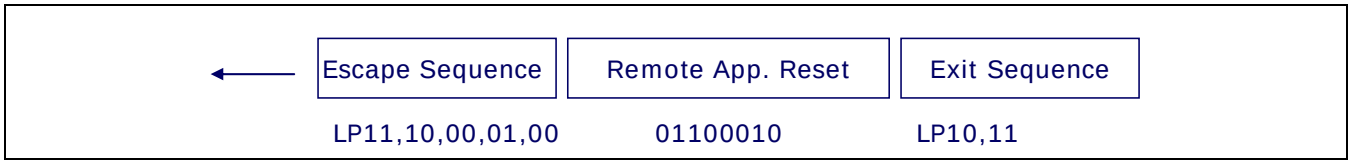


Figure 116 Remote Application Reset Packet

Figure 116 shows MIPI remote application reset packet using LP mode. The host processor can send software reset trigger by Remote Application Reset Packet.

3.7.11 TE SIGNALING

A Command Mode display module has its own timings controller and local frame buffer for display refresh. In some cases the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bi-directional Data Lane.

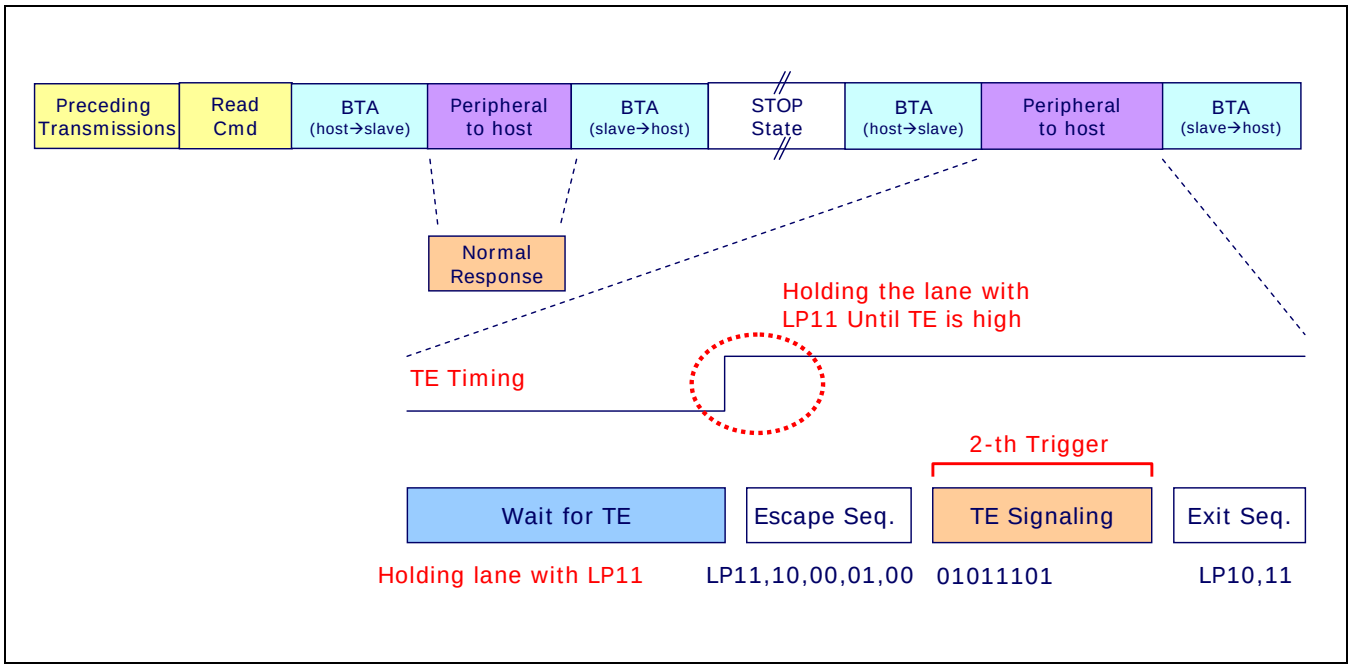


Figure 117 BTA Mode - TE Signaling

The PHY for DSI has no inherent interrupt capability from peripheral to host processor so the host processor shall give bus ownership to the peripheral for extended periods, as it does not know when the peripheral will send the TE message.
Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or request to the display module, because it does not have bus possession. *Figure 117* shows the TE signaling Response procedure.
The TE Signaling function is enabled and disabled by three DCS commands to the display module's controller: set_tear_on, set_tear_off. After sending set_tear_on to enable this function, the host processor ends the transmission with BTA asserted, giving bus possession to the display module. Since the display module's DSI protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession. To enable TE Reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE Signaling has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) BTA signal to its PHY functional block. The PHY layer will then initiate a BTA sequence in LP mode, which gives bus possession to the display module.

3.7.12 BI-DIRECTIONAL DATA LANE TURNAROUND

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. *Figure 118* shows the BTA procedure graphically.

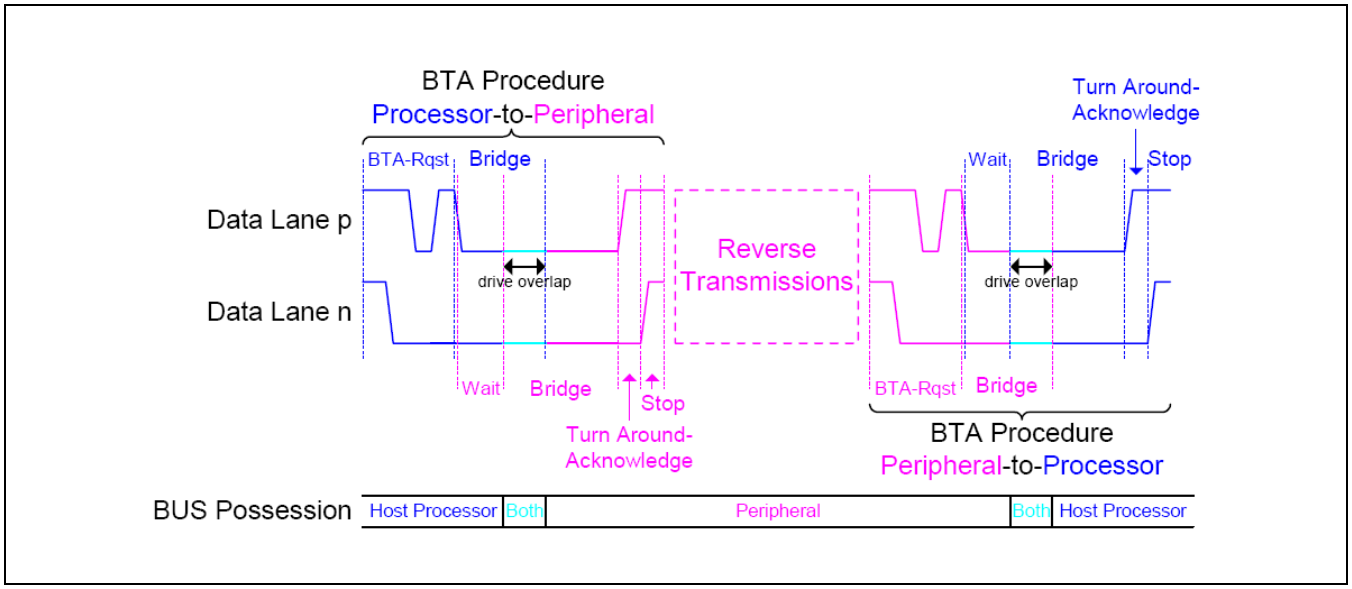


Figure 118 Bus Turn Around Mode

The low power clock timing for both sides of the Link does not have to be the same, but may differ. However, the ratio between the Low Power State Periods, TLPX, is constrained to ensure proper Turnaround behavior. The TLPX(master)/TLPX(slave) shall be between 2/3 (0.667) and 3/2 (1.50). The handshake process for BTA allows only limited mismatch of Escape Mode clock frequencies between a host processor and a peripheral.

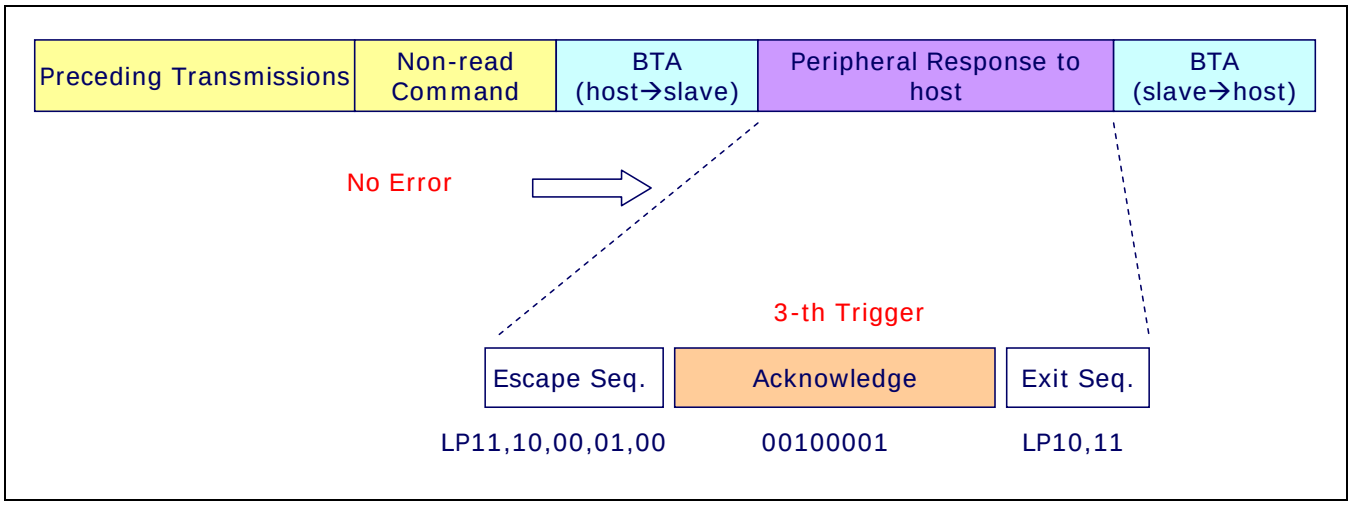


Figure 119 Bta Mode – No Error After Non–Read Command

Figure 119 shows an example of BTA after non-read command. The SLAVE get the lane controllability by BTA procedure to send the acknowledge packet on the successful data reception.

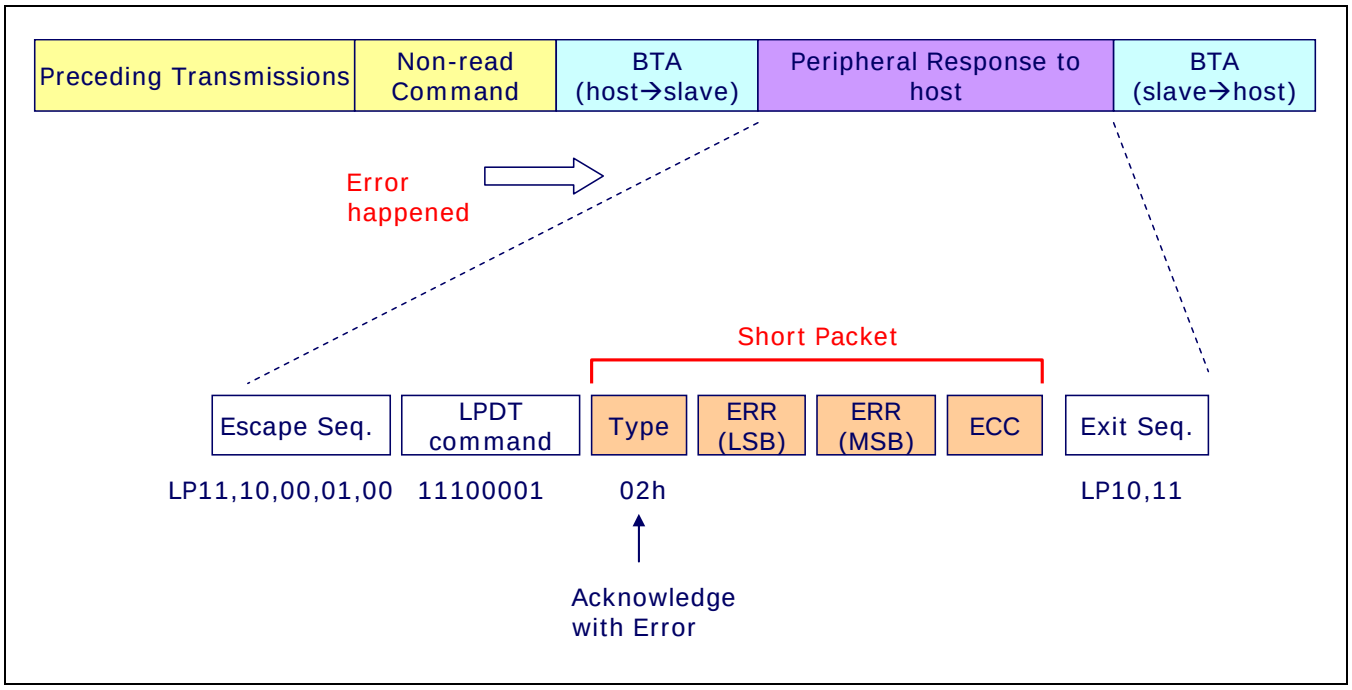


Figure 120 BTA Mode – Error Happened After Non-Read Command

Figure 120 shows an example of BTA after non-read command. The SLAVE gets the lane controllability by BTA procedure to send the acknoledge with error packet on the data reception error.

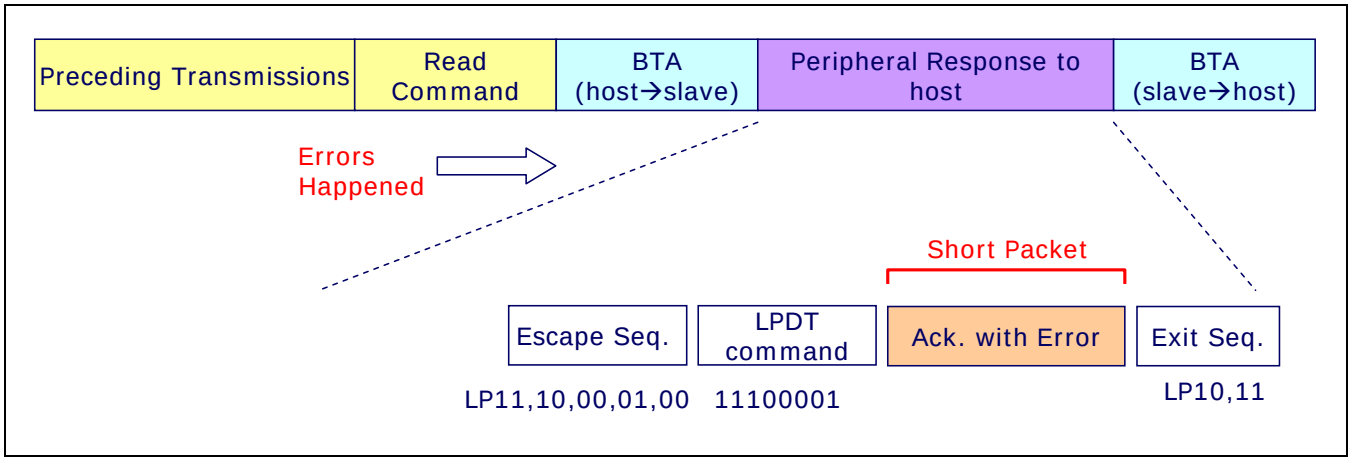


Figure 121 BTA Mode - Error Happened After Read Command

Figure 121 shows an example of BTA after-read command. The SLAVE gets the lane controllability by BTA procedure to send the acknoledge with error packet on the data reception error.

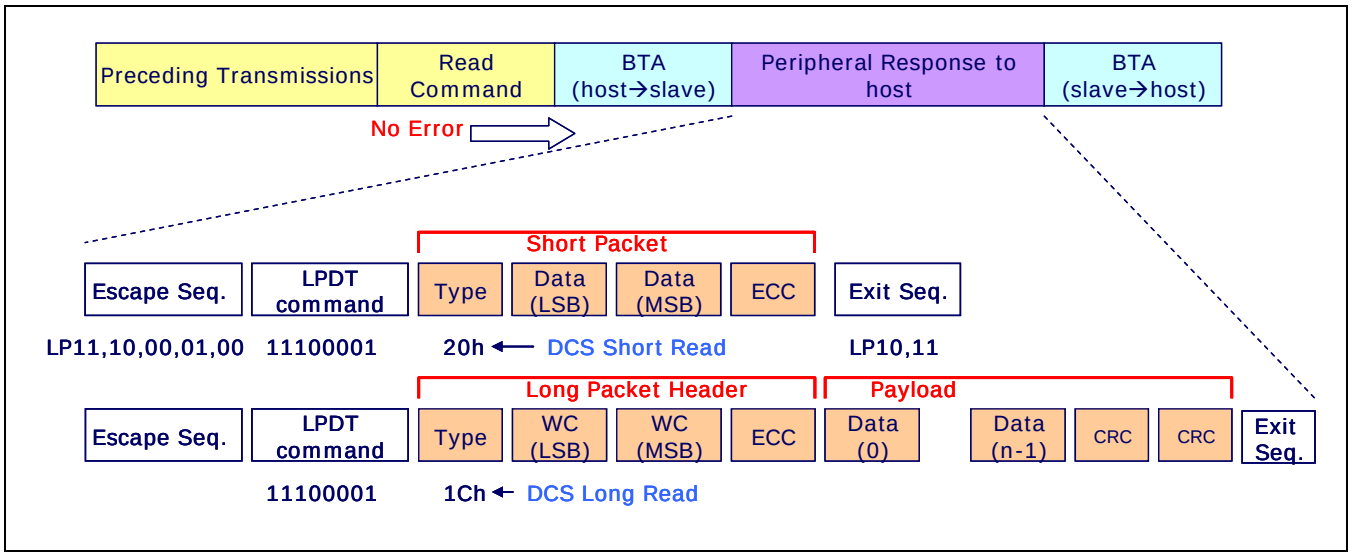


Figure 122 BTA Mode - No Error After Read Command

Figure 122 shows an example of BTA after read command. The SLAVE gets the lane controllability by BTA procedure to send readed data packet on the successful data reception.

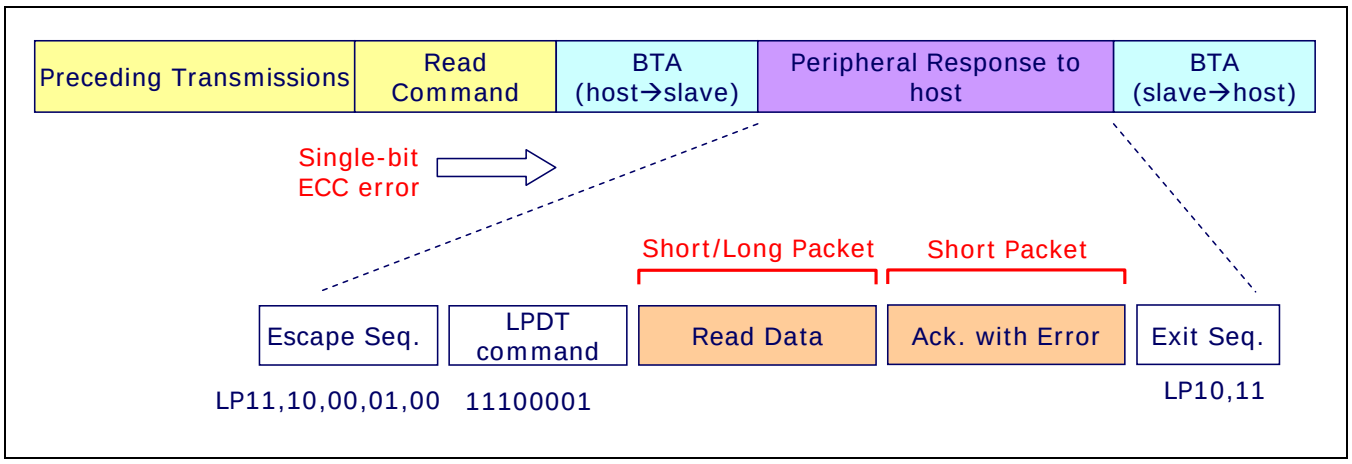


Figure 123 BTA Mode - One Bit Error After Read Command

Figure 123 shows an example of BTA after read command. The SLAVE gets the lane controllability by BTA procedure to send readed data packet and acknowledge with error on the one bit error.

3.7.13 GLOBAL OPERATION TIMINGS

This section specifies global operation timings of the MIPI Interface. Detailed timing specifications are in *Table 73*

3.7.13.1 Global Operation Timing Parameters

0 lists the ranges for all timing parameters used in this section. The values in the table require a clock tolerance no worse than ±10% for implementation.

Table 73 Global Operation Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Detection time that the clock has stopped toggling			60	ns	1
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode	60 ns + 52*UI			ns	2
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8			UI	
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	50		140	ns	
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			ns	
$T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	390			ns	
T_{EOT}	Time from start of THS-TRAIL or TCLK-TRAIL period to start of LP-11 state			105 ns + n*12*UI	ns	4
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			ns	
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns	
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	THS-PREPARE + Time to drive HS-0 before the Sync sequence	145 ns + 10*UI			ns	
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40		55 ns + 4*UI	ns	
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max(n*8* UI, 60 ns + n*4*UI)			ns	3, 4
T_{INIT}	Initialization period	100			µs	
T_{LPX}	Length of any low-power state period	50	100		ns	5
Ratio T_{LPX}	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2		
T_{TA-GET}	Time to drive LP-00 by new TX	5*TLPX			ns	

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{TA-GO}	Time to drive LP-00 after turnaround request	4*TLPX			ns	
$T_{TA-SURE}$	Time-out before new TX side starts driving	TLPX		2*TLPX	ns	

NOTE:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. UI is the instantaneous unit interval.
3. If a] b then max (a, b) = a otherwise max (a, b) = b
4. Where n = 1 for Forward-direction HS mode and n = 4 for reverse-direction HS mode
5. TLPX is an internal state machine timing reference.
   Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

3.8 MIPI DSI

3.8.1 MULTIPLE PACKETS PER TRANSMISSION

The MIPI CORE of S6D05A1 supports two data transmission defined in MIPI DSI specification.
And in order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp packet can be enabled or disabled with register.

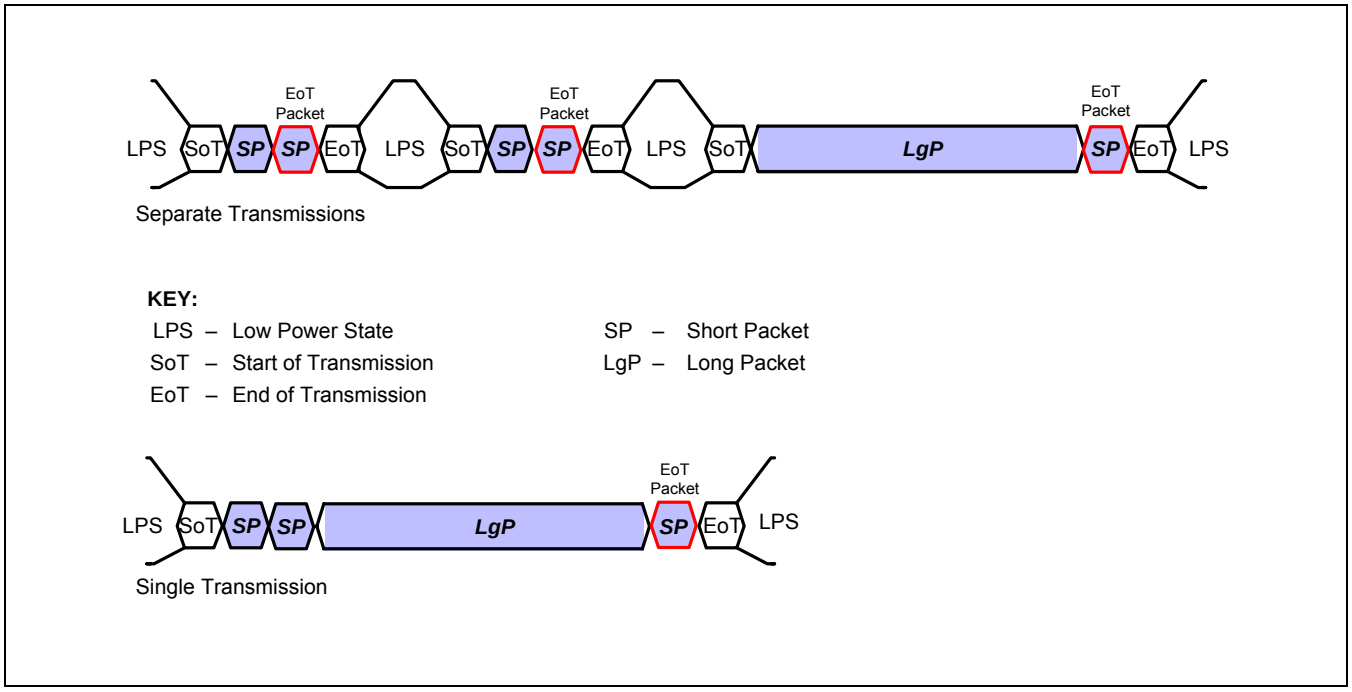


Figure 124 Two Data Transmission Mode (Single, Separate) with EOTp

3.8.2 GENERAL PACKET STRUCTURE

Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier is always the first byte of the packet.

3.8.2.1 Long Packet Format

See “8.4.1 Long Packet Format” in “MIPI Alliance Standard for DSI”

3.8.2.2 Short Packet Structure

See “8.4.2 Short Packet Format” in “MIPI Alliance Standard for DSI”

3.8.3 COMMON PACKET ELEMENT

Long and Short packets have several common elements
See “8.5. Short Packet Format” in “MIPI Alliance Standard for DSI”

3.8.4 ENDIAN POLICY

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

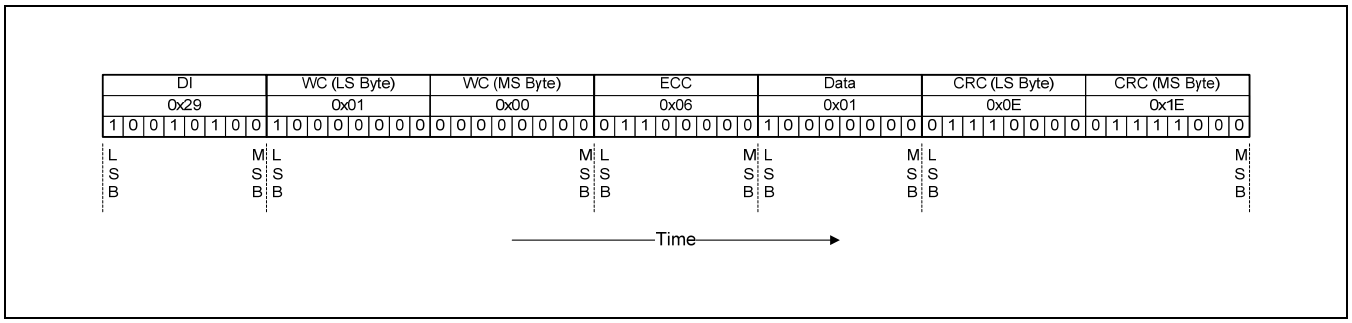


Figure 125 Endian Example (Long Packet)

3.8.5 DATA TYPE COMMAND TABLE

Table 74 Data Types for Processor-Sourced Packets

Data Type,		Description	Packet Size	DCS	VD PKT	GN PKT
Hex	Binary					
01h	00 0001	Sync Event, V Sync Start	Short		O	
11h	01 0001	Sync Event, V Sync End	Short		O	
21h	10 0001	Sync Event, H Sync Start	Short		O	
31h	11 0001	Sync Event, H Sync End	Short		O	
08h	00 1000	End of Transmission Packet	Short	O	O	O
02h	00 0010	Color Mode (CM) Off Command	Short			
12h	01 0010	Color Mode (CM) On Command	Short			
22h	10 0010	Shut Down Peripheral Command	Short			
32h	11 0010	Turn On Peripheral Command	Short			
03h	00 0011	Generic Short WRITE, no parameters	Short			NOP
13h	01 0011	Generic Short WRITE, 1 parameter	Short			O
23h	10 0011	Generic Short WRITE, 2 parameters	Short			O
04h	00 0100	Generic READ, no parameters	Short			O
14h	01 0100	Generic READ, 1 parameter	Short			O
24h	10 0100	Generic READ, 2 parameters	Short			NOP
05h	00 0101	DCS WRITE, no parameters	Short	O	O	O
15h	01 0101	DCS WRITE, 1 parameter	Short	O	O	O
06h	00 0110	DCS READ, no parameters	Short	O	O	O
37h	11 0111	Set Maximum Return Packet Size	Short	O	O	O
09h	00 1001	Null Packet, no data	Long	O	O	O
19h	01 1001	Blanking Packet, no data	Long		O	
29h	10 1001	Generic Long Write	Long			O
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long	O	O	O
0Eh	00_1110	Packet Pixel Stream, 16bit RGB 5-6-5 Format	Long		O	
1Eh	01_1110	Packet Pixel Stream, 18bit RGB 6-6-6 Format	Long		O	
2Eh	10_1110	Packet Pixel Stream, 18bit RGB Loosely 6-6-6 Format	Long		O	
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long		O	
x0h&Fh,	×× 0000 ×× 1111	DO NOT USE All unspecified codes are reserved				

Table 75 Data Types for Peripheral-Sourced Packets

Data Type		Description	Packet Size	DCS.	GN PKT
Hex	Binary				
00h–01h	00 000x	Reserved	Short	-	-
02h	00 0010	Acknowledge with Error Report	Short	O	O
03h–07h	00 0011 – 00 0111	Reserved		-	-
08h	00 1000	End of Transmission Packet	Short	O	O
09h–10h	00 1001 – 01 0000	Reserved		-	-
11h	01 0001	Generic Short READ Response, 1-byte returned	Short		O
12h	01 0010	Generic Short READ Response, 2-bytes returned	Short		O
13h–18h	01 0011 – 01 1000	Reserved		-	-
1Ah	01 1010	Generic Long READ Response	Long		O
1Bh	01 1011	Reserved		-	-
1Ch	01 1100	DCS Long READ Response	Long	O	O
1Dh–20h	01 1101 – 10 0000	Reserved		-	-
21h	10 0001	DCS Short READ Response, 1-byte returned	Short	O	O
22h	10 0010	DCS Short READ Response, 2-bytes returned	Short	O	O
23h–28h	10 0011 – 10 1000	Reserved		-	-
29h–3Fh	10 1001 – 11 1111	Reserved		-	-

3.8.6 ERROR REPORT PACKET

Table 76 Error Report Bit Definitions & Implementation

Bit	Description	Implementation
0	SoT Error	O
1	SoT Sync Error	O
2	EoT Sync Error	O
3	Escape Mode Entry Command Error	O
4	Low-Power Transmit Sync Error	O
5	Timeout Error	O
6	False Control Error	O
7	Contention Detection Error	O
8	ECC Error, single-bit (detected and corrected)	O
9	ECC Error, multi-bit (detected, not corrected)	O
10	Checksum Error (Long packet only)	O
11	DSI Data Type Not Recognized	O
12	DSI VC ID Invalid	O
13	Invalid Transmission Length	O
14	Reserved	-
15	DSI Protocol Violation	O

3.8.7 REVERSE TRANSMISSION TIMING DIAGRAM

The MIPI needs BTA procedure to read data from DDI side. The DSI receiver (S6D05A1) gets the ownership of the lane via BTA. The DSI (S6D05A1) receiver starts the low power data transmission for the previous data packet. If the previous packet is read, the S6D05A1 make the read packet including DSI packet header and read data (payload). The entire timing diagram of the read procedure is described in the following figure.

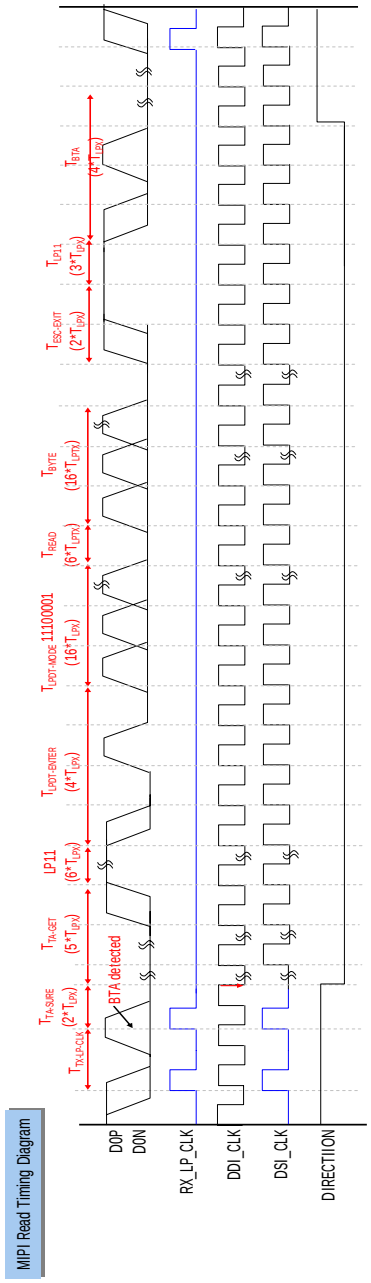


Figure 126 Reverse Transmission Timing Diagram

3.8.8 LINE CONTENTION DETECTION

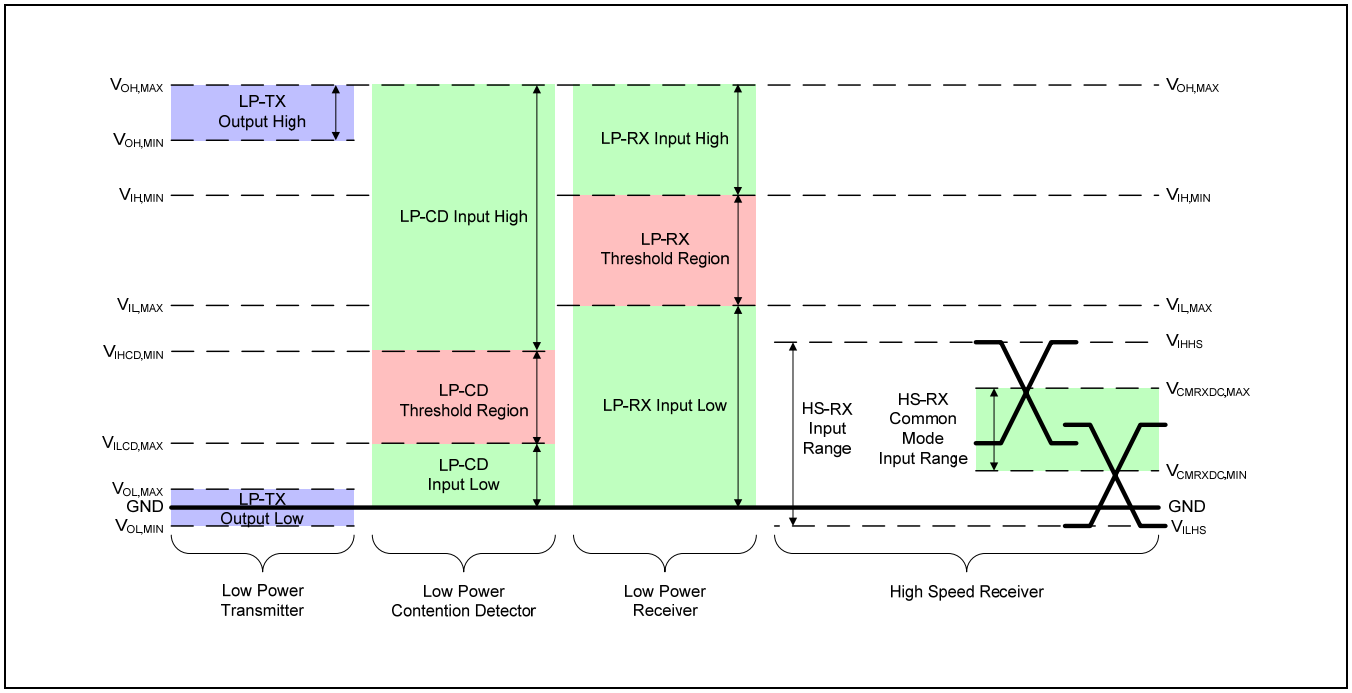


Figure 127 Contention Voltage Levels

The Low-Power receiver and a separate contention detector shall be used in a bi-directional Data Lane to monitor the line voltage on each Low-Power signal. The Low-Power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL. The contention detector shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than VIHCD. An LP low fault shall not be detected when the pin voltage is less than VILCD.

4 FUNCTIONAL DESCRIPTION

4.1 POWER

4.1.1 POWER ON / OFF SEQUENCE

VDD3 and VCI can be applied in any order.
VDD3 and VCI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VCI and VDD3 must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDD3 or VCI can be powered down minimum 0msec after RESX has been released.

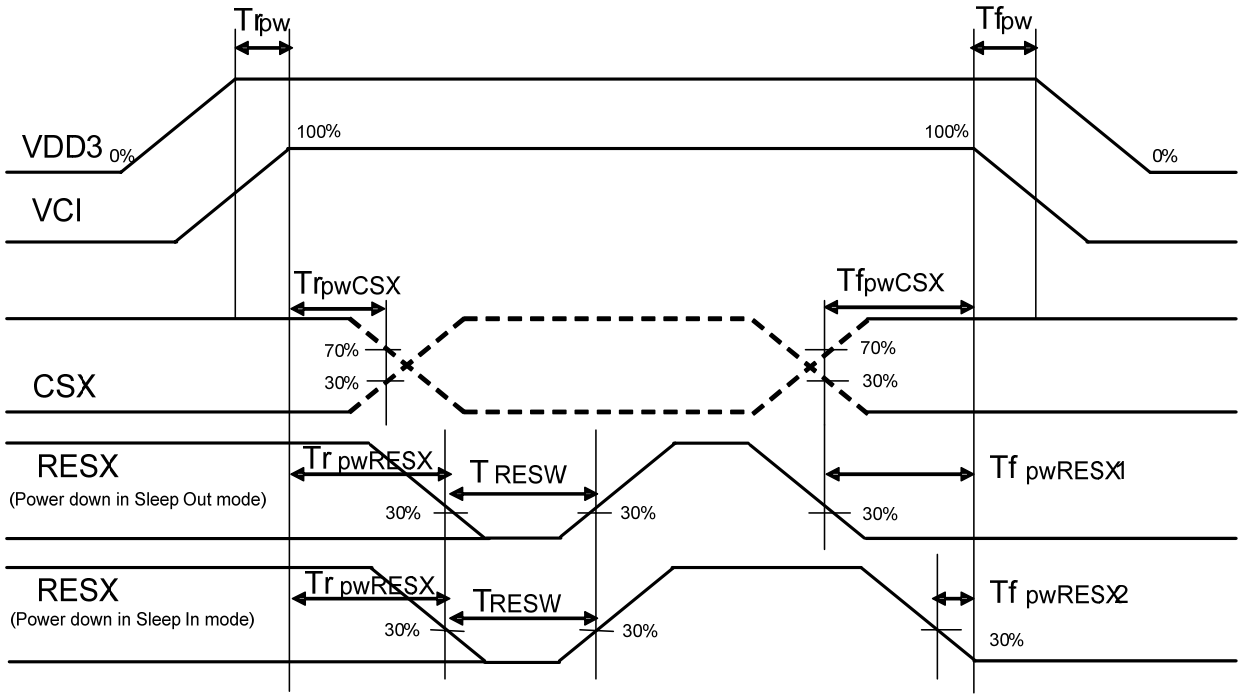
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

NOTE:

There will be damage to the display module if the power sequences are not met.
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
There will be no abnormal visible effects on the display between the end of Power On Sequence and before the reception of Sleep Out command. Same is the case between receiving Sleep In command and Power Off Sequence.
If RESX line is not held stable by host during Power On Sequence, it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

The power on/off sequence is illustrated in the next pages.

4.1.1.1 Case–1, VDD3 Turns on Faster Than VCI and Falls Down Later Than VCI



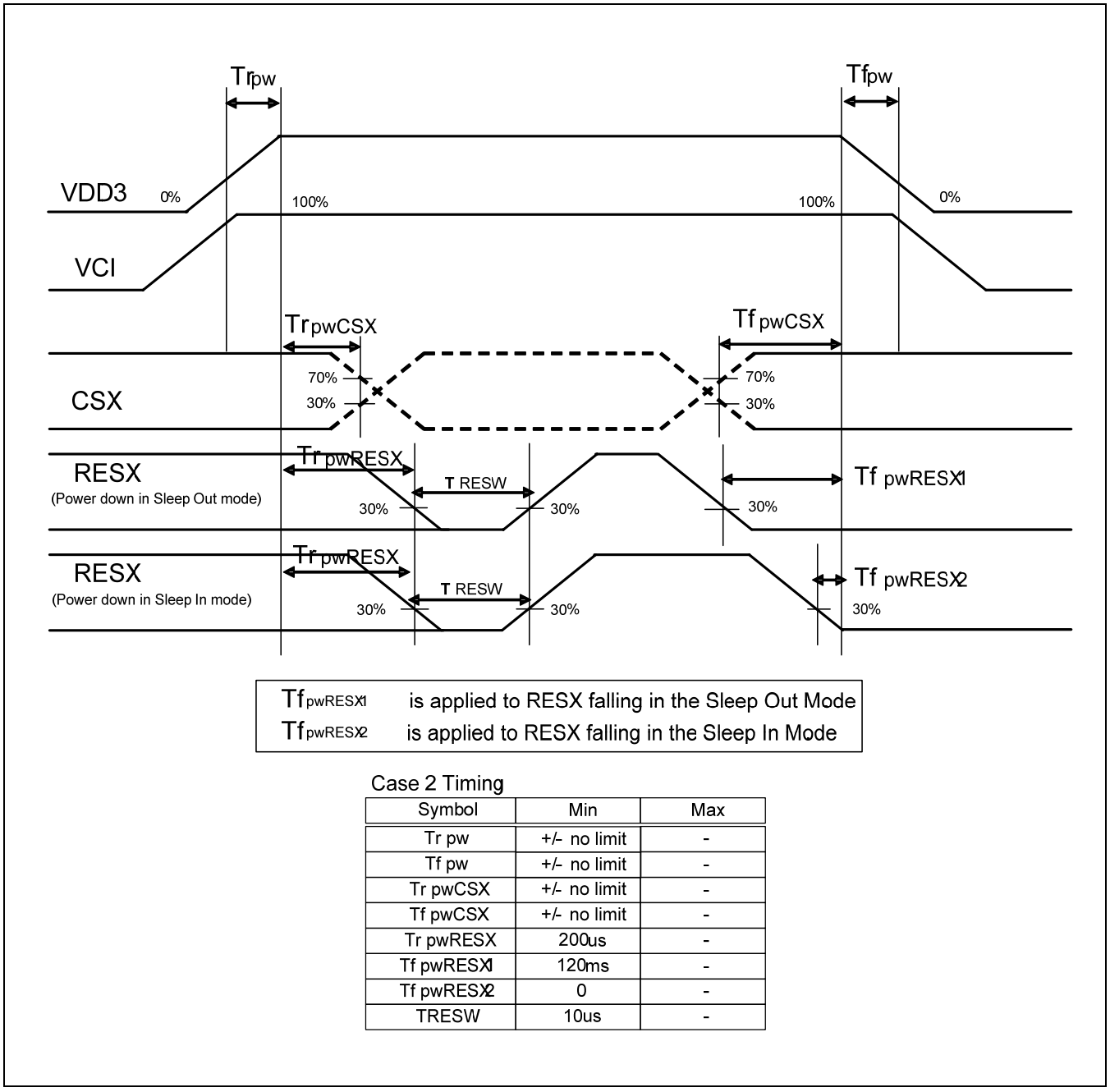
$Tf_{pwRESX1}$	is applied to RESX falling in the Sleep Out Mode
$Tf_{pwRESX2}$	is applied to RESX falling in the Sleep In Mode

Case 1Timing

Symbol	Min	Max
Tr pw	+/- no limit	-
Tf pw	+/- no limit	-
Tr pwCSX	+/- no limit	-
Tf pwCSX	+/- no limit	-
Tr pwRESX	200us	-
Tf pwRESX1	120ms	-
Tf pwRESX2	0	-
TRESW	10us	-

Figure 128 VDD3 Turns On Faster Than VCI and Falls Down Later Than VCI

4.1.1.2 Case-2, VDD3 Turns On later Than VCI and Falls Down Fater Than VCI



Case 2 Timing

Symbol	Min	Max
Tr pw	+/- no limit	-
Tf pw	+/- no limit	-
Tr pwCSX	+/- no limit	-
Tf pwCSX	+/- no limit	-
Tr pwRESX	200us	-
Tf pwRESX1	120ms	-
Tf pwRESX2	0	-
TRESW	10us	-

Figure 129 VDD3 Turns On Later Than VCI and Falls Down Faster Than VCI

4.1.1.3 VDD3 – RESX Timing

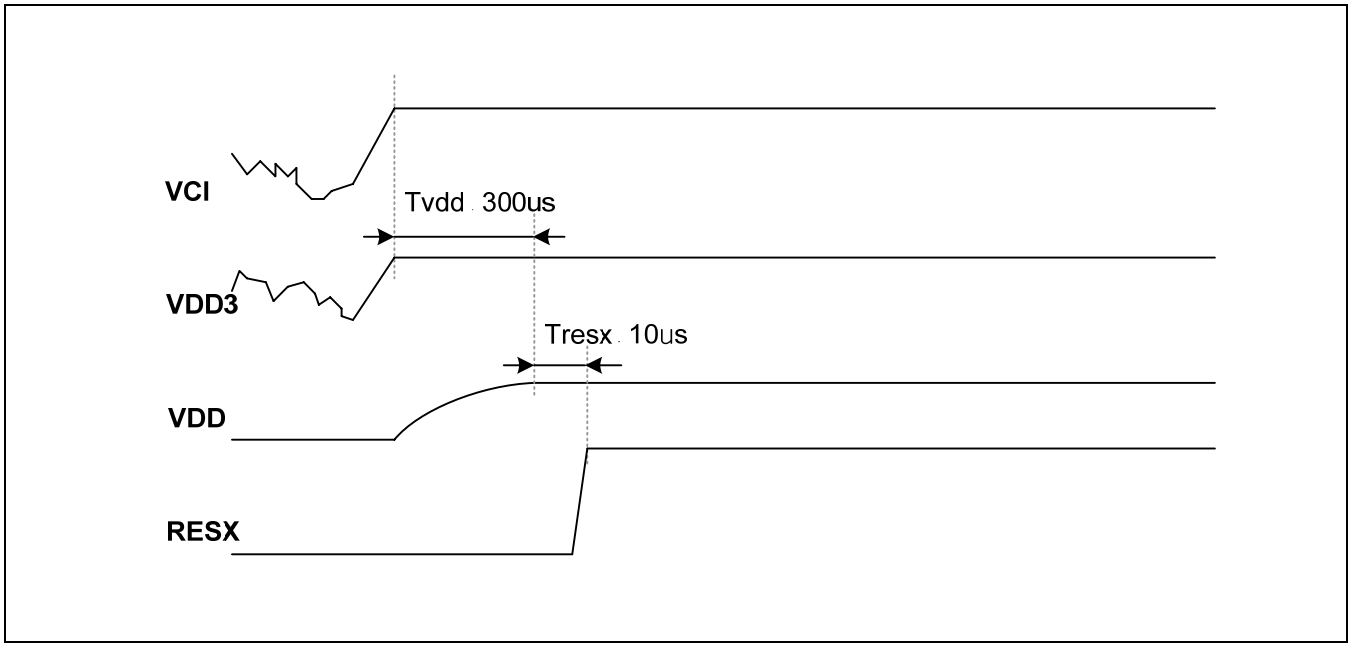


Figure 130 VDD3 – RESX Timing

The VDD3 to RESX timing is determined with internal VDD generation timing. The external RESX signal flows into internal logic block. And internal logic reset signal is generated with VDD voltage. The internal VDD voltage generation time from which external VDD3 power is set up is 300us at least. Therefore the external VDD3 to RESX timing should be longer than 310us.

4.1.2 ABRUPT POWER OFF

The abrupt power-off represents a situation where, for e.g., a battery is removed without the expected power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abrupt power-off, the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power-On Sequence” powers it up. Blank display means: For normally white panel, the blank display indicates white display. For normally black panel, the blank display indicates black display

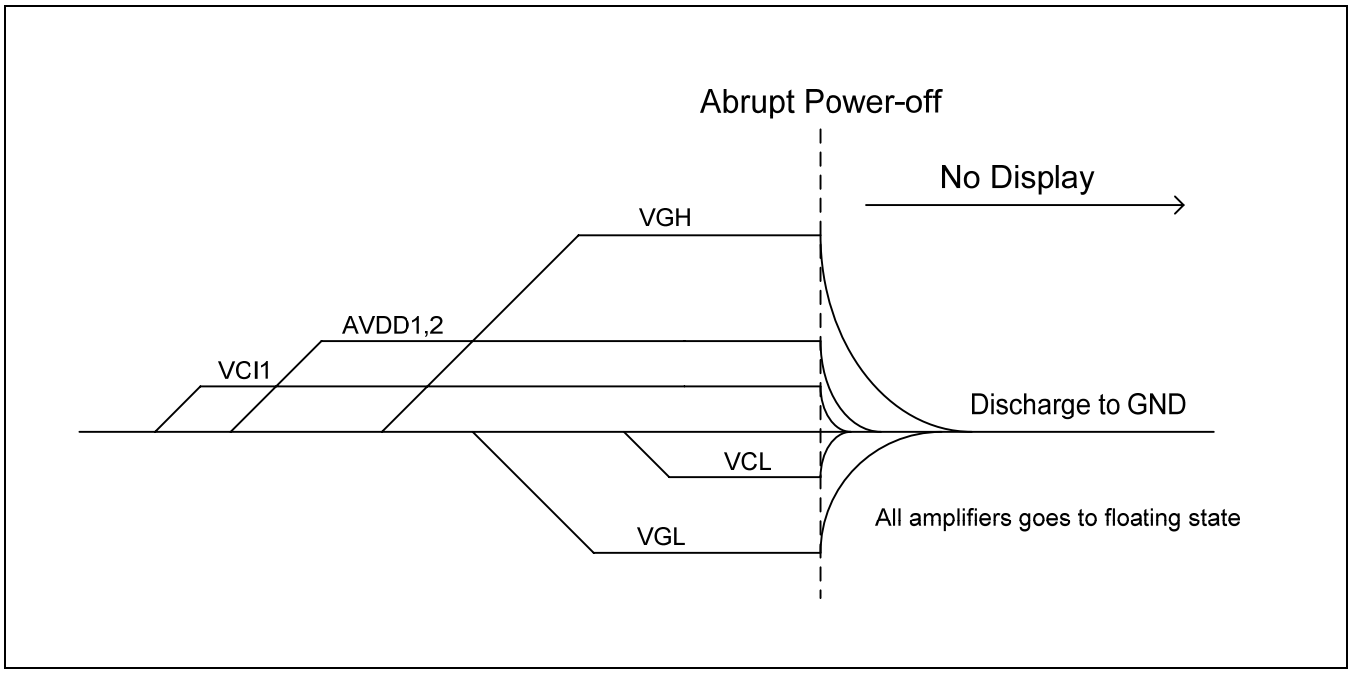


Figure 131 Status of Driver IC at Abrupt Power-off

4.1.3 POWER LEVELS (APON=1)

S6D05A1 supports 6 types of power-consumption modes. Each mode is described as follows:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out
   In this mode, the display is able to show maximum 16,777,216 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 16,777,216 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out
   In this mode, the full display area is used but with 8 colors,

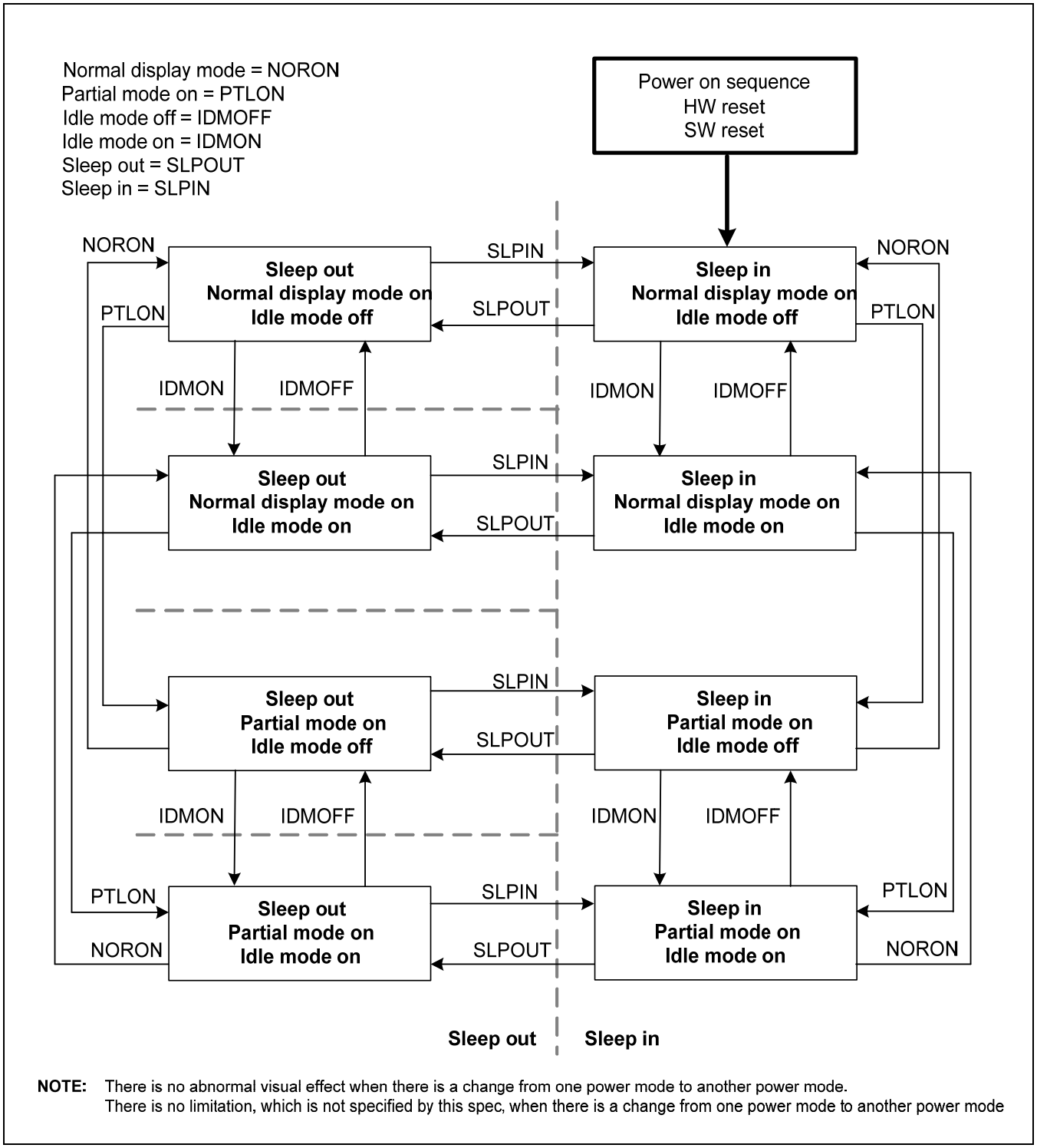
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors

5. Sleep In Mode
   In this mode, the booster, internal oscillator and panel driver circuit are stopped. Only the MPU interface and memory work VDD3 power supply. Contents of the memory are safe.

6. Power Off Mode.
   In this mode, both VCI and VDD3 are removed

NOTE:
Transition between modes 1-5 is controllable by MPU commands. Mode 6 is entered only when both Power supplies are removed.

4.1.4 POWER FLOW CHART FOR DIFFERENT POWER MODES (APON=1)

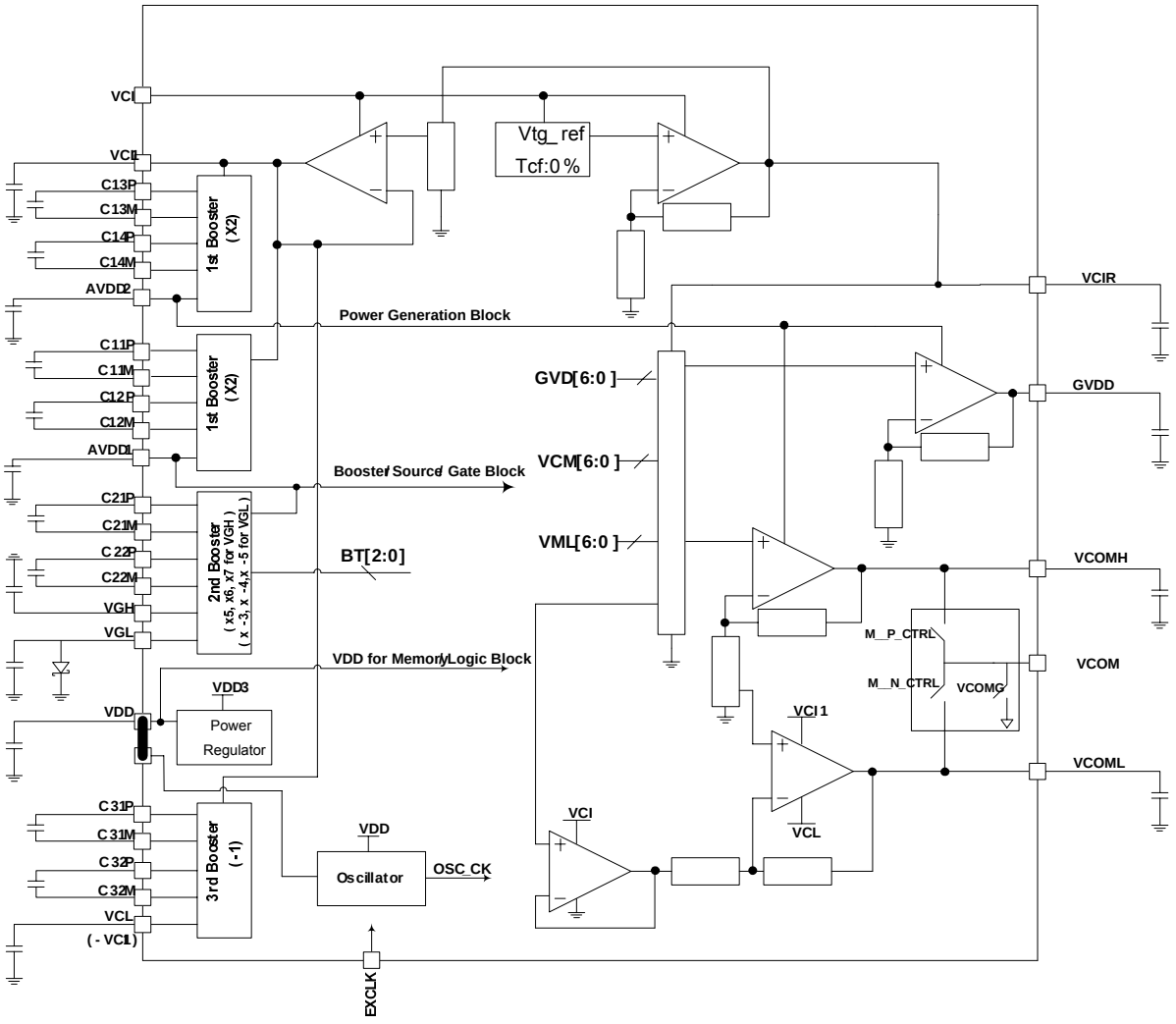


NOTE: There is no abnormal visual effect when there is a change from one power mode to another power mode.
There is no limitation, which is not specified by this spec, when there is a change from one power mode to another power mode

Figure 132 Power-On Flowchart for Various Power Modes

4.1.5 POWER SUPPLY

The following figure shows a configuration of the voltage generation circuit of S6D05A1. The booster circuit consists of booster circuits 1 to 3. Booster circuit1 doubles input voltage supplied from VCI1 for AVDD1, AVDD2 level. Booster circuit2 makes 2.5, 3 or 3.5 times AVDD1 level for VGH level, and makes -1.5, -2 or -2.5 times AVDD1 level for VGL level. Booster circuit3 reverses the VCI1 level with respect to VSS to generate VCL level. These Booster circuits generate power supplies AVDD1, AVDD2, VGH, VGL, and VCL. AVDD2 is used in power of source block. Reference voltages such as GVDD, VCOMH and VCOML are generated with VREF from the voltage adjustment circuit. Connect VCOM to the TFT panel.

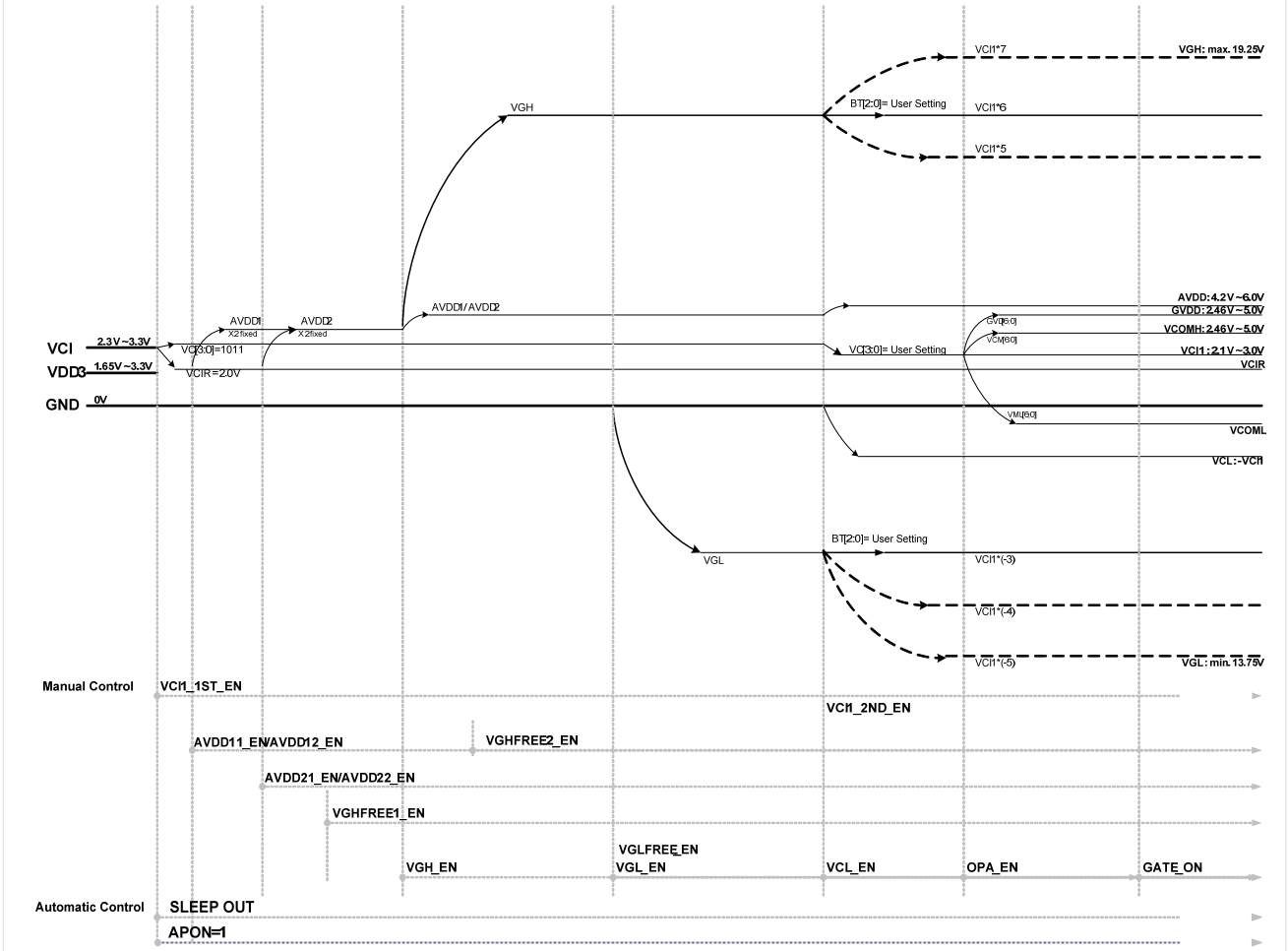


NOTE: Use the 1uF capacitor.
Schottky diode between VGL and VSS is positively necessary for making circuitry latch-up free.
The Capacitor between VCIR and VSS may be used in the case of occurring fluctuation in VCOM swing level.

Figure 133 Configuration of the Internal Power-Supply Circuit

4.1.6 PATTERN DIAGRAMS FOR VOLTAGE SETTING

The following figure shows a pattern diagram for the voltage setting and an example of waveforms



NOTE:

1. Set the conditions of AVDD-GVDD > 0.3V, VCOML- VCL>0.5V with loads because they differ depending on the display load to be driven
2. AVDD11_EN,AVDD12_EN,AVDD21_EN,AVDD22_EN,VGH_EN,VGL_EN,VCL_EN,OPA_EN,VGHFREE1_EN,VGHFREE2_EN,VGL_FREE_EN instructions are separately offered for flexibility of power-up sequence time control.
3. APON instruction is an automatic power- up sequence operating switch

cf> Pattern diagram above shows not only a relationship of each generated levels but practical power up sequence

Figure 134 Power-Up Pattern Diagram

4.1.7 SET UP FLOW OF POWER

Apply the power in a sequential way as shown in the following figure. The settling time of the oscillation circuit, booster1/2/3 circuits, and operational amplifier depends on the external resistance or capacitance value.

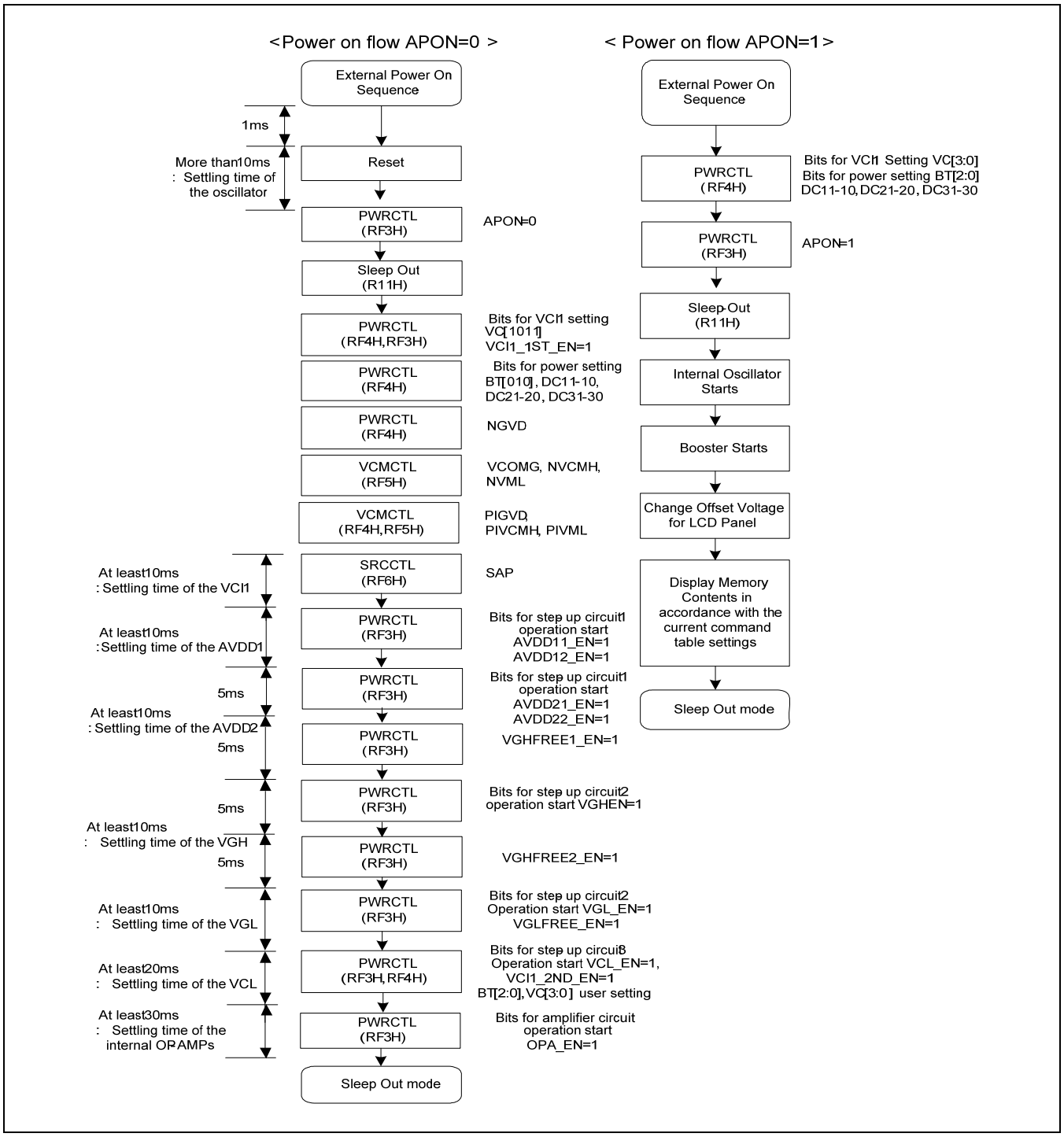


Figure 135 Setup Flow of Power

4.1.8 DEEP-STANDBY SEQUENCE

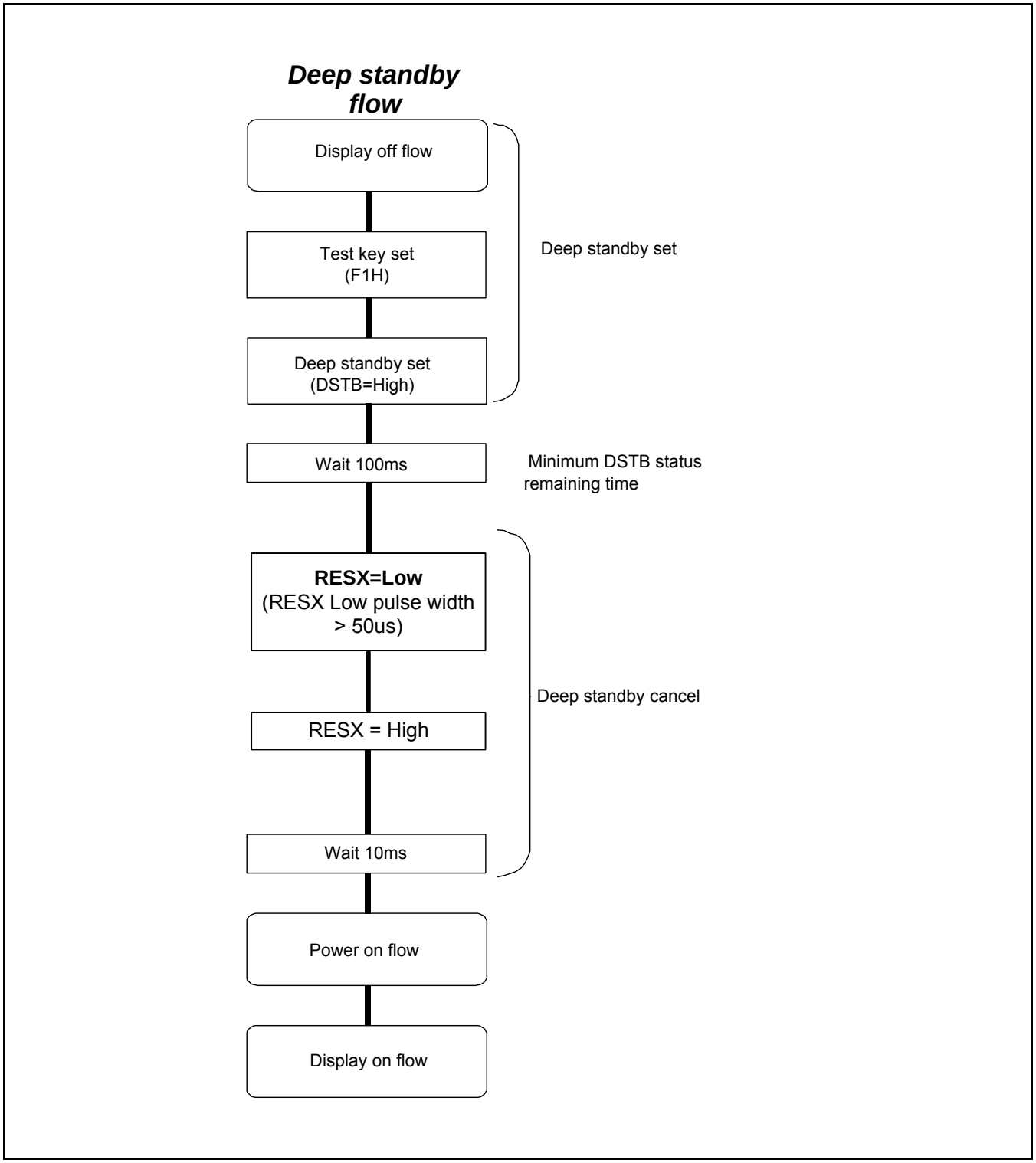


Figure 136 Deep-Standby Sequence (DSTB Sequence (a))

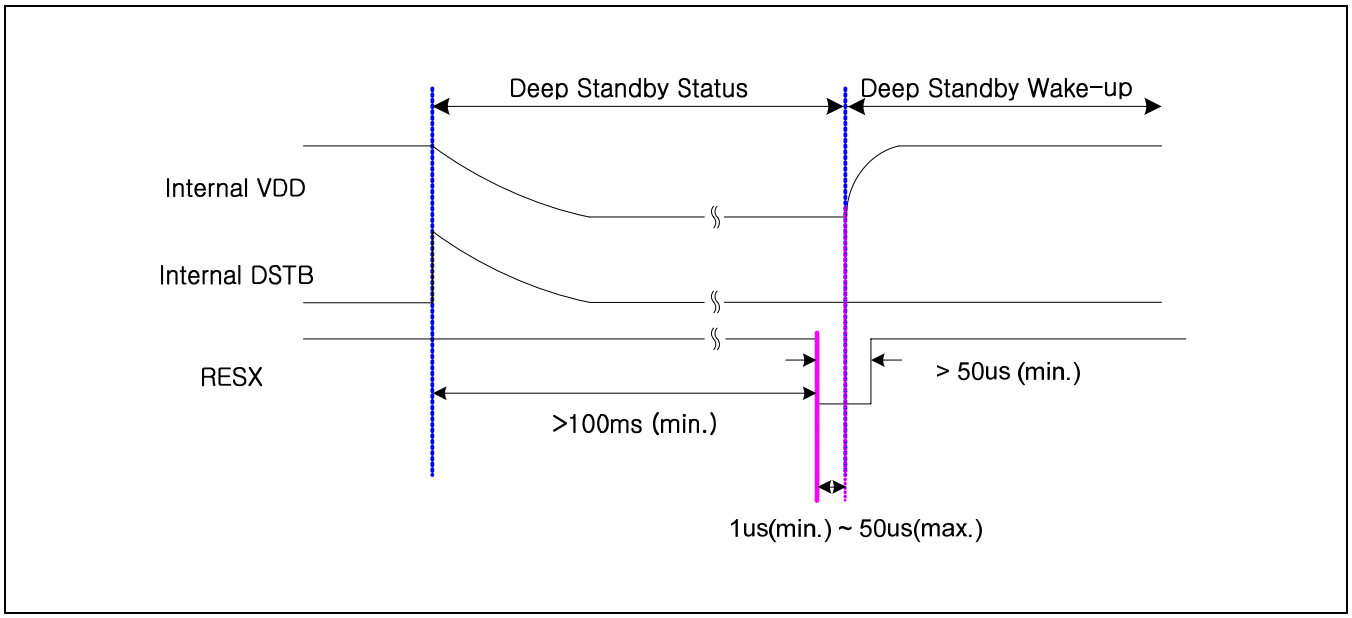


Figure 137 Deep-Standby Sequence (DSTB EXIT Flow : RESX “Low” (b))

4.1.9 DISCHARGE STATUS OF POWER BLOCK

Following Table describes The Discharge status of power block

Table 77 Discharge Status of Power Block

	H/W RESET	S/W RESET	DSTB
VCOM	VSS	VSS	VSS
SOURCE	VSS	VSS	VSS
GATE	VSS	VSS	VSS
VCIR	Floating	Floating	Floating
GVDD	VSS	VSS	VSS
VCOMH	VSS	VSS	VSS
VCOML	VSS	VSS	VSS
VCI1	VSS	VSS	VSS
AVDD1,2	VSS	VSS	VSS
VCL	VSS	VSS	VSS
VGH	VSS	VSS	VSS
VGL	VSS	VSS	VSS

4.1.10 VOLTAGE REGULATION FUNCTION

The S6D05A1 has an internal voltage regulator. By the use of this function, unexpected damages on internal logic circuit can be avoided. Furthermore, low power consumption can also be obtained. Detailed function description and applicable configuration are described in the following diagram.

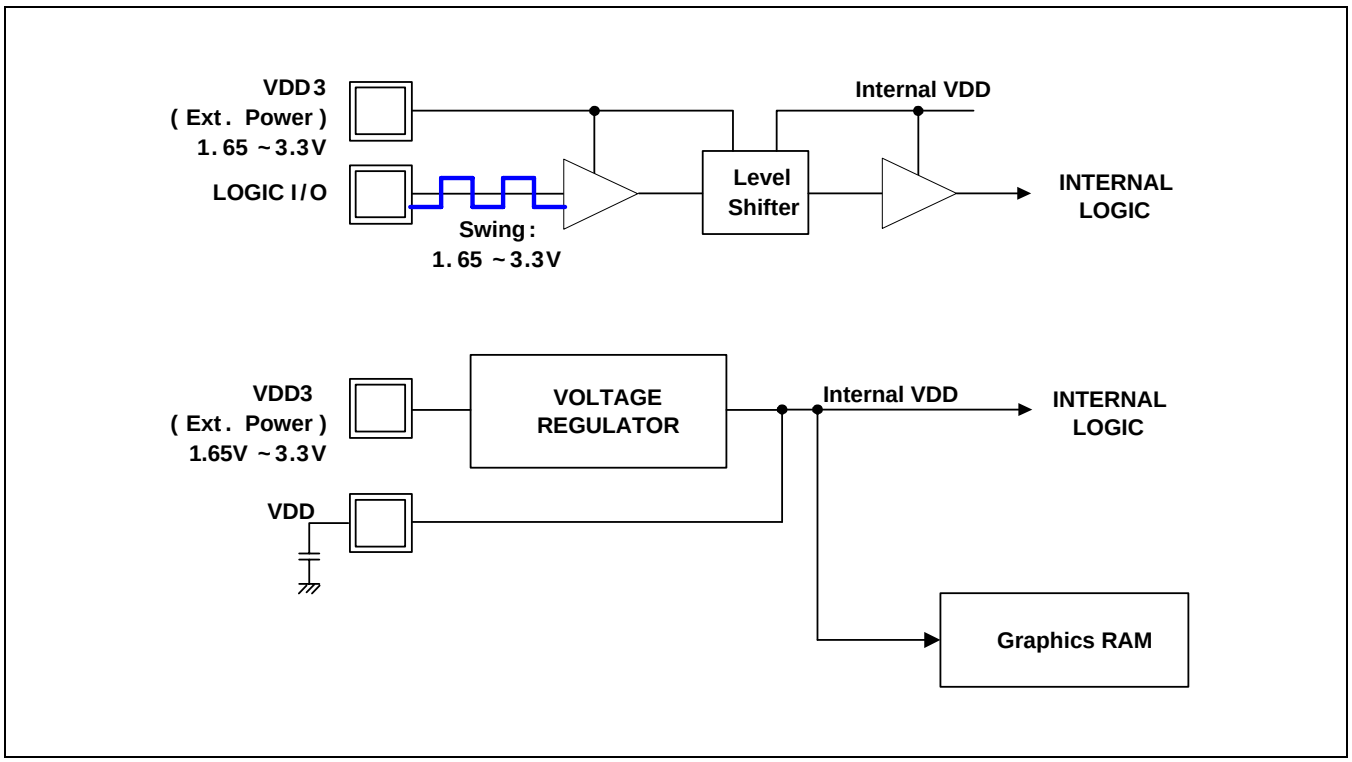


Figure 138 Voltage Regulation Function

4.2 SOURCE

4.2.1 SOURCE DRIVER

The liquid crystal display source driver circuit consists of 1080 drivers (S1 to S1080).
Display pattern data is latched when 1080 Channel data has arrived. Then the latched data enables the source drivers to output to expected voltage level. When less than 1080 sources are required, the unused source outputs should be left open.

4.2.2 GAMMA ADJUSTMENT FUNCTION

S6D05A1 provides the gamma adjustment function to display 16,777,216 colors simultaneously for each R/G/B color. The gamma adjustment executed by the high/ mid/ low level adjustment registers determines 13 grayscale reference levels. Furthermore, since the high-level adjustment register, mid-level adjustment register and the low-level adjustment register have the positive polarities and negative polarities, you can adjust them to match LCD panel and a gamma for each R/G/B color, respectively.

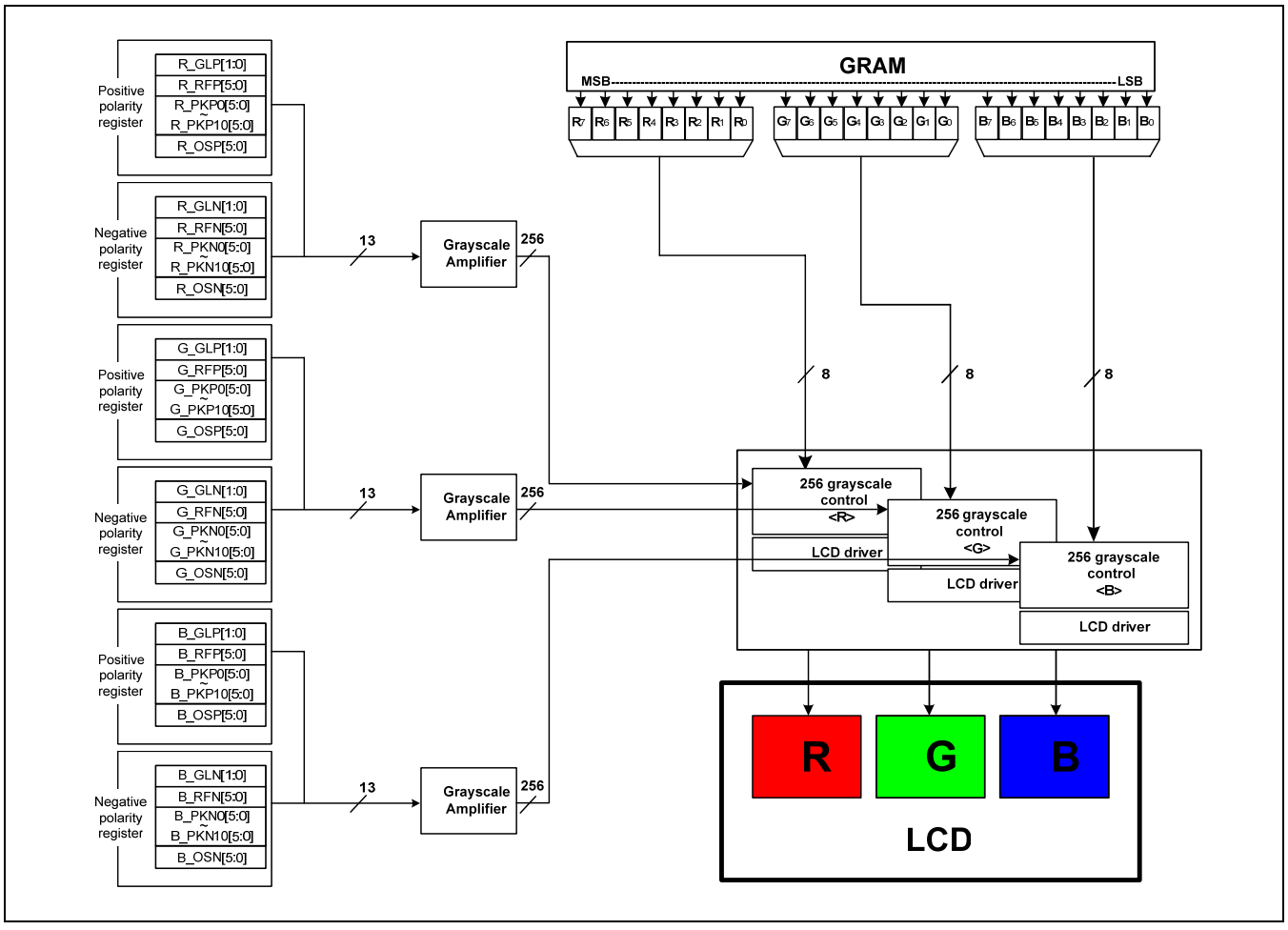


Figure 139 Block Diagram of Gamma Adjustment Function

4.2.3 GAMMA CURVE

4.2.3.1 Gamma Curve

Gamma Curve, applies the function. y = x 2.2

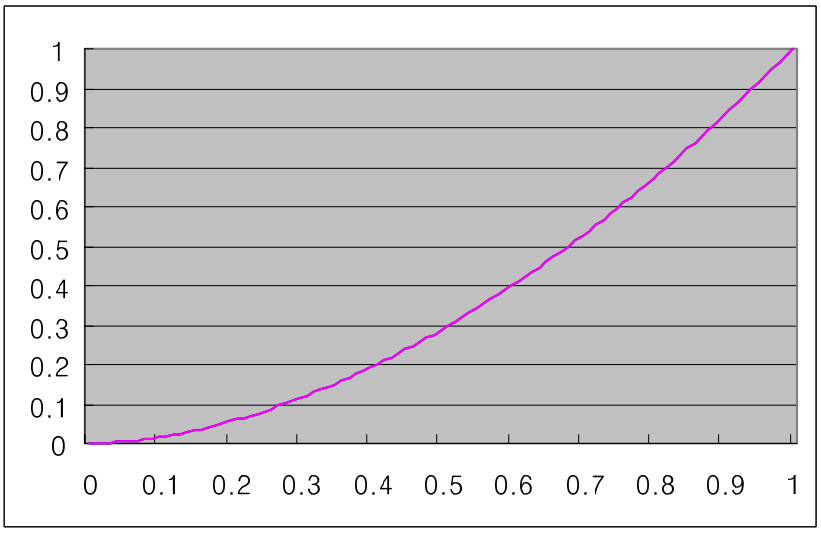


Figure 140 Gamma y = x 2.2

4.2.4 STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of grayscale amplifier is shown as below. The 13 voltage levels (VIN0-VIN12) between GVDD and VGS are determined by the reference adjustment register, the amplitude adjustment resister, the x-axis symmetric adjustment register, the micro-adjustment register and the gray-shift register. Each level is split into 256 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 256 voltage levels ranging from V0 to V255.

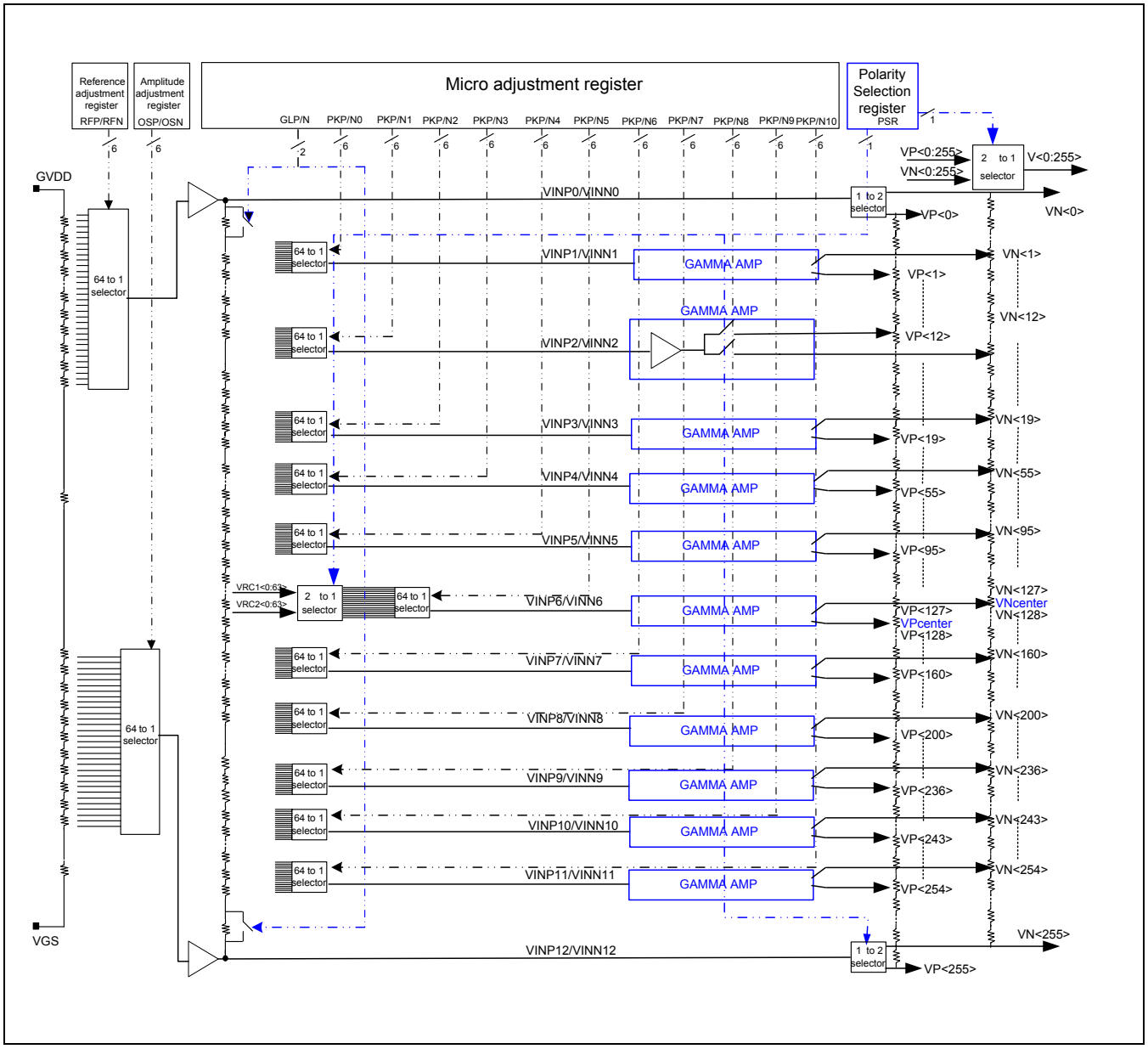


Figure 141 Structure of Gray Scale Amplifier

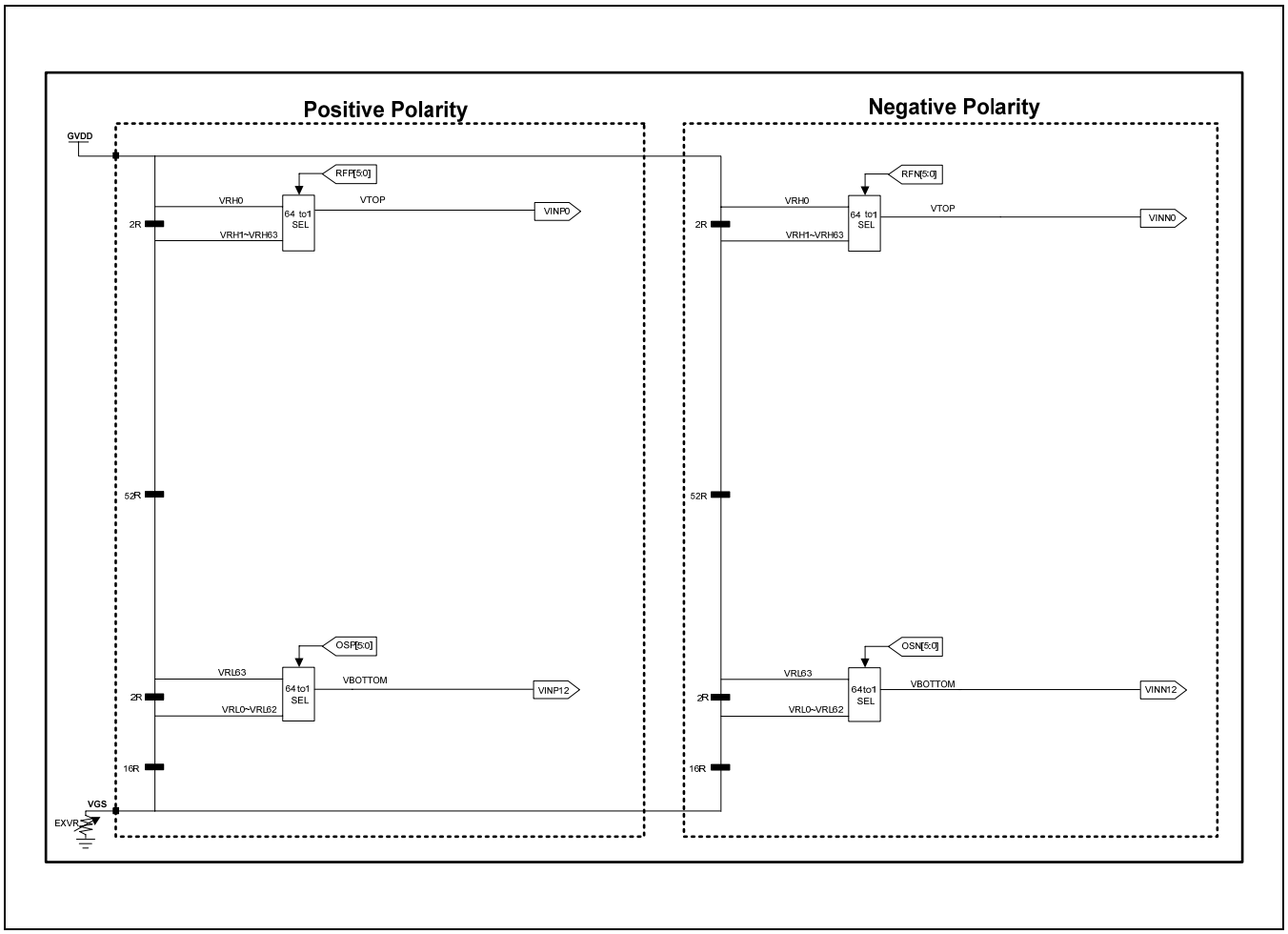


Figure 142 Structure of Resistor Ladder Network 1

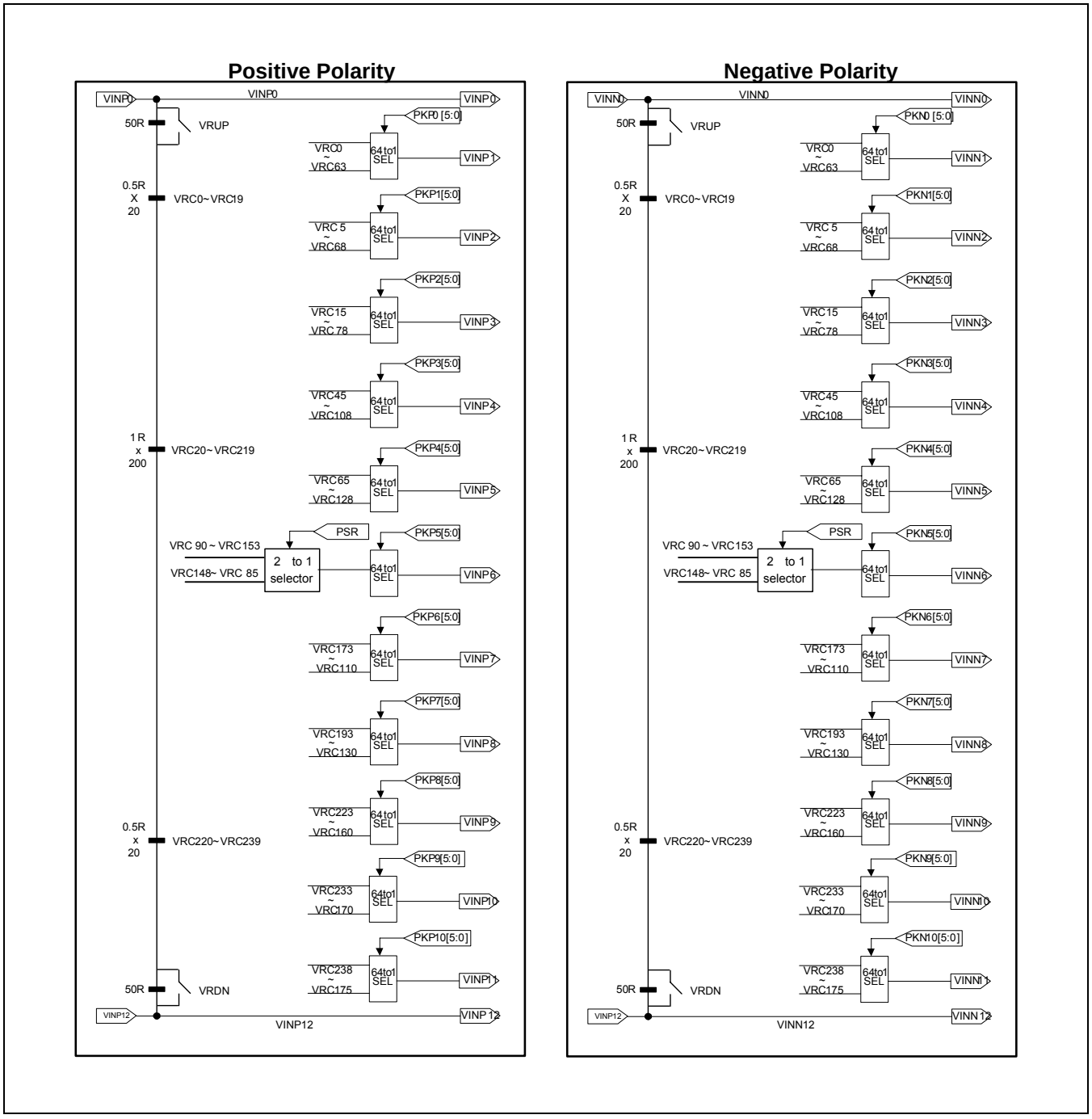


Figure 143 Structure of Resistor Ladder Network 2

4.2.5 GAMMA ADJUSTMENT REGISTER

This block has registers to set up the grayscale voltage according to the gamma specification of the LCD panel. These registers can independently set up the positive/negative polarities. There are 4 types of register groups to adjust the amplitude on the grayscale characteristics of the grayscale voltage, and R/G/B gamma adjustment registers are separated. The following figures indicate the operation of each adjustment registers.

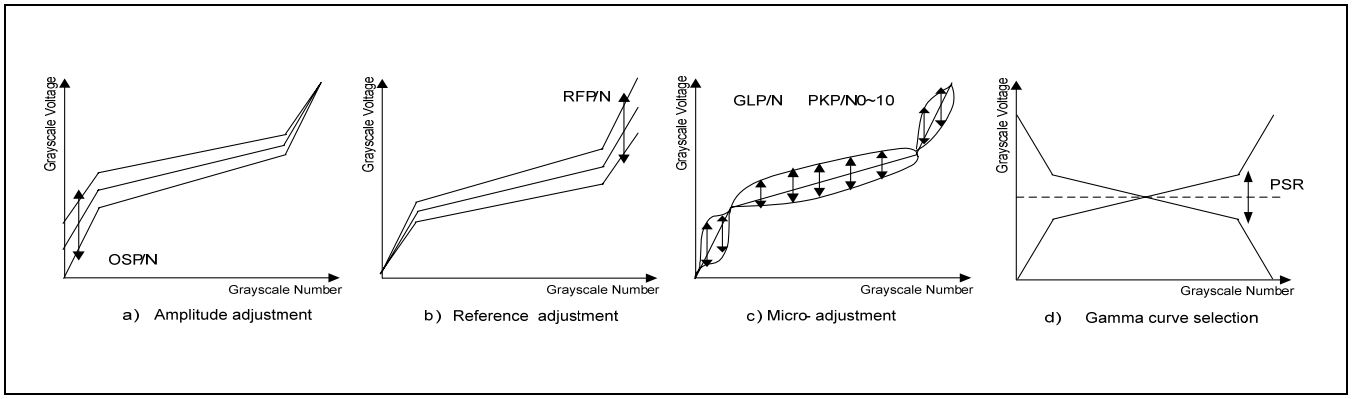


Figure 144 The Operation of Adjusting Register

4.2.5.1 Reference Adjustment Register

The Reference adjustment register is used to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VINN0 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4.2.5.2 Amplitude Adjustment Register

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP12/VINN12 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4.2.5.3 Micro Adjustment Register

The Micro adjustment register is employed to make subtle adjustment to the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

4.2.5.4 Gamma curve Selection Register

The Gamma curve selection register is to adjust X-axis symmetric of the grayscale voltage. This register can be detailedly explained with NGF register selection. 1st case; when SG=0(PSR toggle) and NGF=10,

Vp<N>+Vn<N>=Vp<0>+Vn<0> and gamma symmetric axis is (Vp<0>+Vn<0>)/2. 2nd case; when SG=0(PSR toggle) and NGF=01, negative gamma voltage can be changed using negative gamma register value and symmetric axis will be changed according to negative gamma voltage. 3rd case; when SG=1(PSR=H fix) and NGF=00, Vp<N>=Vn<|255-N|>. 4th case; when SG=1(PSR=H fix) and NGF=01, Vp<N>+Vn<N> ≠ Vp<0>+Vn<0> but can have similar value in some degree using both positive and negative gamma registers.

- PSR=L, Select Positve gamma curve
- PSR=H, Select Negative gamma curve

Table 78 Description of Gamma Adjustment Register

Register	Positive polarity	Negative polarity	Set-up contents
Amplitude adjustment	OSP [5:0]	OSN [5:0]	The voltage of VBOTTOM is selected by the 64 to 1 selector
Reference adjustment	RFP [5:0]	RFN [5:0]	The voltage of VTOP is selected by the 64 to 1 selector
Gamma curve selection	PSR		Selecte positive gamma curve or negative gamma
Micro adjustment	GLP [1:0]	GLN [1:0]	The voltage of grayscale number from 1 to 254 is adjusted by the variable resistor
	PKP0 [5:0]	PKN0 [5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
	PKP1 [5:0]	PKN1 [5:0]	The voltage of grayscale number 12 is selected by the 64 to 1 selector
	PKP2 [5:0]	PKN2 [5:0]	The voltage of grayscale number 19 is selected by the 64 to 1 selector
	PKP3 [5:0]	PKN3 [5:0]	The voltage of grayscale number 55 is selected by the 64 to 1 selector
	PKP4 [5:0]	PKN4[5: 0]	The voltage of grayscale number 95 is selected by the 64 to 1 selector
	PKP5 [5:0]	PKN5 [5:0]	The voltage of grayscale number VC (middle voltage between v<127> and V<128>) is selected by the 64 to 1 selector
	PKP6 [5:0]	PKN6 [5:0]	The voltage of grayscale number 160 is selected by the 64 to 1 selector
	PKP7 [5:0]	PKN7 [5:0]	The voltage of grayscale number 200 is selected by the 64 to 1 selector
	PKP8 [5:0]	PKN8 [5:0]	The voltage of grayscale number 236 is selected by the 64 to 1 selector
	PKP9 [5:0]	PKN9 [5:0]	The voltage of grayscale number 243 is selected by the 64 to 1 selector
	PKP10 [5:0]	PKN10 [5:0]	The voltage of grayscale number 254 is selected by the 64 to 1 selector

4.2.6 RESISTOR LADDER NETWORK / SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are three ladder resistors including the 64 to 1 selector selecting voltage generated by the ladder resistance voltage. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

4.2.6.1 Resistor Ladder Network 1 / Selector

There are 3 adjustments that are for the reference / amplitude adjustment (RFP(N)/ OSP(N)) and micro adjustment (PKP(N)). The voltage level is set by the reference / amplitude adjustment registers and micro adjustments as below.

Table 79 Reference Adjustment

Register value RFP(N) [5:0]	Selected voltage VTOP	Formula of VTOP
000000	VRH0	(320R/320R) * (GVDD-VGS) + VGS
000001	VRH1	(318R/320R) * (GVDD-VGS) + VGS
000010	VRH2	(316R/320R) * (GVDD-VGS) + VGS
000011	VRH3	(314R/320R) * (GVDD-VGS) + VGS
000100	VRH4	(312R/320R) * (GVDD-VGS) + VGS
000101	VRH5	(310R/320R) * (GVDD-VGS) + VGS
000110	VRH6	(308R/320R) * (GVDD-VGS) + VGS
000111	VRH7	(306R/320R) * (GVDD-VGS) + VGS
001000	VRH8	(304R/320R) * (GVDD-VGS) + VGS
001001	VRH9	(302R/320R) * (GVDD-VGS) + VGS
001010	VRH10	(300R/320R) * (GVDD-VGS) + VGS
001011	VRH11	(298R/320R) * (GVDD-VGS) + VGS
001100	VRH12	(296R/320R) * (GVDD-VGS) + VGS
001101	VRH13	(294R/320R) * (GVDD-VGS) + VGS
001110	VRH14	(292R/320R) * (GVDD-VGS) + VGS
001111	VRH15	(290R/320R) * (GVDD-VGS) + VGS
010000	VRH16	(288R/320R) * (GVDD-VGS) + VGS
010001	VRH17	(286R/320R) * (GVDD-VGS) + VGS
010010	VRH18	(284R/320R) * (GVDD-VGS) + VGS
010011	VRH19	(282R/320R) * (GVDD-VGS) + VGS
010100	VRH20	(280R/320R) * (GVDD-VGS) + VGS
010101	VRH21	(278R/320R) * (GVDD-VGS) + VGS
010110	VRH22	(276R/320R) * (GVDD-VGS) + VGS

Register value RFP(N) [5:0]	Selected voltage VTOP	Formula of VTOP
010111	VRH23	(274R/320R) * (GVDD-VGS) + VGS
011000	VRH24	(272R/320R) * (GVDD-VGS) + VGS
011001	VRH25	(270R/320R) * (GVDD-VGS) + VGS
011010	VRH26	(268R/320R) * (GVDD-VGS) + VGS
011011	VRH27	(266R/320R) * (GVDD-VGS) + VGS
011100	VRH28	(264R/320R) * (GVDD-VGS) + VGS
011101	VRH29	(262R/320R) * (GVDD-VGS) + VGS
011110	VRH30	(260R/320R) * (GVDD-VGS) + VGS
011111	VRH31	(258R/320R) * (GVDD-VGS) + VGS
100000	VRH32	(256R/320R) * (GVDD-VGS) + VGS
100001	VRH33	(254R/320R) * (GVDD-VGS) + VGS
100010	VRH34	(252R/320R) * (GVDD-VGS) + VGS
100011	VRH35	(250R/320R) * (GVDD-VGS) + VGS
100100	VRH36	(248R/320R) * (GVDD-VGS) + VGS
100101	VRH37	(246R/320R) * (GVDD-VGS) + VGS
100110	VRH38	(244R/320R) * (GVDD-VGS) + VGS
100111	VRH39	(242R/320R) * (GVDD-VGS) + VGS
101000	VRH40	(240R/320R) * (GVDD-VGS) + VGS
101001	VRH41	(238R/320R) * (GVDD-VGS) + VGS
101010	VRH42	(236R/320R) * (GVDD-VGS) + VGS
101011	VRH43	(234R/320R) * (GVDD-VGS) + VGS
101100	VRH44	(232R/320R) * (GVDD-VGS) + VGS
101101	VRH45	(230R/320R) * (GVDD-VGS) + VGS
101110	VRH46	(228R/320R) * (GVDD-VGS) + VGS
101111	VRH47	(226R/320R) * (GVDD-VGS) + VGS
110000	VRH48	(224R/320R) * (GVDD-VGS) + VGS
110001	VRH49	(222R/320R) * (GVDD-VGS) + VGS
110010	VRH50	(220R/320R) * (GVDD-VGS) + VGS
110011	VRH51	(218R/320R) * (GVDD-VGS) + VGS
110100	VRH52	(216R/320R) * (GVDD-VGS) + VGS
110101	VRH53	(214R/320R) * (GVDD-VGS) + VGS
110110	VRH54	(212R/320R) * (GVDD-VGS) + VGS
110111	VRH55	(210R/320R) * (GVDD-VGS) + VGS
111000	VRH56	(208R/320R) * (GVDD-VGS) + VGS

Register value RFP(N) [5:0]	Selected voltage VTOP	Formula of VTOP
111001	VRH57	(206R/320R) * (GVDD-VGS) + VGS
111010	VRH58	(204R/320R) * (GVDD-VGS) + VGS
111011	VRH59	(202R/320R) * (GVDD-VGS) + VGS
111100	VRH60	(200R/320R) * (GVDD-VGS) + VGS
111101	VRH61	(198R/320R) * (GVDD-VGS) + VGS
111110	VRH62	(196R/320R) * (GVDD-VGS) + VGS
111111	VRH63	(194R/320R) * (GVDD-VGS) + VGS

Table 80 Amplitude Adjustment

Register value OSP(N) [5:0]	Selected voltage VBOTTOM	Formula of VBOTTOM
000000	VRL0	(16R/320R) * (GVDD-VGS) + VGS
000001	VRL1	(18R/320R) * (GVDD-VGS) + VGS
000010	VRL2	(20R/320R) * (GVDD-VGS) + VGS
000011	VRL3	(22R/320R) * (GVDD-VGS) + VGS
000100	VRL4	(24R/320R) * (GVDD-VGS) + VGS
000101	VRL5	(26R/320R) * (GVDD-VGS) + VGS
000110	VRL6	(28R/320R) * (GVDD-VGS) + VGS
000111	VRL7	(30R/320R) * (GVDD-VGS) + VGS
001000	VRL8	(32R/320R) * (GVDD-VGS) + VGS
001001	VRL9	(34R/320R) * (GVDD-VGS) + VGS
001010	VRL10	(36R/320R) * (GVDD-VGS) + VGS
001011	VRL11	(38R/320R) * (GVDD-VGS) + VGS
001100	VRL12	(40R/320R) * (GVDD-VGS) + VGS
001101	VRL13	(42R/320R) * (GVDD-VGS) + VGS
001110	VRL14	(44R/320R) * (GVDD-VGS) + VGS
001111	VRL15	(46R/320R) * (GVDD-VGS) + VGS
010000	VRL16	(48R/320R) * (GVDD-VGS) + VGS
010001	VRL17	(50R/320R) * (GVDD-VGS) + VGS
010010	VRL18	(52R/320R) * (GVDD-VGS) + VGS
010011	VRL19	(54R/320R) * (GVDD-VGS) + VGS
010100	VRL20	(56R/320R) * (GVDD-VGS) + VGS
010101	VRL21	(58R/320R) * (GVDD-VGS) + VGS
010110	VRL22	(60R/320R) * (GVDD-VGS) + VGS
010111	VRL23	(62R/320R) * (GVDD-VGS) + VGS
011000	VRL24	(64R/320R) * (GVDD-VGS) + VGS
011001	VRL25	(66R/320R) * (GVDD-VGS) + VGS
011010	VRL26	(68R/320R) * (GVDD-VGS) + VGS
011011	VRL27	(70R/320R) * (GVDD-VGS) + VGS
011100	VRL28	(72R/320R) * (GVDD-VGS) + VGS
011101	VRL29	(74R/320R) * (GVDD-VGS) + VGS
011110	VRL30	(76R/320R) * (GVDD-VGS) + VGS
011111	VRL31	(78R/320R) * (GVDD-VGS) + VGS
100000	VRL32	(80R/320R) * (GVDD-VGS) + VGS

Register value OSP(N) [5:0]	Selected voltage VBOTTOM	Formula of VBOTTOM
100001	VRL33	(82R/320R) * (GVDD-VGS) + VGS
100010	VRL34	(84R/320R) * (GVDD-VGS) + VGS
100011	VRL35	(86R/320R) * (GVDD-VGS) + VGS
100100	VRL36	(88R/320R) * (GVDD-VGS) + VGS
100101	VRL37	(90R/320R) * (GVDD-VGS) + VGS
100110	VRL38	(92R/320R) * (GVDD-VGS) + VGS
100111	VRL39	(94R/320R) * (GVDD-VGS) + VGS
101000	VRL40	(96R/320R) * (GVDD-VGS) + VGS
101001	VRL41	(98R/320R) * (GVDD-VGS) + VGS
101010	VRL42	(100R/320R) * (GVDD-VGS) + VGS
101011	VRL43	(102R/320R) * (GVDD-VGS) + VGS
101100	VRL44	(104R/320R) * (GVDD-VGS) + VGS
101101	VRL45	(106R/320R) * (GVDD-VGS) + VGS
101110	VRL46	(108R/320R) * (GVDD-VGS) + VGS
101111	VRL47	(110R/320R) * (GVDD-VGS) + VGS
110000	VRL48	(112R/320R) * (GVDD-VGS) + VGS
110001	VRL49	(114R/320R) * (GVDD-VGS) + VGS
110010	VRL50	(116R/320R) * (GVDD-VGS) + VGS
110011	VRL51	(118R/320R) * (GVDD-VGS) + VGS
110100	VRL52	(120R/320R) * (GVDD-VGS) + VGS
110101	VRL53	(122R/320R) * (GVDD-VGS) + VGS
110110	VRL54	(124R/320R) * (GVDD-VGS) + VGS
110111	VRL55	(126R/320R) * (GVDD-VGS) + VGS
111000	VRL56	(128R/320R) * (GVDD-VGS) + VGS
111001	VRL57	(130R/320R) * (GVDD-VGS) + VGS
111010	VRL58	(132R/320R) * (GVDD-VGS) + VGS
111011	VRL59	(134R/320R) * (GVDD-VGS) + VGS
111100	VRL60	(136R/320R) * (GVDD-VGS) + VGS
111101	VRL61	(138R/320R) * (GVDD-VGS) + VGS
111110	VRL62	(140R/320R) * (GVDD-VGS) + VGS
111111	VRL63	(142R/320R) * (GVDD-VGS) + VGS

4.2.6.2 Resistor Ladder Network 2 / Selector

In the 64-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the eleven types of the reference voltage, VINP(N)1 to VINP(N)11.
Following figure explains the relationship between the micro-adjustment register and the selected voltage

Table 81 Relationship Between Micro-Adjustment Register and Selected Voltage

Register value	Selected voltage											
PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINN 6	VINP 6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10	VINP (N)11
000000	VRC 0	VRC 5	VRC 15	VRC 45	VRC 65	VRC 90	VRC 148	VRC 173	VRC 193	VRC 223	VRC 233	VRC 238
000001	VRC 1	VRC 6	VRC 16	VRC 46	VRC 66	VRC 91	VRC 147	VRC 172	VRC 192	VRC 222	VRC 232	VRC 237
000010	VRC 2	VRC 7	VRC 17	VRC 47	VRC 67	VRC 92	VRC 146	VRC 171	VRC 191	VRC 221	VRC 231	VRC 236
000011	VRC 3	VRC 8	VRC 18	VRC 48	VRC 68	VRC 93	VRC 145	VRC 170	VRC 190	VRC 220	VRC 230	VRC 235
000100	VRC 4	VRC 9	VRC 19	VRC 49	VRC 69	VRC 94	VRC 144	VRC 169	VRC 189	VRC 219	VRC 229	VRC 234
000101	VRC 5	VRC 10	VRC 20	VRC 50	VRC 70	VRC 95	VRC 143	VRC 168	VRC 188	VRC 218	VRC 228	VRC 233
000110	VRC 6	VRC 11	VRC 21	VRC 51	VRC 71	VRC 96	VRC 142	VRC 167	VRC 187	VRC 217	VRC 227	VRC 232
000111	VRC 7	VRC 12	VRC 22	VRC 52	VRC 72	VRC 97	VRC 141	VRC 166	VRC 186	VRC 216	VRC 226	VRC 231
001000	VRC 8	VRC 13	VRC 23	VRC 53	VRC 73	VRC 98	VRC 140	VRC 165	VRC 185	VRC 215	VRC 225	VRC 230
001001	VRC 9	VRC 14	VRC 24	VRC 54	VRC 74	VRC 99	VRC 139	VRC 164	VRC 184	VRC 214	VRC 224	VRC 229
001010	VRC 10	VRC 15	VRC 25	VRC 55	VRC 75	VRC 100	VRC 138	VRC 163	VRC 183	VRC 213	VRC 223	VRC 228
001011	VRC 11	VRC 16	VRC 26	VRC 56	VRC 76	VRC 101	VRC 137	VRC 162	VRC 182	VRC 212	VRC 222	VRC 227
001100	VRC 12	VRC 17	VRC 27	VRC 57	VRC 77	VRC 102	VRC 136	VRC 161	VRC 181	VRC 211	VRC 221	VRC 226
001101	VRC 13	VRC 18	VRC 28	VRC 58	VRC 78	VRC 103	VRC 135	VRC 160	VRC 180	VRC 210	VRC 220	VRC 225
001110	VRC 14	VRC 19	VRC 29	VRC 59	VRC 79	VRC 104	VRC 134	VRC 159	VRC 179	VRC 209	VRC 219	VRC 224
001111	VRC 15	VRC 20	VRC 30	VRC 60	VRC 80	VRC 105	VRC 133	VRC 158	VRC 178	VRC 208	VRC 218	VRC 223
010000	VRC 16	VRC 21	VRC 31	VRC 61	VRC 81	VRC 106	VRC 132	VRC 157	VRC 177	VRC 207	VRC 217	VRC 222

Register value	Selected voltage											
PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINN 6	VINP 6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10	VINP (N)11
010001	VRC 17	VRC 22	VRC 32	VRC 62	VRC 82	VRC 107	VRC 131	VRC 156	VRC 176	VRC 206	VRC 216	VRC 221
010010	VRC 18	VRC 23	VRC 33	VRC 63	VRC 83	VRC 108	VRC 130	VRC 155	VRC 175	VRC 205	VRC 215	VRC 220
010011	VRC 19	VRC 24	VRC 34	VRC 64	VRC 84	VRC 109	VRC 129	VRC 154	VRC 174	VRC 204	VRC 214	VRC 219
010100	VRC 20	VRC 25	VRC 35	VRC 65	VRC 85	VRC 110	VRC 128	VRC 153	VRC 173	VRC 203	VRC 213	VRC 218
010101	VRC 21	VRC 26	VRC 36	VRC 66	VRC 86	VRC 111	VRC 127	VRC 152	VRC 172	VRC 202	VRC 212	VRC 217
010110	VRC 22	VRC 27	VRC 37	VRC 67	VRC 87	VRC 112	VRC 126	VRC 151	VRC 171	VRC 201	VRC 211	VRC 216
010111	VRC 23	VRC 28	VRC 38	VRC 68	VRC 88	VRC 113	VRC 125	VRC 150	VRC 170	VRC 200	VRC 210	VRC 215
011000	VRC 24	VRC 29	VRC 39	VRC 69	VRC 89	VRC 114	VRC 124	VRC 149	VRC 169	VRC 199	VRC 209	VRC 214
011001	VRC 25	VRC 30	VRC 40	VRC 70	VRC 90	VRC 115	VRC 123	VRC 148	VRC 168	VRC 198	VRC 208	VRC 213
011010	VRC 26	VRC 31	VRC 41	VRC 71	VRC 91	VRC 116	VRC 122	VRC 147	VRC 167	VRC 197	VRC 207	VRC 212
011011	VRC 27	VRC 32	VRC 42	VRC 72	VRC 92	VRC 117	VRC 121	VRC 146	VRC 166	VRC 196	VRC 206	VRC 211
011100	VRC 28	VRC 33	VRC 43	VRC 73	VRC 93	VRC 118	VRC 120	VRC 145	VRC 165	VRC 195	VRC 205	VRC 210
011101	VRC 29	VRC 34	VRC 44	VRC 74	VRC 94	VRC 119	VRC 119	VRC 144	VRC 164	VRC 194	VRC 204	VRC 209
011110	VRC 30	VRC 35	VRC 45	VRC 75	VRC 95	VRC 120	VRC 118	VRC 143	VRC 163	VRC 193	VRC 203	VRC 208
011111	VRC 31	VRC 36	VRC 46	VRC 76	VRC 96	VRC 121	VRC 117	VRC 142	VRC 162	VRC 192	VRC 202	VRC 207
100000	VRC 32	VRC 37	VRC 47	VRC 77	VRC 97	VRC 122	VRC 116	VRC 141	VRC 161	VRC 191	VRC 201	VRC 206
100001	VRC 33	VRC 38	VRC 48	VRC 78	VRC 98	VRC 123	VRC 115	VRC 140	VRC 160	VRC 190	VRC 200	VRC 205
100010	VRC 34	VRC 39	VRC 49	VRC 79	VRC 99	VRC 124	VRC 114	VRC 139	VRC 159	VRC 189	VRC 199	VRC 204
100011	VRC 35	VRC 40	VRC 50	VRC 80	VRC 100	VRC 125	VRC 113	VRC 138	VRC 158	VRC 188	VRC 198	VRC 203
100100	VRC 36	VRC 41	VRC 51	VRC 81	VRC 101	VRC 126	VRC 112	VRC 137	VRC 157	VRC 187	VRC 197	VRC 202

Register value	Selected voltage											
PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINN 6	VINP 6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10	VINP (N)11
100101	VRC 37	VRC 42	VRC 52	VRC 82	VRC 102	VRC 127	VRC 111	VRC 136	VRC 156	VRC 186	VRC 196	VRC 201
100110	VRC 38	VRC 43	VRC 53	VRC 83	VRC 103	VRC 128	VRC 110	VRC 135	VRC 155	VRC 185	VRC 195	VRC 200
100111	VRC 39	VRC 44	VRC 54	VRC 84	VRC 104	VRC 129	VRC 109	VRC 134	VRC 154	VRC 184	VRC 194	VRC 199
101000	VRC 40	VRC 45	VRC 55	VRC 85	VRC 105	VRC 130	VRC 108	VRC 133	VRC 153	VRC 183	VRC 193	VRC 198
101001	VRC 41	VRC 46	VRC 56	VRC 86	VRC 106	VRC 131	VRC 107	VRC 132	VRC 152	VRC 182	VRC 192	VRC 197
101010	VRC 42	VRC 47	VRC 57	VRC 87	VRC 107	VRC 132	VRC 106	VRC 131	VRC 151	VRC 181	VRC 191	VRC 196
101011	VRC 43	VRC 48	VRC 58	VRC 88	VRC 108	VRC 133	VRC 105	VRC 130	VRC 150	VRC 180	VRC 190	VRC 195
101100	VRC 44	VRC 49	VRC 59	VRC 89	VRC 109	VRC 134	VRC 104	VRC 129	VRC 149	VRC 179	VRC 189	VRC 194
101101	VRC 45	VRC 50	VRC 60	VRC 90	VRC 110	VRC 135	VRC 103	VRC 128	VRC 148	VRC 178	VRC 188	VRC 193
101110	VRC 46	VRC 51	VRC 61	VRC 91	VRC 111	VRC 136	VRC 102	VRC 127	VRC 147	VRC 177	VRC 187	VRC 192
101111	VRC 47	VRC 52	VRC 62	VRC 92	VRC 112	VRC 137	VRC 101	VRC 126	VRC 146	VRC 176	VRC 186	VRC 191
110000	VRC 48	VRC 53	VRC 63	VRC 93	VRC 113	VRC 138	VRC 100	VRC 125	VRC 145	VRC 175	VRC 185	VRC 190
110001	VRC 49	VRC 54	VRC 64	VRC 94	VRC 114	VRC 139	VRC 99	VRC 124	VRC 144	VRC 174	VRC 184	VRC 189
110010	VRC 50	VRC 55	VRC 65	VRC 95	VRC 115	VRC 140	VRC 98	VRC 123	VRC 143	VRC 173	VRC 183	VRC 188
110011	VRC 51	VRC 56	VRC 66	VRC 96	VRC 116	VRC 141	VRC 97	VRC 122	VRC 142	VRC 172	VRC 182	VRC 187
110100	VRC 52	VRC 57	VRC 67	VRC 97	VRC 117	VRC 142	VRC 96	VRC 121	VRC 141	VRC 171	VRC 181	VRC 186
110101	VRC 53	VRC 58	VRC 68	VRC 98	VRC 118	VRC 143	VRC 95	VRC 120	VRC 140	VRC 170	VRC 180	VRC 185
110110	VRC 54	VRC 59	VRC 69	VRC 99	VRC 119	VRC 144	VRC 94	VRC 119	VRC 139	VRC 169	VRC 179	VRC 184
110111	VRC 55	VRC 60	VRC 70	VRC 100	VRC 120	VRC 145	VRC 93	VRC 118	VRC 138	VRC 168	VRC 178	VRC 183
111000	VRC 56	VRC 61	VRC 71	VRC 101	VRC 121	VRC 146	VRC 92	VRC 117	VRC 137	VRC 167	VRC 177	VRC 182

Register value	Selected voltage											
PKP(N) [5:0]	**VINP (N)1**	**VINP (N)2**	**VINP (N)3**	**VINP (N)4**	**VINP (N)5**	**VINN 6**	**VINP 6**	**VINP (N)7**	**VINP (N)8**	**VINP (N)9**	**VINP (N)10**	**VINP (N)11**
111001	VRC 57	VRC 62	VRC 72	VRC 102	VRC 122	VRC 147	VRC 91	VRC 116	VRC 136	VRC 166	VRC 176	VRC 181
111010	VRC 58	VRC 63	VRC 73	VRC 103	VRC 123	VRC 148	VRC 90	VRC 115	VRC 135	VRC 165	VRC 175	VRC 180
111011	VRC 59	VRC 64	VRC 74	VRC 104	VRC 124	VRC 149	VRC 89	VRC 114	VRC 134	VRC 164	VRC 174	VRC 179
111100	VRC 60	VRC 65	VRC 75	VRC 105	VRC 125	VRC 150	VRC 88	VRC 113	VRC 133	VRC 163	VRC 173	VRC 178
111101	VRC 61	VRC 66	VRC 76	VRC 106	VRC 126	VRC 151	VRC 87	VRC 112	VRC 132	VRC 162	VRC 172	VRC 177
111110	VRC 62	VRC 67	VRC 77	VRC 107	VRC 127	VRC 152	VRC 86	VRC 111	VRC 131	VRC 161	VRC 171	VRC 176
111111	VRC 63	VRC 68	VRC 78	VRC 108	VRC 128	VRC 153	VRC 85	VRC 110	VRC 130	VRC 160	VRC 170	VRC 175

The grayscale levels are determined by the following formulas listed in the following equations.
Negative gamma voltages are calculated with the same equation of positive gamma voltages, but the gray scale is symmetric, which means negative V<0> is equal to positive V<255>. Rt and Ra in the below equations are determined by GLP/N[1:0] Registers as follows.

- GLP/N [1:0]=00, Rt = 220R, Ra=0
- GLP/N [1:0]=01, Rt = 270R, Ra=50R
- GLP/N [1:0]=10, Rt = 270R, Ra=0
- GLP/N [1:0]=11, Rt = 320R, Ra=50R

4.2.7 GRAYSCALE LEVELS

Table 82 Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC0	((219.5R+Ra)/Rt) * (VINP0 - VINP12)+VINP12	PKP0[5:0] = “000000”	VINP1
VRC1	((219R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000001”	
VRC2	((218.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000010”	
VRC3	((218R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000011”	
VRC4	((217.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000100”	
VRC5	((217R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000101”	
VRC6	((216.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000110”	VINP1
VRC7	((216R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “000111”	
VRC8	((215.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001000”	
VRC9	((215R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001001”	
VRC10	((214.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001010”	
VRC11	((214R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001011”	
VRC12	((213.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001100”	
VRC13	((213R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001101”	
VRC14	((212.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001110”	
VRC15	((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “001111”	
VRC16	((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010000”	
VRC17	((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010001”	
VRC18	((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010010”	
VRC19	((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010011”	
VRC20	((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010100”	
VRC21	((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010101”	
VRC22	((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010110”	
VRC23	((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “010111”	
VRC24	((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011000”	
VRC25	((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011001”	
VRC26	((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011010”	
VRC27	((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011011”	
VRC28	((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011100”	
VRC29	((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011101”	
VRC30	((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011110”	
VRC31	((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “011111”	
VRC32	((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100000”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC33	((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100001”	VINP1
VRC34	((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100010”	
VRC35	((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100011”	
VRC36	((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100100”	
VRC37	((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100101”	
VRC38	((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100110”	
VRC39	((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “100111”	
VRC40	((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101000”	
VRC41	((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101001”	
VRC42	((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101010”	
VRC43	((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101011”	
VRC44	((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101100”	
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101101”	
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101110”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “101111”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110000”	
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110001”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110010”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110011”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110100”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110101”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110110”	
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “110111”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111000”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111001”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111010”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111011”	
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111100”	
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111101”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111110”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP0[5:0] = “111111”	
VRC5	((217R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000000”	VINP2
VRC6	((216.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000001”	
VRC7	((216R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000010”	
VRC8	((215.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000011”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC9	((215R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000100”	VINP2
VRC10	((214.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000101”	
VRC11	((214R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000110”	
VRC12	((213.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “000111”	
VRC13	((213R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001000”	
VRC14	((212.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001001”	
VRC15	((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001010”	
VRC16	((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001011”	
VRC17	((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001100”	
VRC18	((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001101”	
VRC19	((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001110”	
VRC20	((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “001111”	
VRC21	((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010000”	
VRC22	((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010001”	
VRC23	((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010010”	
VRC24	((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010011”	
VRC25	((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010100”	
VRC26	((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010101”	
VRC27	((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010110”	
VRC28	((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “010111”	
VRC29	((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011000”	
VRC30	((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011001”	
VRC31	((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011010”	
VRC32	((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011011”	
VRC33	((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011100”	
VRC34	((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011101”	
VRC35	((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011110”	
VRC36	((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “011111”	
VRC37	((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100000”	
VRC38	((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100001”	
VRC39	((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100010”	
VRC40	((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100011”	
VRC41	((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100100”	
VRC42	((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100101”	
VRC43	((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100110”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC44	((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “100111”	VINP2
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101000”	
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101001”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101010”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101011”	
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101100”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101101”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101110”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “101111”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110000”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110001”	
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110010”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110011”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110100”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110101”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110110”	
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “110111”	
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111000”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111001”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111010”	
VRC64	((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111011”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111100”	
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111101”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111110”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP1[5:0] = “111111”	
VRC15	((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000000”	VINP3
VRC16	((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000001”	
VRC17	((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000010”	
VRC18	((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000011”	
VRC19	((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000100”	
VRC20	((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000101”	
VRC21	((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000110”	
VRC22	((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “000111”	
VRC23	((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001000”	
VRC24	((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001001”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC25	((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001010”	VINP3
VRC26	((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001011”	
VRC27	((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001100”	
VRC28	((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001101”	
VRC29	((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001110”	
VRC30	((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “001111”	
VRC31	((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010000”	
VRC32	((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010001”	
VRC33	((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010010”	
VRC34	((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010011”	
VRC35	((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010100”	
VRC36	((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010101”	
VRC37	((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010110”	
VRC38	((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “010111”	
VRC39	((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011000”	
VRC40	((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011001”	
VRC41	((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011010”	
VRC42	((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011011”	
VRC43	((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011100”	
VRC44	((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011101”	
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011110”	
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “011111”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100000”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100001”	
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100010”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100011”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100100”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100101”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100110”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “100111”	
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101000”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101001”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101010”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101011”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101100”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101101”	VINP3
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101110”	
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “101111”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110000”	
VRC64	((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110001”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110010”	
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110011”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110100”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110101”	
VRC69	((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110110”	
VRC70	((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “110111”	
VRC71	((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111000”	
VRC72	((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111001”	
VRC73	((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111010”	
VRC74	((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111011”	
VRC75	((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111100”	
VRC76	((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111101”	
VRC77	((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111110”	
VRC78	((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP2[5:0] = “111111”	
VRC45	((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000000”	VINP4
VRC46	((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000001”	
VRC47	((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000010”	
VRC48	((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000011”	
VRC49	((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000100”	
VRC50	((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000101”	
VRC51	((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000110”	
VRC52	((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “000111”	
VRC53	((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001000”	
VRC54	((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001001”	
VRC55	((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001010”	
VRC56	((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001011”	
VRC57	((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001100”	
VRC58	((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001101”	
VRC59	((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001110”	
VRC60	((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “001111”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC61	((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010000”	VINP4
VRC62	((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010001”	
VRC63	((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010010”	
VRC64	((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010011”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010100”	
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010101”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010110”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “010111”	
VRC69	((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011000”	
VRC70	((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011001”	
VRC71	((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011010”	
VRC72	((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011011”	
VRC73	((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011100”	
VRC74	((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011101”	
VRC75	((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011110”	
VRC76	((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “011111”	
VRC77	((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100000”	
VRC78	((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100001”	
VRC79	((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100010”	
VRC80	((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100011”	
VRC81	((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100100”	
VRC82	((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100101”	
VRC83	((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100110”	
VRC84	((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “100111”	
VRC85	((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101000”	
VRC86	((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101001”	
VRC87	((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101010”	
VRC88	((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101011”	
VRC89	((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101100”	
VRC90	((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101101”	
VRC91	((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101110”	
VRC92	((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “101111”	
VRC93	((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110000”	
VRC94	((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110001”	
VRC95	((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110010”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC96	((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110011”	VINP4
VRC97	((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110100”	
VRC98	((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110101”	
VRC99	((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110110”	
VRC100	((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “110111”	
VRC101	((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111000”	
VRC102	((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111001”	
VRC103	((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111010”	
VRC104	((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111011”	
VRC105	((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111100”	
VRC106	((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111101”	
VRC107	((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111110”	
VRC108	((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP3[5:0] = “111111”	
VRC65	((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000000”	VINP5
VRC66	((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000001”	
VRC67	((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000010”	
VRC68	((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000011”	
VRC69	((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000100”	
VRC70	((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000101”	
VRC71	((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000110”	
VRC72	((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “000111”	
VRC73	((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001000”	
VRC74	((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001001”	
VRC75	((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001010”	
VRC76	((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001011”	
VRC77	((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001100”	
VRC78	((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001101”	
VRC79	((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001110”	
VRC80	((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “001111”	
VRC81	((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010000”	
VRC82	((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010001”	
VRC83	((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010010”	
VRC84	((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010011”	
VRC85	((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010100”	
VRC86	((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010101”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC87	((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010110”	VINP5
VRC88	((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “010111”	
VRC89	((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011000”	
VRC90	((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011001”	
VRC91	((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011010”	
VRC92	((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011011”	
VRC93	((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011100”	
VRC94	((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011101”	
VRC95	((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011110”	
VRC96	((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “011111”	
VRC97	((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100000”	
VRC98	((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100001”	
VRC99	((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100010”	
VRC100	((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100011”	
VRC101	((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100100”	
VRC102	((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100101”	
VRC103	((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100110”	
VRC104	((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “100111”	
VRC105	((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101000”	
VRC106	((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101001”	
VRC107	((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101010”	
VRC108	((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101011”	
VRC109	((120R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101100”	
VRC110	((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101101”	
VRC111	((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101110”	
VRC112	((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “101111”	
VRC113	((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110000”	
VRC114	((115R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110001”	
VRC115	((114R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110010”	
VRC116	((113R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110011”	
VRC117	((112R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110100”	
VRC118	((111R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110101”	
VRC119	((110R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110110”	
VRC120	((109R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “110111”	
VRC121	((108R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111000”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC122	((107R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111001”	
VRC123	((106R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111010”	
VRC124	((105R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111011”	
VRC125	((104R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111100”	
VRC126	((103R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111101”	
VRC127	((102R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111110”	
VRC128	((101R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP4[5:0] = “111111”	
VRC148	((81R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000000”	VINP6
VRC147	((82R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000001”	
VRC146	((83R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000010”	
VRC145	((84R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000011”	
VRC144	((85R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000100”	
VRC143	((86R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000101”	
VRC142	((87R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000110”	
VRC141	((88R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “000111”	
VRC140	((89R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001000”	
VRC139	((90R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001001”	
VRC138	((91R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001010”	
VRC137	((92R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001011”	
VRC136	((93R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001100”	
VRC135	((94R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001101”	
VRC134	((95R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001110”	
VRC133	((96R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “001111”	
VRC132	((97R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010000”	
VRC131	((98R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010001”	
VRC130	((99R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010010”	
VRC129	((100R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010011”	
VRC128	((101R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010100”	
VRC127	((102R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010101”	
VRC126	((103R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010110”	
VRC125	((104R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “010111”	
VRC124	((105R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011000”	
VRC123	((106R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011001”	
VRC122	((107R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011010”	
VRC121	((108R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011011”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC120	((109R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011100”	VINP6
VRC119	((110R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011101”	
VRC118	((111R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011110”	
VRC117	((112R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “011111”	
VRC116	((113R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100000”	
VRC115	((114R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100001”	
VRC114	((115R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100010”	
VRC113	((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100011”	
VRC112	((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100100”	
VRC111	((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100101”	
VRC110	((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100110”	
VRC109	((120R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “100111”	
VRC108	((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101000”	
VRC107	((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101001”	
VRC106	((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101010”	
VRC105	((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101011”	
VRC104	((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101100”	
VRC103	((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101101”	
VRC102	((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101110”	
VRC101	((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “101111”	
VRC100	((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110000”	
VRC99	((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110001”	
VRC98	((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110010”	
VRC97	((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110011”	
VRC96	((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110100”	
VRC95	((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110101”	
VRC94	((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110110”	
VRC93	((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “110111”	
VRC92	((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111000”	
VRC91	((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111001”	
VRC90	((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111010”	
VRC89	((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111011”	
VRC88	((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111100”	
VRC87	((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111101”	
VRC86	((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111110”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC85	((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP5[5:0] = “111111”	
VRC173	((56R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000000”	VINP7
VRC172	((57R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000001”	
VRC171	((58R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000010”	
VRC170	((59R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000011”	
VRC169	((60R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000100”	
VRC168	((61R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000101”	
VRC167	((62R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000110”	
VRC166	((63R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “000111”	
VRC165	((64R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001000”	
VRC164	((65R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001001”	
VRC163	((66R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001010”	
VRC162	((67R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001011”	
VRC161	((68R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001100”	
VRC160	((69R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001101”	
VRC159	((70R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001110”	
VRC158	((71R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “001111”	
VRC157	((72R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010000”	
VRC156	((73R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010001”	
VRC155	((74R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010010”	
VRC154	((75R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010011”	
VRC153	((76R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010100”	
VRC152	((77R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010101”	
VRC151	((78R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010110”	
VRC150	((79R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “010111”	
VRC149	((80R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011000”	
VRC148	((81R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011001”	
VRC147	((82R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011010”	
VRC146	((83R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011011”	
VRC145	((84R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011100”	
VRC144	((85R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011101”	
VRC143	((86R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011110”	
VRC142	((87R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “011111”	
VRC141	((88R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100000”	
VRC140	((89R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100001”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC139	((90R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100010”	VINP7
VRC138	((91R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100011”	
VRC137	((92R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100100”	
VRC136	((93R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100101”	
VRC135	((94R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100110”	
VRC134	((95R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “100111”	
VRC133	((96R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101000”	
VRC132	((97R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101001”	
VRC131	((98R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101010”	
VRC130	((99R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101011”	
VRC129	((100R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101100”	
VRC128	((101R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101101”	
VRC127	((102R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101110”	
VRC126	((103R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “101111”	
VRC125	((104R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110000”	
VRC124	((105R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110001”	
VRC123	((106R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110010”	
VRC122	((107R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110011”	
VRC121	((108R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110100”	
VRC120	((109R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110101”	
VRC119	((110R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110110”	
VRC118	((111R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “110111”	
VRC117	((112R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111000”	
VRC116	((113R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111001”	
VRC115	((114R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111010”	
VRC114	((115R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111011”	
VRC113	((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111100”	
VRC112	((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111101”	
VRC111	((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111110”	
VRC110	((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP6[5:0] = “111111”	
VRC193	((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000000”	VINP8
VRC192	((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000001”	
VRC191	((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000010”	
VRC190	((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000011”	
VRC189	((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000100”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC188	((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000101”	VINP8
VRC187	((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000110”	
VRC186	((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “000111”	
VRC185	((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001000”	
VRC184	((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001001”	
VRC183	((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001010”	
VRC182	((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001011”	
VRC181	((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001100”	
VRC180	((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001101”	
VRC179	((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001110”	
VRC178	((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “001111”	
VRC177	((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010000”	
VRC176	((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010001”	
VRC175	((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010010”	
VRC174	((55R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010011”	
VRC173	((56R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010100”	
VRC172	((57R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010101”	
VRC171	((58R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010110”	
VRC170	((59R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “010111”	
VRC169	((60R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011000”	
VRC168	((61R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011001”	
VRC167	((62R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011010”	
VRC166	((63R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011011”	
VRC165	((64R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011100”	
VRC164	((65R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011101”	
VRC163	((66R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011110”	
VRC162	((67R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “011111”	
VRC161	((68R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100000”	
VRC160	((69R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100001”	
VRC159	((70R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100010”	
VRC158	((71R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100011”	
VRC157	((72R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100100”	
VRC156	((73R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100101”	
VRC155	((74R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100110”	
VRC154	((75R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “100111”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC153	((76R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101000”	VINP8
VRC152	((77R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101001”	
VRC151	((78R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101010”	
VRC150	((79R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101011”	
VRC149	((80R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101100”	
VRC148	((81R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101101”	
VRC147	((82R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101110”	
VRC146	((83R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “101111”	
VRC145	((84R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110000”	
VRC144	((85R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110001”	
VRC143	((86R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110010”	
VRC142	((87R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110011”	
VRC141	((88R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110100”	
VRC140	((89R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110101”	
VRC139	((90R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110110”	
VRC138	((91R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “110111”	
VRC137	((92R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111000”	
VRC136	((93R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111001”	
VRC135	((94R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111010”	
VRC134	((95R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111011”	
VRC133	((96R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111100”	
VRC132	((97R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111101”	
VRC131	((98R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111110”	
VRC130	((99R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP7[5:0] = “111111”	
VRC223	((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000000”	VINP9
VRC222	((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000001”	
VRC221	((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000010”	
VRC220	((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000011”	
VRC219	((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000100”	
VRC218	((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000101”	
VRC217	((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000110”	
VRC216	((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “000111”	
VRC215	((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001000”	
VRC214	((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001001”	
VRC213	((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001010”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC212	((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001011”	VINP9
VRC211	((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001100”	
VRC210	((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001101”	
VRC209	((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001110”	
VRC208	((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “001111”	
VRC207	((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010000”	
VRC206	((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010001”	
VRC205	((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010010”	
VRC204	((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010011”	
VRC203	((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010100”	
VRC202	((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010101”	
VRC201	((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010110”	
VRC200	((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “010111”	
VRC199	((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011000”	
VRC198	((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011001”	
VRC197	((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011010”	
VRC196	((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011011”	
VRC195	((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011100”	
VRC194	((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011101”	
VRC193	((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011110”	
VRC192	((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “011111”	
VRC191	((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100000”	
VRC190	((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100001”	
VRC189	((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100010”	
VRC188	((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100011”	
VRC187	((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100100”	
VRC186	((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100101”	
VRC185	((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100110”	
VRC184	((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “100111”	
VRC183	((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101000”	
VRC182	((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101001”	
VRC181	((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101010”	
VRC180	((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101011”	
VRC179	((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101100”	
VRC178	((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101101”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC177	((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101110”	VINP9
VRC176	((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “101111”	
VRC175	((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110000”	
VRC174	((55R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110001”	
VRC173	((56R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110010”	
VRC172	((57R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110011”	
VRC171	((58R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110100”	
VRC170	((59R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110101”	
VRC169	((60R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110110”	
VRC168	((61R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “110111”	
VRC167	((62R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111000”	
VRC166	((63R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111001”	
VRC165	((64R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111010”	
VRC164	((65R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111011”	
VRC163	((66R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111100”	
VRC162	((67R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111101”	
VRC161	((68R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111110”	
VRC160	((69R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP8[5:0] = “111111”	
VRC233	((3R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000000”	VINP10
VRC232	((3.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000001”	
VRC231	((4R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000010”	
VRC230	((4.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000011”	
VRC229	((5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000100”	
VRC228	((5.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000101”	
VRC227	((6R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000110”	
VRC226	((6.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “000111”	
VRC225	((7R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001000”	
VRC224	((7.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001001”	
VRC223	((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001010”	
VRC222	((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001011”	
VRC221	((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001100”	
VRC220	((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001101”	
VRC219	((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001110”	
VRC218	((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “001111”	
VRC217	((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010000”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC216	((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010001”	VINP10
VRC215	((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010010”	
VRC214	((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010011”	
VRC213	((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010100”	
VRC212	((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010101”	
VRC211	((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010110”	
VRC210	((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “010111”	
VRC209	((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011000”	
VRC208	((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011001”	
VRC207	((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011010”	
VRC206	((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011011”	
VRC205	((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011100”	
VRC204	((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011101”	
VRC203	((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011110”	
VRC202	((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “011111”	
VRC201	((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100000”	
VRC200	((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100001”	
VRC199	((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100010”	
VRC198	((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100011”	
VRC197	((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100100”	
VRC196	((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100101”	
VRC195	((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100110”	
VRC194	((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “100111”	
VRC193	((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101000”	
VRC192	((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101001”	
VRC191	((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101010”	
VRC190	((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101011”	
VRC189	((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101100”	
VRC188	((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101101”	
VRC187	((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101110”	
VRC186	((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “101111”	
VRC185	((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110000”	
VRC184	((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110001”	
VRC183	((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110010”	
VRC182	((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110011”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC181	((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110100”	VINP10
VRC180	((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110101”	
VRC179	((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110110”	
VRC178	((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “110111”	
VRC177	((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111000”	
VRC176	((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111001”	
VRC175	((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111010”	
VRC174	((55R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111011”	
VRC173	((56R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111100”	
VRC172	((57R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111101”	
VRC171	((58R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111110”	
VRC170	((59R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP9[5:0] = “111111”	
VRC238	((0.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000000”	VINP11
VRC237	((1R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000001”	
VRC236	((1.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000010”	
VRC235	((2R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000011”	
VRC234	((2.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000100”	
VRC233	((3R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000101”	
VRC232	((3.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000110”	
VRC231	((4R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “000111”	
VRC230	((4.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001000”	
VRC229	((5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001001”	
VRC228	((5.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001010”	
VRC227	((6R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001011”	
VRC226	((6.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001100”	
VRC225	((7R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001101”	
VRC224	((7.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001110”	
VRC223	((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “001111”	
VRC222	((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010000”	
VRC221	((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010001”	
VRC220	((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010010”	
VRC219	((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010011”	
VRC218	((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010100”	
VRC217	((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010101”	
VRC216	((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010110”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC215	((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “010111”	VINP11
VRC214	((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011000”	
VRC213	((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011001”	
VRC212	((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011010”	
VRC211	((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011011”	
VRC210	((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011100”	
VRC209	((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011101”	
VRC208	((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011110”	
VRC207	((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “011111”	
VRC206	((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100000”	
VRC205	((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100001”	
VRC204	((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100010”	
VRC203	((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100011”	
VRC202	((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100100”	
VRC201	((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100101”	
VRC200	((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100110”	
VRC199	((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “100111”	
VRC198	((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101000”	
VRC197	((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101001”	
VRC196	((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101010”	
VRC195	((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101011”	
VRC194	((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101100”	
VRC193	((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101101”	
VRC192	((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101110”	
VRC191	((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “101111”	
VRC190	((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110000”	
VRC189	((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110001”	
VRC188	((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110010”	
VRC187	((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110011”	
VRC186	((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110100”	
VRC185	((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110101”	
VRC184	((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110110”	
VRC183	((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “110111”	
VRC182	((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111000”	
VRC181	((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111001”	

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC180	((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111010”	
VRC179	((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111011”	
VRC178	((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111100”	
VRC177	((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111101”	
VRC176	((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111110”	
VRC175	((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12	PKP10[5:0] = “111111”	

Table 83 Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 2

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VINP0	V128	VC-(VC-V160)*(0.5/32.5)
V1	VINP1	V129	VC-(VC-V160)*(1.5/32.5)
V2	V1-(V1-V12)*(2.5/21.5)	V130	VC-(VC-V160)*(2.5/32.5)
V3	V1-(V1-V12)*(5/21.5)	V131	VC-(VC-V160)*(4/32.5)
V4	V1-(V1-V12)*(7/21.5)	V132	VC-(VC-V160)*(5/32.5)
V5	V1-(V1-V12)*(9/21.5)	V133	VC-(VC-V160)*(6/32.5)
V6	V1-(V1-V12)*(11/21.5)	V134	VC-(VC-V160)*(7/32.5)
V7	V1-(V1-V12)*(13/21.5)	V135	VC-(VC-V160)*(8/32.5)
V8	V1-(V1-V12)*(15/21.5)	V136	VC-(VC-V160)*(9/32.5)
V9	V1-(V1-V12)*(17/21.5)	V137	VC-(VC-V160)*(10/32.5)
V10	V1-(V1-V12)*(18.5/21.5)	V138	VC-(VC-V160)*(11/32.5)
V11	V1-(V1-V12)*(20/21.5)	V139	VC-(VC-V160)*(12/32.5)
V12	VINP2	V140	VC-(VC-V160)*(13/32.5)
V13	V12-(V12-V19)*(2/13.5)	V141	VC-(VC-V160)*(14/32.5)
V14	V12-(V12-V19)*(4/13.5)	V142	VC-(VC-V160)*(15/32.5)
V15	V12-(V12-V19)*(6/13.5)	V143	VC-(VC-V160)*(16/32.5)
V16	V12-(V12-V19)*(8/13.5)	V144	VC-(VC-V160)*(17/32.5)
V17	V12-(V12-V19)*(10/13.5)	V145	VC-(VC-V160)*(18/32.5)
V18	V12-(V12-V19)*(11.5/13.5)	V146	VC-(VC-V160)*(19/32.5)
V19	VINP3	V147	VC-(VC-V160)*(20/32.5)
V20	V19-(V19-V55)*(2/45)	V148	VC-(VC-V160)*(21/32.5)
V21	V19-(V19-V55)*(3.5/45)	V149	VC-(VC-V160)*(22/32.5)
V22	V19-(V19-V55)*(5/45)	V150	VC-(VC-V160)*(23/32.5)
V23	V19-(V19-V55)*(7/45)	V151	VC-(VC-V160)*(24/32.5)
V24	V19-(V19-V55)*(8.5/45)	V152	VC-(VC-V160)*(25/32.5)
V25	V19-(V19-V55)*(10/45)	V153	VC-(VC-V160)*(26/32.5)
V26	V19-(V19-V55)*(11.5/45)	V154	VC-(VC-V160)*(26.5/32.5)
V27	V19-(V19-V55)*(13/45)	V155	VC-(VC-V160)*(27.5/32.5)
V28	V19-(V19-V55)*(14.5/45)	V156	VC-(VC-V160)*(28.5/32.5)
V29	V19-(V19-V55)*(15.5/45)	V157	VC-(VC-V160)*(29.5/32.5)
V30	V19-(V19-V55)*(17/45)	V158	VC-(VC-V160)*(30.5/32.5)
V31	V19-(V19-V55)*(18.5/45)	V159	VC-(VC-V160)*(31.5/32.5)
V32	V19-(V19-V55)*(19.5/45)	V160	VINP7
V33	V19-(V19-V55)*(21/45)	V161	V160-(V160-V200)*(1/43)
V34	V19-(V19-V55)*(22/45)	V162	V160-(V160-V200)*(2/43)

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V35	V19-(V19-V55)*(23.5/45)	V163	V160-(V160-V200)*(3/43)
V36	V19-(V19-V55)*(24.5/45)	V164	V160-(V160-V200)*(4/43)
V37	V19-(V19-V55)*(26/45)	V165	V160-(V160-V200)*(5/43)
V38	V19-(V19-V55)*(27/45)	V166	V160-(V160-V200)*(6/43)
V39	V19-(V19-V55)*(28/45)	V167	V160-(V160-V200)*(7/43)
V40	V19-(V19-V55)*(29.5/45)	V168	V160-(V160-V200)*(8/43)
V41	V19-(V19-V55)*(30.5/45)	V169	V160-(V160-V200)*(9/43)
V42	V19-(V19-V55)*(31.5/45)	V170	V160-(V160-V200)*(10/43)
V43	V19-(V19-V55)*(33/45)	V171	V160-(V160-V200)*(11/43)
V44	V19-(V19-V55)*(34/45)	V172	V160-(V160-V200)*(12/43)
V45	V19-(V19-V55)*(35/45)	V173	V160-(V160-V200)*(13/43)
V46	V19-(V19-V55)*(36/45)	V174	V160-(V160-V200)*(14/43)
V47	V19-(V19-V55)*(37/45)	V175	V160-(V160-V200)*(15/43)
V48	V19-(V19-V55)*(38/45)	V176	V160-(V160-V200)*(16/43)
V49	V19-(V19-V55)*(39/45)	V177	V160-(V160-V200)*(17/43)
V50	V19-(V19-V55)*(40/45)	V178	V160-(V160-V200)*(18/43)
V51	V19-(V19-V55)*(41/45)	V179	V160-(V160-V200)*(19/43)
V52	V19-(V19-V55)*(42/45)	V180	V160-(V160-V200)*(20/43)
V53	V19-(V19-V55)*(43/45)	V181	V160-(V160-V200)*(21/43)
V54	V19-(V19-V55)*(44/45)	V182	V160-(V160-V200)*(22/43)
V55	VINP4	V183	V160-(V160-V200)*(22.5/43)
V56	V55-(V55-V95)*(1.5/43)	V184	V160-(V160-V200)*(23.5/43)
V57	V55-(V55-V95)*(2.5/43)	V185	V160-(V160-V200)*(24.5/43)
V58	V55-(V55-V95)*(4/43)	V186	V160-(V160-V200)*(25.5/43)
V59	V55-(V55-V95)*(5/43)	V187	V160-(V160-V200)*(26.5/43)
V60	V55-(V55-V95)*(6.5/43)	V188	V160-(V160-V200)*(27.5/43)
V61	V55-(V55-V95)*(7.5/43)	V189	V160-(V160-V200)*(28.5/43)
V62	V55-(V55-V95)*(9/43)	V190	V160-(V160-V200)*(30/43)
V63	V55-(V55-V95)*(10/43)	V191	V160-(V160-V200)*(32/43)
V64	V55-(V55-V95)*(11/43)	V192	V160-(V160-V200)*(33.5/43)
V65	V55-(V55-V95)*(12.5/43)	V193	V160-(V160-V200)*(34.5/43)
V66	V55-(V55-V95)*(13.5/43)	V194	V160-(V160-V200)*(36/43)
V67	V55-(V55-V95)*(14.5/43)	V195	V160-(V160-V200)*(37/43)
V68	V55-(V55-V95)*(16/43)	V196	V160-(V160-V200)*(38/43)
V69	V55-(V55-V95)*(17/43)	V197	V160-(V160-V200)*(39.5/43)
V70	V55-(V55-V95)*(18/43)	V198	V160-(V160-V200)*(40.5/43)

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V71	V55-(V55-V95)*(19/43)	V199	V160-(V160-V200)*(42/43)
V72	V55-(V55-V95)*(20/43)	V200	VINP8
V73	V55-(V55-V95)*(21/43)	V201	V200-(V200-V236)*(1/45)
V74	V55-(V55-V95)*(22/43)	V202	V200-(V200-V236)*(2/45)
V75	V55-(V55-V95)*(23/43)	V203	V200-(V200-V236)*(3/45)
V76	V55-(V55-V95)*(24.5/43)	V204	V200-(V200-V236)*(3.5/45)
V77	V55-(V55-V95)*(25.5/43)	V205	V200-(V200-V236)*(4.5/45)
V78	V55-(V55-V95)*(27/43)	V206	V200-(V200-V236)*(5.5/45)
V79	V55-(V55-V95)*(28/43)	V207	V200-(V200-V236)*(6.5/45)
V80	V55-(V55-V95)*(29/43)	V208	V200-(V200-V236)*(7/45)
V81	V55-(V55-V95)*(30/43)	V209	V200-(V200-V236)*(8/45)
V82	V55-(V55-V95)*(31/43)	V210	V200-(V200-V236)*(9/45)
V83	V55-(V55-V95)*(32/43)	V211	V200-(V200-V236)*(10/45)
V84	V55-(V55-V95)*(33/43)	V212	V200-(V200-V236)*(11/45)
V85	V55-(V55-V95)*(34/43)	V213	V200-(V200-V236)*(12/45)
V86	V55-(V55-V95)*(35/43)	V214	V200-(V200-V236)*(13/45)
V87	V55-(V55-V95)*(35.5/43)	V215	V200-(V200-V236)*(14/45)
V88	V55-(V55-V95)*(36.5/43)	V216	V200-(V200-V236)*(15.5/45)
V89	V55-(V55-V95)*(37.5/43)	V217	V200-(V200-V236)*(16.5/45)
V90	V55-(V55-V95)*(38.5/43)	V218	V200-(V200-V236)*(17.5/45)
V91	V55-(V55-V95)*(39.5/43)	V219	V200-(V200-V236)*(19/45)
V92	V55-(V55-V95)*(40/43)	V220	V200-(V200-V236)*(20/45)
V93	V55-(V55-V95)*(41/43)	V221	V200-(V200-V236)*(21.5/45)
V94	V55-(V55-V95)*(42/43)	V222	V200-(V200-V236)*(23/45)
V95	VINP5	V223	V200-(V200-V236)*(24/45)
V96	V95-(V95-VC)*(1/32.5)	V224	V200-(V200-V236)*(25.5/45)
V97	V95-(V95-VC)*(2.5/32.5)	V225	V200-(V200-V236)*(27/45)
V98	V95-(V95-VC)*(3.5/32.5)	V226	V200-(V200-V236)*(28/45)
V99	V95-(V95-VC)*(4.5/32.5)	V227	V200-(V200-V236)*(29/45)
V100	V95-(V95-VC)*(5.5/32.5)	V228	V200-(V200-V236)*(31/45)
V101	V95-(V95-VC)*(6.5/32.5)	V229	V200-(V200-V236)*(33/45)
V102	V95-(V95-VC)*(7.5/32.5)	V230	V200-(V200-V236)*(34.5/45)
V103	V95-(V95-VC)*(8.5/32.5)	V231	V200-(V200-V236)*(36/45)
V104	V95-(V95-VC)*(9.5/32.5)	V232	V200-(V200-V236)*(37.5/45)
V105	V95-(V95-VC)*(10.5/32.5)	V233	V200-(V200-V236)*(39.5/45)
V106	V95-(V95-VC)*(11.5/32.5)	V234	V200-(V200-V236)*(41/45)

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V107	V95-(V95-VC)*(12.5/32.5)	V235	V200-(V200-V236)*(42/45)
V108	V95-(V95-VC)*(13.5/32.5)	V236	VINP9
V109	V95-(V95-VC)*(14.5/32.5)	V237	V236-(V236-V243)*(1.5/13.5)
V110	V95-(V95-VC)*(16/32.5)	V238	V236-(V236-V243)*(3/13.5)
V111	V95-(V95-VC)*(17/32.5)	V239	V236-(V236-V243)*(4.5/13.5)
V112	V95-(V95-VC)*(18/32.5)	V240	V236-(V236-V243)*(6.5/13.5)
V113	V95-(V95-VC)*(19/32.5)	V241	V236-(V236-V243)*(8.5/13.5)
V114	V95-(V95-VC)*(20/32.5)	V242	V236-(V236-V243)*(10.5./13.5)
V115	V95-(V95-VC)*(21/32.5)	V243	VINP10
V116	V95-(V95-VC)*(22/32.5)	V244	V243-(V243-V254)*(2/21.5)
V117	V95-(V95-VC)*(23/32.5)	V245	V243-(V243-V254)*(4.5/21.5)
V118	V95-(V95-VC)*(23.5/32.5)	V246	V243-(V243-V254)*(7/21.5)
V119	V95-(V95-VC)*(24.5/32.5)	V247	V243-(V243-V254)*(9/21.5)
V120	V95-(V95-VC)*(25.5/32.5)	V248	V243-(V243-V254)*(11.5/21.5)
V121	V95-(V95-VC)*(26.5/32.5)	V249	V243-(V243-V254)*(13.5/21.5)
V122	V95-(V95-VC)*(27.5/32.5)	V250	V243-(V243-V254)*(15.5/21.5)
V123	V95-(V95-VC)*(28.5/32.5)	V251	V243-(V243-V254)*(17.5/21.5)
V124	V95-(V95-VC)*(29.5/32.5)	V252	V243-(V243-V254)*(19/21.5)
V125	V95-(V95-VC)*(30/32.5)	V253	V243-(V243-V254)*(20/21.5)
V126	V95-(V95-VC)*(31/32.5)	V254	VINP11
V127	V95-(V95-VC)*(32/32.5)	V255	VINP12
VC	VINP6		

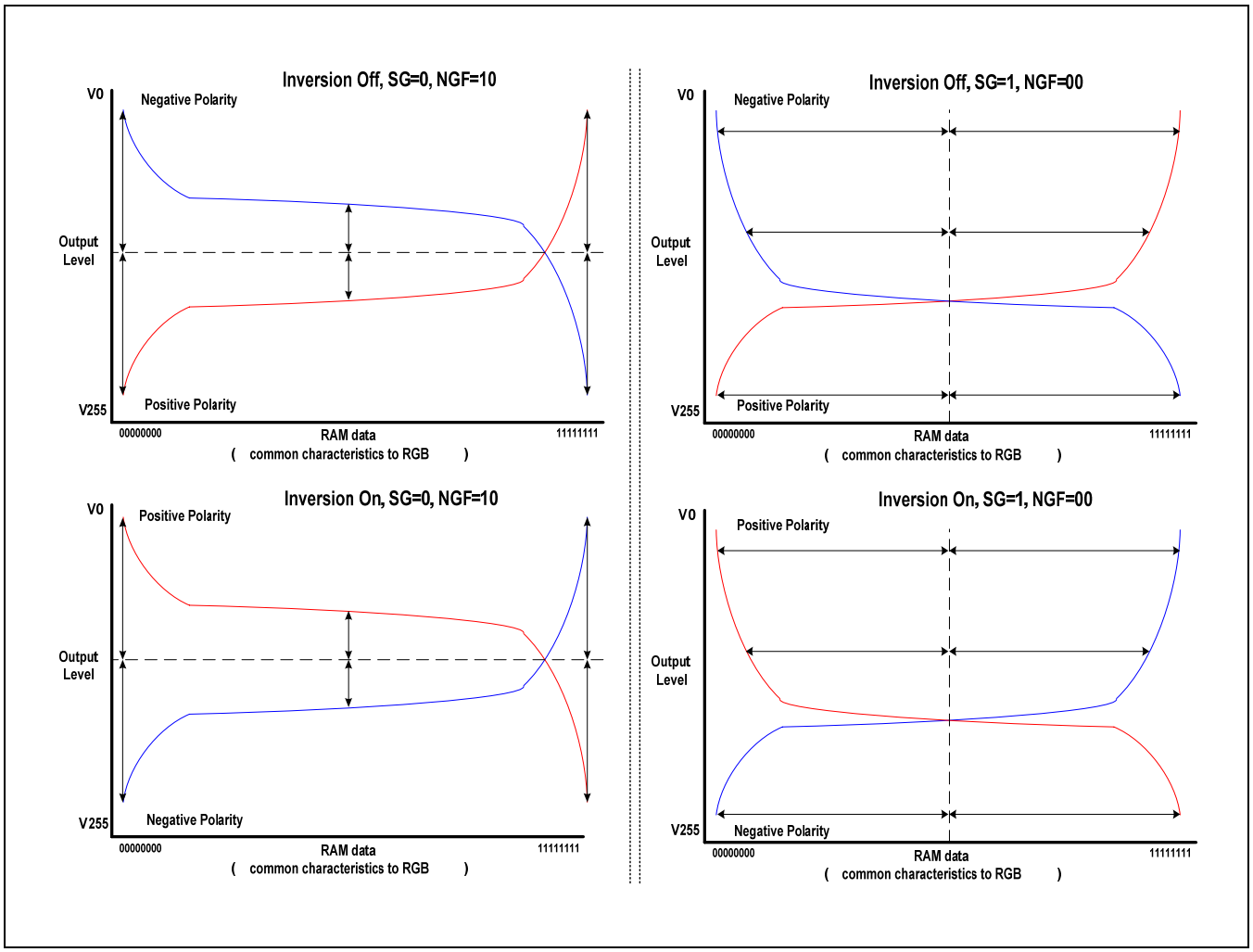


Figure 145 Relationship Between RAM Data and Output Voltage

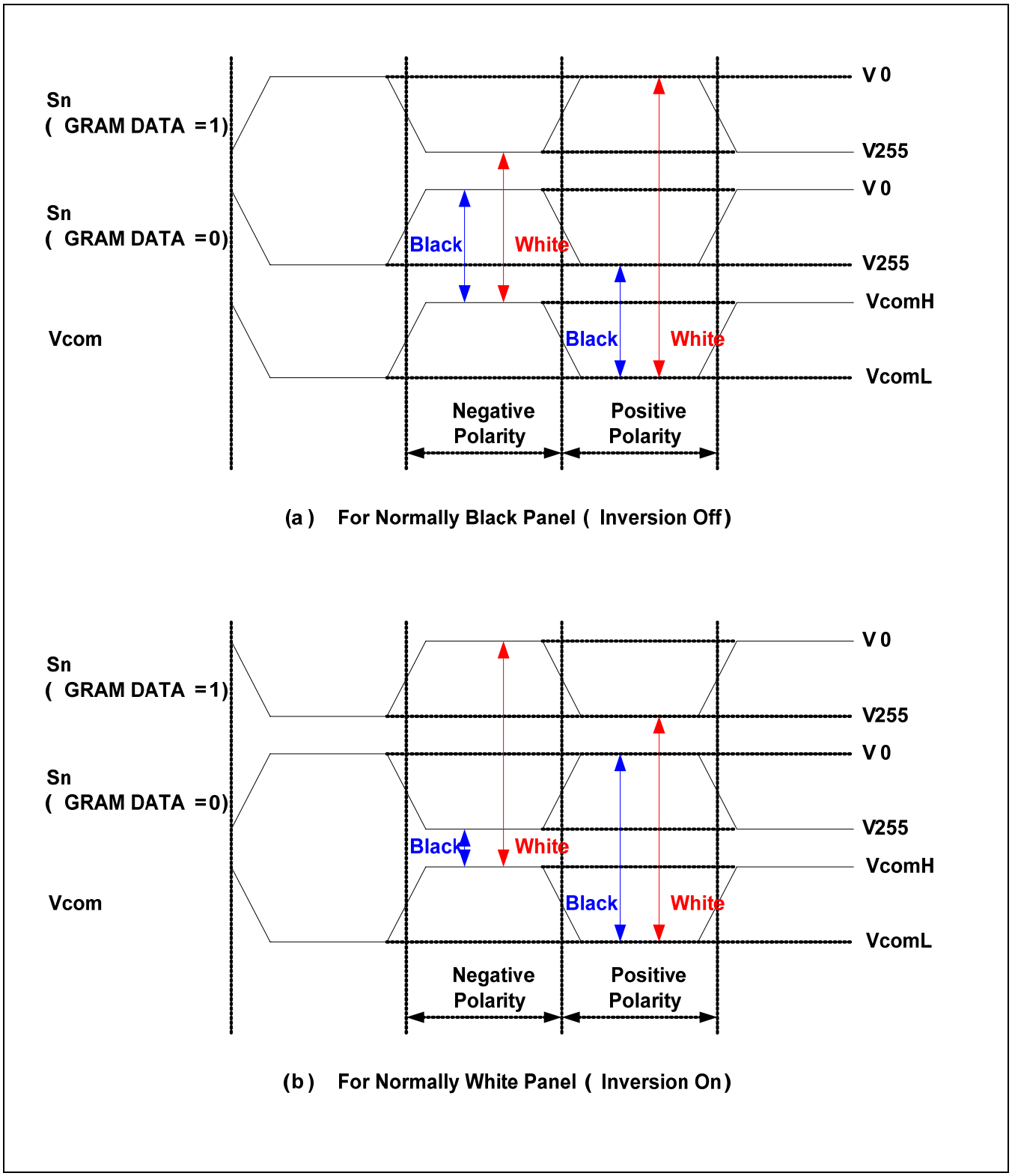


Figure 146 Relationship Between Source Output and VCOM

4.3 GATE

4.3.1 GATE DRIVER

The gate driver block includes gate control outputs (G1 to G480) which should be connected directly to the TFT-LCD.

4.4 OSCILLATOR- SYSTEM CLOCK GENERATOR

S6D05A1 has an on-chip oscillator which does not require any external components. This oscillator output signal is used for the system clock generation for internal display operation.

4.4.1 OSCILLATOR CIRCUIT

The S6D05A1 can provide R-C oscillation. S6D05A1 internal oscillator does not need to attach the external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the oscillator frequency control register setting. Since R-C oscillation stops during the sleep mode, power consumption can be reduced.

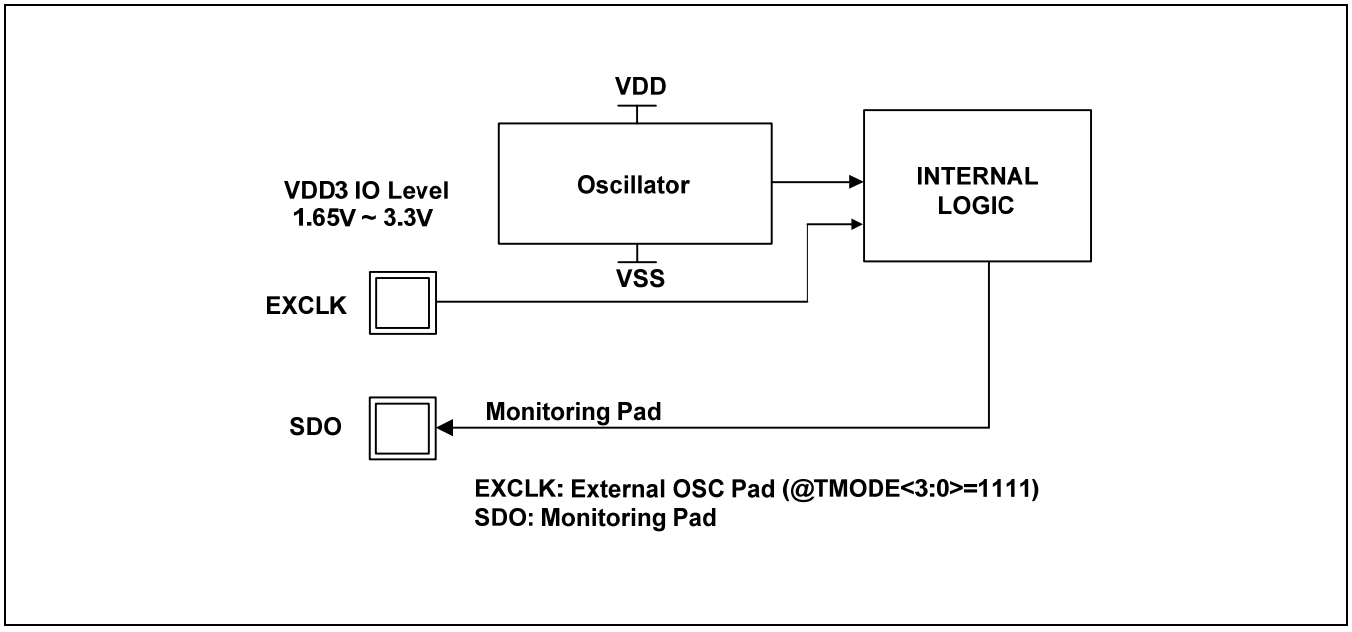


Figure 147 Application Diagram for Oscillator Circuitry

4.4.2 FRAME FREQUENCY ADJUSTING FUNCTION

The S6D05A1 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting during the LCD driver operation as the oscillation frequency is always same. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display is required, the frame frequency can be set high.

The relationship between the LCD driving duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the NHW.

Formula for the frame frequency

$$\text{Frame Frequency} = \frac{\text{Fosc}}{8 \times \text{NHW/PIHW} \times (\text{Line} + \text{B})} \text{ [Hz]}$$

NOTE:

Fosc : R–C oscillation frequency(Fixed to 20MHz)
Line : Number of raster rows
NHW/PIHW : Click cycles per raster rows
B : Blank period(Back porch + Front porch) / B+2 is used in the self refresh mode.

Calculation Example:

- Line : 480
- B : Blank Period (BP+FP) : 16
- Clock cycles of per raset rows : 63 (NHW =011_1111)
- Frame Frequency = 20MHz / (63 x 8 x (480+16)) = 80 Hz
- Frame Frequency = 20MHz / (63 x 8 x (480+18)) = 79.68 Hz (Self refresh mode)

4.5 DISPLAY DATA RAM

This Chapter is based on the assumption that the number of 360-RGB source channels.

4.5.1 ADDRESS COUNTER

The address counter sets the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 8-8-8-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=359 (167h) and Y=0 to Y=479 (1DFh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined onto which it will be written. The window is programmable via the command registers SC, SP designating the start address and EC, EP designating the end address. For example, the whole display contents will be written, and the window will be defined by the following values: SC=0 (0h), SP=0 (0h) and EC=359 (167h), EP=479 (1DFh).

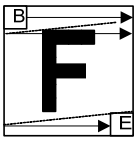
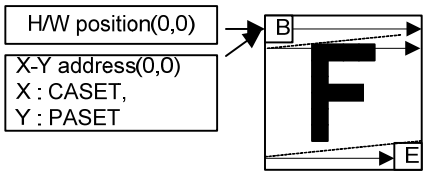
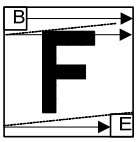
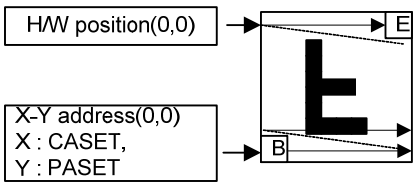
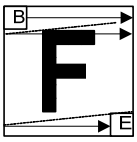
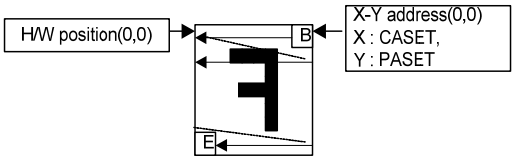
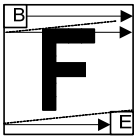
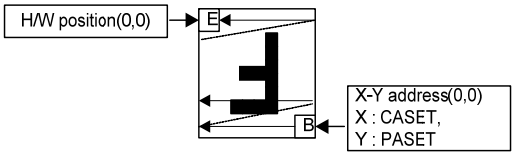
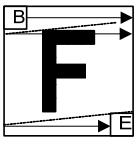
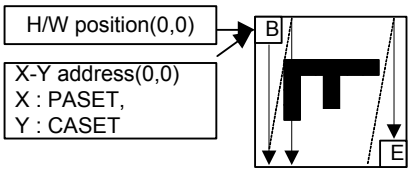
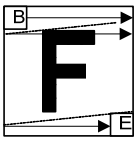
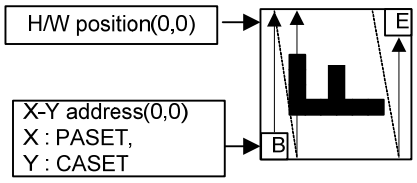
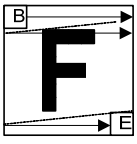
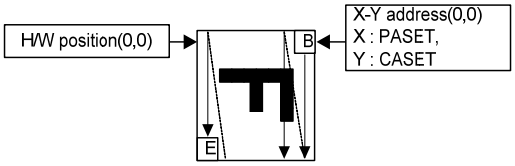
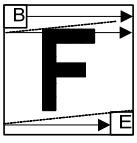
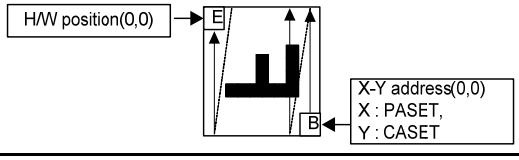
In vertical addressing mode (D5=1), the Y-address increments after each byte. After the last Y-address (Y=EP), Y wraps around to SP and X increments to address the next column. In horizontal addressing mode (D5=0), the X-address increments after each byte. After the last X-address (X=EC), X wraps around to SC and Y increments to address the next page. After every last address (X=EC and Y=EP) the address pointers wrap around to address (X=SC and Y=SP). For flexibility in handling a wide variety of display architectures, the commands “CASET, PASET” and “MADCTL” (see section 5 command lists) define flags D6 and D7, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Following Figure shows the available combinations of writing to the display RAM. When D6, D7 and D5 will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and page counters apply as below:

Table 84 Control for Column and Page Counter

Condition	Column counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “start column(SC)”	Return to “start page(SP)”
Complete pixel read/write action	Increment by 1	No change
The column counter value is large than “End column (EC)”	Return to “start column(SC)”	Increment by 1
The page counter value is large than “End page (EP)”	Return to “start column(SC)”	Return to “start page(SP)”

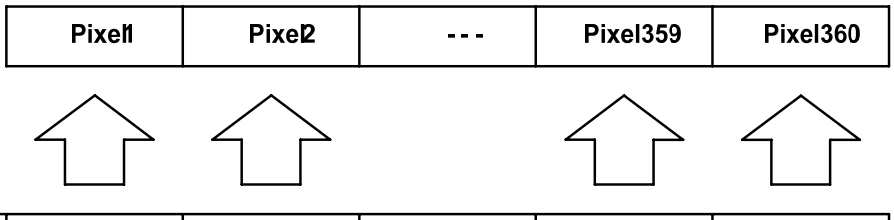
Table 85 Frame Data Write Direction According to the MADCTL Parameters (D5, D6 and D7)

Display Data direction	MADCTL Parameter			Image in the Host(MPU)	Image in the Driver (DDRAM)
	D5	D6	D7		
Normal	0	0	0		
Y-mirror	0	0	1		
X-mirror	0	1	0		
X-mirror Y-mirror	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-mirror	1	0	1		
X-Y exchange X-mirror	1	1	0		
X-Y exchange X-mirror Y-mirror	1	1	1		

NOTE: D5, D6 and D7 are parameters of MADCTL command. D5(MV), D6(MX), D7(MY)

4.5.2 MEMORY TO DISPLAY ADDRESS MAPPING

4.5.2.1 When Using 360RGB x 480 Resolution (MX = MY = RGB = '0')



Source out		S1			S2			- - -	S 359			S 360				
		RGB=0		RGB=1	RGB=0		RGB=1	RGB order	RGB=0		RGB=1	RGB=0		RGB=1		
RA															SA	
MY =0	MY =1														ML= 0	ML =1
0	479	$R0_{7-0}$	$G0_{7-0}$	$B0_{7-0}$	$R1_{7-0}$	$G1_{7-0}$	$B1_{7-0}$		$R358_{7-0}$	$G358_{7-0}$	$B358_{7-0}$	$R359_{7-0}$	$G359_{7-0}$	$B359_{7-0}$	0	479
1	478							- - -							1	478
2	477							- - -							2	477
3	476							- - -							3	476
4	475							- - -							4	475
5	474							- - -							5	474
6	473							- - -							6	473
7	472							- - -							7	472
8	471							- - -							8	471
9	470							- - -							9	470
10	469							- - -							10	469
11	468							- - -							11	468
		Display pattern data														
472	7							- - -							472	7
473	6							- - -							473	6
474	5							- - -							474	5
475	4							- - -							475	4
476	3							- - -							476	3
477	2							- - -							477	2
478	1							- - -							478	1
479	0							- - -							479	0
CA	MX =0	0			1			- - -	358			359				
	MX =1	359			358			- - -	1			0				

NOTE:
RA = Page Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Page address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

Figure 148 Memory to Display Address Mapping

4.5.3 NORMAL DISPLAY ON OR PARTIAL MODE ON

4.5.3.1 When Using 360RGB x 480 Resolution

In this mode, the content of the frame memory within an area where column pointer is 00h to 167h and page pointer is 000h to 1DFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

1). Example for Normal Display On (D6 = D7 = D4 = '0')

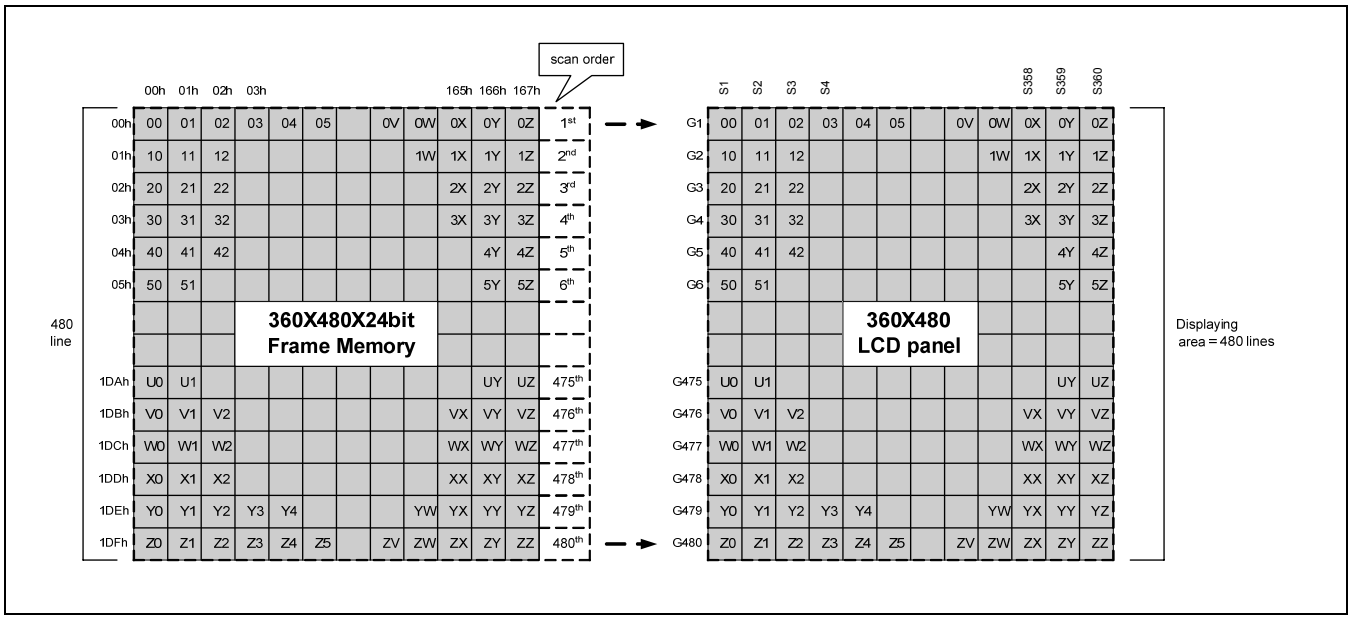


Figure 149 Example for Normal Display On (D6 = D7 = D4 = '0')

2). Partial Display On: SR [15:0] = 04h, ER [15:0] = 1DCh, MADCTL

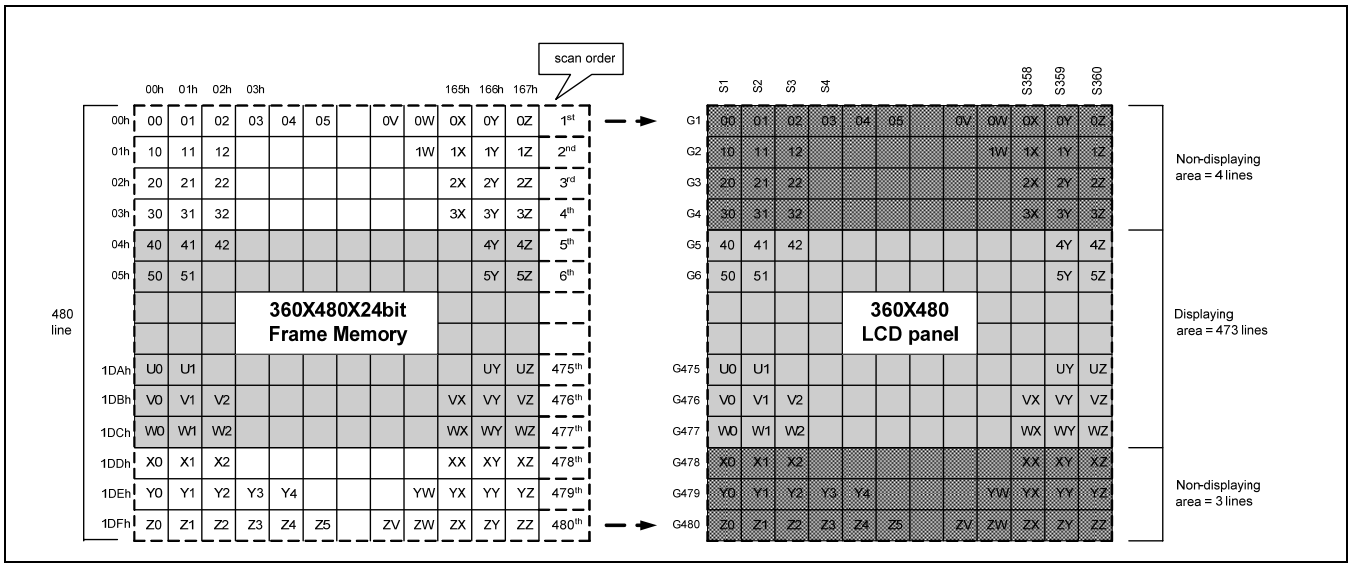


Figure 150 Partial Display on: SR [15:0] = 04h, ER [15:0] = 1DCh, MADCTL

4.5.4 COMMAND DEFINITION IS INDEPENDENT OF THE IC MOUNT POSITION

Depending on how the MADCTL command is set, the top-bottom / left-right definitions are changed in the driver IC to adapt to the mounted form.

4.5.4.1 Model of LCD Module for the S6D05A1

The LCD module for the S6D05A1 is shown below. The top-bottom / left-right positions, RGB filter and white/ black back ground defined in this development specification are in accordance with the diagram shown below.

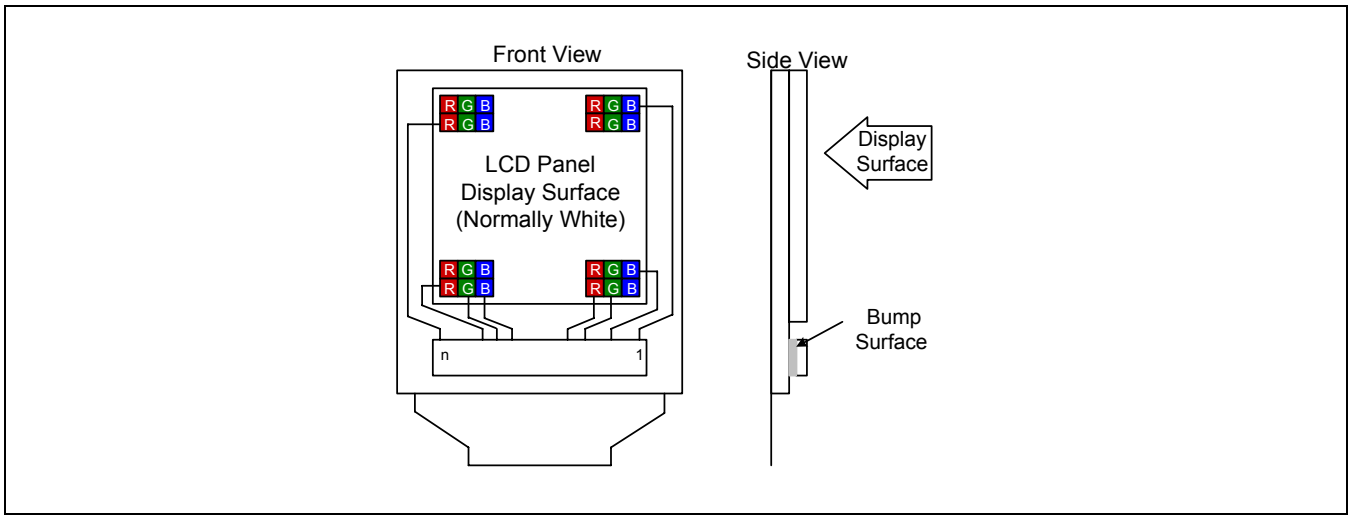


Figure 151 Model of LCD Module for the S6D05A1

In the case of MADCTL set to “00h,” the result of memory access is controlled as show below.

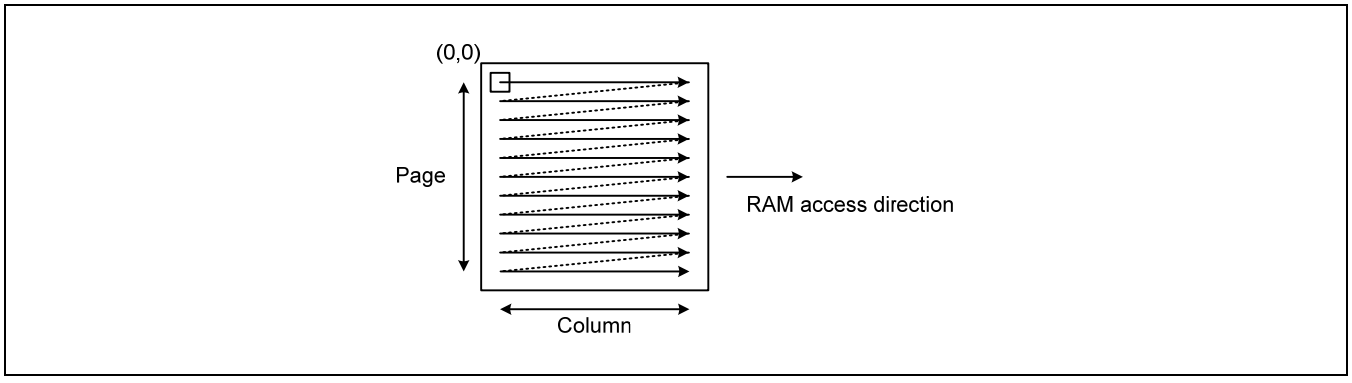
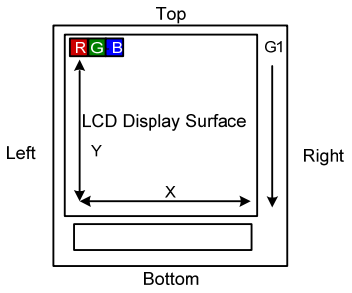
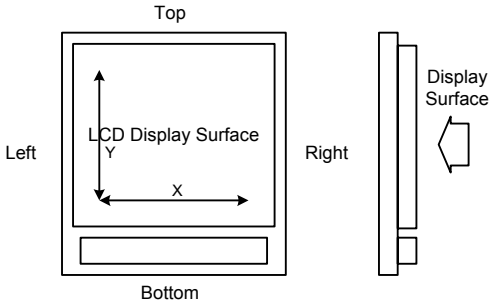
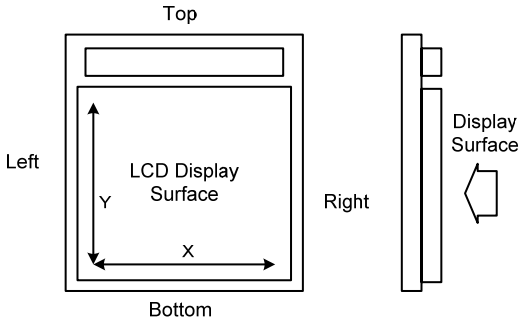
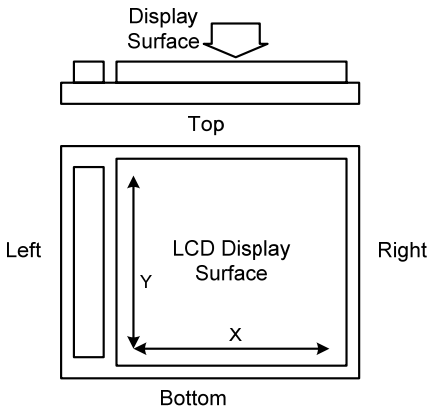
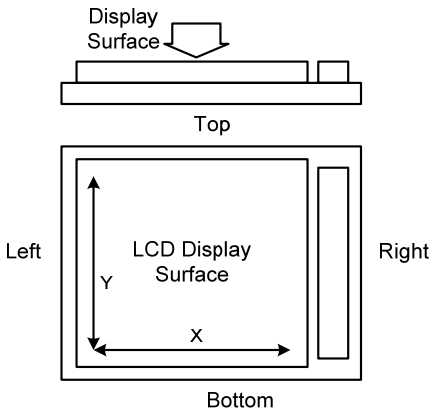


Figure 152 An Example of MADCTL(00h)

Refer to the top-bottom / left-right relationship. (The non-bump plane is the surface.)
If the driver IC is left-mounted or right-mounted due to the device structure, the display data RAM to LCD display data readout and gate scan direction should be set left-right rather than top-bottom.

Table 86 Cases of Panel Position Mounted IC

<table>
<tr><th colspan="4">Case of bottom-mounted IC</th></tr>
<tr><td colspan="4"> 

IFCTL(Level2 command) = 48h</td></tr>
<tr><th colspan="2">0° rotated MADCTL(00h)</th><th colspan="2">180° rotated MADCTL(D8h)</th></tr>
<tr><td colspan="2"> 
</td><td colspan="2"> 
</td></tr>
<tr><td>RAM address (0,0) Position</td><td>Left-top</td><td>RAM address (0,0) Position</td><td>Left-top</td></tr>
<tr><td>RAM Access Direction</td><td>Column Direction</td><td>RAM Access Direction</td><td>Column Direction</td></tr>
<tr><td>Column</td><td>X direction</td><td>Column</td><td>X direction</td></tr>
<tr><td>Page</td><td>Y direction</td><td>Page</td><td>Y direction</td></tr>
<tr><td>RAM→LCD readout direction</td><td>Top to Bottom</td><td>RAM→LCD readout direction</td><td>Top to Bottom</td></tr>
<tr><td>Gate line scan Direction</td><td>Top to Bottom</td><td>Gate line scan Direction</td><td>Top to Bottom</td></tr>
<tr><th colspan="2">90° rotated MADCTL(A0h)</th><th colspan="2">270° rotated MADCTL(60h)</th></tr>
<tr><td colspan="2"> 
</td><td colspan="2"> 
</td></tr>
</table>

RAM address (0,0) Position	Left-top	RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction	RAM Access Direction	Column Direction
Column	X direction	Column	X direction
Page	Y direction	Page	Y direction
RAM→LCD readout direction	Right to Left	RAM→LCD readout direction	Left to Right
Gate line scan Direction	Right to Left	Gate line scan Direction	Left to Right

4.5.4.2 0-Address Position and RAM Access Scan Direction

Refer to MADCTL

Table 87 0-Address Position and RAM Access Scan Direction (D5=0)

Written image and direction from the host to the frame memory

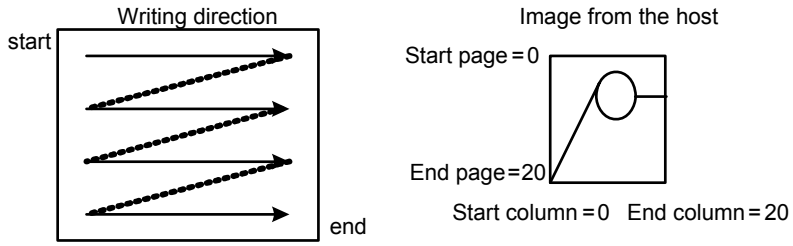


Image position on the frame memory with D7 = 0/1, D6 = 0/1 and D5 = 0

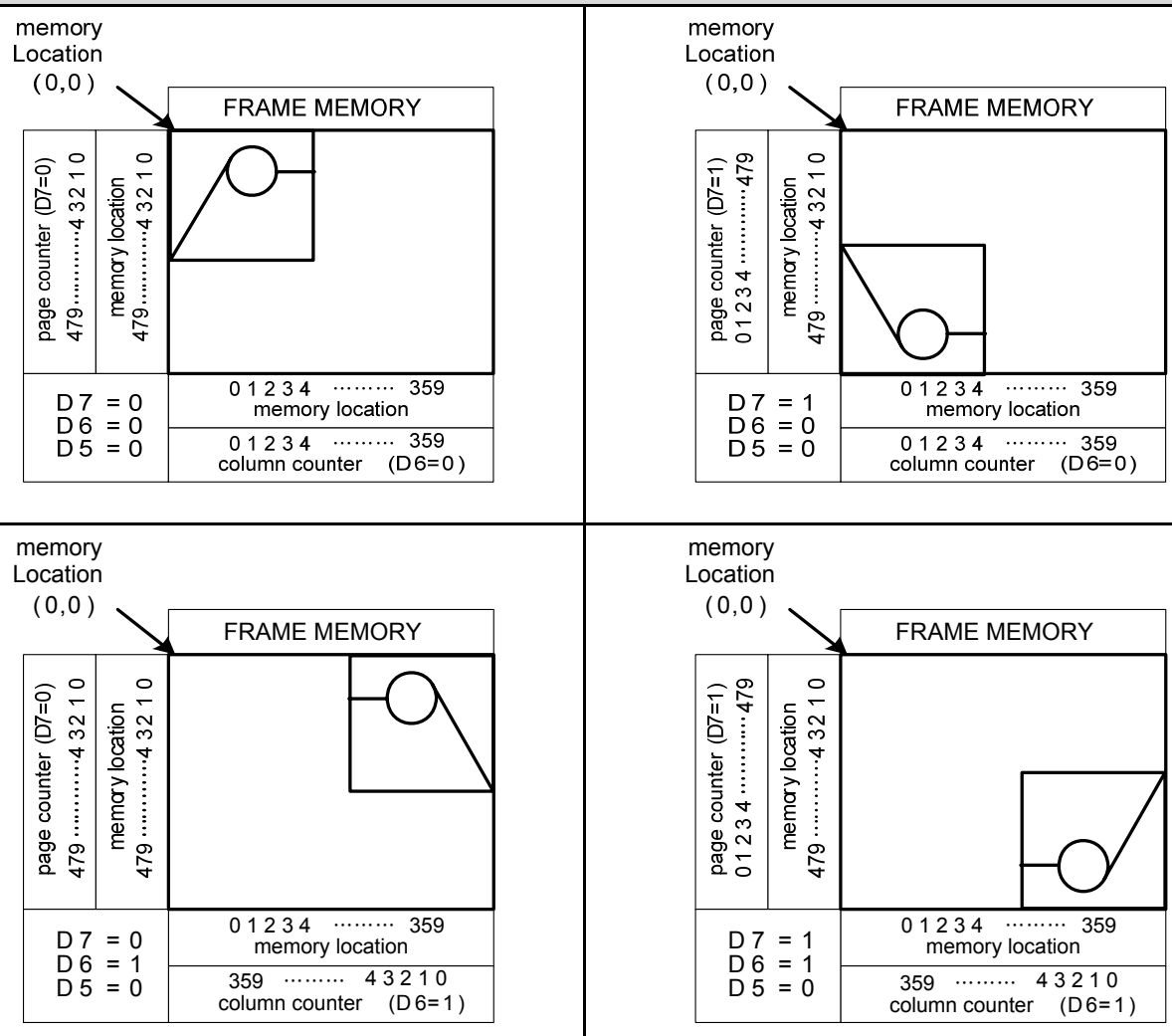


Table 88 0-Address Position and RAM Access Scan Direction (D5=1)

Written image and direction from the host to the frame memory

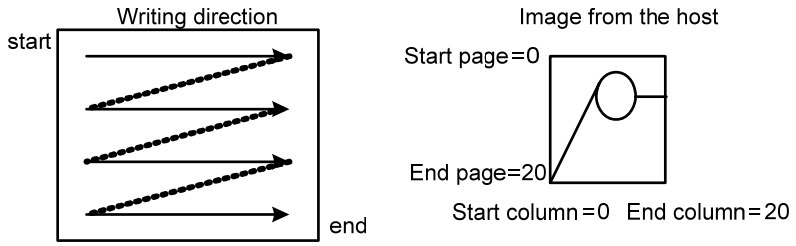
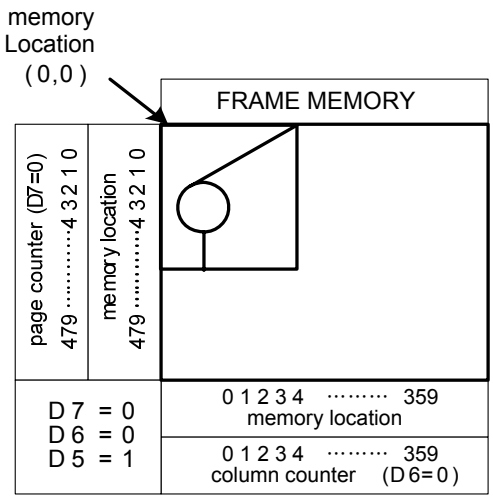
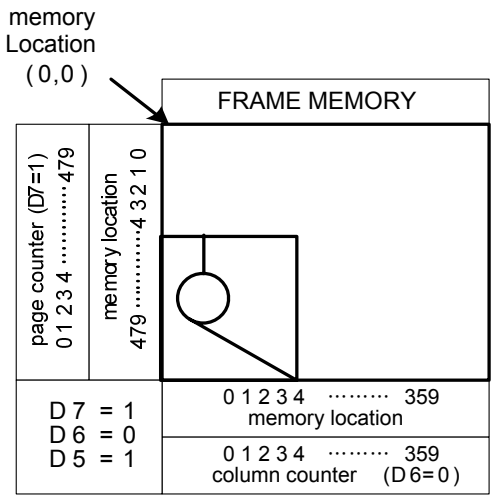
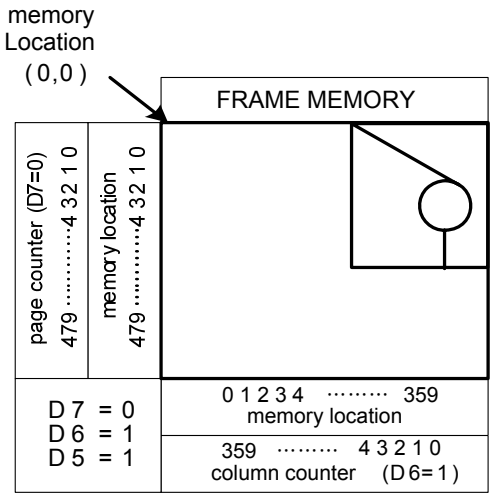
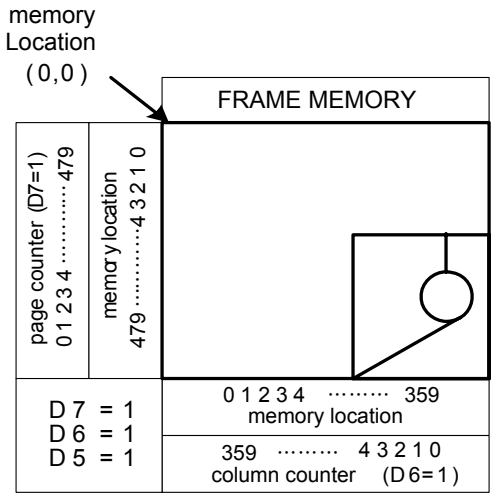


Image position on the frame memory with D7 = 0/1, D6 = 0/1 and D5 = 1





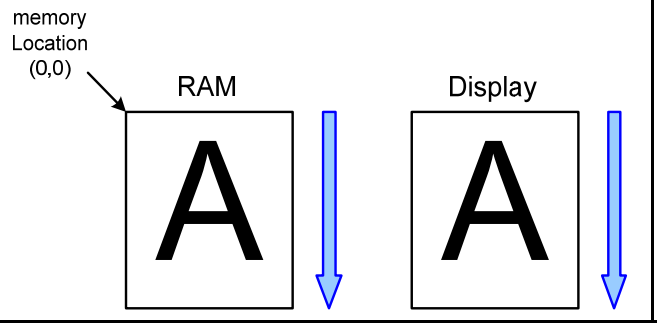
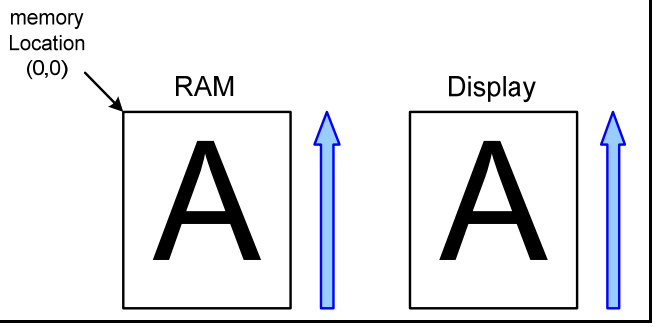




4.5.4.3 LCD Read Scan Direction and Common Scan Direction

Refer to MADCTL

Table 89 LCD Read Scan DIRECTION and common Scan Direction

D4 : Memory Scan Direction	
0	**1**
Top to Bottom	**Bottom to Top**
	

4.5.4.4 Partial Area and Scan Direction

Refer to MADCTL, PTLAR

A. Partial Mode

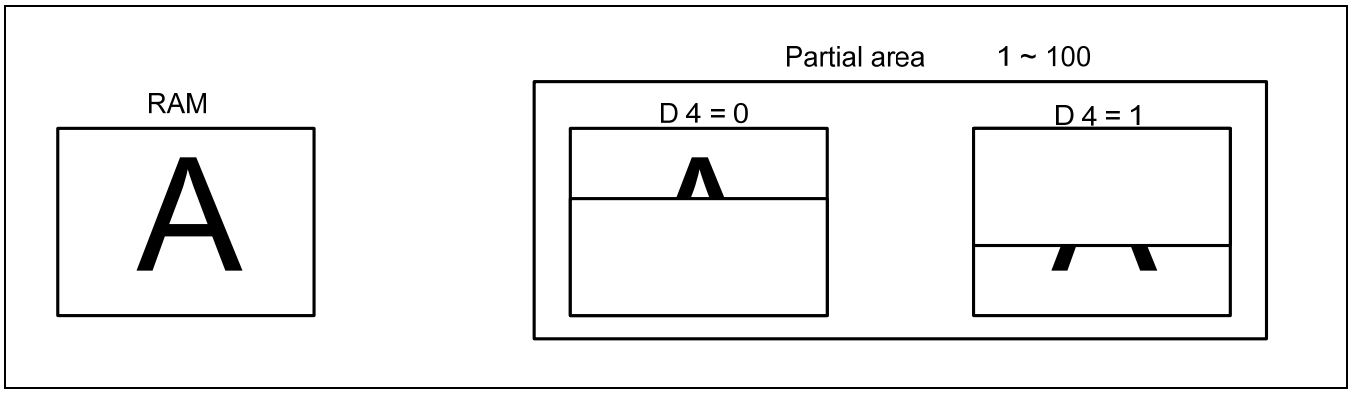


Figure 153 Partial Area and Scan Directi

4.6 RESET

4.6.1 REGISTERS

Table 90 The Default Value of the Register Set (Level I)

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Column: Start Address (SC)	0000h	0000h	0000h
Column: End Address (EC)	013Fh(319d)	013Fh(319d)	013Fh(319d)
Page: Start Address (SP)	0000h	0000h	0000h
Page: End Address (EP)	01DFh (479d)	01DFh (479d)	01DFh (479d)
Partial: Start Address (SR)	0000h	0000h	0000h
Partial: End Address (ER)	01DFh	01DFh	01DFh
Color Pixel Fomat	(77h) IFPF:24bit/pixel VFPF:24bit/pixel	(77h) FPF:24bit/pixel VFPF:24bit/pixel	(77h) FPF:24bit/pixel VFPF:24bit/pixel
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode	00h (Mode1)	00h (Mode1)	00h (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	0/0/0/0/0
RDDST (09h)	00710000h	00710000h	00710000h
Idle Mode	Off	Off	Off
RDDPM (0Ah)	08h	08h	08h
RDDMADCTL (0Bh)	00h	00h	00h
RDDCOLMOD(0Ch)	77h	77h	77h
RDDIM (0Dh)	00h	00h	00h
RDDSM (0Eh)	00h	00h	00h
RDDSDR (0Fh)	00h	00h	00h
TESCL (44h)	00h	00h	00h
RDSCL (45h)	00h	00h	00h
WRDISBV(51h)	00h	00h	00h
RDDISBV(52h)	00h	00h	00h
WRCTRLD(53h)	00h	00h	00h
RDCTRLD(54h)	00h	00h	00h
WRCABC(55h)	00h	00h	00h

Item	After Power On	After Hardware Reset	After Software Reset
RDCABC(56h)	00h	00h	00h
WRCABCMB(5Eh)	00h	00h	00h
RDCABCMB(5Fh)	00h	00h	00h
RDDDBS (A1h)	F0h	F0h	F0h
RDDDBC (A8h)	F0h	F0h	F0h
RDID1 (DAh)	(MTP values)	(MTP values)	(MTP values)
RDID2 (DBh)	(MTP values)	(MTP values)	(MTP values)
RDID3 (DCh)	(MTP values)	(MTP values)	(MTP values)

NOTE: There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.
Powered-On Reset finishes within 10µs after both VDD3 & VCI are applied.
TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

Table 91 The Default Value of the Register Set 1 (Level II)

Item	After Power On / After Hardware Reset / After Software Reset
MIECTL1(C0h)	808010h
BCMODE(C1h)	13h
WRMIECTL2 (C2h)	08_00_00_01_DF_00_00_01_67h
WRBLCTL (C3h)	00_03_14h
MTPCTL (D0h)	0Eh
MTPWR (D2h)	00_00_00_00_00_00h
MTPRD (D3h)	(MTP values)
DSTB (DFh)	00h
MDDICTL (EAh)	00h
MDDILIK (EBh)	00_00h
PASSWD1 (F0h)	A5_A5h
PASSWD2 (F1h)	A5_A5h
DISCTL (F2h)	3B_40_03_08_08_08_08_00_08_08_00_00_00_00_40_08_08_08_08h
MANPWRSEQ (F3h)	03_00_00_00_00h
PWRCTL (F4h)	00_00_00_00_00_00_00_00_04_00_02_04_00_02h
VCMCTL (F5h)	00_00_00_00_00_04_00_00_04_00_00_00h
SRCCTL (F6h)	04_00_08_03_01_00_01_00_00h
IFCTL (F7h)	00_80_10_02_00h
PANELCTL (F8h)	11_00h
GAMMASEL (F9h)	27h
PGAMMACTL (FAh)	00_00_00_00_00_00_00_00_00_00_00_00_00_00_00_00_00h
NGAMMACTL (FBh)	00_00_00_00_00_00_00_00_00_00_00_00_00_00_00_00_00h

4.6.2 MODULS INPUT/OUTPUT/BI-DIRECTION (I/O) PADS

4.6.2.1 Output or Bi-directional (I/O) Pads

Table 92 Reset States of Output Pads

Output or Bi-directional pads	When RESX is Low	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low	Low
DB23 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDA (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDO	Low	Low	Low	Low
BC	Low	Low	Low	Low
BC_CTL	High	High	High	High

NOTE: There will be no output from DB23-DB0 during Power On/Off sequence, Hardware Reset and Software Reset

4.6.2.2 Input Pads

Table 93 Reset States of Input Pads

Input pads	When RESX is Low	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	-	See Section 4.1.1	Input valid	Input valid	Input valid	See Section 4.1.1
CSX	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
DCX	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB23 to DB0 (Input driver)	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
SDA (Input driver)	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input valid (RGB IF) Input invalid (The other cases)
VSYNC	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input valid (RGB IF) Input invalid (The other cases)
DOTCLK	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input valid (RGB IF) Input invalid (The other cases)
ENABLE	Input invalid	Input invalid	Input valid	Input valid	Input valid	Input invalid

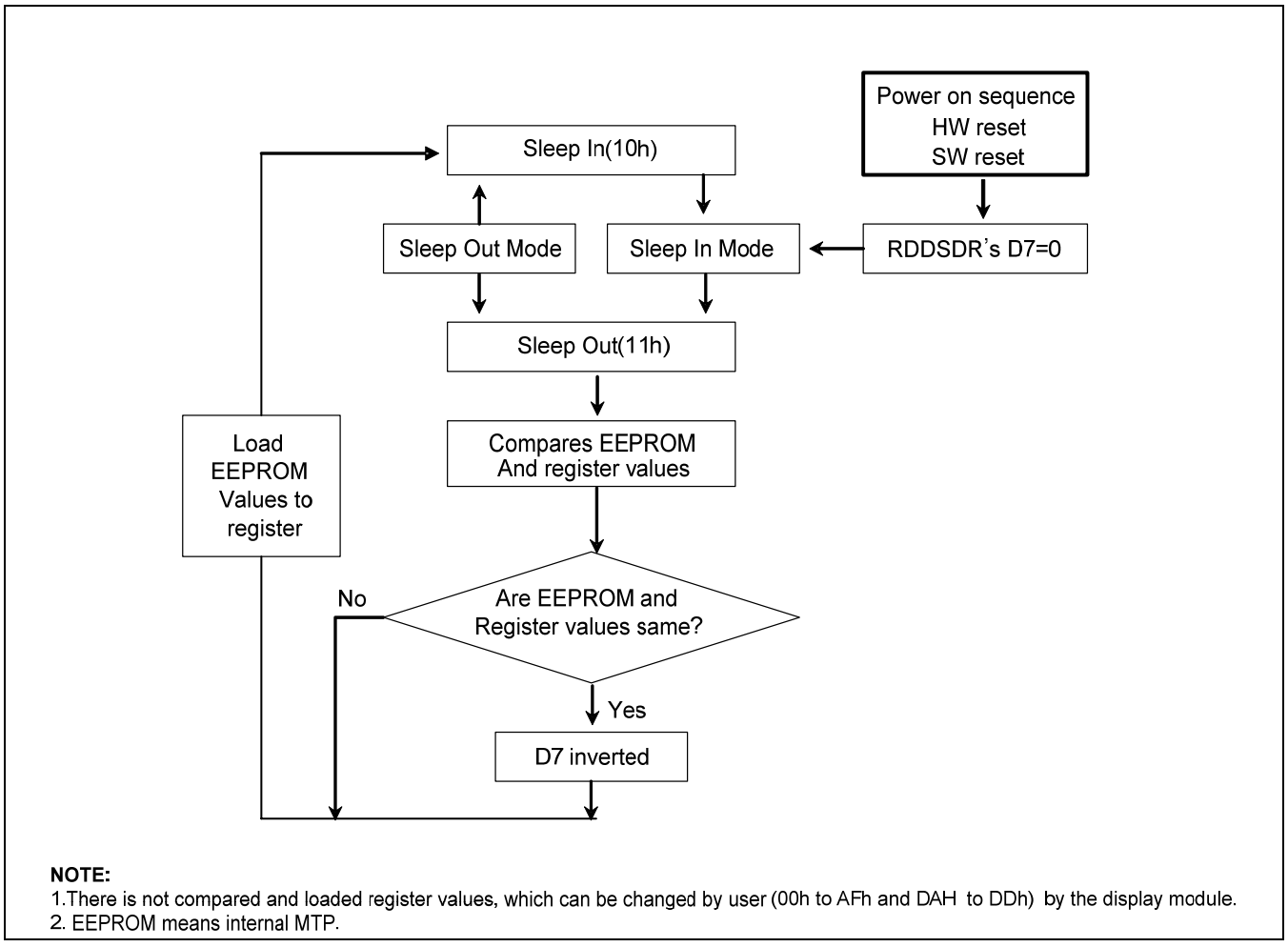
4.7 SLEEP-OUT COMMAND AND SELF-DIAGNOSTIC FUNCTIONS OF THE DISPLAY MODULE

4.7.1 REGISTER LOADING DETECTION

Sleep-out command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

Data of the EEPROM and register values of driver IC are compared as shown in the figure below. If those both values (EEPROM and register values) are the same, there is an inverted (=increased by 1) bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If both those values are not same, this bit (D7) is not inverted (= not increased by 1).

The flowchart of the function described above is as follows.



NOTE:
1.There is not compared and loaded register values, which can be changed by user (00h to AFh and DAH to DDh) by the display module.
2. EEPROM means internal MTP.

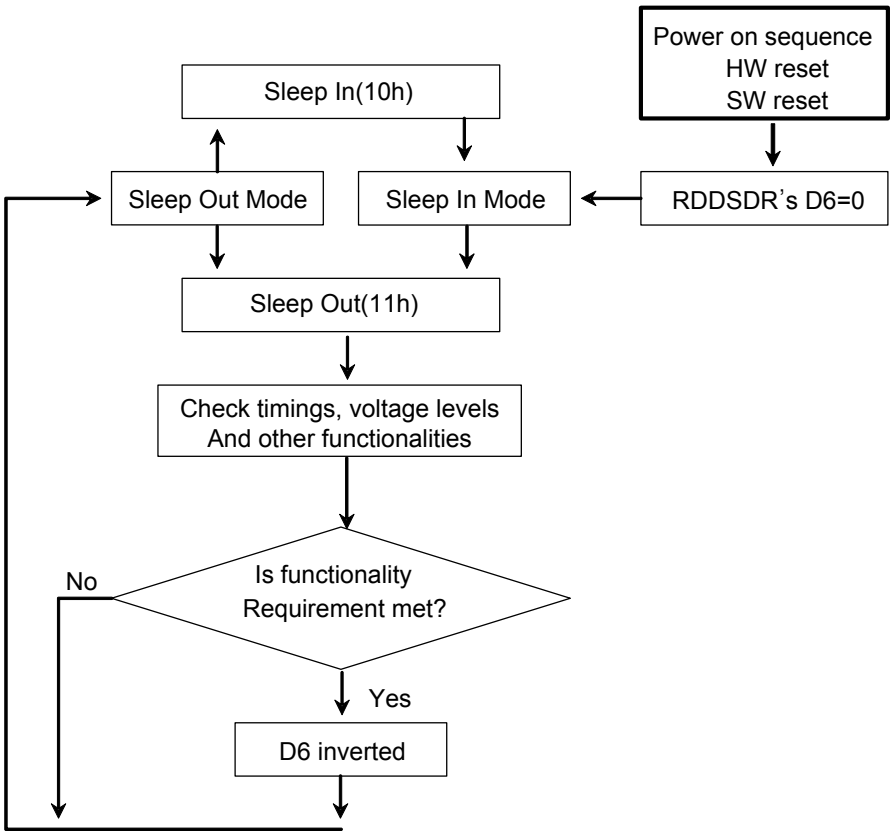
Figure 154 Flowchart of Register Loading Detection

4.7.2 FUNCTIONALITY DETECTION

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1).

The flow chart for this internal function is following:



NOTE: There is needed 120msec after Sleep-Out command, when there is changing From Sleep-In Mode to Sleep-Out mode, before there is possible to check if Functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep-Out Command is sent in Sleep- Out mode.

Figure 155 Flowchart of Functionality Detection

4.8 NVM MEMORY CONTROL

4.8.1 MTP CONTROL

4.8.1.1 MTP Control Flow

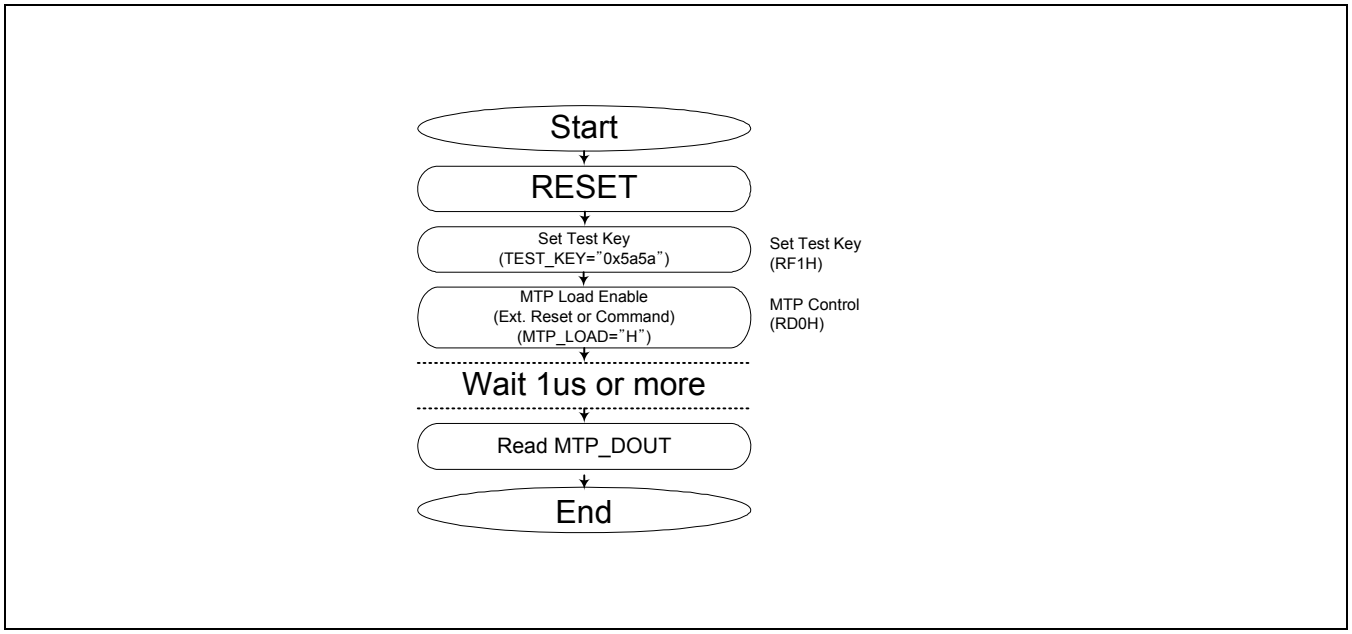


Figure 156 Flow of MTP Load / Read

4.8.1.2 Internal Control

a. Using VCI for MTP

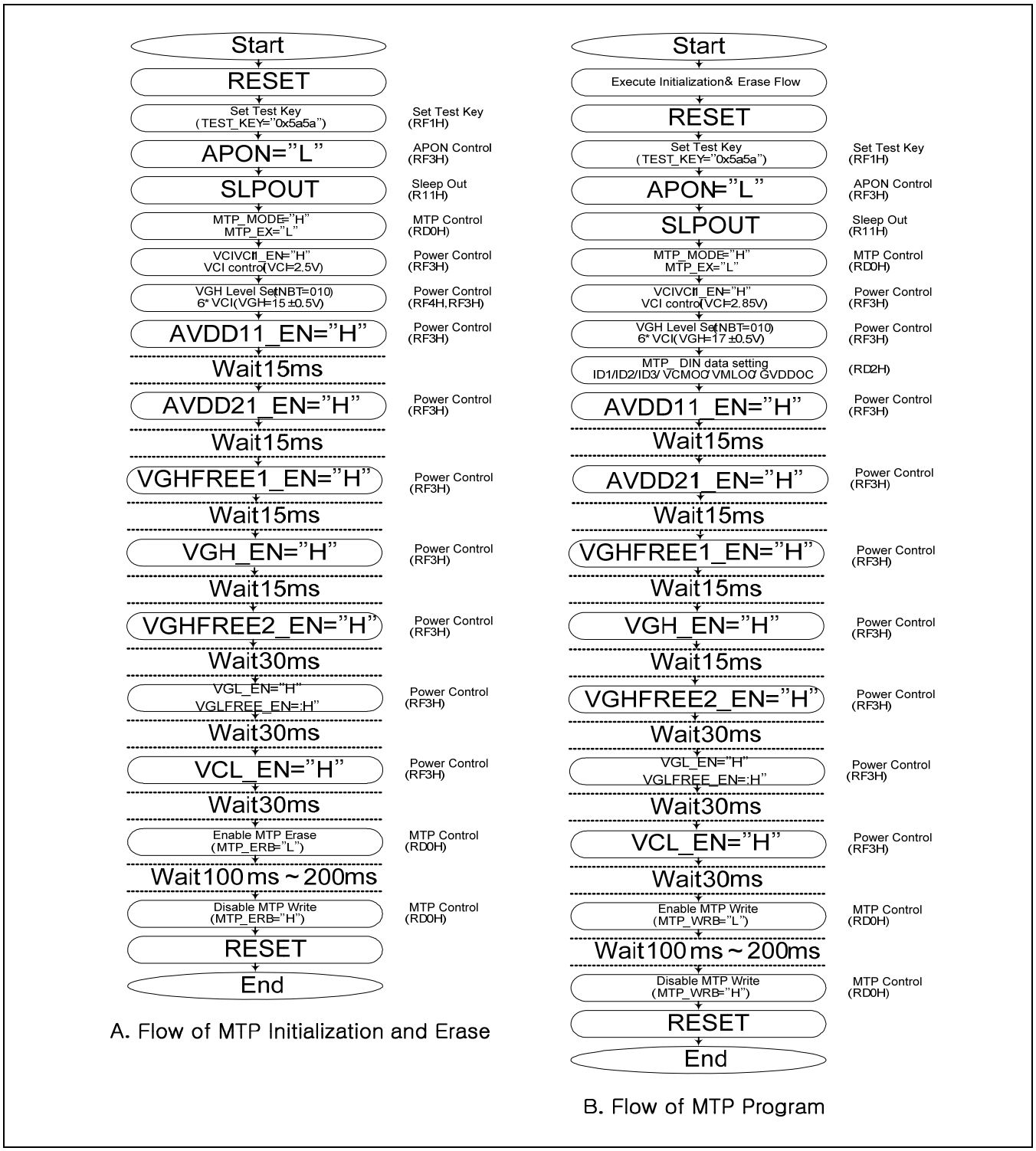


Figure 157 MTP Initialization, Erase and Program (Internal Mode Using VCI)

b. Using VCI1 for MTP

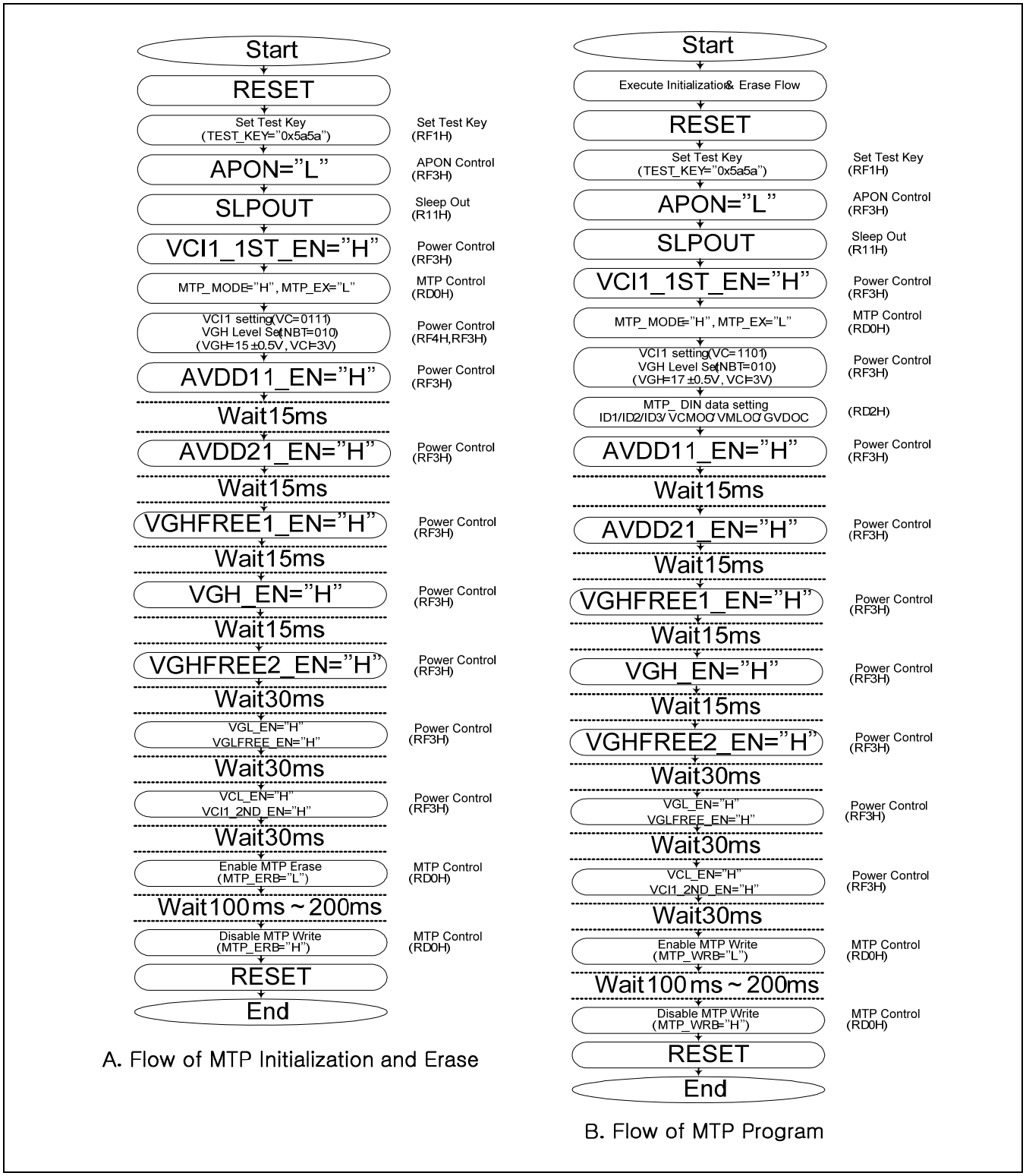


Figure 158 MTP Initialization, Erase and Program (Internal Mode Using VCI1)

4.8.1.3 External Control

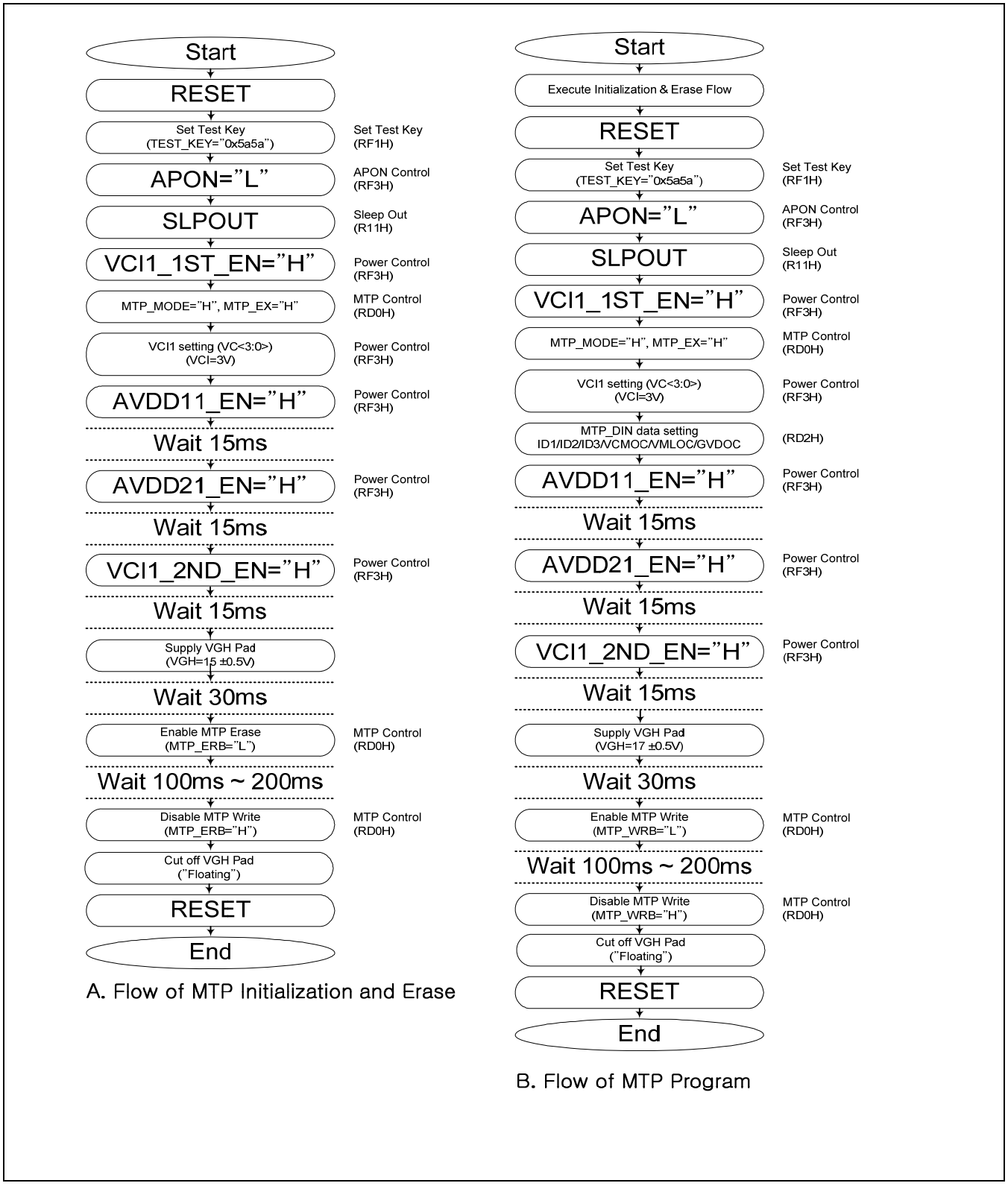


Figure 159 MTP Initialization, Erase and Program (External Mode)

4.8.1.4 Timing of MTP Control

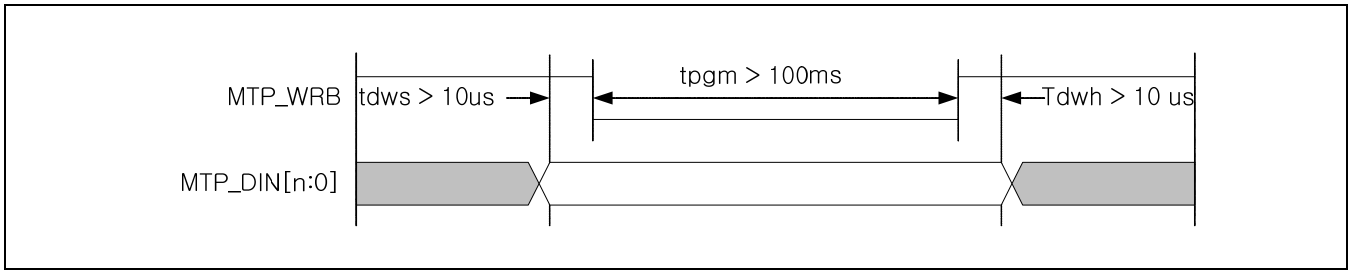


Figure 160 Timing of MTP Program

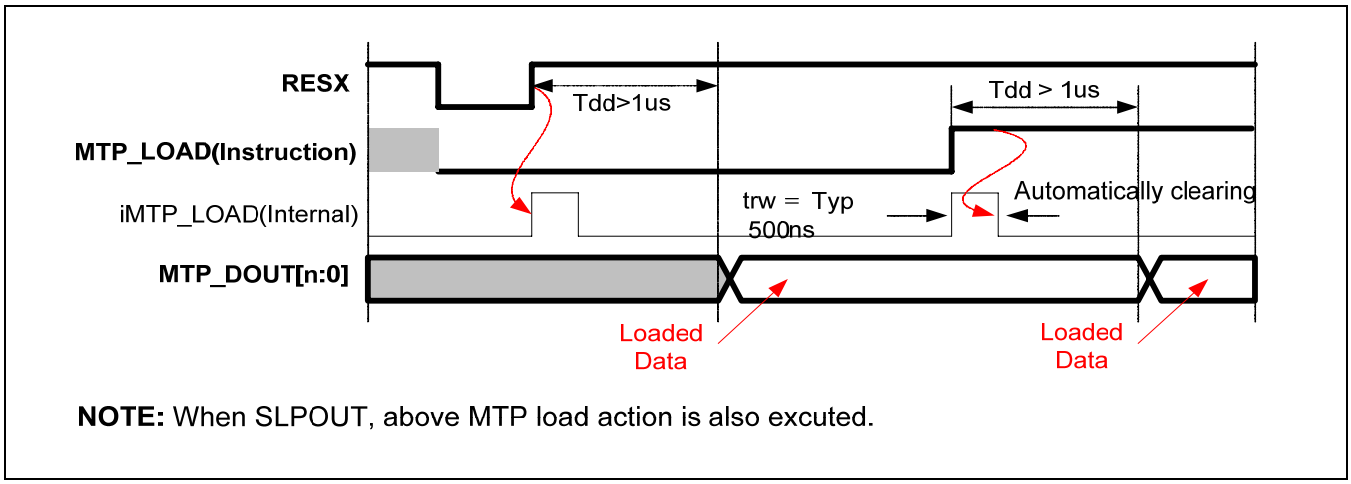


Figure 161 Timing of MTP Load

4.9 8-COLOR DISPLAY MODE

An 8-color display mode is also provided by the S6D05A1. In an 8-color mode of operation, gray scale voltage generation (V0-V255) is halted to conserve power and the values of gamma micro-adjustment registers (PKP and PKN) become invalid. Also, the only MSB of each R, G, and B in the Frame Memory are displayed. (Refer to 39h Command)

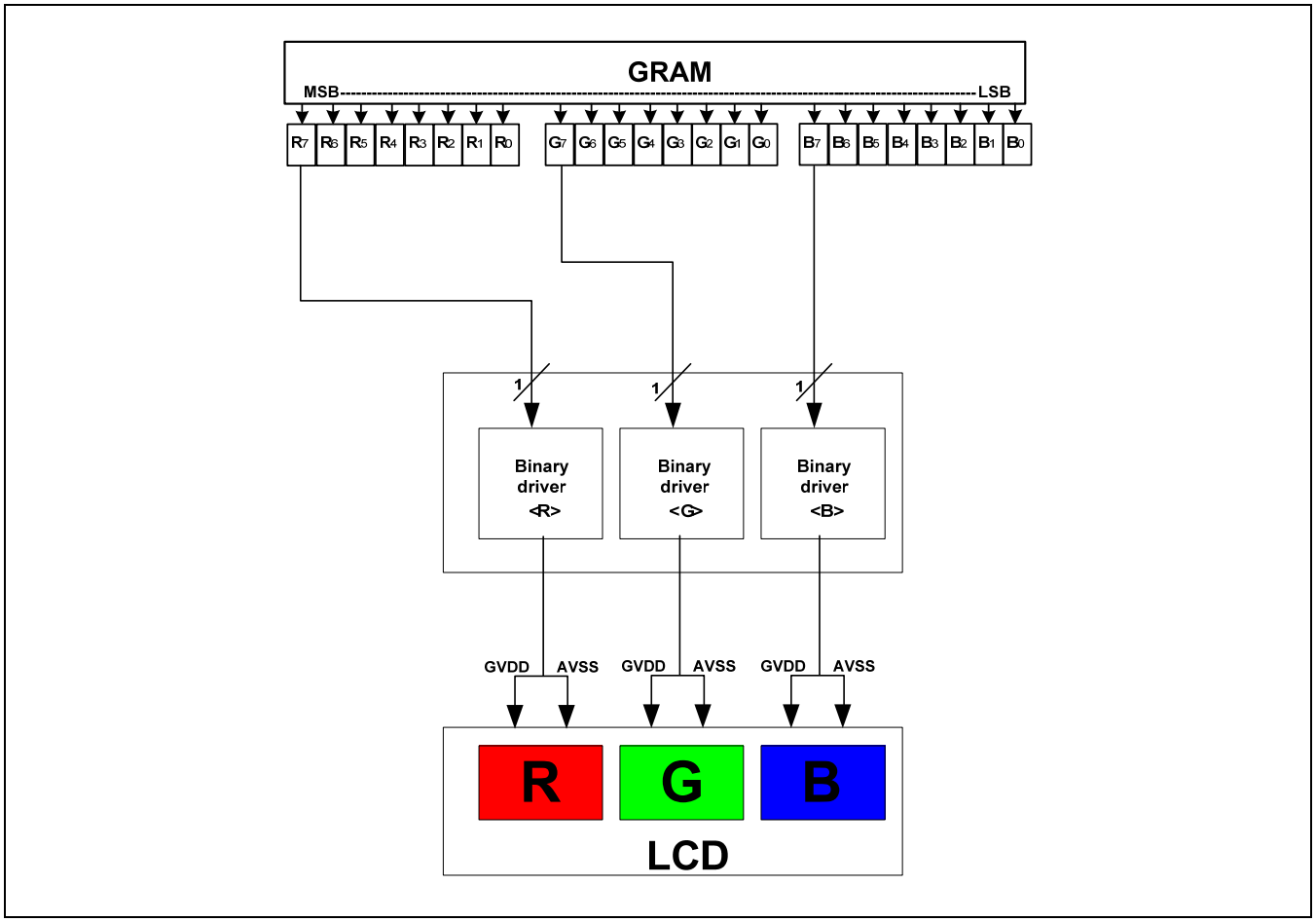


Figure 162 8-color Display Control.

4.10 INSTRUCTION SETUP FLOW

4.10.1 POWER OFF SEQUENCE

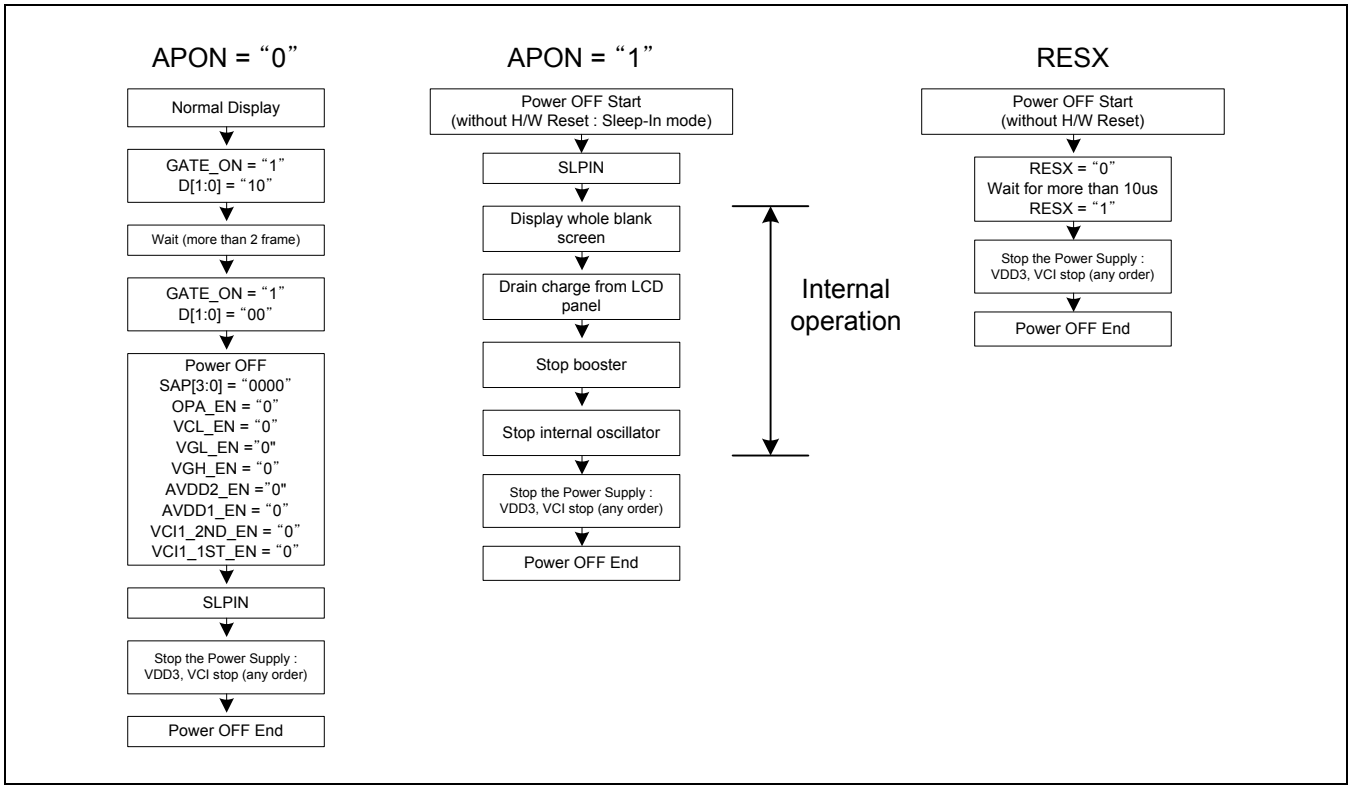


Figure 163 Power OFF Sequence

4.10.2 AUTO DISPLAY SEQUENCE (APON=1 AND DISP_SEL=1)

4.10.2.1 SLPOUT

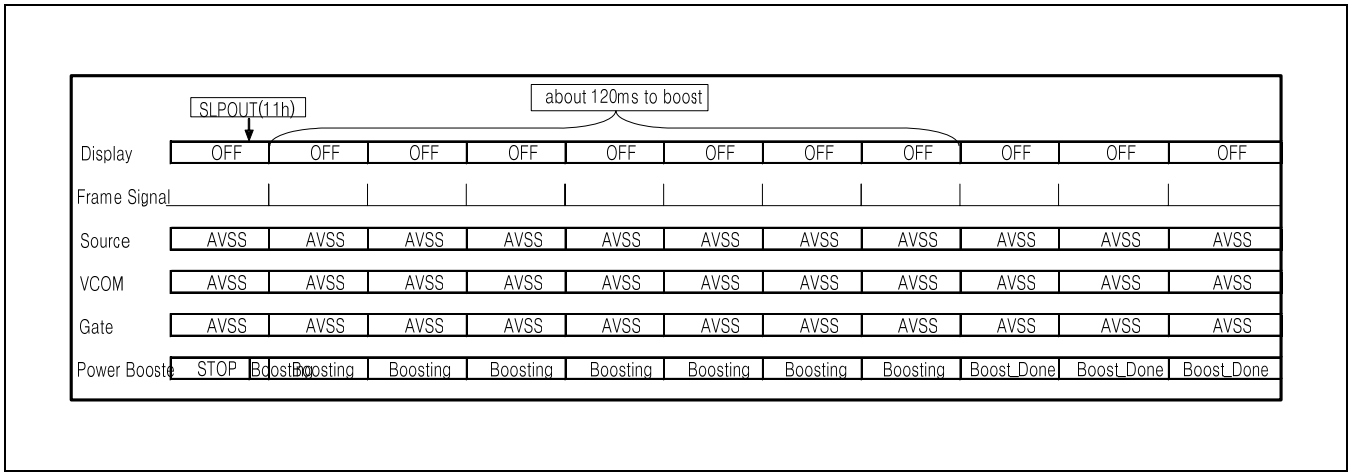


Figure 164 SLPOUT Auto Sequence

4.10.2.2 SLPOUT and DISPON

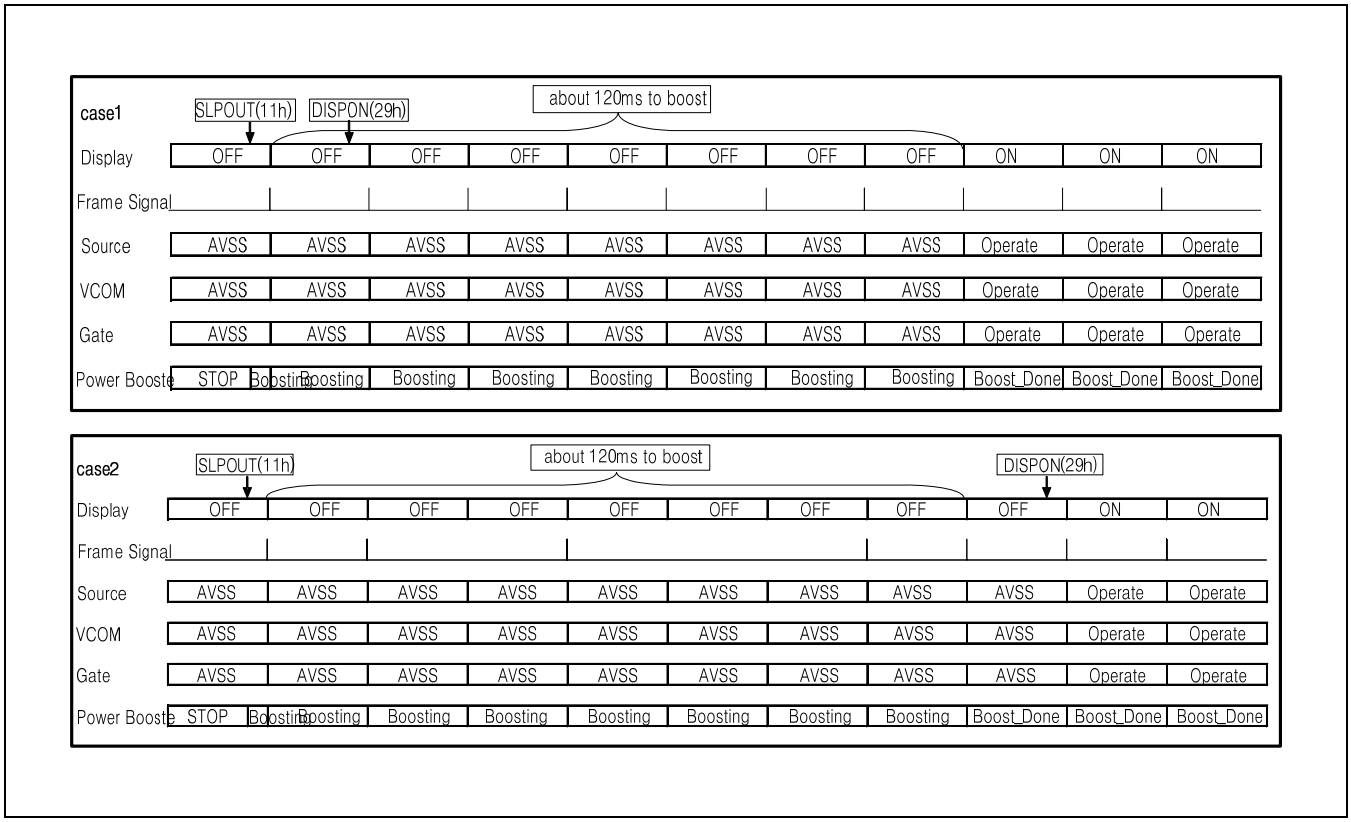


Figure 165 SLPOUT and DISPON Auto Sequence

4.10.2.3 DISPOFF and SLPIN

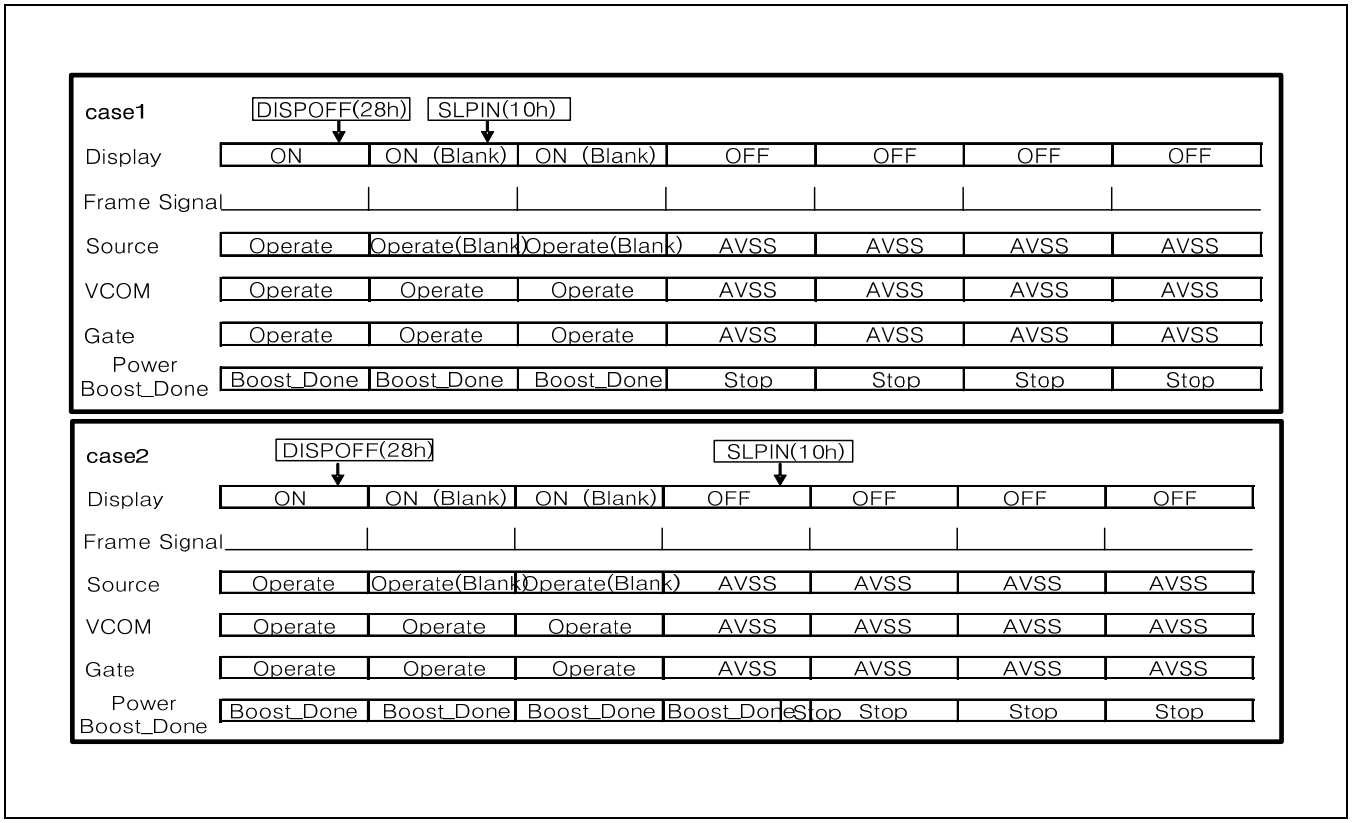


Figure 166 DISPOFF and SLPIN Auto Sequence

4.10.2.4 SLPIN

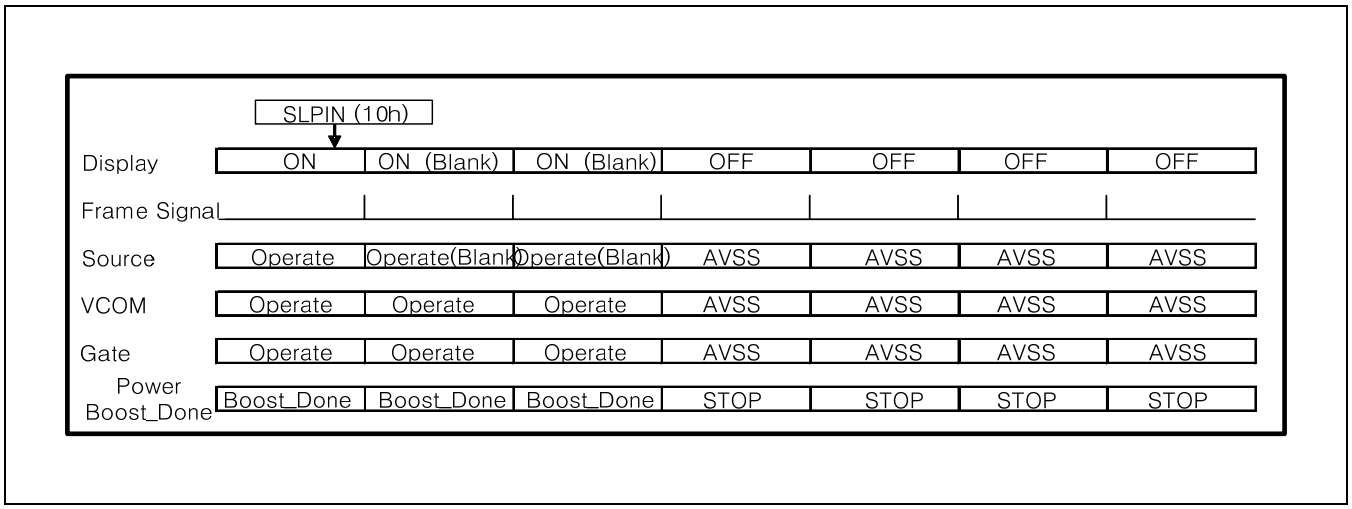


Figure 167 SLPIN Auto Sequence

4.11 TEARING EFFECT OUTPUT LINE

The Tearing Effect output line supplies a Panel synchronization signal to the MPU. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

4.11.1 TEARING EFFECT LINE MODES

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

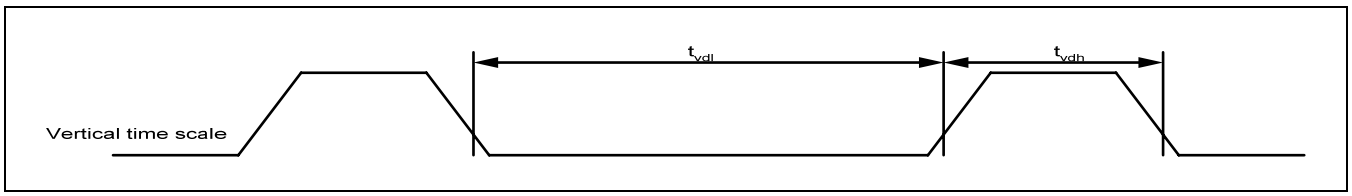


Figure 168 Tearing Effect Output Signal Consists of V-Blanking Information Only

t_{vdh} = The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480H-sync pulses per field.

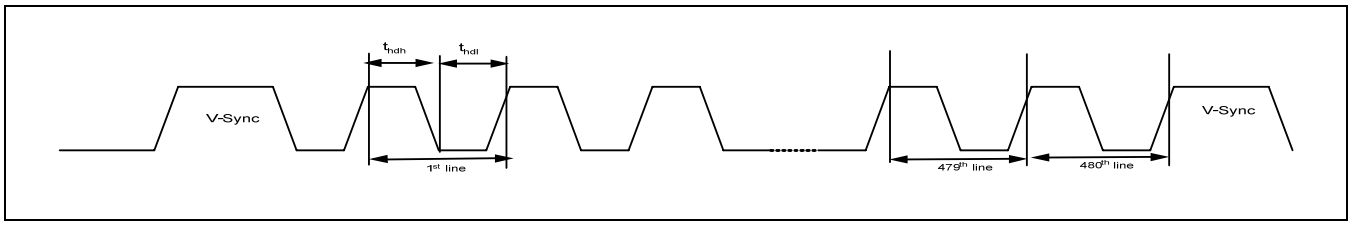


Figure 169 Tearing Effect Output Signal Consists of V-Blanking and H-Blanking Information

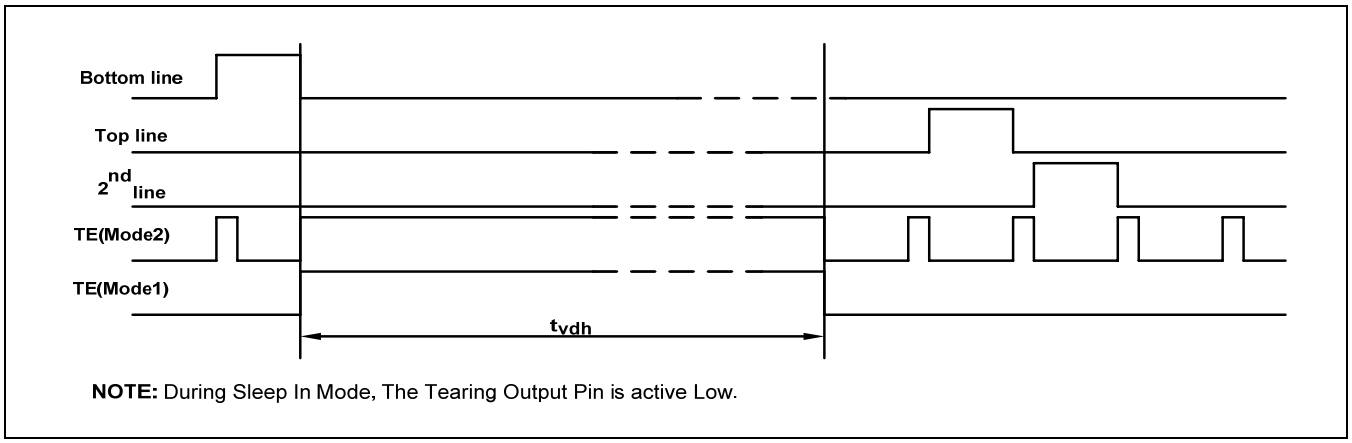


Figure 170 Tearing Effect Output Signal

4.11.2 TEARING EFFECT LINE TIMINGS

The Tearing effect signal is described below.

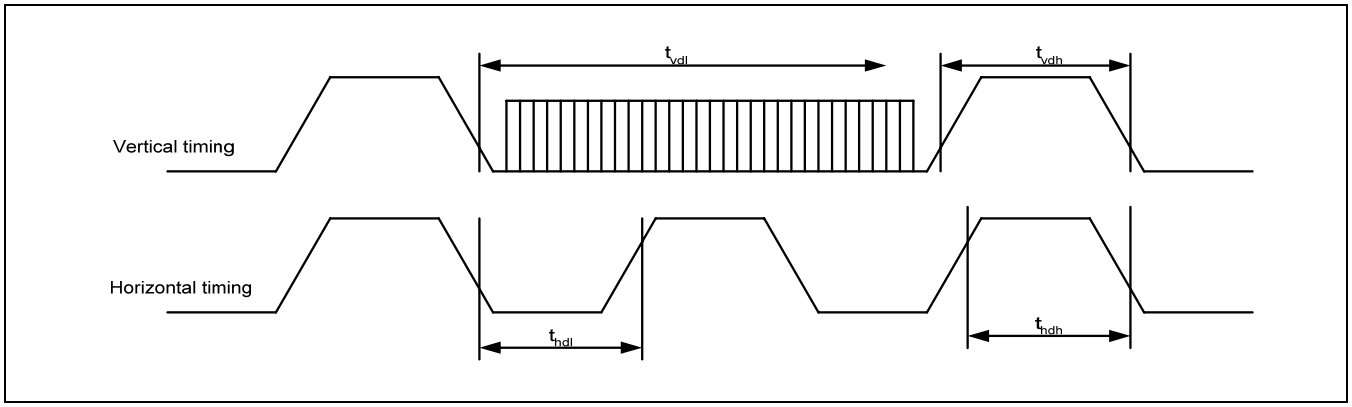


Figure 171 Tearing Effect Output Signal Timing

Table 94 AC Characteristics of Tearing Effect Signal (IDLE Mode Off)

Symbol	Parameter	min	max	unit	Description
tvdl	Vertical timing low duration	-	-	ms	
tvdh	Vertical timing high duration	-	-	us	
thdl	Horizontal timing low duration	-	-	us	
thdh	Horizontal timing high duration	-	500	us	

NOTE:
1. The timings in above Table apply when MADCTL D4=0 and D4=1
2. When TE MODE1 tvdh = VBP+VFP-1, When TE MODE2 tvdh = VBP+VFP-thdl
   When self refresh mode (SELF_REF=1) in RGB I/F, tvdh = VBP+VFP+1
3. When TE MODE2 in MPU Interface, the high period of TE signal in horizontal timing is 10 INCLK

The rise and fall time of TE signal is stipulated to be equal to or less than 15ns.

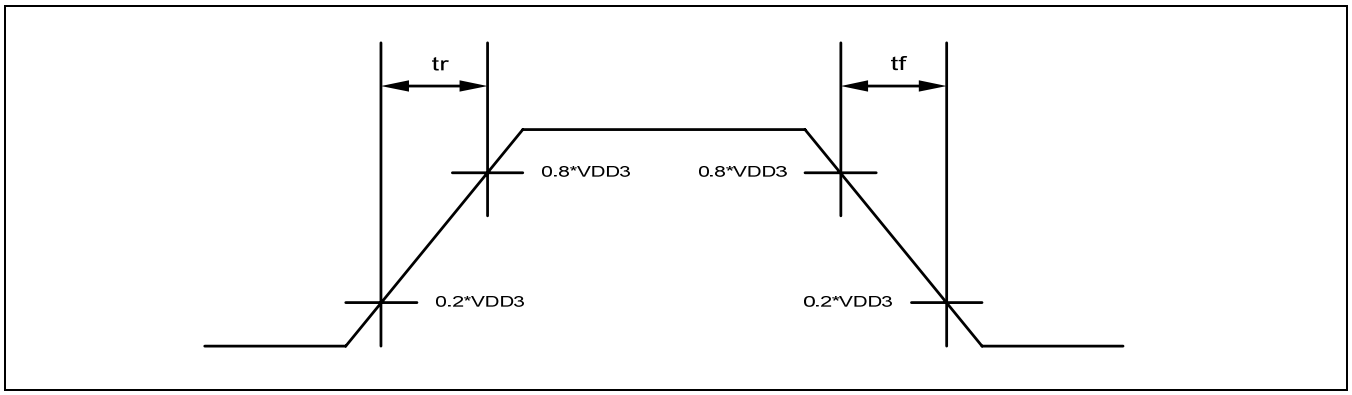


Figure 172 Rise and Fall Time of TE Signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect.

4.11.2.1 Example 1: MPU Write is Faster Than Panel Read.

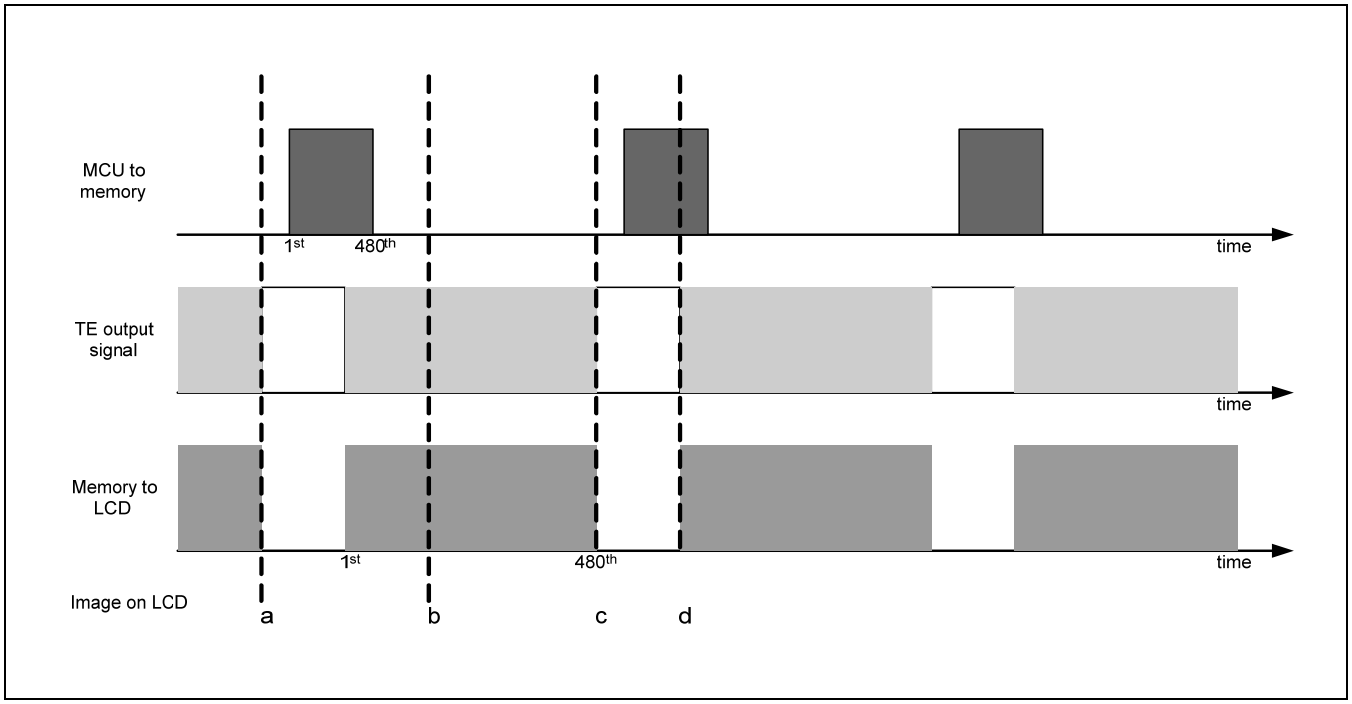


Figure 173 Method 1 to Avoid Tearing Effect

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image.

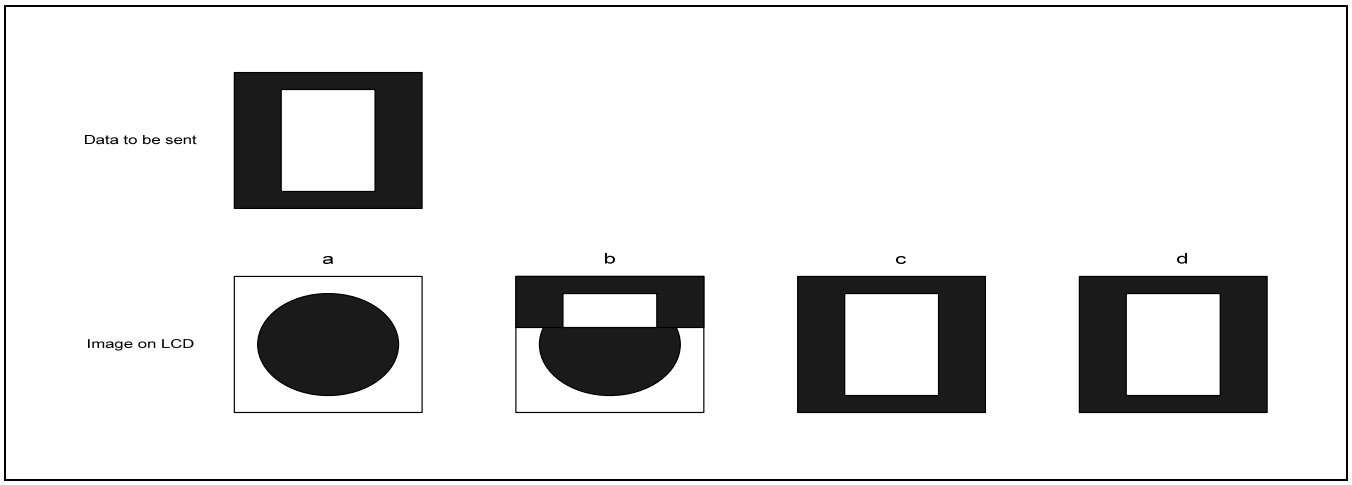


Figure 174 Panel Image Refreshment of Method 1

4.11.2.2 Example 2 : MPU Write is Slower Than Panel Read.

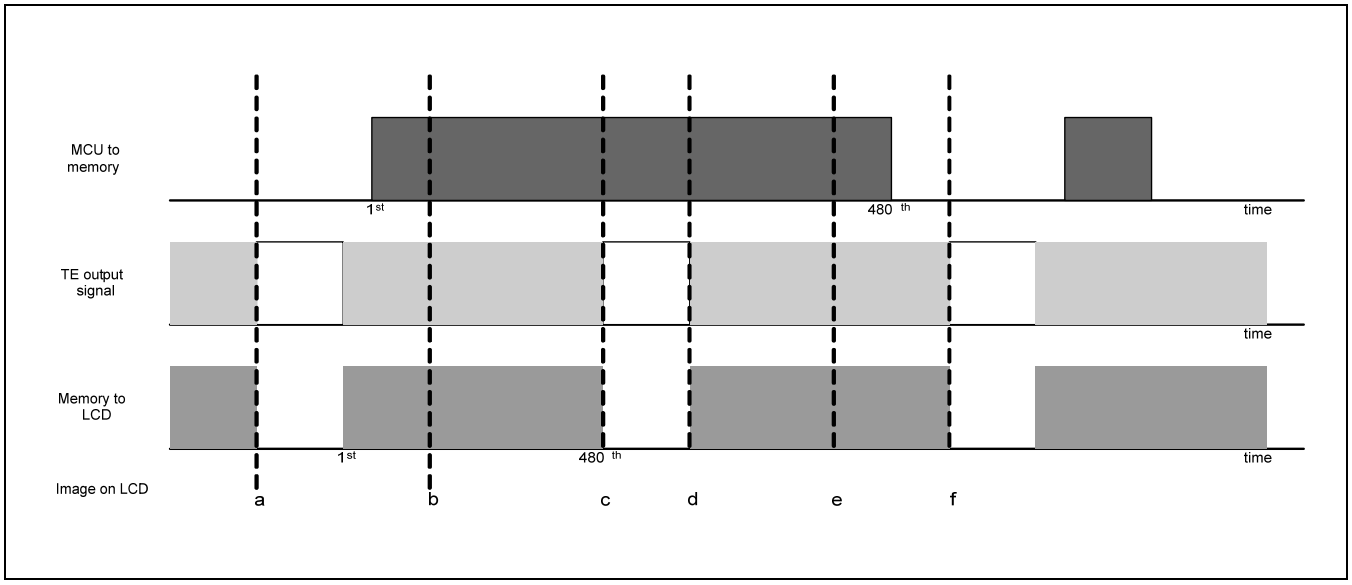


Figure 175 Method 2 to Avoid Tearing Effect

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and to finish downloading during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

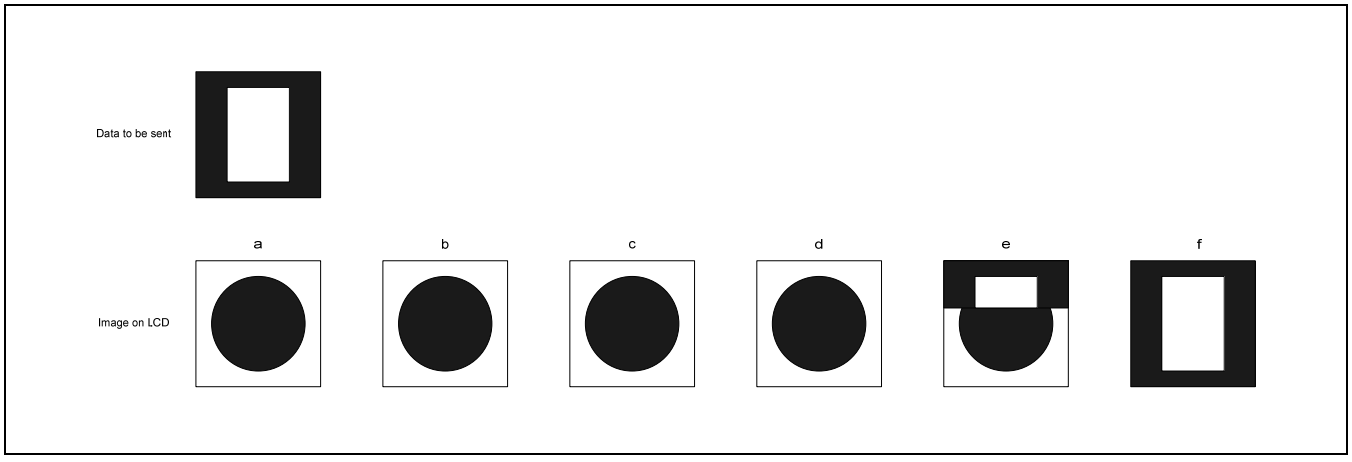


Figure 176 Panel Image Refreshment of Method 2

4.12 MIE FUNCTION

S6D05A1 has a special image enhancement function. MIE (Mobile Image Enhancement) reduces power consumption of backlight unit by adaptive enhancement of luminance and contrast. According the brightness enhancement rate of input image, the power reduction of BLU is controlled automatically.

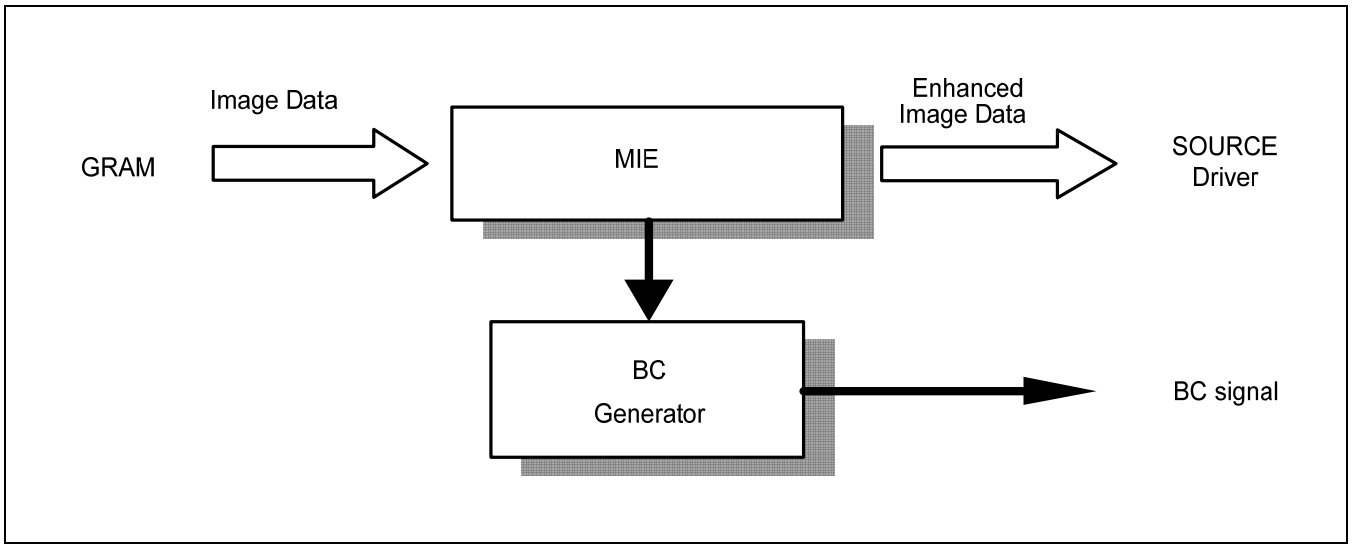


Figure 177 Flowchart of MIE Function

When MIE is enabled, MIE dynamically changes the brightness of backlight unit by on-chip BC(Backlight Control) Generator. Host can control the rate of BLU power reduction by setting RRC value (Refer to C0h Command.)

When MIE is enabled, the enhanced data is outputted to Source block. Host processor should select movie or still-Image mode (Refer to 55h Command).

5 COMMAND

5.1 DESCRIPTION OF LEVEL 1 COMMAND

Table 95 List of level 1 Command

Operational Code (HEX)	Function	Read/Write/ Command	Number of Parameter	CPU	SPI	MDDI	MIPI	
				(80/68)	(3/4-wire)		DCS	Generic
00	No Operation	C	0	O	O	O	O	O
01	Software Reset	C	0	O	O	O	O	O
09	Read Display Status	R	4	O	O	O	X	O
0A	Read Display Power Mode	R	1	O	O	O	O	X
0B	Read Display MADCTL	R	1	O	O	O	O	X
0C	Read Display Pixel Format	R	1	O	O	O	O	X
0D	Read Display Image Mode	R	1	O	O	O	O	X
0E	Read Display Signal Mode	R	1	O	O	O	O	X
0F	Read Display Self Diagnostic Result	R	1	O	O	O	O	X
10	Sleep In	C	0	O	O	O	O	O
11	Sleep Out	C	0	O	O	O	O	O
12	Partial Mode On	C	0	O	O	O	O	O
13	Normal Display Mode On	C	0	O	O	O	O	O
20	Invervison Off	C	0	O	O	O	O	O
21	Invervison On	C	0	O	O	O	O	O
28	Display Off	C	0	O	O	O	O	O
29	Display On	C	0	O	O	O	O	O
2A	Column Address Set	W	4	O	O	O	O	O
2B	Page Address Set	W	4	O	O	O	O	O
2C	Memory Write	W	Any Length	O	O	O	O	O

2E	Memory Read	R	Any length	O	X	O	O	X
30	Partial Area	W	4	O	O	O	O	O
34	Tearing Effect Line Off	C	0	O	O	O	O	O
35	Tearing Effect Line On	W	1	O	O	O	O	O
36	Memory Data Access Control	W	1	O	O	O	O	O
38	Idle Mode Off	C	0	O	O	O	O	O
39	Idle Mode On	C	0	O	O	O	O	O
3A	Interface Pixel format	W	1	O	O	O	O	O
3C	Write Memory Continue	W	Any length	O	O	O	O	O
3E	Read Memory Continue	R	Any length	O	X	O	O	X
44	Tearing Scan line	W	2	O	O	O	O	O
45	Read Scan line	R	2	O	O	O	O	X
51	Write Manual Brightness	W	1	O	O	O	O	O
52	Read Display Brightness	R	1	O	O	O	O	X
53	Write BL Control	W	1	O	O	O	O	O
54	Read BL Control	R	1	O	O	O	O	X
55	Write MIE Mode	W	1	O	O	O	O	O
56	Read MIE Mode	R	1	O	O	O	O	X
5E	Write Minimum Brightness	W	1	O	O	O	O	O
5F	Read Minimum Brightness	R	1	O	O	O	O	X
A1	Read DDB Start	R	2	O	O	O	O	X
A8	Read DDB Continue	R	2	O	O	O	O	X
DA	Read ID1	R	1	O	O	O	O	X
DB	Read ID2	R	1	O	O	O	O	X
DC	Read ID3	R	1	O	O	O	O	X

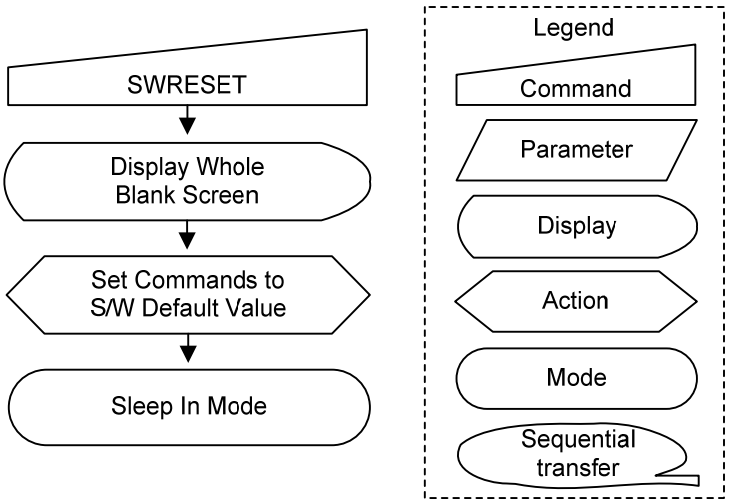
NOTE:

1. Undefined commands are treated as NOP (00h) command.
2. Commands 10h, 12h, 13h, 20h, 21h, 28h, 29h, 30h, 38h and 39h are updated during V-sync when Module is in Sleep Out mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Display Self Diagnostic Result (0Fh) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.
3. The number of parameter is the number of real parameter except dummy parameter.
4. When command 2Ch, 3Ch in SPI, memory write function is supported only at the Self-refresh mode.

5.1.1 NOP (00H)

00H	NOP (No Operation)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER											
Description	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.											
Restriction												
Register Availability	**Status**							**Availability**				
	Normal Mode On, Idle Mode Off, Sleep Out							Yes				
	Normal Mode On, Idle Mode On, Sleep Out							Yes				
	Partial Mode On, Idle Mode Off, Sleep Out							Yes				
	Partial Mode On, Idle Mode On, Sleep Out							Yes				
	Sleep In or Step up circuit Off							Yes				
Default	**Status**							**Default Value**				
	Power On Sequence							N/A				
	S/W Reset							N/A				
	H/W Reset							N/A				
Flow Chart												

5.1.2 SOFTWARE RESET (01H)

<table>
<tr><th>01H</th><th colspan="12">SWRESET (Software Reset)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
NOTE: The Frame Memory contents are unaffected by this command.</td></tr>
<tr><td>Restriction</td><td colspan="12">It is necessary to wait for 5msec before sending new commands following the software reset. The display module loads all of display supplier’s factory default values to the registers during 5msec.
Case APON=1 (If Software Reset is applied during Sleep Out mode, it is necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.)</td></tr>
<tr><td rowspan="6">Register Availability</td><td colspan="6">Status</td><td colspan="6">Availability</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Sleep In or Step up circuit Off</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="4">Default</td><td colspan="6">Status</td><td colspan="6">Default Value</td></tr>
<tr><td colspan="6">Power On Sequence</td><td colspan="6">N/A</td></tr>
<tr><td colspan="6">S/W Reset</td><td colspan="6">N/A</td></tr>
<tr><td colspan="6">H/W Reset</td><td colspan="6">N/A</td></tr>
<tr><td>Flow Chart</td><td colspan="12">Case APON=1
 
</td></tr>
</table>

5.1.3 READ DISPLAY STATUS (09H)

09H	RDDST (Read Display Status)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	0	1	09
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	D31	D30	D29	D28	D27	D26	0	0	00
3rd Parameter	1	↑	1	0	D22	D21	D20	D19	D18	D17	D16	71
4th Parameter	1	↑	1	0	0	D13	0	0	D10	D9	D8	00
5th Parameter	1	↑	1	D7	D6	D5	0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:
The 1st Parameter is dummy data.
When using the MIPI, DCS read not supported.

Bit	Description	Value
D31	Booster Voltage Status	“1”=Booster on, “0”=off
D30	Page Address Order (MY)	“1”=Decrement, “0”=Increment
D29	Column Address Order (MX)	“1”=Decrement, “0”=Increment
D28	Page/Column Exchange (MV)	“1”= Page/column exchange (MV=1), “0”= Normal (MV=0)
D27	Vertical Refresh Order (ML)	“1”=Decrement, “0”=Increment
D26	RGB/BGR Order (RGB)	“1”=BGR, “0”=RGB
D25	Not Used	“0”
D24	Not Used	“0”
D23	Not Used	“0”
D22 D21 D20	Interface Color Pixel Format Definition (IFPF)	“101”=16-bits/pixel “110”=18-bits/pixel "111"= 24-bits/pixel The Others = not defined
D19	Idle Mode On/Off	“1” = On, “0” = Off
D18	Partial Mode On/Off	“1” = On, “0” = Off
D17	Sleep In/Out	“1” = Out, “0” = In
D16	Display Normal Mode On/Off	“1” = Normal Display, “0” = Partial Display
D15	Not Used	“0”

09H	RDDST (Read Display Status)		
	Bit	**Description**	**Value**
	D14	Not Used	“0”
	D13	Inversion Status	“1” = On, “0” = Off
	D12	Not Used	“0”
	D11	Not Used	“0”
	D10	Display On/Off	“1” = On, “0” = Off
	D9	Tearing effect line on/off	“1” = On, “0” = Off
	D8~D6	Gamma Curve Selection	Fixed “000”
	D5	Tearing effect line mode	“0” = mode1, V_Blanking only “1” = mode2, Both H & V-Blanking.
	D4	Not Used	“0”
	D3	Not Used	“0”
	D2	Not Used	“0”
	D1	Not Used	“0”
	D0	Not Used	“0”
	Bit	**Description**	**Value**

Bit Values are explained overleaf.

- D31: Step up circuit Voltage status.

– ”0”: Step up circuit Off or has a fault.
– ”1”: Step up circuit On and working OK.

- D30: Page Address Order.

– “0”: Top to Bottom (When MADCTL B7 = ‘0’).
– “1”: Bottom to Top (When MADCTL B7 = ‘1’).

- D29: Column Address Order.

– “0”: Left to Right (When MADCTL B6 = ‘0’).
– “1”: Right to Left (When MADCTL B6 = ‘1’).

- D28: Page/Column Order.

– “0”: Normal Mode (When MADCTL B5 = ‘0’).
– “1”: Reverse Mode (When MADCTL B5 = ‘1’).

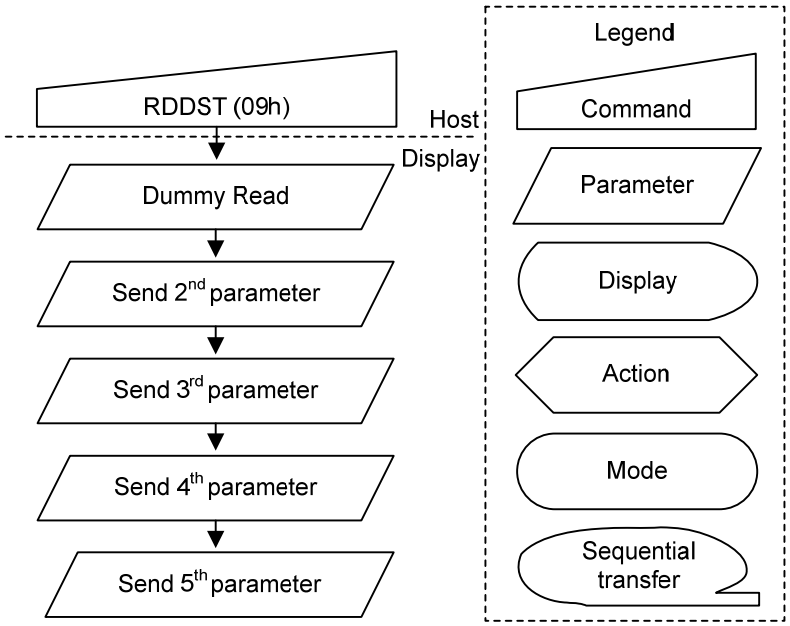
09H	RDDST (Read Display Status)
	• D27: Line Address Order • – “0”: LCD Refresh Top to Bottom (When MADCTL B4 = ‘0’). – “1”: LCD Refresh Bottom to Top (When MADCTL B4 = ‘1’). • D26: RGB/BGR Order – “0”: RGB (When MADCTL B3 = ‘0’). – “1”: BGR (When MADCTL B3 = ‘1’). • D25: Set to “0” • D24: Set to “0” • D23: Set to “0” • D22, D21, D20: Interface Color Pixel Format Definition. • D19: Idle Mode On/Off – “0”: Idle Mode Off. – “1” : Idle Mode On. • D18: Partial Mode On/Off – “0”: Partial Mode Off. – “1” : Partial Mode On. • D17: Sleep In/Out – “0”: Sleep In Mode. – “1”: Sleep Out Mode. • D16: Display Normal Mode – “0”: Display Normal Mode Off. – “1”: Display Normal Mode On. • D15 Set to “0” • D14: Set to “0” • D13: Inversion Status – “0”: Inversion is Off. – “1”: Inversion is On. • D12: Set to “0” • D11: Set to “0” • D10: Display On/Off – “0”: Display is Off. – “1”: Display is On.

<table>
<tr><th>09H</th><th colspan="2">RDDST (Read Display Status)</th></tr>
<tr><td></td><td colspan="2">• D9: Tearing Effect Line On/Off
– “0”: Tearing Effect Line Off.
– “1”: Tearing Effect Line On.

• D8, D7, D6: Gamma Curve Selection. Not Support.

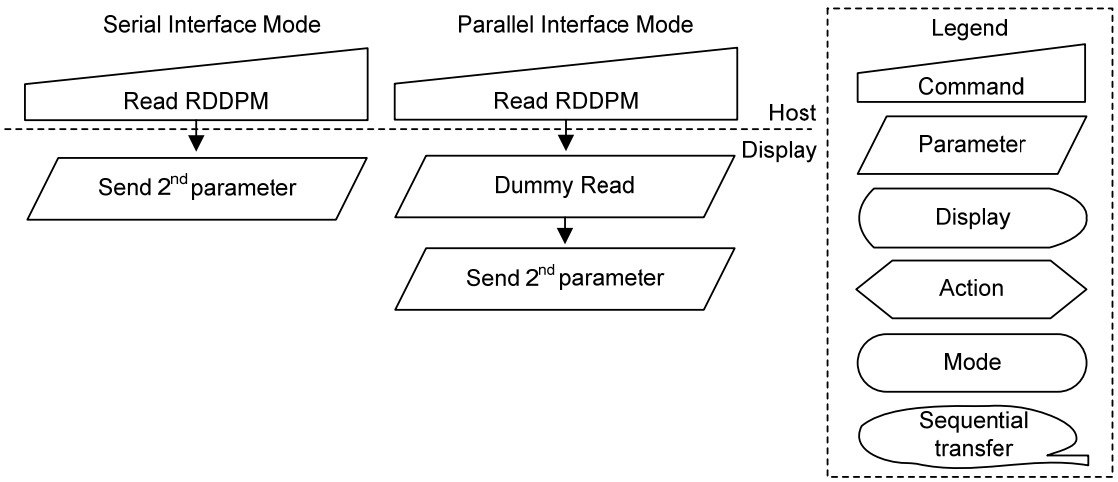
• D5: Tearing Effect Line Output Mode.
– “0”: Mode 1, V-Blanking only.
– “1”: Mode 2, both H-Blanking and V-Blanking.

• D4: Set to “0”
• D3: Set to “0”
• D2: Set to “0”
• D1: Set to “0”
• D0: Set to “0”</td></tr>
<tr><td>Restriction</td><td colspan="2"></td></tr>
<tr><td rowspan="6">Register Availability</td><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
<tr><td rowspan="4">Default</td><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>0000_0000_0111_0001_0000 0000_0000_0000</td></tr>
<tr><td>S/W Reset</td><td>0000_0000_0111_0001_0000 0000_0000_0000</td></tr>
<tr><td>H/W Reset</td><td>0000_0000_0111_0001_0000 0000_0000_0000</td></tr>
</table>

09H	RDDST (Read Display Status)
Flow Chart	

5.1.4 READ DISPLAY POWER MODE (0AH)

<table>
<tr><th>0AH</th><th colspan="12">RDDPM (Read Display Power Mode)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>0</td><td>0</td><td>08</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:</td></tr>
<tr><td></td><td colspan="3">Bit</td><td colspan="4">Description</td><td colspan="5">Value</td></tr>
<tr><td></td><td colspan="3">D7</td><td colspan="4">Booster Voltage Status</td><td colspan="5">“1”=Booster on, “0”=off</td></tr>
<tr><td></td><td colspan="3">D6</td><td colspan="4">Idle Mode On/Off</td><td colspan="5">“1” = Idle Mode On, “0”= idle Mode Off</td></tr>
<tr><td></td><td colspan="3">D5</td><td colspan="4">Partial Mode On/Off</td><td colspan="5">“1” = Partial Mode On, “0” = Partial Mode Off</td></tr>
<tr><td></td><td colspan="3">D4</td><td colspan="4">Sleep In/Out</td><td colspan="5">“1” = Sleep Out, “0” = Sleep In</td></tr>
<tr><td></td><td colspan="3">D3</td><td colspan="4">Display Normal Mode On/Off</td><td colspan="5">“1” = Normal Display, “0” = Partial Display</td></tr>
<tr><td></td><td colspan="3">D2</td><td colspan="4">Display On/Off</td><td colspan="5">“1” = Display On, “0” = Display Off</td></tr>
<tr><td></td><td colspan="3">D1</td><td colspan="4">Not Used</td><td colspan="5">“0”</td></tr>
<tr><td></td><td colspan="12">NOTE: “X“ denotes “Don’t care”</td></tr>
<tr><td>Restrictions</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="6">Status</td><td colspan="6">Availability</td></tr>
<tr><td></td><td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td></td><td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td></td><td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td></td><td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td></td><td colspan="6">Sleep In or Step up circuit Off</td><td colspan="6">Yes</td></tr>
<tr><td>Default</td><td colspan="6">Status</td><td colspan="6">Default Value</td></tr>
<tr><td></td><td colspan="6">Power On Sequence</td><td colspan="6">0000_1000</td></tr>
<tr><td></td><td colspan="6">S/W Reset</td><td colspan="6">0000_1000</td></tr>
<tr><td></td><td colspan="6">H/W Reset</td><td colspan="6">0000_1000</td></tr>
</table>

0AH	RDDPM (Read Display Power Mode)
Flow Chart	

5.1.5 READ DISPLAY MADCTL (0BH)

0BH	RDDMADCTL (Read Display MADCTL)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	1	1	0B
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	D7	D6	D5	D4	D3	0	0	0	00

Description

This command indicates the current status of the display MADCTL(memory address control) as described in the table below:

Bit	Description	Value
D7	Page Address Order	"1"=Decrement, "0"=Increment
D6	Column Address Order	"1"=Decrement, "0"=Increment
D5	Page/Column Order (MV)	"1"= Page/column exchange (MV=1) "0"= Normal (MV=0)
D4	Vertical refresh Order (ML)	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order(RGB)	"1"=BGR, "0"=RGB
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

NOTE: "X" denotes "Don't care"

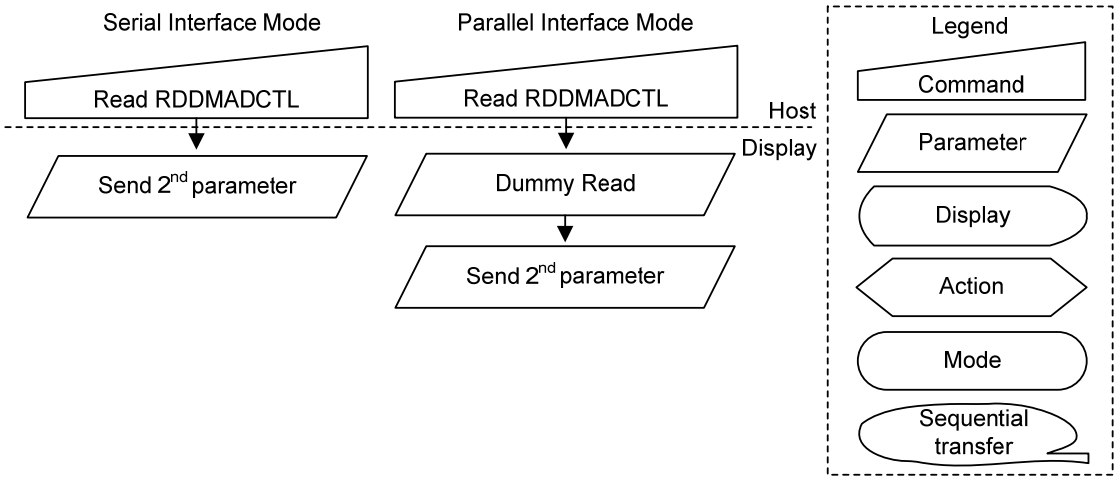
Restrictions

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

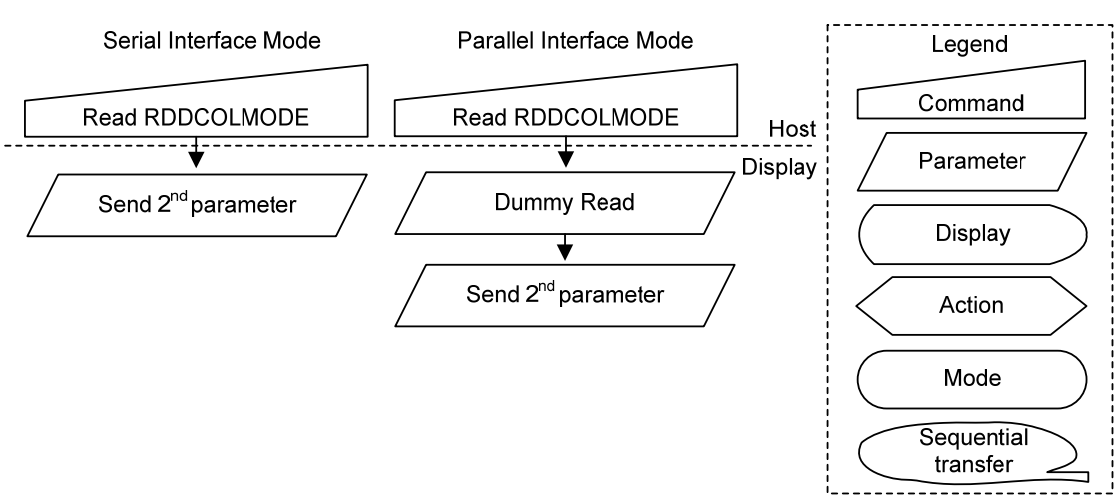
Status	Default Value
Power On Sequence	00
S/W Reset	00
H/W Reset	00

0BH	RDDMADCTL (Read Display MADCTL)
Flow Chart	

5.1.6 READ DISPLAY PIXEL FORMAT (0CH)

<table>
<tr><th>0CH</th><th colspan="12">RDDCOLMOD (Read Display COLMOD)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0C</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>D6</td><td>D5</td><td>D4</td><td>0</td><td>D2</td><td>D1</td><td>D0</td><td>77</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>“0” (Not Used)</td></tr>
<tr><td>D6
D5
D4</td><td>RGB Interface Color Format (VFPF)</td><td>“101”=16-bits/pixel
“110”=18-bits/pixel
"111"= 24-bits/pixel
Others = not defined</td></tr>
<tr><td>D3</td><td>-</td><td>“0” (Not Used)</td></tr>
<tr><td>D2
D1
D0</td><td>Control Interface Color Format (MPU Interface:IFPF)</td><td>“101”=16-bits/pixel
“110”=18-bits/pixel
"111"= 24-bits/pixel
Others = not defined</td></tr>
</table>
Bit D7: Set to’0’.
Bit D6~4 : RGB Interface Color Pixel format Definition
Bit D3 : Set to ‘0’
Bit D2~0 : Control Interface Color Pixel Format Definition

NOTE: “X“ denotes “Don’t care”</td></tr>
<tr><td>Restrictions</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0111_0111</td></tr>
<tr><td>S/W Reset</td><td>0111_0111</td></tr>
<tr><td>H/W Reset</td><td>0111_0111</td></tr>
</table></td></tr>
</table>

0CH	RDDCOLMOD (Read Display COLMOD)
Flow Chart	

5.1.7 READ DISPLAY IMAGE MODE (0DH)

0DH	RDDIM (Read Display Image Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	0	0	0C
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	0	0	D5	0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	-	0
D6	-	0
D5	Inversion On/Off	
D4	-	0
D3	-	0
D2	-	0
D1	-	0
D0	-	0

Bit D7~6: Set to'0'.
Bit D4~0 : Set to '0'

NOTE: "X" denotes "Don't care"

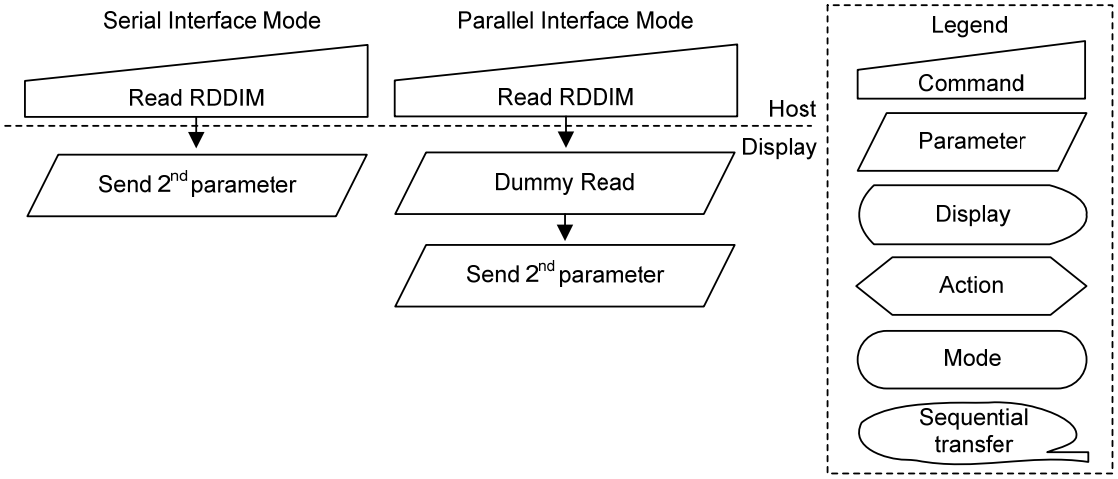
Restrictions

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

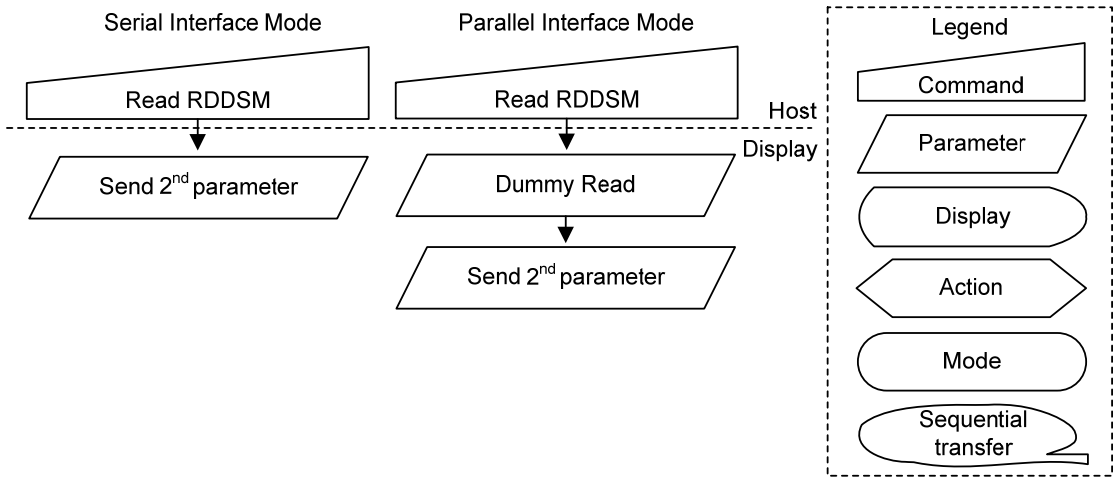
Default

Status	Default Value
Power On Sequence	00
S/W Reset	00
H/W Reset	00

0DH	RDDIM (Read Display Image Mode)
Flow Chart	

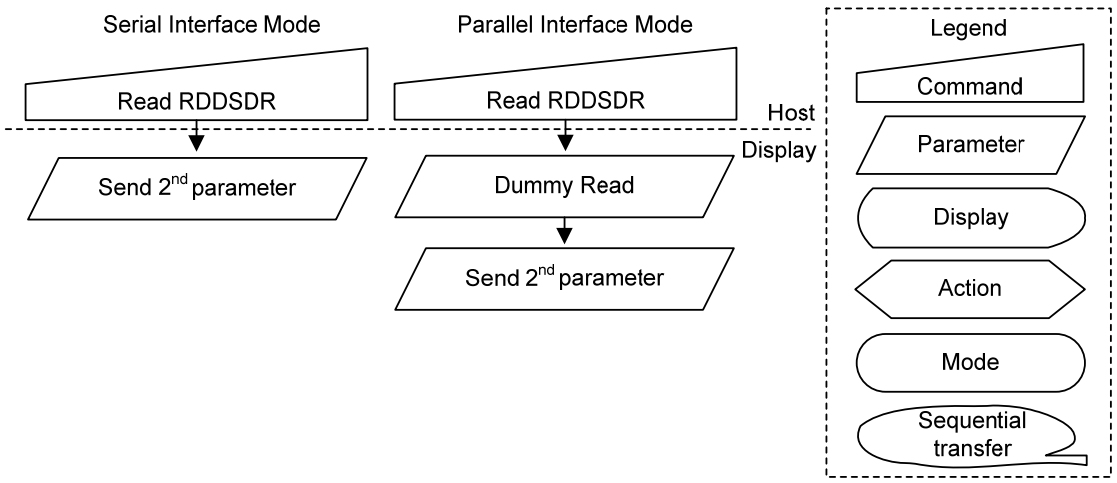
5.1.8 READ DISPLAY SIGNAL MODE (0EH)

<table>
<tr><th>0EH</th><th colspan="12">RDDSM (Read Display Signal Mode)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0E</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>D7</td><td>D6</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display signal mode as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Tearing Effect Line On/Off</td><td>“1” = On, “0” = Off</td></tr>
<tr><td>D6</td><td>Tearing effect line mode</td><td>“0” = Mode1
“1” = Mode2</td></tr>
<tr><td>D5</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D4</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D3</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D2</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D1</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D0</td><td>Not Used</td><td>“0”</td></tr>
</table>
NOTE: “X“ denotes “Don’t care”</td></tr>
<tr><td>Restrictions</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="6">Status</td><td colspan="6">Availability</td></tr>
<tr><td></td><td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td></td><td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td></td><td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td></td><td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td></td><td colspan="6">Sleep In or Step up circuit Off</td><td colspan="6">Yes</td></tr>
<tr><td>Default</td><td colspan="6">Status</td><td colspan="6">Default Value</td></tr>
<tr><td></td><td colspan="6">Power On Sequence</td><td colspan="6">0000_0000</td></tr>
<tr><td></td><td colspan="6">S/W Reset</td><td colspan="6">0000_0000</td></tr>
<tr><td></td><td colspan="6">H/W Reset</td><td colspan="6">0000_0000</td></tr>
</table>

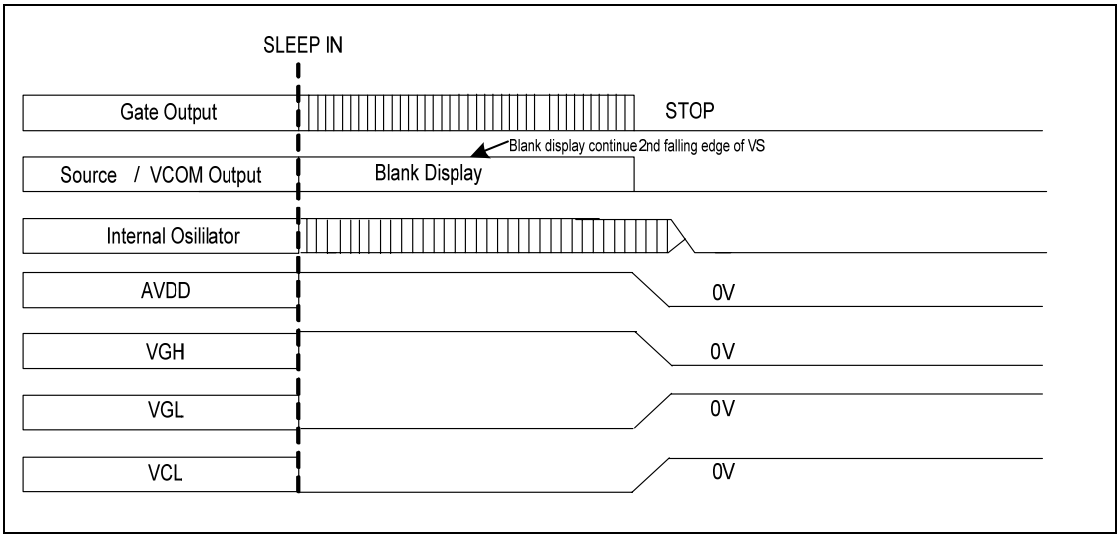
0EH	RDDSM (Read Display Signal Mode)
Flow Chart	

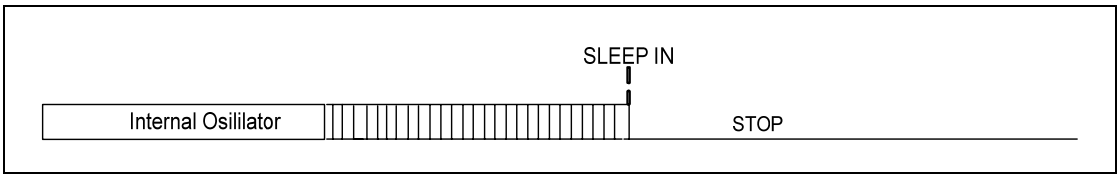
5.1.9 READ DISPLAY SELF-DIAGNOSTIC RESULT (0FH)

<table>
<tr><th>0FH</th><th colspan="12">RDDSDR (Read Display Self-Diagnostic Result)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0F</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>D7</td><td>D6</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display self-diagnostics as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Register Loading Detection</td><td>See section 4.7</td></tr>
<tr><td>D6</td><td>Functionality Detection</td><td></td></tr>
<tr><td>D5</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D4</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D3</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D2</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D1</td><td>Not Used</td><td>“0”</td></tr>
<tr><td>D0</td><td>Not Used</td><td>“0”</td></tr>
<tr><td colspan="3">NOTE: “X“ denotes “Don’t care”</td></tr>
</table></td></tr>
<tr><td>Restrictions</td><td colspan="12"></td></tr>
<tr><td rowspan="6">Register Availability</td><td colspan="6">Status</td><td colspan="6">Availability</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Sleep In or Step up circuit Off</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="4">Default</td><td colspan="6">Status</td><td colspan="6">Default Value</td></tr>
<tr><td colspan="6">Power On Sequence</td><td colspan="6">0000_0000</td></tr>
<tr><td colspan="6">S/W Reset</td><td colspan="6">0000_0000</td></tr>
<tr><td colspan="6">H/W Reset</td><td colspan="6">0000_0000</td></tr>
</table>

0FH	RDDSDR (Read Display Self-Diagnostic Result)
Flow Chart	

5.1.10 SLPIN: SLEEP IN (10H)

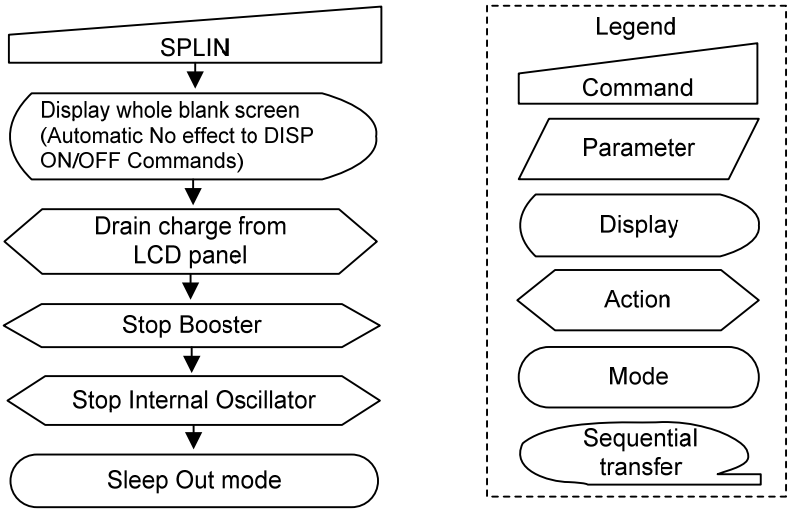
<table>
<tr><th>10H</th><th colspan="10">SLPIN: SLEEP IN</th></tr>
<tr><td>Inst/Para</td><td>R/W</td><td>DCX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>SLPIN</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10h</td></tr>
<tr><td>Parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">
A Case (APON=1 && DISP_SEL=1)
This command causes the LCD module to enter the power saving mode.
During this mode, the Booster, Internal display oscillator and panel scanning are not in operation.


A Case (APON=0 && DISP_SEL=0)
This command causes halting OSC Operation.


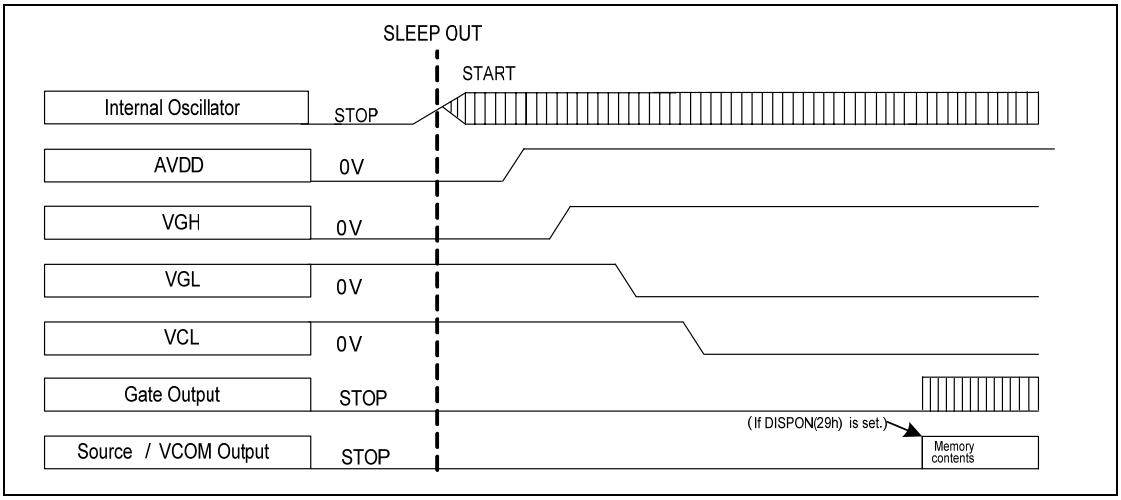
MPU interface and memory are still in normal operation and the memory keeps its contents.
</td></tr>
<tr><td>Restriction</td><td colspan="10">
This command has no effect when module is already in sleep in mode. Sleep In Mode can only exit by the Sleep Out Command (11h).
It is necessary to wait for 5msec after SLPIN command, to send next command, It is allowing time for the supply voltages and clock circuits to stabilize.

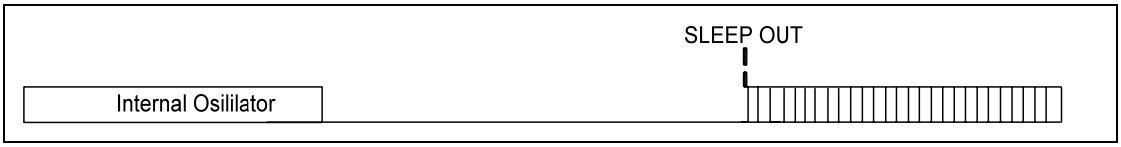
A Case (APON=1)
It is necessary to wait for 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.
</td></tr>
<tr><td rowspan="3">Register Availability</td><td colspan="6">Status</td><td colspan="4">Availability</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="4">Yes</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="4">Yes</td></tr>
</table>

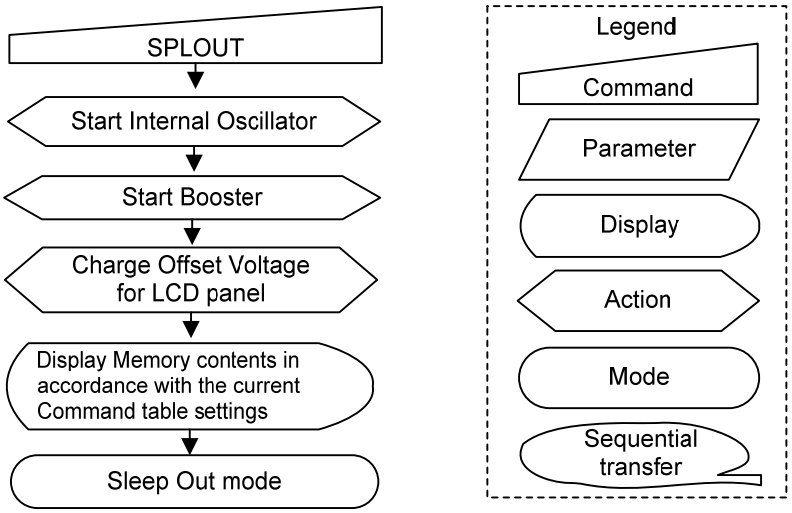
10H	SLPIN: SLEEP IN	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	**Status**	**Default Value**
	Power On Sequence	Sleep in mode
	S/W Reset	Sleep in mode
	H/W Reset	Sleep in mode
Flow Chart	**A Case (APON=1)** It takes about 120msec before it goes into Sleep-in Mode (Booster off state) after SLPIN command. The Booster States can be checked by RDDST(09h) command Bit 31.	



5.1.11 SLPOUT: SLEEP OUT (11H)

<table>
<tr><th>11H</th><th colspan="10">SLPOUT: SLEEP OUT</th></tr>
<tr><td>Inst/Para</td><td>R/W</td><td>DCX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>SLPOUT</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="10">No Parameter</td></tr>
<tr><td>Description</td><td colspan="10">A Case (APON=1 and DISP_SEL=1)
This command turns off the sleep mode.
During this mode, the Booster, the Internal display oscillator, and panel scanning are in normal operation.
 

B Case (APON=0 and DISP_SEL=0)
This command causes starting OSC Operation.
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the module is already in sleep out mode. Sleep Out Mode can only exit by the Sleep In Command (10h).
It is necessary to wait for 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
S6D05A1 loads the default values of extended and test commands to the registers during this 5msec duration. There cannot be any abnormal visual effect on the display image if those default and register values are the same when this loading is done and when the S6D05A1 is already in Sleep Out –mode.
S6D05A1 performs self-diagnostic during this 5msec. See also section 4.7.
A Case (APON=1)
It is necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td rowspan="2">Register</td><td colspan="6">Status</td><td colspan="4">Availability</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="4">Yes</td></tr>
</table>

11H	SLPOUT: SLEEP OUT	
Availability	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	**Status**	**Default Value**
	Power On Sequence	Sleep in mode
	S/W Reset	Sleep in mode
	H/W Reset	Sleep in mode
Flow Chart	**A Case (APON=1)** It takes 120msec to be in Sleep Out mode (booster on mode) after SLPOUT command is issued. The booster on status can be checked by RDDST (09h) command Bit31. 	

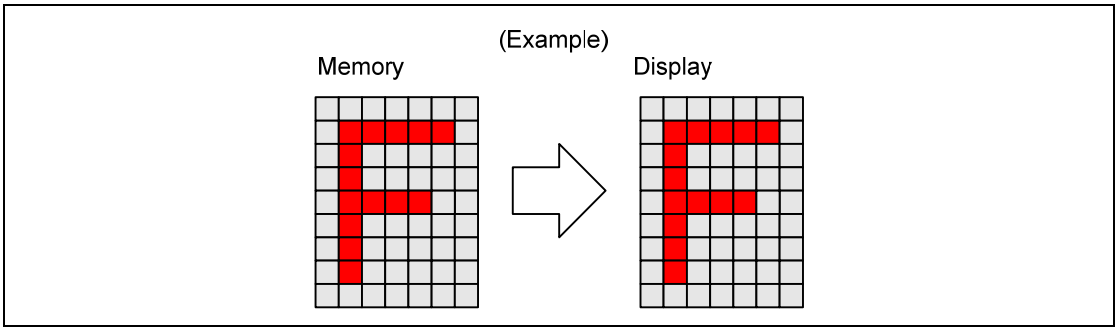
5.1.12 PTLON: PARTIAL DISPLAY MODE ON (12H)

12H	PTLON: PARTIAL DISPLAY MODE ON										
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	W	0	0	0	0	1	0	0	1	0	12h
Parameter	No Parameter										
Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. There is no abnormal visual effect during mode change between Normal mode On and Partial mode On.										
Restriction	This command has no effect when Partial mode is active.										
Register Availability	**Status**						**Availability**				
	Normal Mode On, Idle Mode Off, Sleep Out						Yes				
	Normal Mode On, Idle Mode On, Sleep Out						Yes				
	Partial Mode On, Idle Mode Off, Sleep Out						Yes				
	Partial Mode On, Idle Mode On, Sleep Out						Yes				
	Sleep In						Yes				
Default	**Status**						**Default Value**				
	Power On Sequence						Normal Mode On				
	S/W Reset						Normal Mode On				
	H/W Reset						Normal Mode On				
Flow Chart	See Partial Area (30h)										

5.1.13 NORON: NORMAL DISPLAY MODE ON (13H)

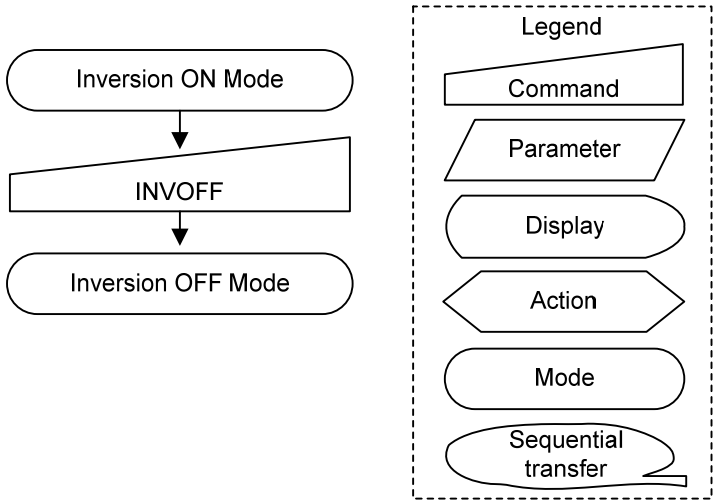
13H	NORON: NORMAL DISPLAY MODE ON										
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NORON	W	0	0	0	0	1	0	0	1	1	13h
Parameter	No Parameter										
Description	This command returns the display to normal mode. Turning normal display mode on means Partial mode off. Exiting from NORON can be done by the Partial mode On command (12h). There is no abnormal visual effect during the mode change from Normal mode On to Partial mode On.										
Restriction	This command has no effect when Normal Display mode is active.										
Register Availability	**Status**							**Availability**			
	Normal Mode On, Idle Mode Off, Sleep Out							Yes			
	Normal Mode On, Idle Mode On, Sleep Out							Yes			
	Partial Mode On, Idle Mode Off, Sleep Out							Yes			
	Partial Mode On, Idle Mode On, Sleep Out							Yes			
	Sleep In							Yes			
Default	**Status**							**Default Value**			
	Power On Sequence							Normal Mode On			
	S/W Reset							Normal Mode On			
	H/W Reset							Normal Mode On			
Flow Chart	See Partial Area for details of when to use this command.										

5.1.14 DISPLAY INVERSION OFF (20H)

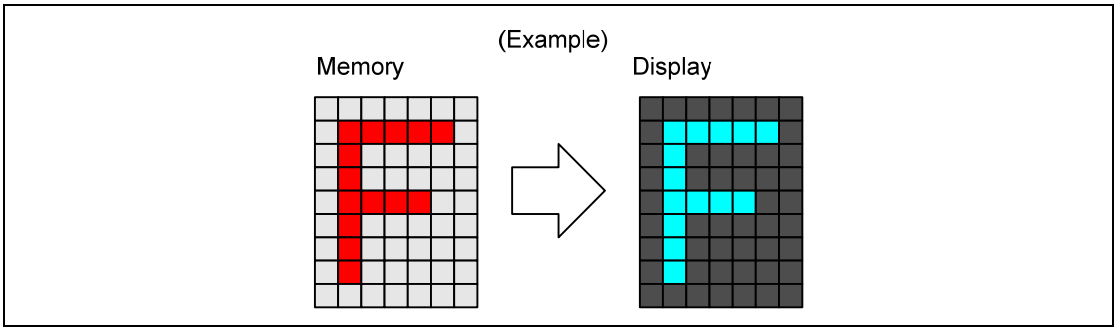
20H	DISPLAY INVERSION OFF										
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	W	0	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter										
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. 										
Restriction	This command has no effect when module is already in inversion off mode.										

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	Display Inversion off
	S/W Reset	Display inversion off
	H/W Reset	Display inversion off

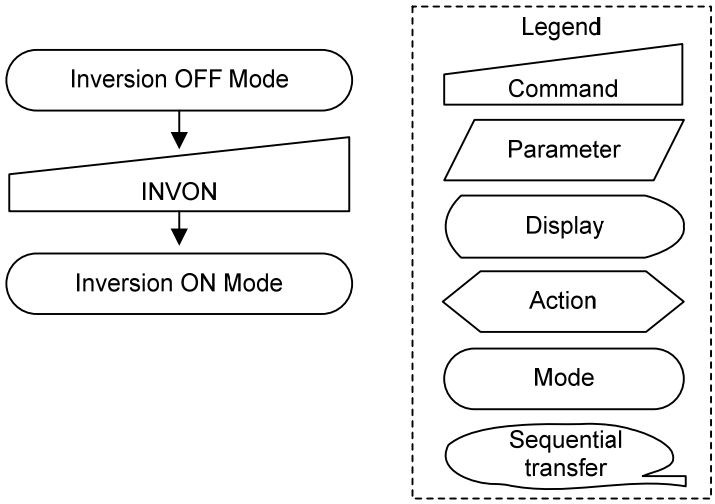
20H	DISPLAY INVERSION OFF
Flow Chart	

5.1.15 DISPLAY INVERSION ON (21H)

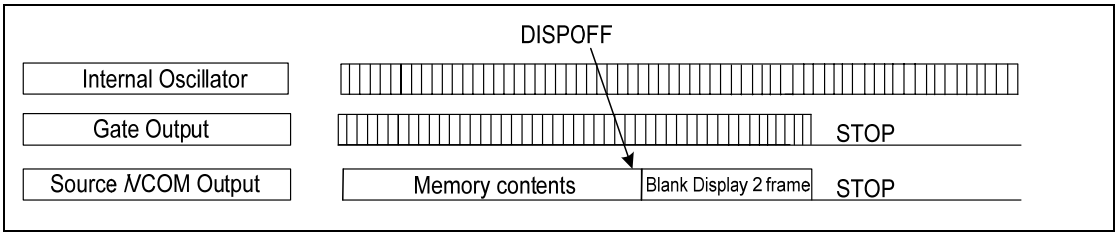
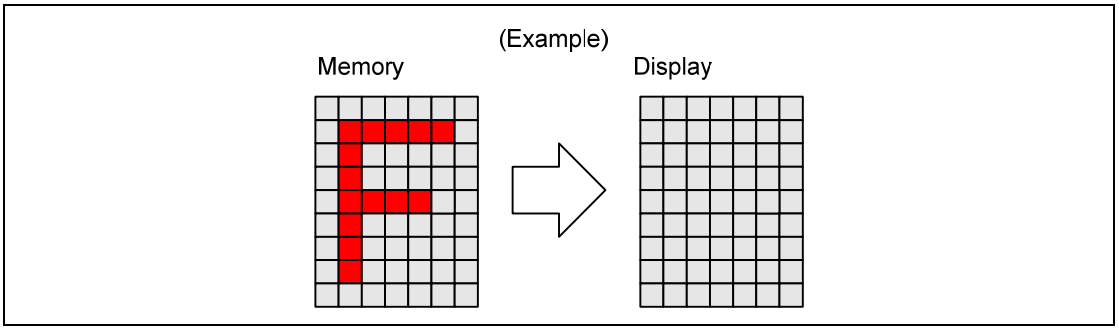
21H	DISPLAY INVERSION ON										
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	W	0	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter										
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status 										
Restriction	This command has no effect when module is already in inversion off mode.										

Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	**Status**	**Default Value**
	Power On Sequence	Display Inversion off
	S/W Reset	Display inversion off
	H/W Reset	Display inversion off

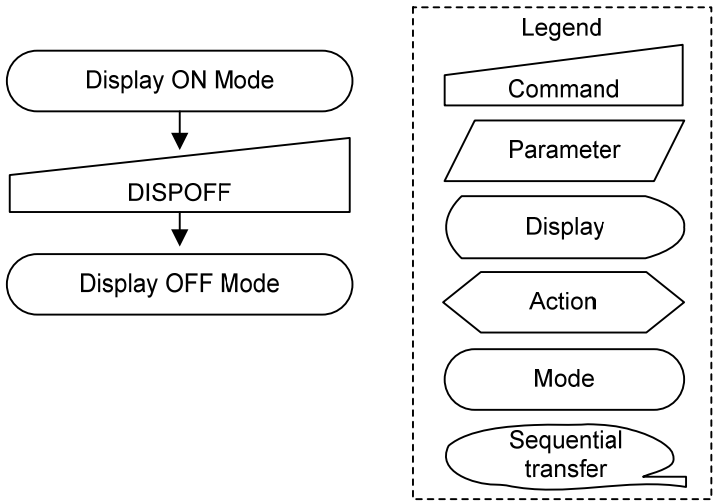
21H	DISPLAY INVERSION ON
Flow Chart	

5.1.16 DISPOFF: DISPLAY OFF (28H)

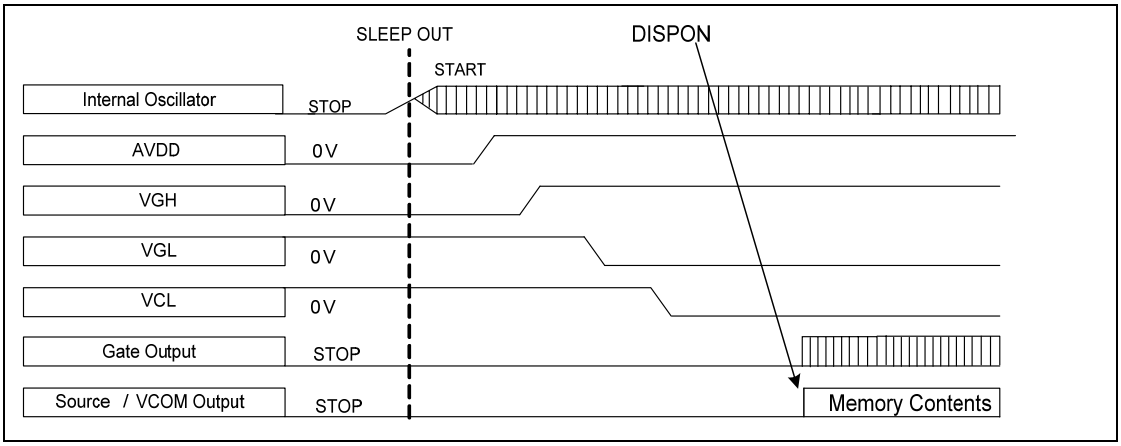
28H	DISPOFF: DISPLAY OFF										
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	W	0	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter										
Description	This command turns on DISPLAY OFF mode. During this mode, the output from the Frame Memory is disabled. This command makes no change to the contents of frame memory. This command does not alter any other status. There will be no abnormal visible effect on the display. **A Case (DISP_SEL=1)**  Exiting from this command can be done by Display On (29h)  										
Restriction	This command has no effect when module is already in Display Off mode. When DISP_SEL is Low, DISPOFF Command is ignored, and Display Status is controled by D[1:0]										

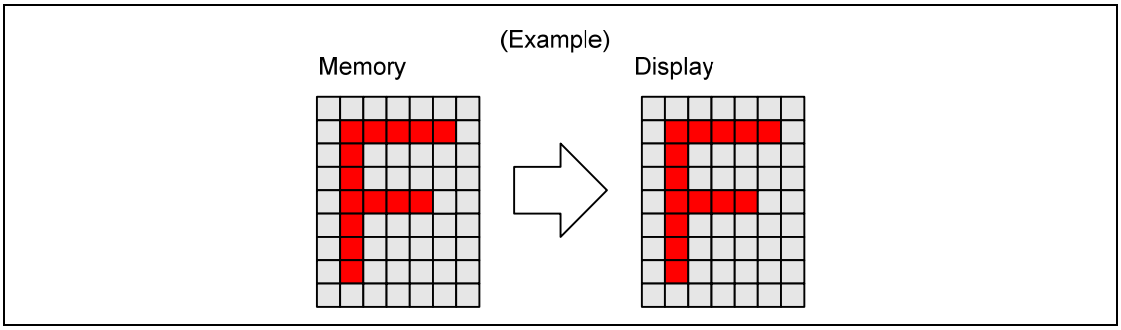
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

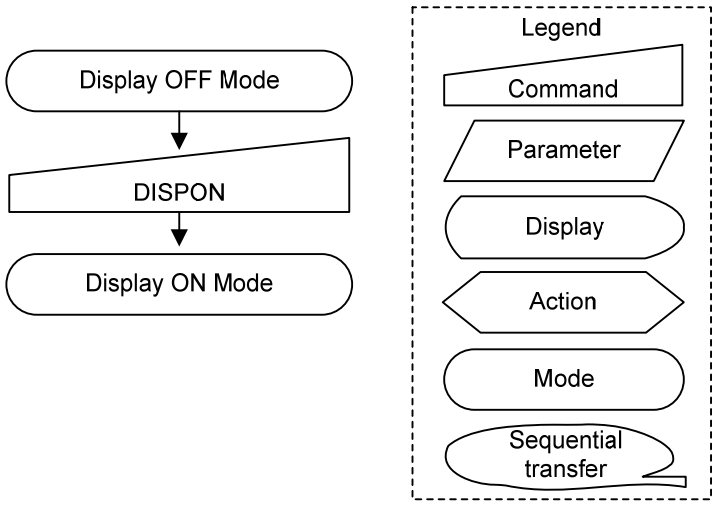
Default	**Status**	**Default Value**
	Power On Sequence	Display off
	Status	**Default Value**
	S/W Res	Display off

28H	DISPOFF: DISPLAY OFF	
	H/W Reset	Display off
Flow Chart		

5.1.17 DISPON: DISPLAY ON (29H)

<table>
<tr><th>29H</th><th colspan="11">DISPON: DISPLAY ON</th></tr>
<tr><td>Inst/Para</td><td>R/W</td><td>DCX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>DISPON</td><td>W</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="11">No Parameter</td></tr>
<tr><td>Description</td><td colspan="11">This command enables DISPLAY ON mode. Output from the Frame Memory is enabled.
This command makes no change to the contents of frame memory.
A Case (APON=1 and DISP_SEL=1)
 

This command does not alter any other status.
 
</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when the module is already in Display On mode.
When DISP_SEL is Low, DISPON Command is ignored, Display Status is controled by D[1:0]</td></tr>
<tr><td rowspan="6">Register Availability</td><td colspan="8">Status</td><td colspan="3">Availability</td></tr>
<tr><td colspan="8">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="3">Yes</td></tr>
<tr><td colspan="8">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="3">Yes</td></tr>
<tr><td colspan="8">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="3">Yes</td></tr>
<tr><td colspan="8">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="3">Yes</td></tr>
<tr><td colspan="8">Sleep In</td><td colspan="3">Yes</td></tr>
<tr><td rowspan="2">Default</td><td colspan="8">Status</td><td colspan="3">Default Value</td></tr>
<tr><td colspan="8">Power On Sequence</td><td colspan="3">Display off</td></tr>
</table>

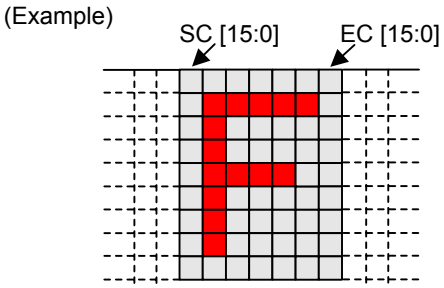
29H	DISPON: DISPLAY ON	
	S/W Reset	Display off
	H/W Reset	Display off
Flow Chart		

5.1.18 COLUMN ADDRESS SET (2AH)

2AH	CASET (Column Address Set)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	0	2A
1st Parameter	1	1	↑	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note
2nd Parameter	1	1	↑	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note
4th Parameter	1	1	↑	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MPU can access.
This command makes No Change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes.
Each value represents one column line in the Frame Memory.



Restriction

SC[15:0] always must be equal to or less than EC[15:0]. When SC[15:0] or EC[15:0] is greater than maximum address as below, data of out of range will be ignored.

NOTE:

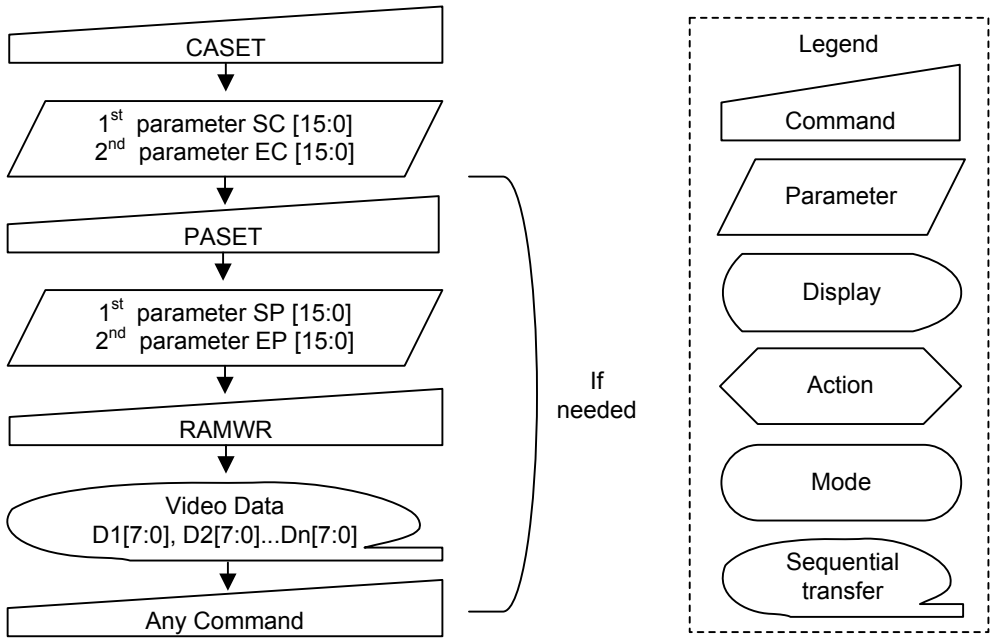
(Parameter range: 0 ≤ SC[15:0], EC[15:0] ≤ 359 (0167h) (B5=0)
(Parameter range: 0 ≤ SC[15:0], EC[15:0] ≤ 479 (01DFh) (B5=1)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000h	EC[15:0]=013Fh (319d)
S/W Reset	SC[15:0]=0000h	EC[15:0]=013Fh (319d)
H/W Reset	SC[15:0]=0000h	EC[15:0]=013Fh (319d)

2AH	CASET (Column Address Set)
Flow Chart	

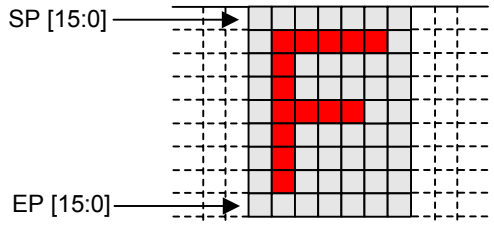
5.1.19 PAGE ADDRESS SET (2BH)

2BH	PASET (Page Address Set)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	1	2B
1st Parameter	1	1	↑	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note
2nd Parameter	1	1	↑	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd Parameter	1	1	↑	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note
4th Parameter	1	1	↑	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MPU can access.
This command makes No Change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.

(Example)



Restriction

SP[15:0] always must be equal to or less than EP[15:0]. When SP[15:0] or EP[15:0] is greater than maximum address as below, data of out of range will be ignored.

NOTE:

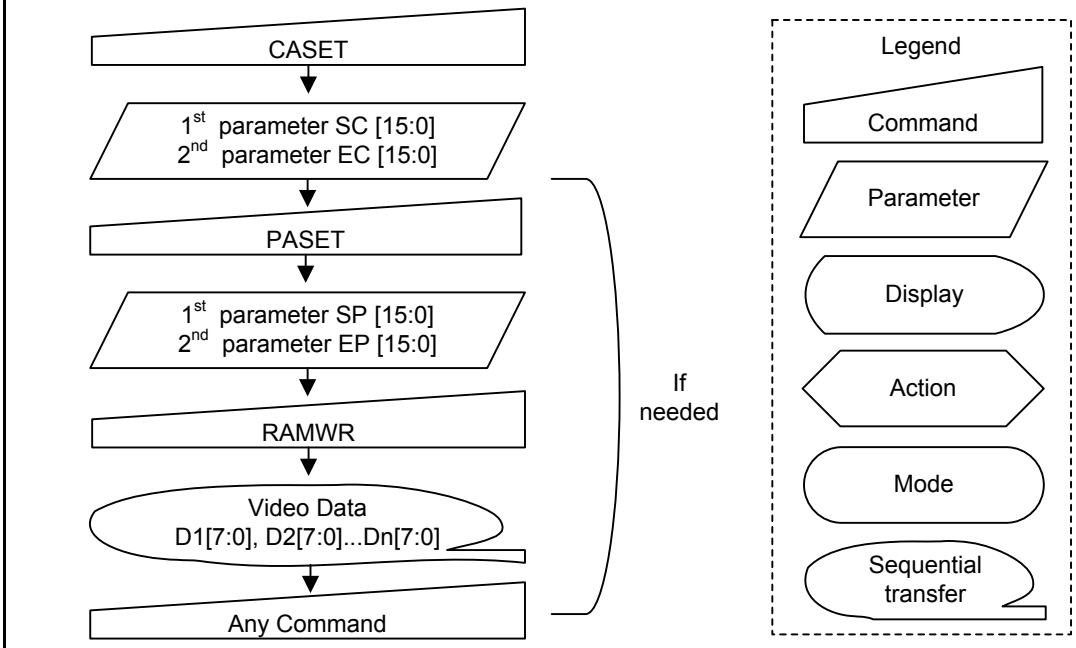
(Parameter range: 0 ≤ SP[15:0], EP[15:0] ≤ 479 (01DFh) (B5=0)
(Parameter range: 0 ≤ SP[15:0], EP[15:0] ≤ 359 (0167h) (B5=1)

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Step up circuit Off	Yes

Default

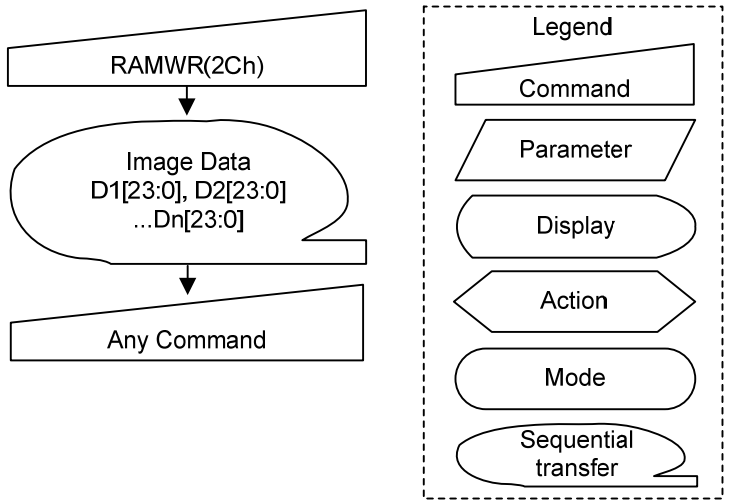
Status	Default Value	
Power On Sequence	SP[15:0]=0000h	EP[15:0]=01DFh
S/W Reset	SP[15:0]=0000h	EP[15:0]=01DFh (479d)
H/W Reset	SP[15:0]=0000h	EP[15:0]=01DFh (479d)

2BH	PASET (Page Address Set)
Flow Chart	

5.1.20 RAMWR: MEMORY WRITE (2CH)

2CH	RAMWR: MEMORY WRITE											
Inst/Para	R/W	DCX	D23 ~ D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	W	0	X	0	0	1	0	1	1	0	0	2Ch
1st para		1	D123 ~ 18	D17	D16	D15	D14	D13	D12	D11	D10	000000h~ FFFFFFh
:		1	Dx ~ Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	000000h~ FFFFFFh
Nth para		1	Dn23 ~ n8	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	000000h~ FFFFFFh

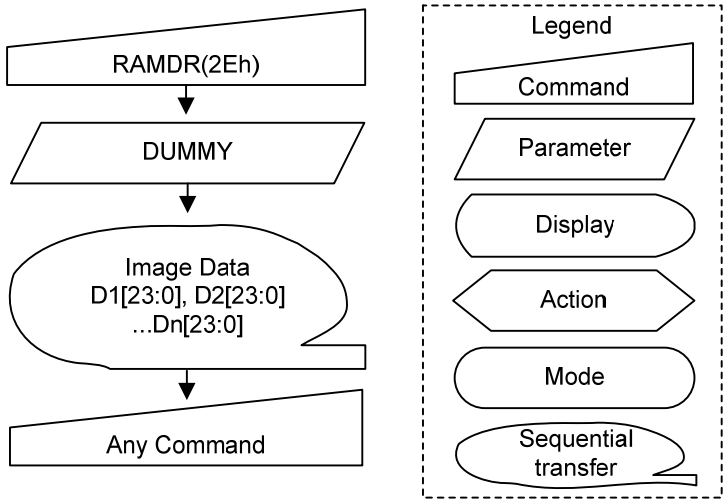
Description	This command is used to transfer data from MPU to the frame memory. This command makes no change to the other status of the driver. When this command is issued, the Column register and the Page register are programmed to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See section 4.5.2) Then D [23:0] is stored in the frame memory, the Column register and the Page register increments as in section 4.5.2 Sending any other command can stop the Frame Write.	
Restriction	In all color modes, there is no restriction on the length of the parameters.	
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	**Status**	**Default Value**
	Power On Sequence	Contents of memory is set randomly
	S/W Reset	Contents of memory is not cleared
	H/W Reset	Contents of memory is not cleared

2CH	RAMWR: MEMORY WRITE
Flow Chart	

5.1.21 RAMRD: MEMORY READ (2EH)

2EH	RAMRD: MEMORY READ											
Inst/Para	R/W	DCX	D23 ~ D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	R	0	X	0	0	1	0	1	1	1	0	2Eh
Dummy read		1	X	X	X	X	X	X	X	X	X	XX
2nd para		1	D123 ~ 8	D17	D16	D15	D14	D13	D12	D11	D10	000000h~ FFFFFFh
:		1	Dx ~ Dx	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	000000h~ FFFFFFh
(N+1)th para		1	Dn23 ~ 8	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	000000h~ FFFFFFh

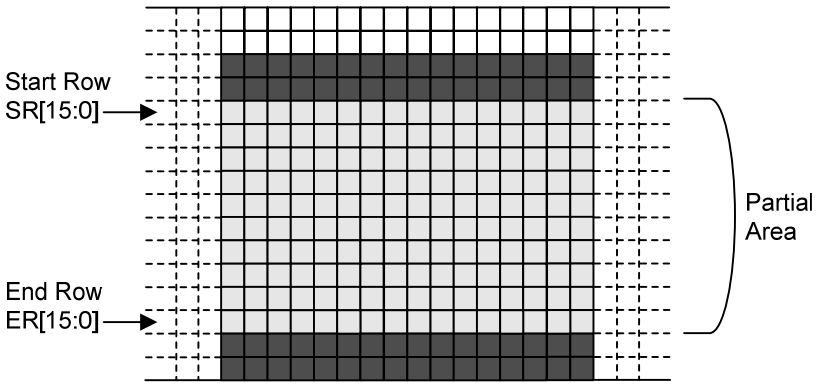
Description	This command is used to transfer data from the frame memory to MPU. This command makes no change to the other driver status. With this command, the column register and the Page register are programmed to the Start Column/Start Page positions.The Start Column/Start Page positions are different in accordance with MADCTL setting. (See section 4.5.2) Then D[23:0] is read back from the frame memory, and the column register and the Page register increments as in section 4.5.2 Frame Read can be cancelled by sending any other command. See section 3.2 “Display Data Format” for color coding. **NOTE:** “X“ denotes “Don’t care"	
Restriction	-	
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	**Status**	**Default Value**
	Power On Sequence	Contents of memory is set randomly
	S/W Reset	Contents of memory is not cleared
	H/W Reset	Contents of memory is not cleared

2EH	RAMRD: MEMORY READ
Flow Chart	

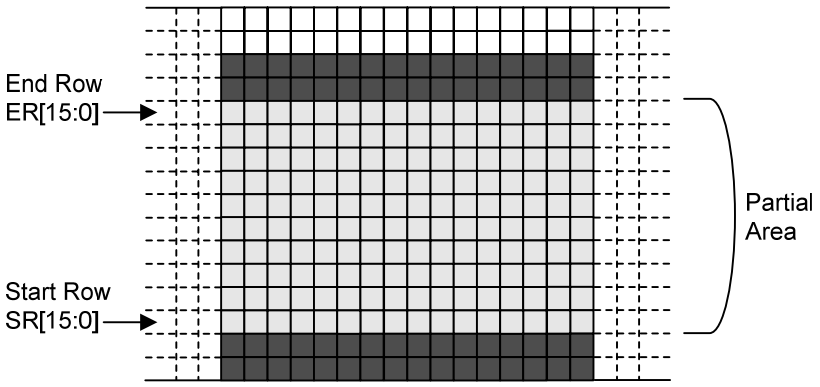
5.1.22 PARTIAL AREA (30H)

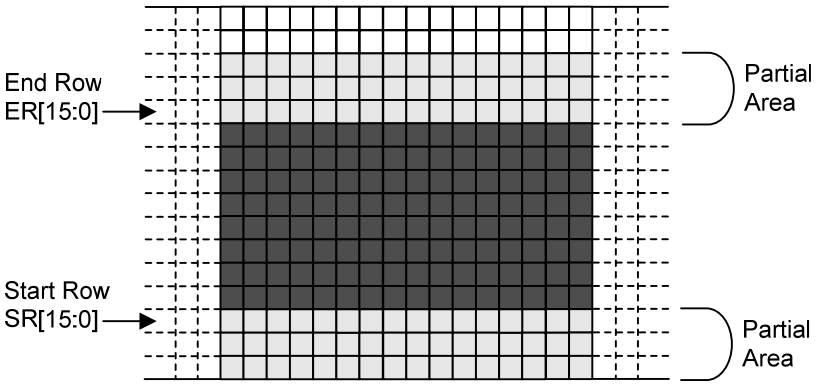
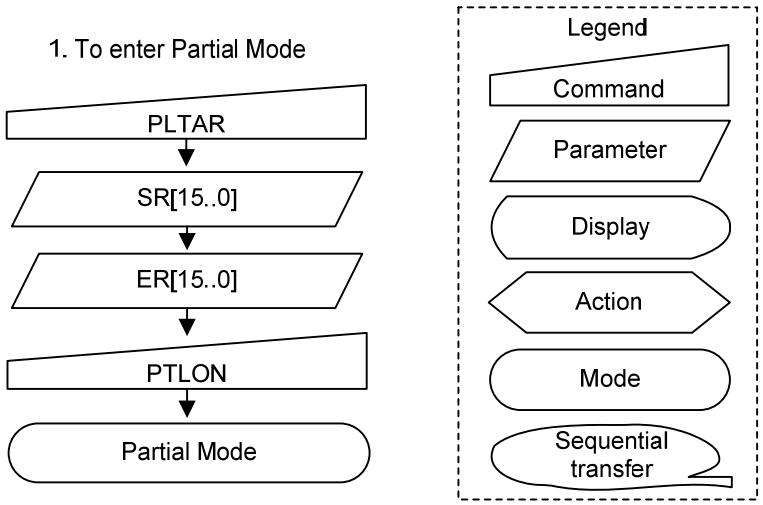
30H	PLTAR (Partial Area)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	0	0	30
1st Parameter	1	1	↑	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000… 01DF
2nd Parameter	1	1	↑	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
3rd Parameter	1	1	↑	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000… 01DF
4th Parameter	1	1	↑	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row(SR) and the second defines the End Row(ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.											

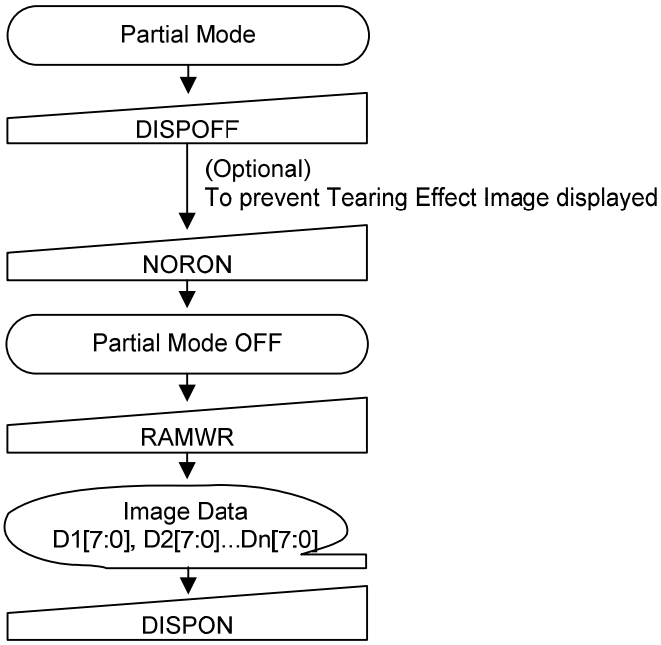
If End Row>Start Row When MADCTL B4=0:



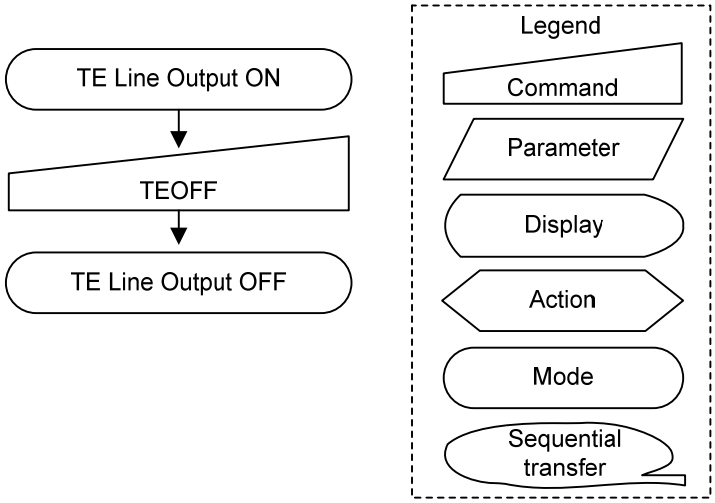
If End Row>Start Row When MADCTL B4=1:



30H	PLTAR (Partial Area)	
	If End Row<Start Row When MADCTL B4=0:  If End Row=Start Row then the Partial Area will be one row deep.	
Restriction	Each detail initial values by the display resolution will be updated.	
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes
Default	**Status**	**Default Value**
	Power On Sequence	SR[15:0]=0000h ER[15:0]=01DFh
	S/W Reset	SR[15:0]=0000h ER[15:0]=01DFh
	H/W Reset	SR[15:0]=0000h ER[15:0]=01DFh
Flow Chart	 	

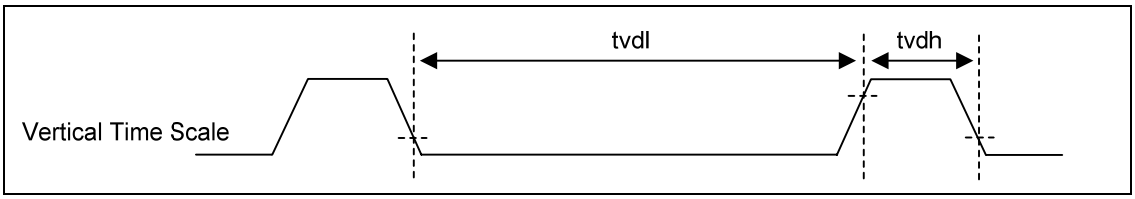
30H	PLTAR (Partial Area)
	2. To exit Partial Mode: 

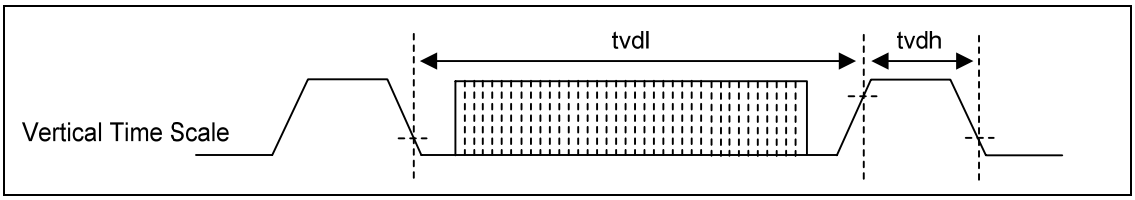
5.1.23 TEARING EFFECT LINE OFF (34H)

<table>
<tr><th>34 H</th><th colspan="11">TEOFF (Tearing Effect Line OFF)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34</td></tr>
<tr><td>Parameter</td><td colspan="11">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to turn Off (Active Low) the Tearing Effect output signal from TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when Tearing Effect output is already Off.</td></tr>
<tr><td rowspan="6">Register Availability</td><td colspan="6">Status</td><td colspan="6">Availability</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Sleep In or Step up circuit Off</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="4">Default</td><td colspan="6">Status</td><td colspan="6">Default Value</td></tr>
<tr><td colspan="6">Power On Sequence</td><td colspan="6">Off</td></tr>
<tr><td colspan="6">S/W Reset</td><td colspan="6">Off</td></tr>
<tr><td colspan="6">H/W Reset</td><td colspan="6">Off</td></tr>
<tr><td>Flow Chart</td><td colspan="11"> 
</td></tr>
</table>

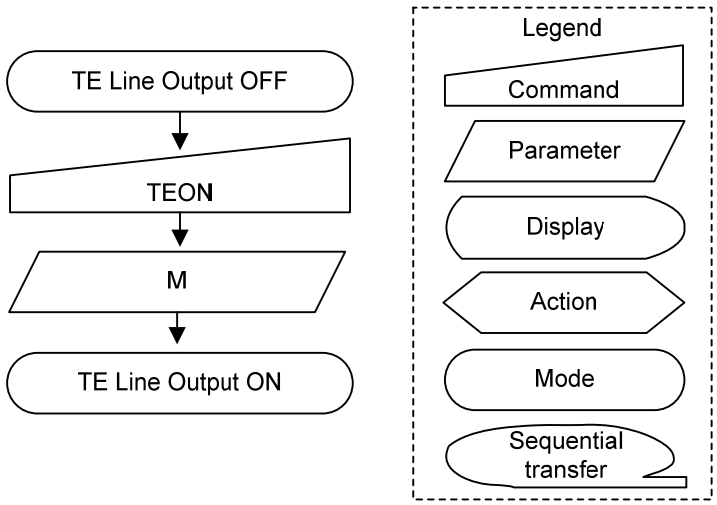
5.1.24 TEARING EFFECT LINE ON (35H)

<table>
<tr><th>35 H</th><th colspan="12">TEON (Tearing Effect Line ON)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>M</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to turn On the Tearing Effect output signal from the TE signal line.
This output is not affected by changing Memory Address Control command bit “B4”.
The Tearing Effect Line On has one parameter that describes the mode of the Tearing Effect Output Line. (X = don’t care).

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:
 

During Sleep In mode with Tearing Effect Line On, Tearing Effect output pin will be active low.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Tearing Effect output is already On.</td></tr>
<tr><td rowspan="6">Register Availability</td><td colspan="6">Status</td><td colspan="6">Availability</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="6">Yes</td></tr>
<tr><td colspan="6">Sleep In or Step up circuit Off</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="4">Default</td><td colspan="6">Status</td><td colspan="6">Default Value</td></tr>
<tr><td colspan="6">Power On Sequence</td><td colspan="6">Off</td></tr>
<tr><td colspan="6">S/W Reset</td><td colspan="6">Off</td></tr>
<tr><td colspan="6">H/W Reset</td><td colspan="6">Off</td></tr>
</table>

35 H	TEON (Tearing Effect Line ON)
Flow Chart	

5.1.25 MEMORY DATA ACCESS CONTROL (36H)

36 H	MADCTL (Memory Data Access Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	0	36
Parameter	1	1	↑	B7	B6	B5	B4	B3	x	x	x	xx

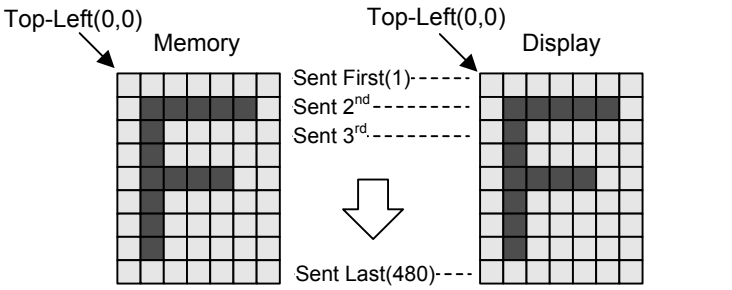
Description: This command defines read/write scanning direction of frame memory.
This command makes No Change on the other driver status.

Bit	NAME	DESCRIPTION
B7	Page Address order(MY)	These 3bits control MPU to memory write / read Direction.
B6	Column Address order(MX)	
B5	Page/Column exchange(MV)	
B4	Vertical refresh order(ML)	LCD refresh direction control
B3	RGB-BGR order(RGB)	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)

B4 - Vertical Updating Order

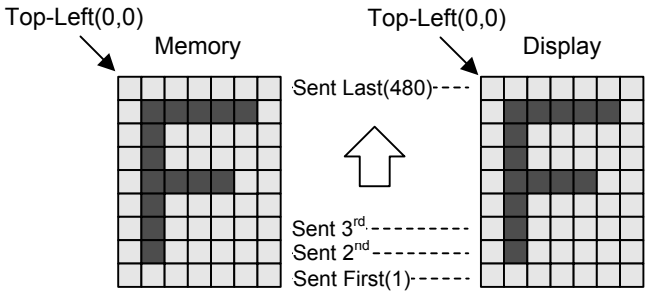
B4 = "0"

(Example)

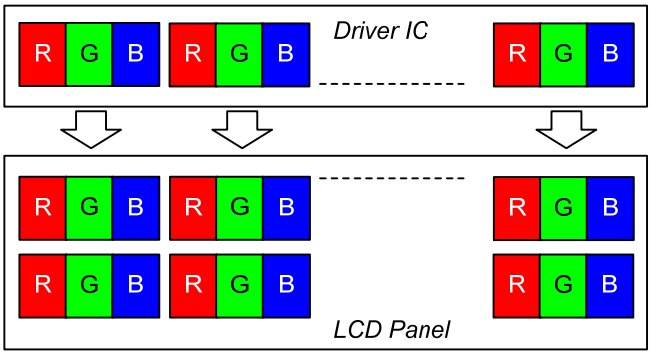


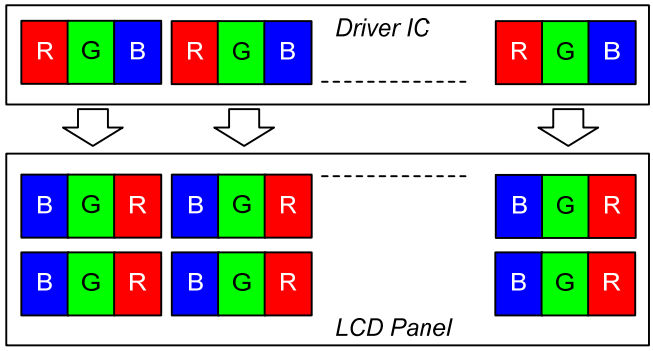
B4 = "1"

(Example)

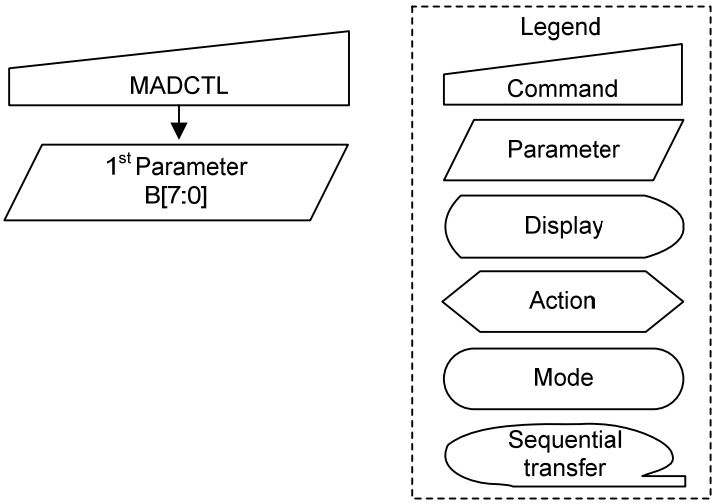


<table>
<tr><th>36 H</th><th colspan="2">MADCTL (Memory Data Access Control)</th></tr>
<tr><td></td><td colspan="2">D3(RGB) : RGB - BGR Order

RGB = “0”
 

RGB = “1”
 

NOTE:
1. D3 setting is effective When display the panel, not Memory write action
2: Top-Left (0,0) means a physical memory location</td></tr>
<tr><td>Restriction</td><td colspan="2">D2, D1 and D0 of the 1st parameter are set to ‘00’ internally.
When GS=1, do not set D4 to 1, When NL is not 480 line, set D4 to 0.</td></tr>
<tr><td rowspan="6">Register Availability</td><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
<tr><td rowspan="4">Default</td><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>B7=0, B6=0, B5=0, B4=0, B3=0</td></tr>
<tr><td>S/W Reset</td><td>B7=0, B6=0, B5=0, B4=0, B3=0</td></tr>
<tr><td>H/W Reset</td><td>B7=0, B6=0, B5=0, B4=0, B3=0</td></tr>
</table>

36 H	MADCTL (Memory Data Access Control)
Flow Chart	

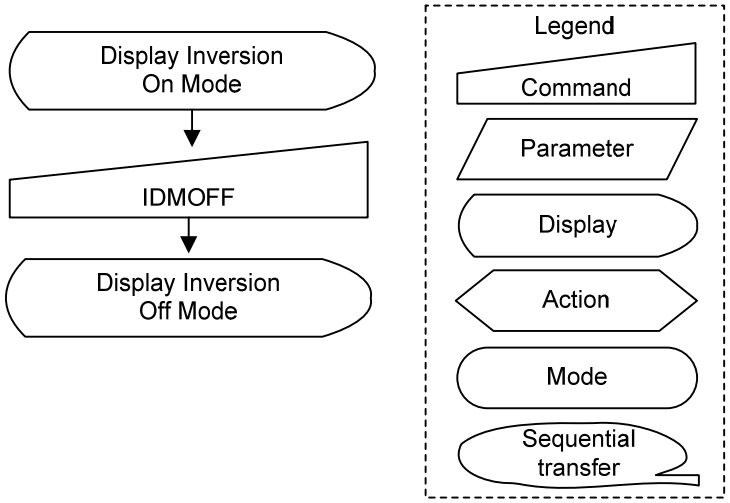
5.1.26 IDLE MODE OFF (38H)

38H	IDMOFF (Idle Mode Off)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER											
Description	This command is used to recover from idle mode on. In the idle off mode, LCD can display maximum 16.7M colors.											
Restriction	This command has no effect when module is already in idle off mode.											

Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

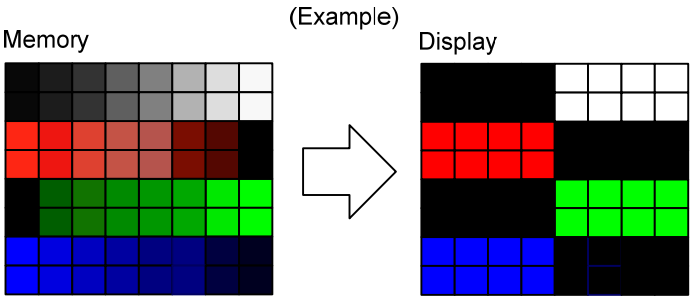
Default	**Status**	**Default Value**
	Power On Sequence	Idle off mode
	S/W Reset	Idle off mode
	H/W Reset	Idle off mode

Flow Chart



5.1.27 IDLE MODE ON (39H)

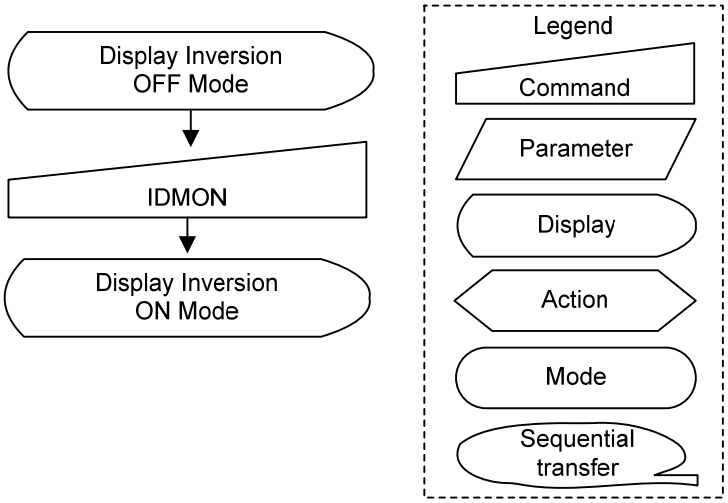
39H	IDMON (Idle Mode On)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER											
Description	This command turns Idle mode on. (Refer to section 4.9 8-Color mode) There will be no abnormal visible effect during mode transition. During the idle on mode, 1. Color expression is reduced to 8-color. 8-color is displayed by MSB of each R, G, and B in the Frame Memory. 2. 8-Color mode frame frequency is applied. 3. Exit from IDMON by Idle Mode Off (38h) command											



Color	$R_7R_6R_5R_4R_3R_2R_1R_0$	$G_7G_6G_5G_4G_3G_2G_1G_0$	$B_7B_6B_5B_4B_3B_2B_1B_0$
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

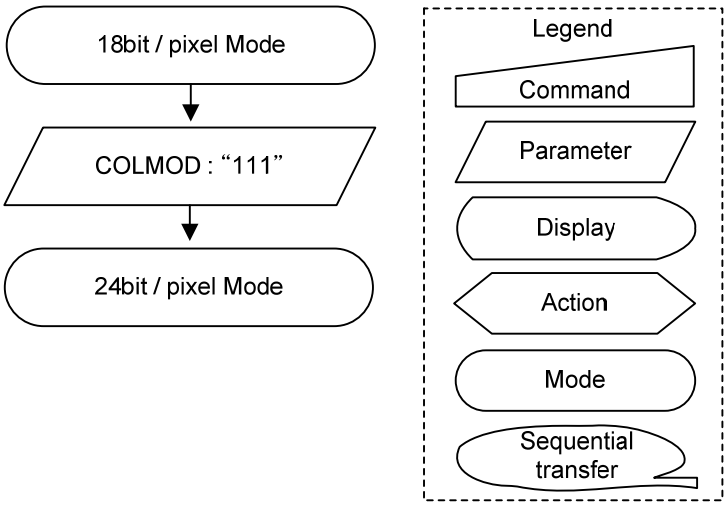
NOTE: "X" denotes "Don't care"

Restriction	This command has no effect when module is already in idle on mode.	
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes
Default	**Status**	**Default Value**

39H	IDMON (Idle Mode On)	
	Power On Sequence	Idle Off Mode
	S/W Reset	Idle Off Mode
	H/W Reset	Idle Off Mode
Flow Chart		

5.1.28 INTERFACE PIXEL FORMAT (3AH)

<table>
<tr><th>3AH</th><th colspan="12">COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td>DCX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>x</td><td>D6</td><td>D5</td><td>D4</td><td>x</td><td>D2</td><td>D1</td><td>D0</td><td>77</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to define the format of RGB picture data, which is to be transferred via the MPU interface. The formats are as shown in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>“0” (Not Used)</td></tr>
<tr><td>D6
D5
D4</td><td>RGB Interface Color Format (VFPF)</td><td>“101”=16-bits/pixel
“110”=18-bits/pixel
"111"= 24-bits/pixel
Others = not defined</td></tr>
<tr><td>D3</td><td>-</td><td>“0” (Not Used)</td></tr>
<tr><td>D2
D1
D0</td><td>Control Interface Color Format (IFPF)</td><td>“101”=16-bits/pixel
“110”=18-bits/pixel
"111"= 24-bits/pixel
Others = not defined</td></tr>
</table>
NOTE:
1. In 16-bit/pixel or 18-bit/pixel mode, display data is expended to 24bit data. Refer to Section 3.2.1
2. 12-bits/pixel (4096 color mode) is not supported.</td></tr>
<tr><td>Restriction</td><td colspan="12">There is no visible effect until the Frame Memory is written to.</td></tr>
<tr><td>Register Availability</td><td colspan="8">Status</td><td colspan="4">Availability</td></tr>
<tr><td></td><td colspan="8">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="4">Yes</td></tr>
<tr><td></td><td colspan="8">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="4">Yes</td></tr>
<tr><td></td><td colspan="8">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="4">Yes</td></tr>
<tr><td></td><td colspan="8">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="4">Yes</td></tr>
<tr><td></td><td colspan="8">Sleep In or Step up circuit Off</td><td colspan="4">Yes</td></tr>
<tr><td>Default</td><td colspan="8">Status</td><td colspan="4">Default Value</td></tr>
<tr><td></td><td colspan="8">Power On Sequence</td><td colspan="4">24 bit / pixel</td></tr>
<tr><td></td><td colspan="8">S/W Reset</td><td colspan="4">24 bit / pixel</td></tr>
<tr><td></td><td colspan="8">H/W Reset</td><td colspan="4">24 bit / pixel</td></tr>
</table>

3AH	COLMOD (Interface Pixel Format)
Flow Chart	

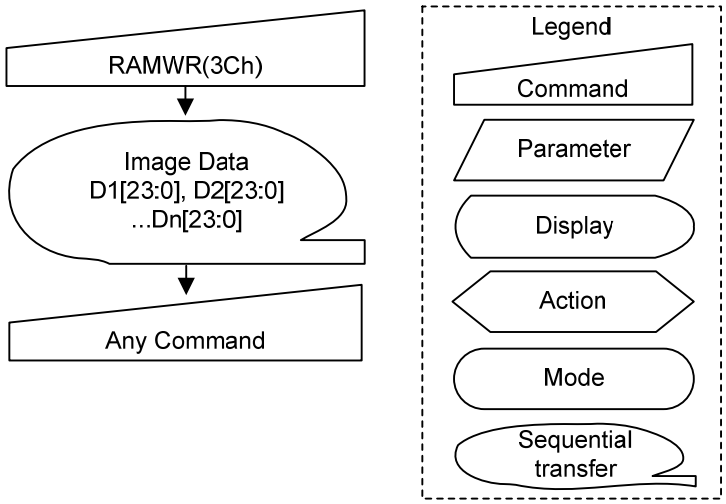
5.1.29 MEMORY WRITE CONTINUE (3CH)

3CH	RAMWRC (Memory Write Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	1	0	0	3C
1st Parameter	1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth Parameter	1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF

Description	This command is transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5=0:** Data is written continuing from the pixel location after the write range of the previous write_memory_continue or write_memory_start. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC +1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5=1:** Data is written continuing from the pixel location after the write range of the previous write_memory_continue or write_memory_start. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC +1) * (EP – SP + 1) the extra pixels are ignored.
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

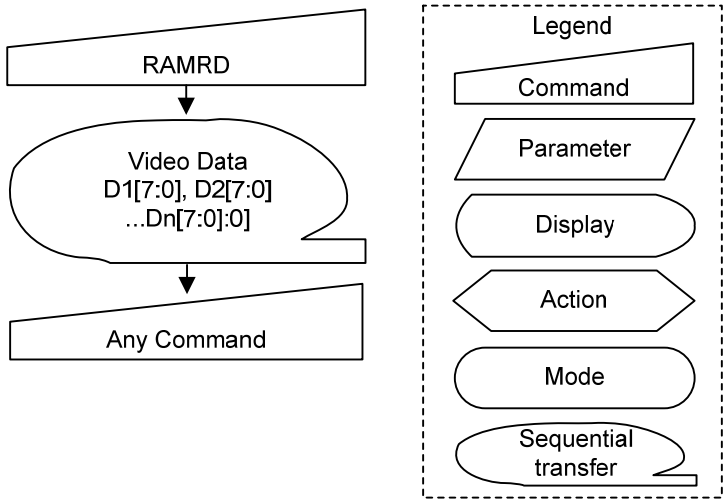
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

Default	**Status**	**Default Value**
	Power On Sequence	Contents of memory is set randomly
	S/W Reset	Contents of memory is not cleared
	H/W Reset	Contents of memory is not cleared

3CH	RAMWRC (Memory Write Continue)
Flow Chart	

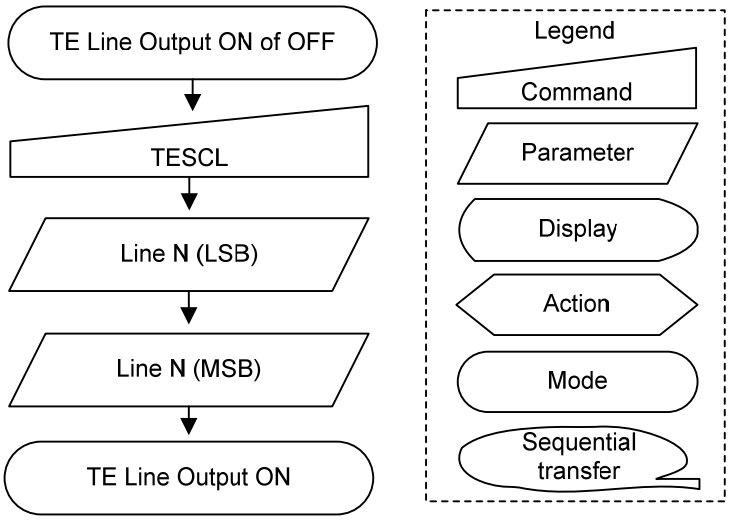
5.1.30 MEMORY READ CONTINUE (3EH)

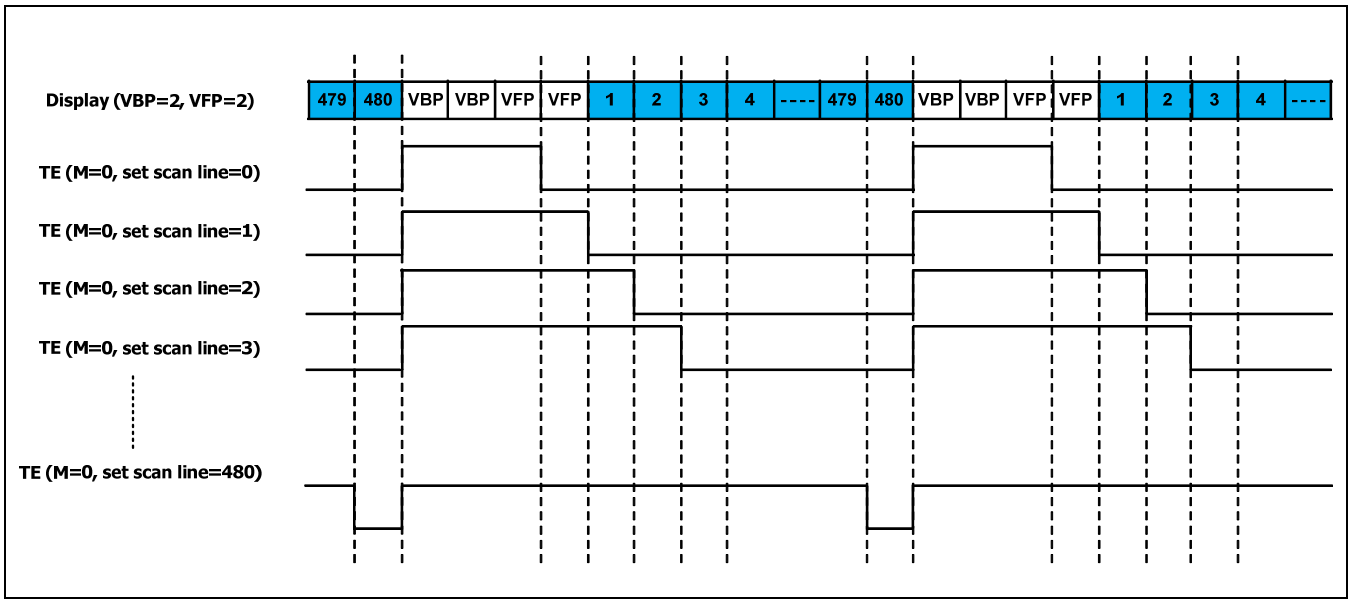
3EH	RAMRDC (Memory Read Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	1	1	0	3E
1st Parameter	1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth Parameter	1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command is transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. **If set_address_mode B5=0:** Pixels are read continuing from the pixel location after the read range of the previous read_memory_continue or read_memory_start. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. **If set_address_mode B5=1:** Pixels are read continuing from the pixel location after the read range of the previous read_memory_continue or read_memory_start. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.											
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data. A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read address. Otherwise, data read with read_memory_continue is undefined.											
Register Availability	**Status**							**Availability**				
	Normal Mode On, Idle Mode Off, Sleep Out							Yes				
	Normal Mode On, Idle Mode On, Sleep Out							Yes				
	Partial Mode On, Idle Mode Off, Sleep Out							Yes				
	Partial Mode On, Idle Mode On, Sleep Out							Yes				
	Sleep In or Step up circuit Off							Yes				
Default	**Status**							**Default Value**				
	Power On Sequence							Contents of memory is set randomly				
	S/W Reset							Contents of memory is not cleared				
	H/W Reset							Contents of memory is not cleared				

3EH	RAMRDC (Memory Read Continue)
Flow Chart	

5.1.31 TEAR SCAN LINE (44H)

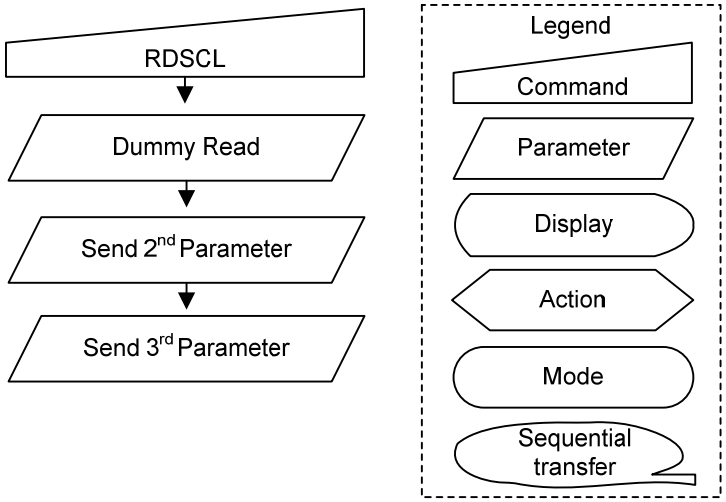
44H	TESCL (Tear Scan Line)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	0	0	1	0	0	44
1st Parameter	1	1	↑	N15	N14	N13	N12	N11	N10	N9	N8	00..FF
2nd Parameter	1	1	↑	N7	N6	N5	N4	N3	N2	N1	N0	00..FF
Description	This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only. Note that set_tear_scanline with N = 0 is equivalent to set_tear_on with M = 0. The Tearing Effect Output line shall be active low when the display module is in Sleep mode. See MIPI Alliance Standard for Display Bus Interface for definitions of tvdl and tvdh and MIPI Alliance Standard for Display Serial Interface for definition of display module line numbers											
Restriction	This command takes affect on the frame following the current frame. Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous set_tear_on, or set_tear_scanline, command until the end of the frame.											
Register Availability	**Status**										**Availability**	
	Normal Mode On, Idle Mode Off, Sleep Out										Yes	
	Normal Mode On, Idle Mode On, Sleep Out										Yes	
	Partial Mode On, Idle Mode Off, Sleep Out										Yes	
	Partial Mode On, Idle Mode On, Sleep Out										Yes	
	Sleep In										Yes	
Default	**Status**										**Default Value**	
	Power On Sequence										8'h00	
	S/W Reset										8'h00	
	H/W Reset										8'h00	

44H	TESCL (Tear Scan Line)
Flow Chart	



5.1.32 READ SCAN LINE (45H)

45H	RDSCL (Read Scan Line)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	0	0	1	0	1	45
1st Parameter	1	↑	1	N15	N14	N13	N12	N11	N10	N9	N8	00..FF
2nd Parameter	1	↑	1	N7	N6	N5	N4	N3	N2	N1	N0	00..FF

Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined. See video mode specification, See section “3.2 Display Module Data color Coding” for color coding.	
Restriction	There is no restriction for number of parameters. No access in the frame memory in Sleep In mode.	
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	**Status**	**Default Value**
	Power On Sequence	Refer to corresponding command parameter
	S/W Reset	Refer to corresponding command parameter
	H/W Reset	Refer to corresponding command parameter
Flow Chart		

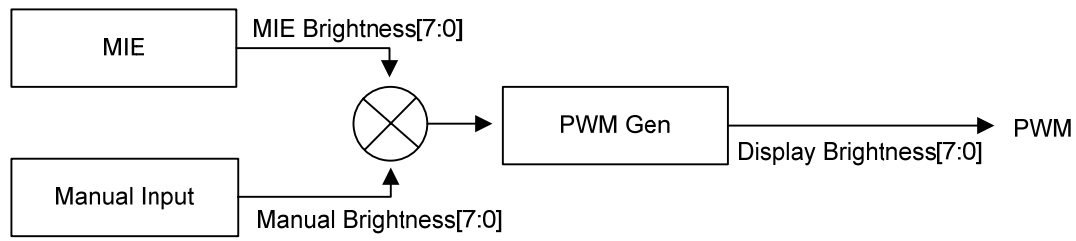
5.1.33 WRITE MANUAL BRIGHTNESS (51H)

51H	WRDISBV (Write Manual Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	0	1	51
Parameter	1	1	↑	MAN_ BR[7]	MAN_ BR[6]	MAN_ BR[5]	MAN_ BR[4]	MAN_ BR[3]	MAN_ BR[2]	MAN_ BR[1]	MAN_ BR[0]	00

Description

This command is used to set the manual brightness value. If the manual brightness is used (BC_MODE = “01” or “11”), the value of register “MAN_BR [7:0] is selected or merged with the MIE brightness to generate PWM.

MAN_BR [7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
…	…
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

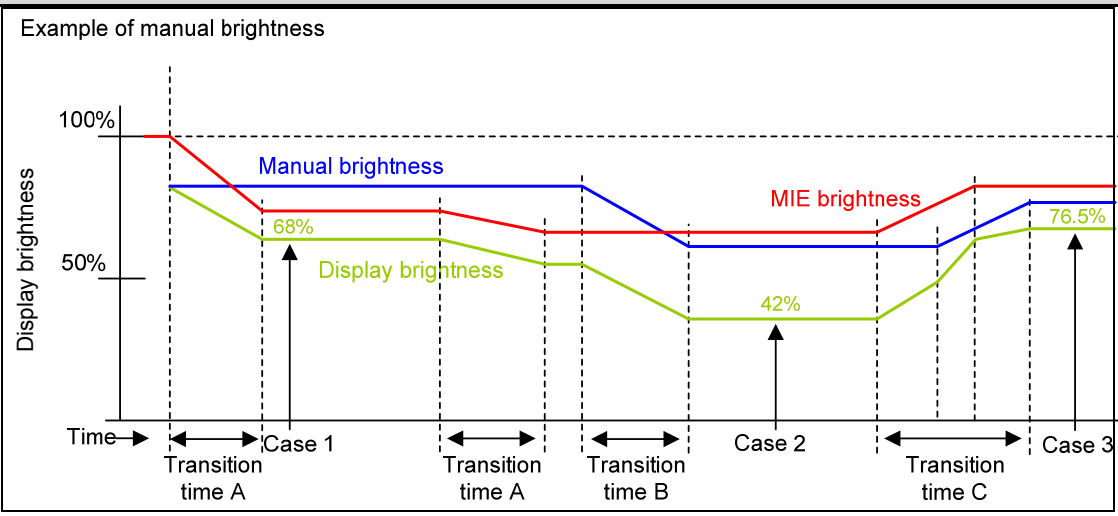


The display brightness level is calculated with the following formula.

$$\text{Display Brightness} = \text{MIE Brightness} \times \frac{\text{Manual Brightness}}{255}$$

The MIE brightness has transition time A and the manual brightness has transition time B. The maximum transition time is transition time C (C ≤ A + B).

51H	WRDISBV (Write Manual Brightness)



Operation Mode	Manual Brightness	MIE Brightness	Display Brightness
Case 1	85 %	80 %	68 %
Case 2	60 %	70 %	42 %
Case 3	85 %	90 %	76.5 %

Restriction		
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes
Default	**Status**	**Default Value**
	Power On Sequence	00
	S/W Reset	00
	H/W Reset	00

5.1.34 READ DISPLAY BRIGHTNESS (52H)

52H	RDDISBV (Read Display Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	1	0	52
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	
2nd Parameter	1	↑	1	DISP_BR7	DISP_BR6	DISP_BR5	DISP_BR4	DISP_BR3	DISP_BR2	DISP_BR1	DISP_BR0	00

Description	This command is used to read the display brightness value. It is a real brightness value of PWM output which is calculated with MIE brightness and manual brightness. The value of this register is updated after display V-sync and host can read exact value after display V-sync.	
	DISP_BR [7:0]	**Brightness Level**
	0000_0000	0
	0000_0001	1
	0000_0010	2
	0000_0011	3
	…	…
	1111_1100	252
	1111_1101	253
	1111_1110	254
	1111_1111	255
Restriction		
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes
Default	**Status**	**Default Value**
	Power On Sequence	00
	S/W Reset	00
	H/W Reset	00

5.1.35 WRITE BL CONTROL (53H)

53H	WRCTRLD (Write BL Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	1	1	53
Parameter	1	1	↑	0	0	BCTRL	0	DD	BL	0	0	00

Description

– BCTRL

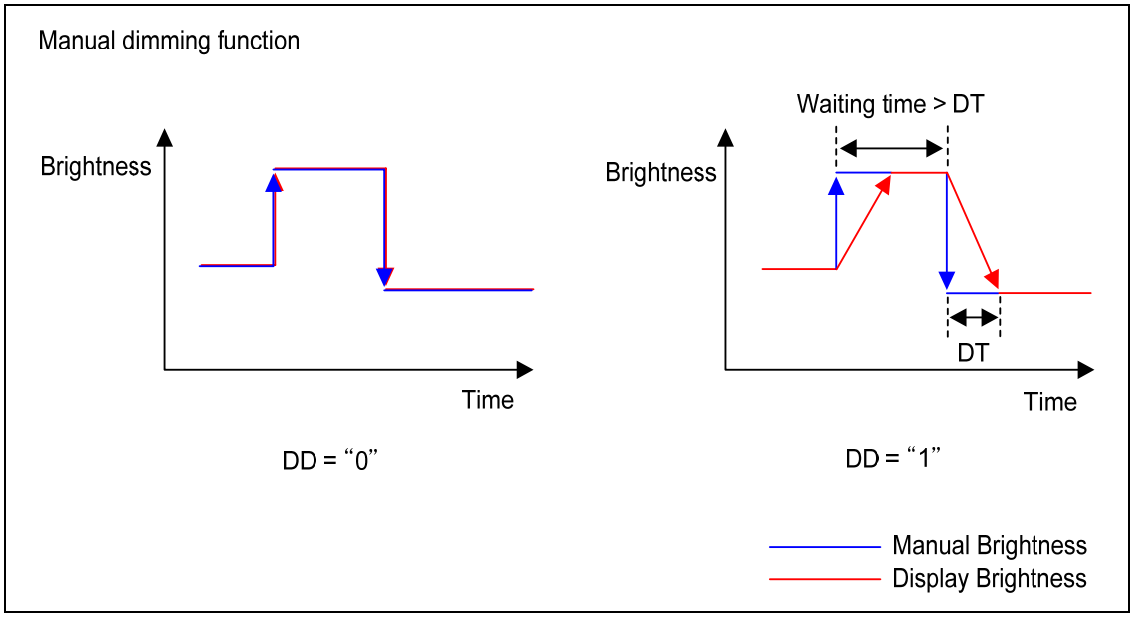
This register is used to enable the backlight control block. If BCTRL is turned off, the BL control block is not working and PWM output is fixed to low.

BRCTRL	BL Control
0	Off
1	On

– DD

This register is used to enable the manual brightness dimming function. The manual brightness should be changed smoothly for preventing a visible artifact, e.g. flicker. So the dimming function is needed when the transition of input manual brightness is fast to make a visible artifact. When the manual dimming is enabled, the new manual brightness value has to be changed after former dimming transition is finished. The transition time is controlled by DT[2:0].

DD	Manual Dimming Function
0	Off
1	On



<table>
<tr><th>53H</th><th colspan="2">WRCTRLD (Write BL Control)</th></tr>
<tr><td rowspan="4"></td><td colspan="2">– BL
This register is used to enable the PWM output. Even if the value of BL is “0”, the backlight control block is working when BCTRL is “1”. And the host can read the display brightness value(DISP_BRIGHT[7:0]) and control the BLU directly.</td></tr>
<tr><td>BL</td><td>PWM state</td></tr>
<tr><td>0</td><td>Low</td></tr>
<tr><td>1</td><td>Active</td></tr>
<tr><td>Restriction</td><td colspan="2"></td></tr>
<tr><td rowspan="6">Register Availability</td><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Step up circuit Off</td><td>Yes</td></tr>
<tr><td rowspan="4">Default</td><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>00</td></tr>
<tr><td>S/W Reset</td><td>00</td></tr>
<tr><td>H/W Reset</td><td>00</td></tr>
</table>

5.1.36 READ BL CONTROL (54H)

54H	RDCTRLD (Read BL Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	0	0	54
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	x	x	BCTRL	x	DD	BL	x	x	00
Description	This command is used to read BL control register. For details, refer to Write BL Control (53h).											
Restriction												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

Default	Status	Default Value
	Power On Sequence	00
	S/W Reset	00
	H/W Reset	00

5.1.37 WRITE MIE MODE (55H)

55H	WRCABC (Write MIE Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	0	1	55
Parameter	1	1	↑	0	0	0	0	0	0	MIE_ MODE[1]	MIE_ MODE[0]	00
Description	This command is used to select the operation mode of MIE. In UI or Still-image mode, the host should send same image at least two times to apply MIE algorithm exactly. If the MIE is off mode, the BLU brightness value of MIE is set to 255.											
	MIE_MODE[1:0]						**Operation Mode**					
	00						Off					
	01						UI (User Interface)					
	10						Still Image					
	11						Moving Image					
Restriction												
Register Availability	**Status**						**Availability**					
	Normal Mode On, Idle Mode Off, Sleep Out						Yes					
	Normal Mode On, Idle Mode On, Sleep Out						Yes					
	Partial Mode On, Idle Mode Off, Sleep Out						Yes					
	Partial Mode On, Idle Mode On, Sleep Out						Yes					
	Sleep In or Step up circuit Off						Yes					
Default	**Status**						**Default Value**					
	Power On Sequence						00					
	S/W Reset						00					
	H/W Reset						00					

5.1.38 READ MIE MODE (56H)

56H	RDCABC (Read MIE Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	1	0	56
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	0	0	0	0	0	0	MIE_ MODE[1]	MIE_ MODE[0]	xx
Description	This command is used to read MIE mode register. For details, refer to Write MIE Mode (55h).											
Restriction												

Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

Default	**Status**	**Default Value**
	Power On Sequence	00
	S/W Reset	00
	H/W Reset	00

5.1.39 WRITE MINIMUM BRIGHTNESS (5EH)

5EH	WRCABCMB (Write Minimum Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	1	1	1	0	5E
Parameter	1	1	↑	MIN_ BRIG HT[7]	MIN_ BRIG HT[6]	MIN_ BRIG HT[5]	MIN_ BRIG HT[4]	MIN_ BRIG HT[3]	MIN_ BRIG HT[2]	MIN_ BRIG HT[1]	MIN_ BRIG HT[0]	xx

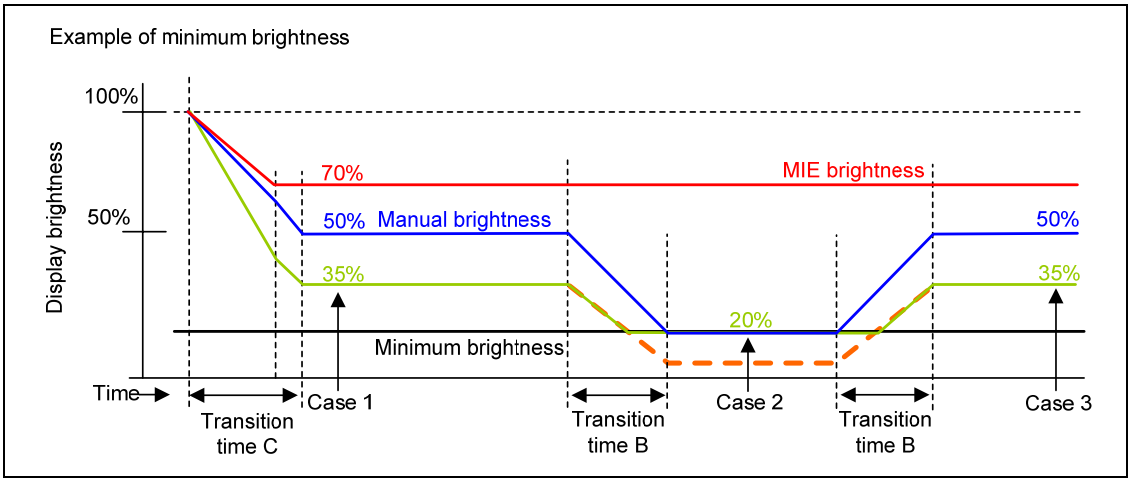
Description

This command is used to set the minimum brightness value.

The MIE function is automatically reduced the backlight brightness based on the content of image. In the case of the combination with the manual brightness setting, the display brightness can be too dark. It must affect to image quality degradation. So the minimum brightness setting is used to avoid too much brightness reduction.

When the MIE is activated, the display brightness can not be reduced less than the value of minimum brightness setting. The image processing function is worked as normal, even if the display brightness can not be decreased by the minimum brightness setting.

This function of the manual brightness setting does not affect to the other functions. The smooth transition and dimming function can be worked as normal. The manual brightness shouldn't be set less than the minimum brightness. When the BL control block is turned off (BCTRL=0), the MIE minimum brightness setting is ignored.



Operation Mode	Manual Brightness	MIE Brightness	Calculated Display Brightness	Display Brightness
Case 1	50 %	70 %	35%	35 %
Case 2	20 %	70 %	14%	20 %
Case 3	50 %	70 %	35%	35 %

MIN_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
MIN_BRIGHT[7:0]	**Brightness Level**

5EH	WRCABCMB (Write Minimum Brightness)	
	0000_0010	2
	0000_0011	3
	…	…
	1111_1100	252
	1111_1101	253
	1111_1110	254
	1111_1111	255
	Status	**Default Value**
	Initial	MIN_BRIGHT[7:0] = 0000_0000
Restriction		
Register Availability	**Status**	**Availability**
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes
Default	**Status**	**Default Value**
	Power On Sequence	00
	S/W Reset	00
	H/W Reset	00
Flow Chart		

5.1.40 READ MINIMUM BRIGHTNESS (5FH)

5FH	RDCABCMB (Read Minimum Brightness)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	1	1	1	1	5F
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	MIN_ BRIG HT[7]	MIN_ BRIG HT 6]	MIN_ BRIG HT[5]	MIN_ BRIG HT[4]	MIN_ BRIG HT[3]	MIN_ BRIG HT[2]	MIN_ BRIG HT[1]	MIN_ BRIG HT[0]	xx
Description	This command is used to read Minimum Brightness register. For details, refer to Write Minimum Brightness (5Eh).											
Restriction												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

Default	Status	Default Value
	Power On Sequence	00
	S/W Reset	00
	H/W Reset	00

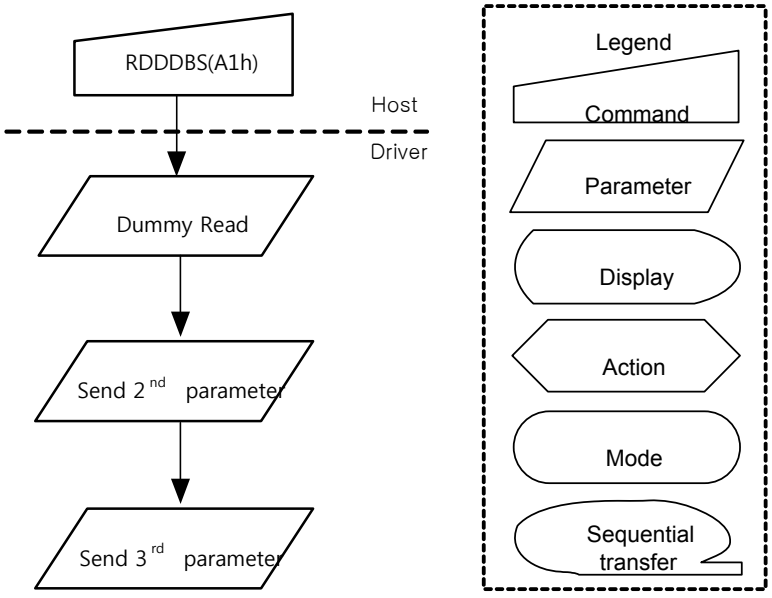
5.1.41 READ DDB START (A1H)

A1H	RDDDBS (Read DDB Start)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	0	0	0	1	A1
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	F0
3rd Parameter	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	F0
Description	This command returns supplier identification and display module model/revision information. This read sequence can be interrupted by any command and it can be continued by “5.1.45 Read DDB Continue (A8h)” command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd Parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.											
Restriction												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	F0
	S/W Reset	F0
	H/W Reset	F0

Flow Chart



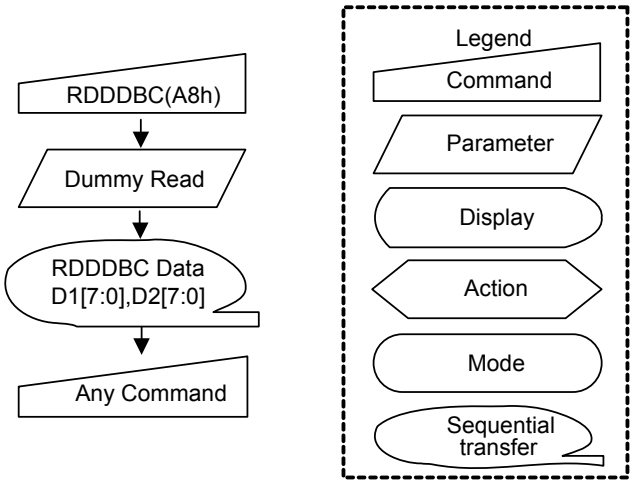
5.1.42 READ DDB CONTINUE (A8H)

A8H	RDDDBC (Read DDB Continue)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	1	0	0	0	A8
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	F0
3rd Parameter	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	F0
Description	This command returns supplier's identification and display module model/revision information from the point where RDDDBS command was interrupt by another command e.g. RDDDBS was interrupted after 2nd parameter. The first parameter, what RDDDBC is returning, is 3rd parameter.											
Restriction	There is no restriction for number of parameters. No access in the frame memory in Sleep In mode											

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	F0
	S/W Reset	F0
	H/W Reset	F0

Flow Chart



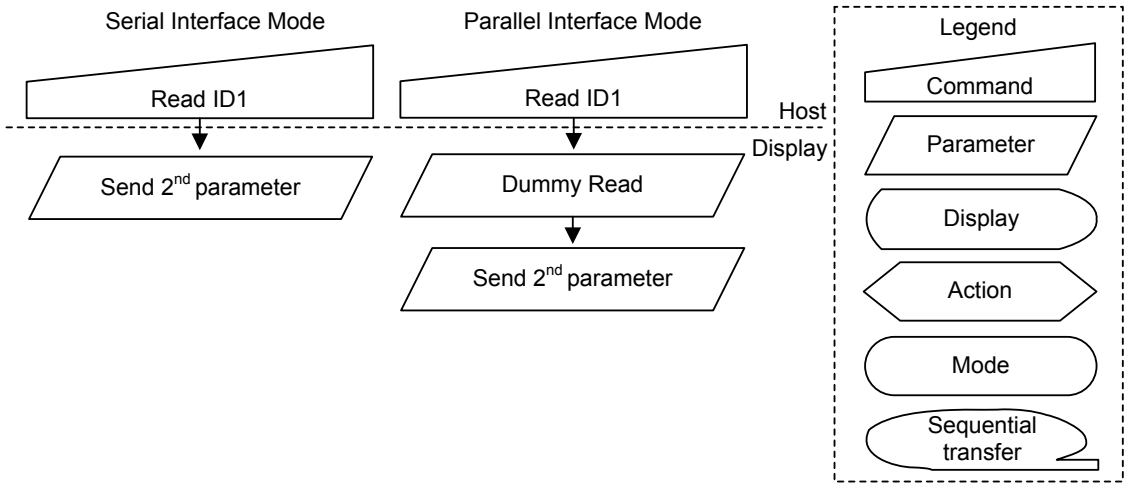
5.1.43 READ ID1 (DAH)

DAH	RDID1 (Read ID1)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	0	DA
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	xx
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module's manufacturer.											
Restriction												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

Default	Status	Default Value
	Power On Sequence	MTP
	S/W Reset	MTP
	H/W Reset	MTP

Flow Chart



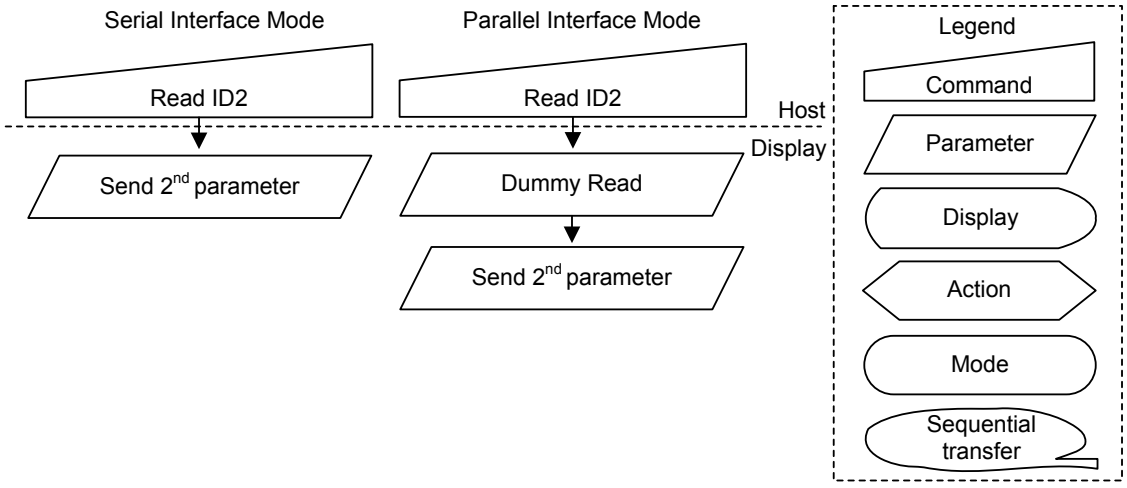
5.1.44 READ ID2 (DBH)

DBH	RDID2 (Read ID2)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	1	DB
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	xx
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module / driver version ID.											
Restriction												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

Default	Status	Default Value
	Power On Sequence	MTP
	S/W Reset	MTP
	H/W Reset	MTP

Flow Chart



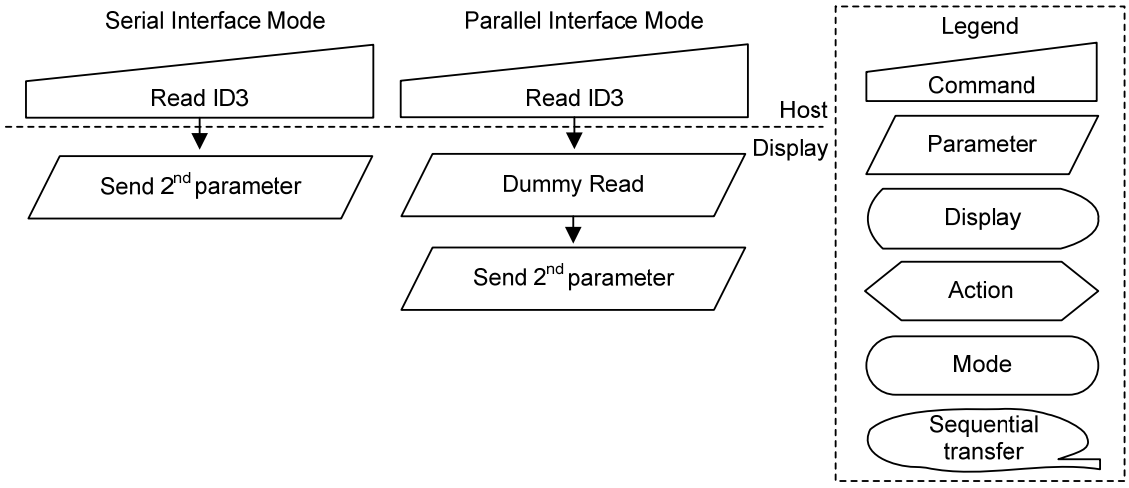
5.1.45 READ ID3 (DCH)

DCH	RDID3 (Read ID3)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	0	0	DC
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	xx
2nd Parameter	1	↑	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	xx
Description	The 1st Parameter is dummy data. This read byte identifies the LCD module/driver.											
Restriction												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Step up circuit Off	Yes

Default	Status	Default Value
	Power On Sequence	MTP
	S/W Reset	MTP
	H/W Reset	MTP

Flow Chart



5.2 DESCRIPTION OF LEVEL 2 COMMAND

Table 96 List of level 2 Command

Operational Code (HEX)	Function	Read/Write / Command	Number of Parameter	CPU	SPI	MDDI	MIPI DSI	
				(80/68)	(3/4-wire)		DCS	Gerneric
C0	MIECTL	W	3	O	O	O	O	O
C1	BCMODE	W	1	O	O	O	O	O
C2	WRMIECTL	W	9	O	O	O	O	O
C3	WRBLCTL	W	3	O	O	O	O	O
D0	MTPCTL	W	1	O	O	O	O	O
D2	MTPWR	W	6	O	O	O	O	O
D3	MTPRD	R	6	O	X	O	X	O
DF	DSTB	W	1	O	O	O	O	O
EA	MDDICTL	W	1	O	O	O	O	O
EB	MDDILIK	W	2	O	O	O	O	O
F0	PASSWD1	W	2	O	O	O	O	O
F1	PASSWD2	W	2	O	O	O	O	O
F2	DISCTL	W	19	O	O	O	O	O
F3	MANPWRSEQ	W	5	O	O	O	O	O
F4	PWRCTL	W	14	O	O	O	O	O
F5	VCMCTL	W	12	O	O	O	O	O
F6	SRCCTL	W	9	O	O	O	O	O
F7	IFCTL	W	5	O	O	O	O	O
F8	PANELCTL	W	2	O	O	O	O	O
F9	GAMMASEL	W	1	O	O	O	O	O
FA	PGAMMACTL	W	16	O	O	O	O	O
FB	NGAMMACTL	W	16	O	O	O	O	O

NOTE:
1. The number of parameter is the number of real parameter except dummy parameter.
2. Following registers are synchronized with frame sync. : *INV, REV, D, GATE_ON, VBP, VFP, SELF_REF
3. B0h to BFh and C4 to C9 and D4h to D9h are for factory (= IC supplier) use.

5.2.1 MIECTL1 (C0H)

C0h	MIECTL1 (MIE Control1)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	0	0	C0
1st Parameter	1	1	↑	RRC [7]	RRC [6]	RRC [5]	RRC [4]	RRC [3]	RRC [2]	RRC [1]	RRC [0]	80
2nd Parameter	1	1	↑	IERC [7]	IERC [6]	IERC [5]	IERC [4]	IERC [3]	IERC [2]	IERC [1]	IERC [0]	80
3rd Parameter	1	1	↑	0	0	ONOFF DIMMEN	SER C[4]	SER C[3]	SER C[2]	SER C[1]	SER C[0]	10

5.2.1.1 RRC [7:0]

Reduction Rate Control of Backlight Power. Default Value is RRC[7:0]=10000000.

Expression of Power Reduction Rate

$$Power\_Reduction\_Rate = Contents\_Based\_Reduction\_Rate \times \frac{RRC}{128}$$

Contents_Based_Reduction_Rate is the power reduction rate. Reduction range is from '0' (no reduction) to two times of contents adaptive backlight power.

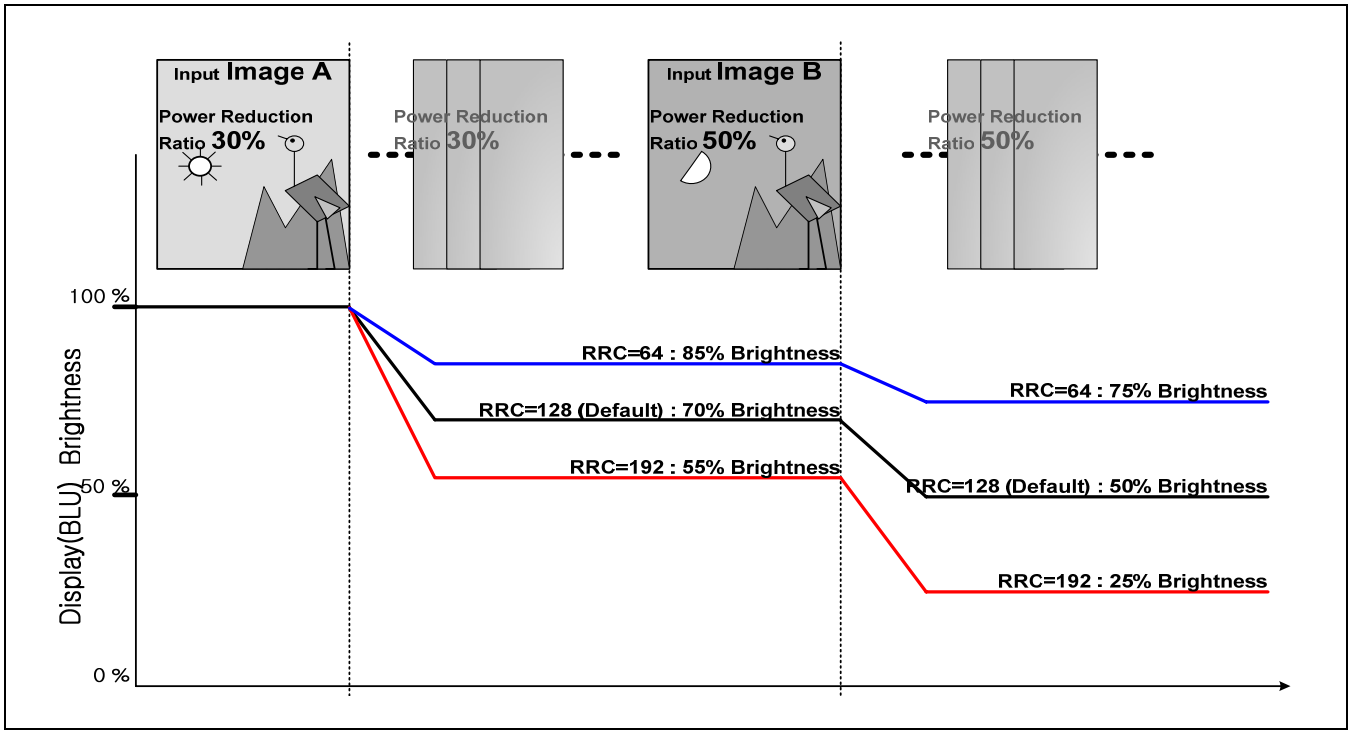


Figure 178 According to RRC Value, Brightness Variation

Table 97 RRC [7:0]

RRC[7:0]	Adjusted Power Reduction Rate
0000_0000	Power Reduction Rate x 0/128
0000_0001	Power Reduction Rate x 1/128
0000_0010	Power Reduction Rate x 2/128
…	…
1000_0000	Power Reduction Rate x 128/128
…	…
1111_1101	Power Reduction Rate x 253/128
1111_1110	Power Reduction Rate x 254/128
1111_1111	Power Reduction Rate x 255/128

Status	Default Value
Initial	RRC[7:0] = 1000_0000

5.2.1.2 IERC [7:0]

Image Enhancement Rate Control. If IERC is '0', there is no enhancement of input image. If its value is '255', enhancement rate is two times of Image_Enhancement_Rate. Default value is RRC[7:0]=10000000.

Expression of Adjusted Image Enhancement Rate

$$\text{Adjusted\_Image\_Enhancement\_Rate} = \text{Image\_enhancement\_Rate} \times \frac{\text{IERC}}{128}$$

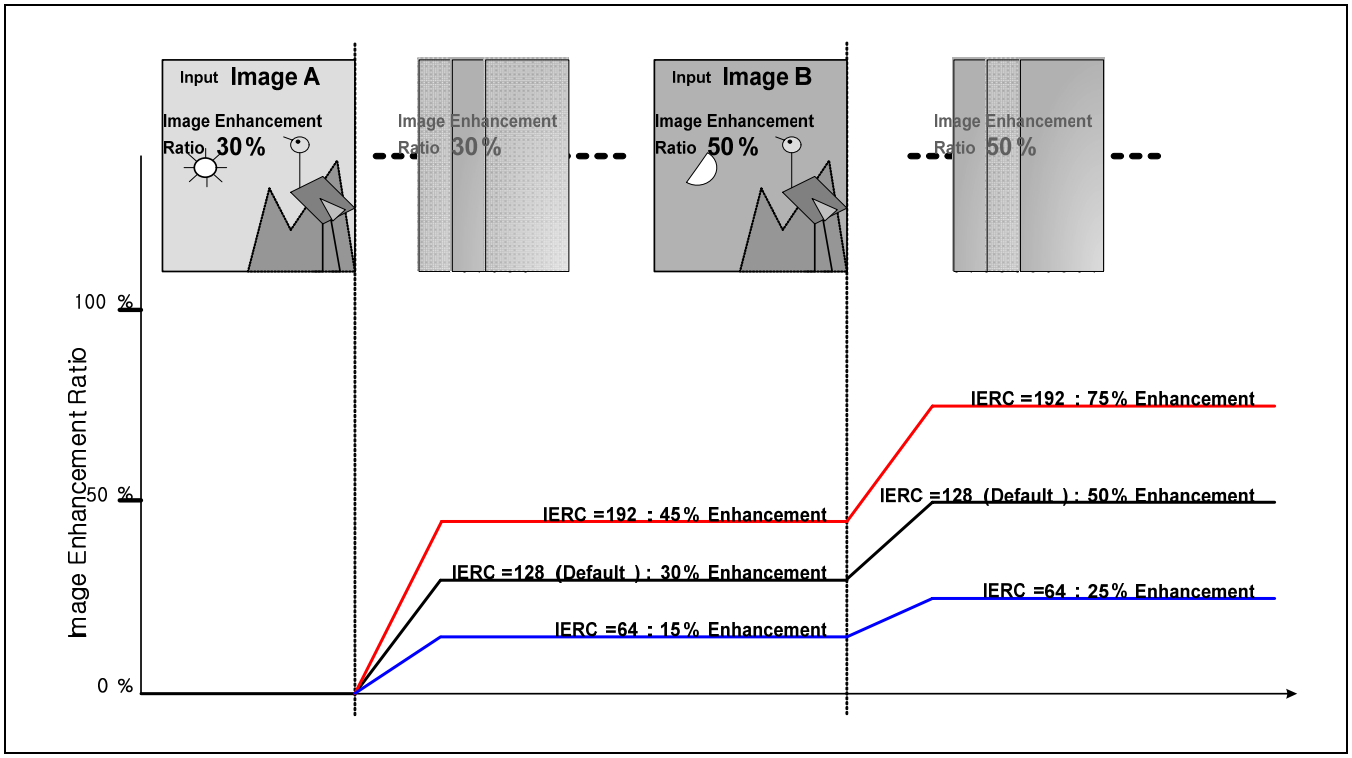


Figure 179 According to IERC Value, Image Enhancement Ratio Variation

Table 98 IERC[7:0]

IERC[7:0]	Adjust Image Enhancement Rate
0000_0000	Image Enhancement Rate x 0/128
0000_0001	Image Enhancement Rate x 1/128
0000_0010	Image Enhancement Rate x 2/128
…	…
1000_0000	Image Enhancement Rate x 128/128
…	…

1111_1101	Image Enhancement Rate x 253/128
1111_1110	Image Enhancement Rate x 254/128
1111_1111	Image Enhancement Rate x 255/128

Status	Default Value
Initial	IERC[7:0] = 1000_0000

5.2.1.3 ONOFF_DIMM_EN

This register is used to enable the on/off dimming function of MIE.

The MIE has a dimming function for preventing abnormal visible artifacts when the MIE is turning on or off.
If the ONOFF_DIMM_EN is “1”, the MIE is smoothly turning on or off. When the ONOFF_DIMM_EN is “0”, the MIE is turning on or off immediately. The transition time is controlled by CST[1:0].
If this dimming function is enabled in UI or STILL mode, the host must write frames more than the transition time of CST[1:0] to finish the dimming transition. If the MIE mode is changed during on/off dimming transition, it will be updated after finishing the dimming transition.

Table 99 ONOFF_DIMM_EN

ONOFF_DIMM_EN	On / Off Dimming Function
0	Disable
1	Enable

Status	Default Value
Initial	ONOFF_DIMM_EN = 0

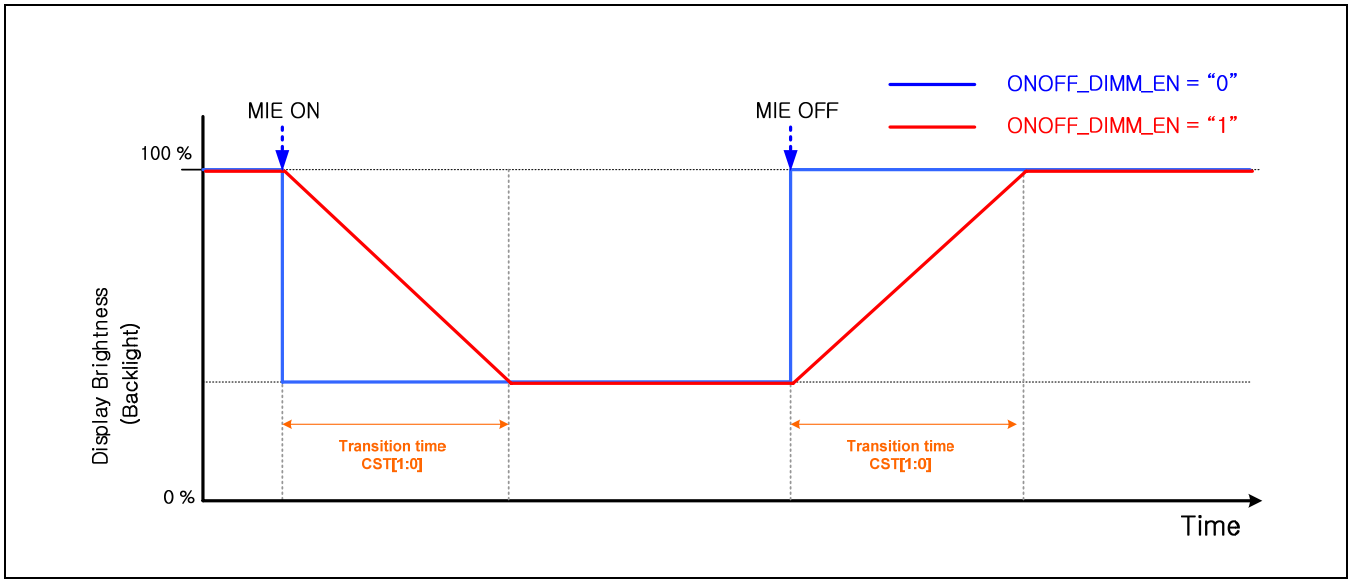


Figure 180 Example of MIE On / Off Dimming Transition Control

5.2.1.4 SERC [4:0]

This register is used to adjust the Image Saturation Enhancement Rate.

Saturation Enhancement Rate

$$\text{Adjusted\_Saturation\_Enhancement\_Rate} = \text{Saturation\_Enhancement\_Rate} \times \frac{\text{SERC}}{16}$$

If the value of SERC is '0', there is no saturation enhancement in output image. If the value of SERC is increased, the saturation enhancement rate will be increased and more vivid image is obtained. The other way, if the value of SERC is decreased, the saturation enhancement rate will be decreased.

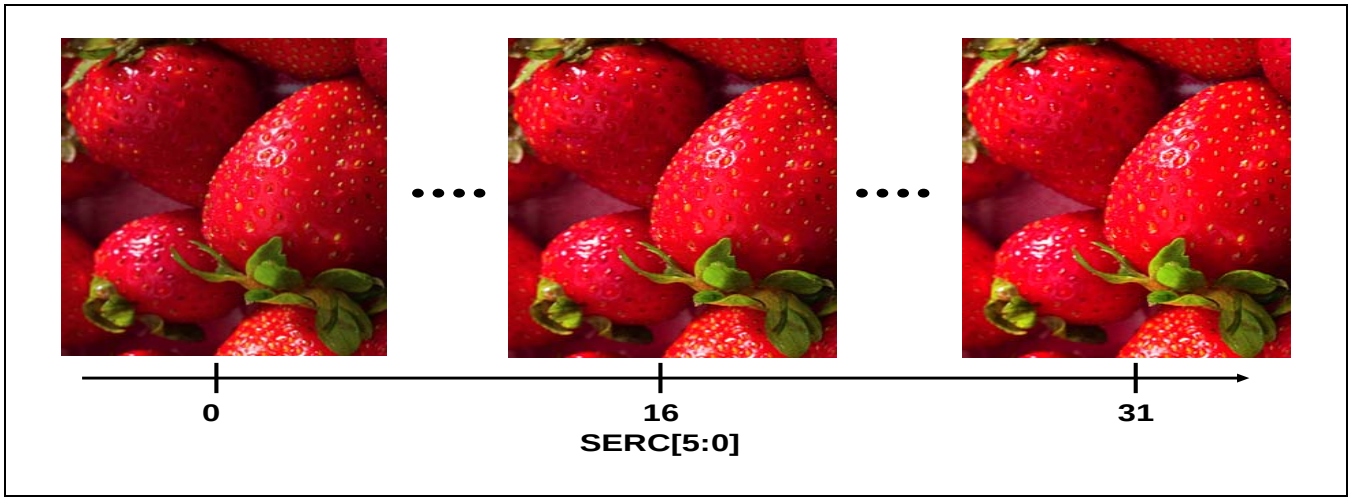


Figure 181 Example of SERC

Table 100 SERC [4:0]

SERC[4:0]	Adjust Saturation Enhancement Rate
00000	Saturation Enhancement Rate x 0/16
00001	Saturation Enhancement Rate x 1/16
00010	Saturation Enhancement Rate x 2/16
…	…
10000	Saturation Enhancement Rate x 16/16
…	…
11101	Saturation Enhancement Rate x 29/16
11110	Saturation Enhancement Rate x 30/16
11111	Saturation Enhancement Rate x 31/16

Status	Default Value
Initial	SERC[4:0] = 10000

5.2.2 BCMODE (C1H)

C1h	BCMODE											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	0	1	C1
Parameter	1	1	↑	0	0	0	PWM_CLK_SEL	0	0	BC_MODE[1]	BC_MODE[0]	13

This command is used to select the source of brightness value for the display brightness calculation

5.2.2.1 PWM_CLK_SEL

This register is used to select the clock source of PWM Block.

Table 101 PWM_CLK_SEL

PWM_CLK_SEL	PWM Clock Source @RGB Mode
0	External DOT Clock
1	Internal OSC Clock

Status	Default Value
Initial	PWM_CLK_SEL = 1

Table 102 BC_MODE[1:0]

BC_MODE[1:0]	Brightness Source
00	Setting disabled
01	Manual Brightness
10	MIE Brightness
11	Merged Brightness (MIE + Manual)

Status	Default Value
Initial	BC_MODE[1:0] = 11

5.2.3 WRMIECTL2 (C2H)

C2h	Write MIE Control 2											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	0	C2
1st Parameter	1	1	↑	0	0	0	0	CAT [1]	CAT [0]	CST [1]	CST [0]	08
2nd Parameter	1	1	↑	0	0	0	0	0	0	0	WIN VAD DR0 [8]	00
3rd Parameter	1	1	↑	WIN VAD DR0 [7]	WIN VAD DR0 [6]	WIN VAD DR0 [5]	WIN VAD DR0 [4]	WIN VAD DR0 [3]	WIN VAD DR0 [2]	WIN VAD DR0 [1]	WIN VAD DR0 [0]	00
4th Parameter	1	1	↑	0	0	0	0	0	0	0	WIN VAD DR1 [8]	01
5th Parameter	1	1	↑	WIN VAD DR1 [7]	WIN VAD DR1 [6]	WIN VAD DR1 [5]	WIN VAD DR1 [4]	WIN VAD DR1 [3]	WIN VAD DR1 [2]	WIN VAD DR1 [1]	WIN VAD DR1 [0]	DF
6th Parameter	1	1	↑	0	0	0	0	0	0	0	WIN HAD DR0 [8]	00
7th Parameter	1	1	↑	WIN HAD DR0 [7]	WIN HAD DR0 [6]	WIN HAD DR0 [5]	WIN HAD DR0 [4]	WIN HAD DR0 [3]	WIN HAD DR0 [2]	WIN HAD DR0 [1]	WIN HAD DR0 [0]	00
8th Parameter	1	1	↑	0	0	0	0	0	0	0	WIN HAD DR1 [8]	01
9th Parameter	1	1	↑	WIN HAD DR1 [7]	WIN HAD DR1 [6]	WIN HAD DR1 [5]	WIN HAD DR1 [4]	WIN HAD DR1 [3]	WIN HAD DR1 [2]	WIN HAD DR1 [1]	WIN HAD DR1 [0]	67

5.2.3.1 CAT [1:0]

This register is used to select the abrupt transition time. The MIE has two transition times based on image contents for preventing abnormal visible artifacts (e.g. flicker). The MIE controls transition time between CAT and CST automatically in moving mode (MIE_MODE = “11”).

- Abrupt transition time : If input image is changed abruptly, short transition time is needed.
- Smooth transition time : If input image is changed smoothly, long transition time is needed.

Table 103 CAT [1:0]

CAT[1:0]	Abrupt Transition Time
00	1 frame
01	2 frames
10	4 frames
11	8 frames

Status	Default Value
Initial	CAT[1:0] = 10

5.2.3.2 CST [1:0]

This register is used to select the smooth transition time

Table 104 CST [1:0]

CST[1:0]	Smooth Transition Time
00	32 frames
01	64 frames
10	128 frames
11	256 frames

Status	Default Value
Initial	CST[1:0] = 00

An example of MIE transition time is illustrated as below. If the input image is changed abruptly, the MIE has an abrupt transition time “case (1)” and if the input image is changed smoothly, the MIE has a smooth transition time “case (2)”. The display brightness changes to target brightness abruptly “case (4)” when the abrupt change of image is happened during the smooth transition “case (3)”.

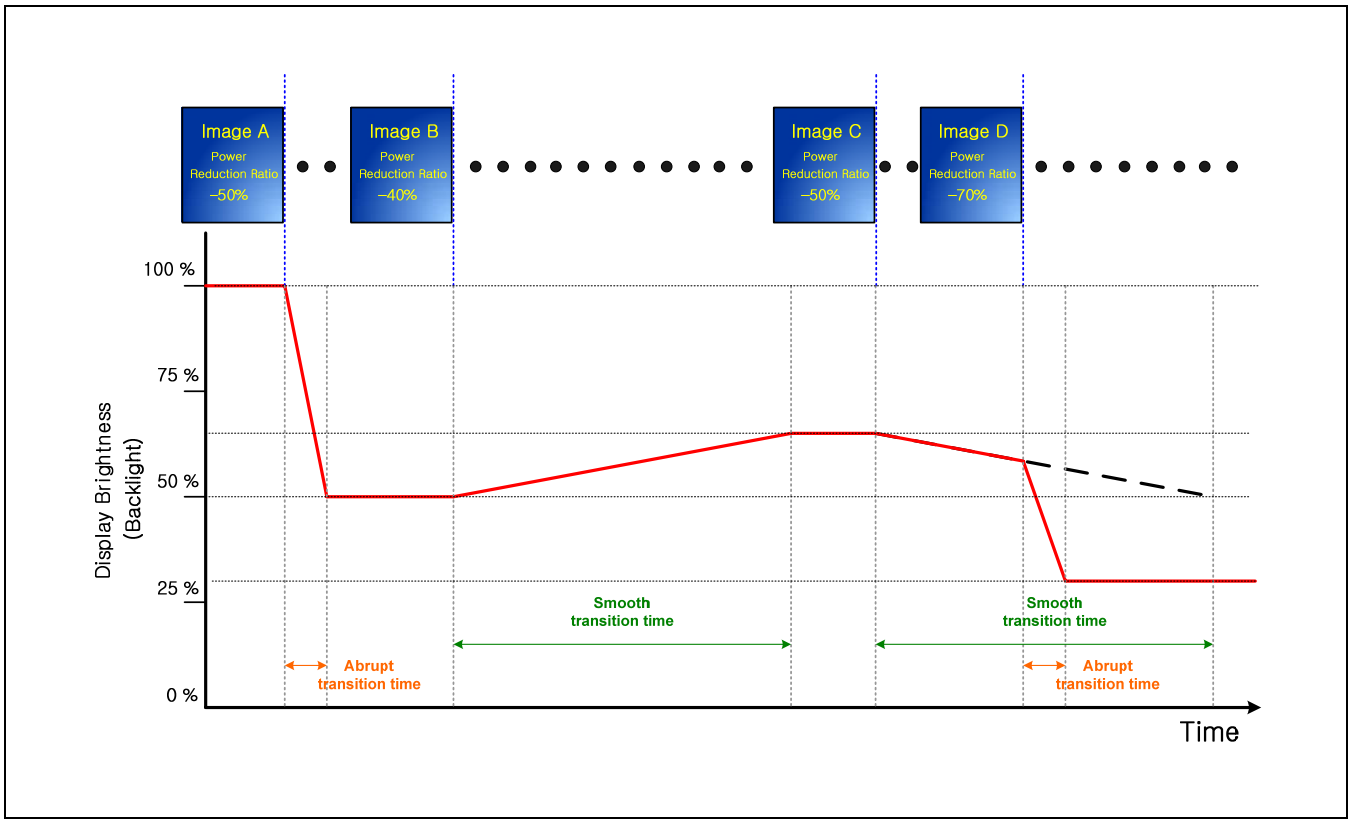


Figure 182 Example of MIE Transition Control

5.2.3.3 WINVADDR0 [8:0]

This register is used to set the vertical start address of MIE window.

Table 105 WINVADDR0 [8:0]

WINVADDR0[8:0]	Vertical Start Address of MIE Window
00_0000_0000	0
00_0000_0001	1
00_0000_0010	2
00_0000_0011	3
…	…
1_1101_1110	478
1_1101_1111	479
1_1110_0000	Setting disabled
…	…
1_1111_1111	Setting disabled

Status	Default Value
Initial	WINVADDR0[8:0] = 0_0000_0000

5.2.3.4 WINVADDR1 [8:0]

This register is used to set the vertical end address of MIE window.

Table 106 WINVADDR1 [8:0]

WINVADDR1[8:0]	Vertical End Address of MIE Window
00_0000_0000	0
00_0000_0001	1
00_0000_0010	2
00_0000_0011	3
…	…
1_1101_1110	478
1_1101_1111	479
1_1110_0000	Setting disabled
…	…
1_1111_1111	Setting disabled

Status	Default Value
Initial	WINVADDR1[8:0] = 1_1101_1111

NOTE: WINVADDR1 – WINVADDR0 ≥ 8

5.2.3.5 WINHADDR0 [8:0]

This register is used to set the horizontal start address of MIE window.

Table 107 WINHADDR0 [8:0]

WINHADDR0[8:0]	Horizontal Start Address of MIE Window
0_0000_0000	0
0_0000_0001	1
0_0000_0010	2
0_0000_0011	3
…	…
1_0110_0110	358
1_0110_0111	359
1_0110_1000	Setting disabled
…	…
1_1111_1111	Setting disabled

Status	Default Value
Initial	WINHADDR0[8:0] = 0_0000_0000

5.2.3.6 WINHADDR1 [8:0]

This register is used to set the horizontal end address of MIE window.

Table 108 WINHADDR1 [8:0]

WINHADDR1[8:0]	Horizontal End Address of MIE Window
0_0000_0000	0
0_0000_0001	1
0_0000_0010	2
0_0000_0011	3
…	…
1_0110_0110	358
1_0110_0111	359
1_0110_1000	Setting disabled

…	…
1_1111_1111	Setting disabled

Status	Default Value
Initial	WINHADDR1[8:0] = 1_0110_0111

NOTE: WINHADDR1 – WINHADDR0 ≥ 100

The MIE can select the window area which is used to analysis and enhance input image. The outside area of the MIE window is not used to MIE analysis and there is no image enhancement.

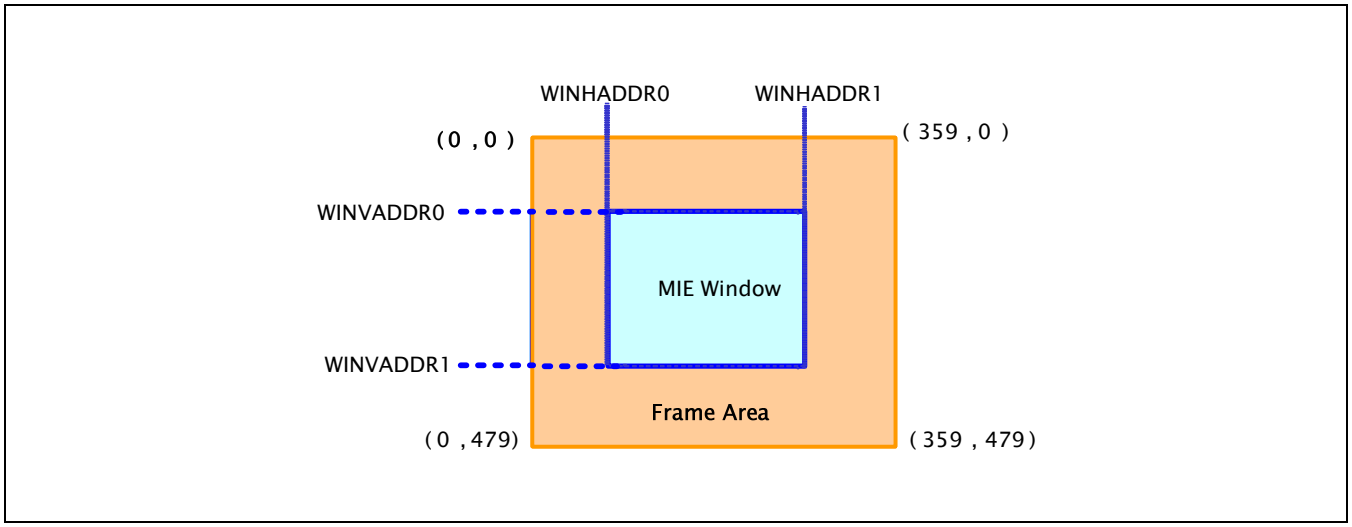


Figure 183 MIE Window

5.2.4 WRBLCTL (C3H)

C3h	WRBLCTL											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	1	C3
1st Parameter	1	1	↑	0	0	0	0	0	0	0	BCFRQSEL [8]	00
2nd Parameter	1	1	↑	BCFRQSEL [7]	BCFRQSEL [6]	BCFRQSEL [5]	BCFRQEL [4]	BCFRQSEL [3]	BCFRQSEL [2]	BCFRQSEL [1]	BCFRQSEL [0]	03
3rd Parameter	1	1	↑	BL_MODE_IN_SLP	DT [2]	DT [1]	DT [0]	BL_DRV_EN	BL_DIMM_STEP [2]	BL_DIMM_STEP [1]	BL_DIMM_STEP [0]	14

5.2.4.1 BCFRQSEL [8:0]

This register is used to select the frequency of PWM. To select the PWM frequency, two registers are needed. Those register are BCFRQSEL [8:0] and BL_DIMM_STEP[2:0].

For details, refer to the table of PWM frequency.

Status	Default Value
Initial	BCFRQSEL[8:0] = 0_0000_0011

5.2.4.2 BL_DIMM_STEP [2:0]

This register is used to select the dimming step of PWM level. It is used to select the frequency of PWM with BCFRQSEL [8:0]

Table 109 BL_DIMM_STEP[2:0]

BL_DIMM_STEP[2:0]	Dimming Steps of PWM
000	1024
001	512
010	256
011	128
100	64
101	32
110	Disable

111	Disable

Status	Default Value
Initial	BL_DIMM_STEP[2:0] = 100

The PWM frequency is calculated with the following formula.

Calculation Formula of PWM Frequency

Num. of PWM / 1 frame = (BCFRQSEL + 1) × $2^{BL\_DIMM\_SETP}$

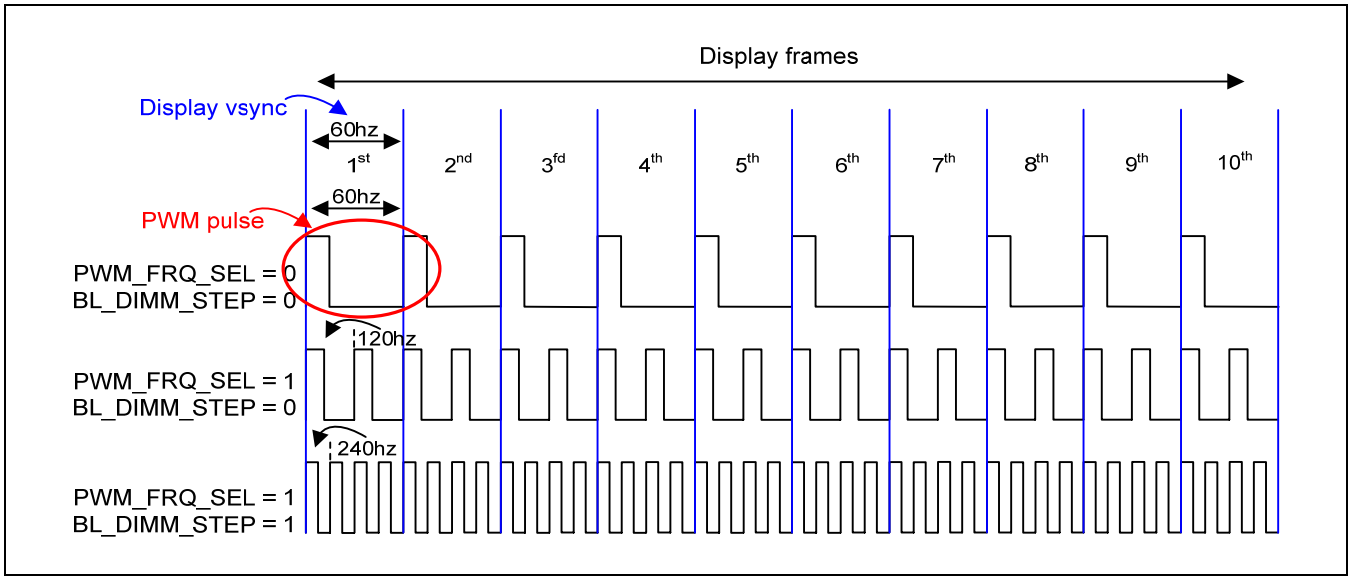


Figure 184 Example of PWM Frequency Selection

Table 110 PWM Frequency

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
000000000	F.F x 1	F.F x 2	F.F x 4	F.F x 8	F.F x 16	F.F x 32
000000001	F.F x 2	F.F x 4	F.F x 8	F.F x 16	F.F x 32	F.F x 64
000000010	F.F x 3	F.F x 6	F.F x 12	F.F x 24	F.F x 48	F.F x 96
000000011	F.F x 4	F.F x 8	F.F x 16	F.F x 32	F.F x 64	F.F x 128
000000100	F.F x 5	F.F x 10	F.F x 20	F.F x 40	F.F x 80	F.F x 160

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
000000101	F.F x 6	F.F x 12	F.F x 24	F.F x 48	F.F x 96	F.F x 192
000000110	F.F x 7	F.F x 14	F.F x 28	F.F x 56	F.F x 112	F.F x 224
000000111	F.F x 8	F.F x 16	F.F x 32	F.F x 64	F.F x 128	F.F x 256
000001000	F.F x 9	F.F x 18	F.F x 36	F.F x 72	F.F x 144	F.F x 288
000001001	F.F x 10	F.F x 20	F.F x 40	F.F x 80	F.F x 160	F.F x 320
000001010	F.F x 11	F.F x 22	F.F x 44	F.F x 88	F.F x 176	F.F x 352
000001011	F.F x 12	F.F x 24	F.F x 48	F.F x 96	F.F x 192	F.F x 384
000001100	F.F x 13	F.F x 26	F.F x 52	F.F x 104	F.F x 208	F.F x 416
000001101	F.F x 14	F.F x 28	F.F x 56	F.F x 112	F.F x 224	F.F x 448
000001110	F.F x 15	F.F x 30	F.F x 60	F.F x 120	F.F x 240	F.F x 480
000001111	F.F x 16	F.F x 32	F.F x 64	F.F x 128	F.F x 256	F.F x 512
000010000	F.F x 17	F.F x 34	F.F x 68	F.F x 136	F.F x 272	F.F x 544
000010001	F.F x 18	F.F x 36	F.F x 72	F.F x 144	F.F x 288	F.F x 576
000010010	F.F x 19	F.F x 38	F.F x 76	F.F x 152	F.F x 304	F.F x 608
000010011	F.F x 20	F.F x 40	F.F x 80	F.F x 160	F.F x 320	F.F x 640
000010100	F.F x 21	F.F x 42	F.F x 84	F.F x 168	F.F x 336	F.F x 672
000010101	F.F x 22	F.F x 44	F.F x 88	F.F x 176	F.F x 352	F.F x 704
000010110	F.F x 23	F.F x 46	F.F x 92	F.F x 184	F.F x 368	F.F x 736
000010111	F.F x 24	F.F x 48	F.F x 96	F.F x 192	F.F x 384	F.F x 768
000011000	F.F x 25	F.F x 50	F.F x 100	F.F x 200	F.F x 400	F.F x 800
000011001	F.F x 26	F.F x 52	F.F x 104	F.F x 208	F.F x 416	F.F x 832
000011010	F.F x 27	F.F x 54	F.F x 108	F.F x 216	F.F x 432	F.F x 864
000011011	F.F x 28	F.F x 56	F.F x 112	F.F x 224	F.F x 448	F.F x 896
000011100	F.F x 29	F.F x 58	F.F x 116	F.F x 232	F.F x 464	F.F x 928
000011101	F.F x 30	F.F x 60	F.F x 120	F.F x 240	F.F x 480	F.F x 960
000011110	F.F x 31	F.F x 62	F.F x 124	F.F x 248	F.F x 496	F.F x 992
000011111	F.F x 32	F.F x 64	F.F x 128	F.F x 256	F.F x 512	F.F x 1024
000100000	F.F x 33	F.F x 66	F.F x 132	F.F x 264	F.F x 528	F.F x 1056
000100001	F.F x 34	F.F x 68	F.F x 136	F.F x 272	F.F x 544	F.F x 1088
000100010	F.F x 35	F.F x 70	F.F x 140	F.F x 280	F.F x 560	F.F x 1120
000100011	F.F x 36	F.F x 72	F.F x 144	F.F x 288	F.F x 576	F.F x 1152
000100100	F.F x 37	F.F x 74	F.F x 148	F.F x 296	F.F x 592	F.F x 1184
000100101	F.F x 38	F.F x 76	F.F x 152	F.F x 304	F.F x 608	F.F x 1216

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
000100110	F.F x 39	F.F x 78	F.F x 156	F.F x 312	F.F x 624	F.F x 1248
000100111	F.F x 40	F.F x 80	F.F x 160	F.F x 320	F.F x 640	F.F x 1280
000101000	F.F x 41	F.F x 82	F.F x 164	F.F x 328	F.F x 656	F.F x 1312
000101001	F.F x 42	F.F x 84	F.F x 168	F.F x 336	F.F x 672	F.F x 1344
000101010	F.F x 43	F.F x 86	F.F x 172	F.F x 344	F.F x 688	F.F x 1376
000101011	F.F x 44	F.F x 88	F.F x 176	F.F x 352	F.F x 704	F.F x 1408
000101100	F.F x 45	F.F x 90	F.F x 180	F.F x 360	F.F x 720	F.F x 1440
000101101	F.F x 46	F.F x 92	F.F x 184	F.F x 368	F.F x 736	F.F x 1472
000101110	F.F x 47	F.F x 94	F.F x 188	F.F x 376	F.F x 752	F.F x 1504
000101111	F.F x 48	F.F x 96	F.F x 192	F.F x 384	F.F x 768	F.F x 1536
000110000	F.F x 49	F.F x 98	F.F x 196	F.F x 392	F.F x 784	F.F x 1568
000110001	F.F x 50	F.F x 100	F.F x 200	F.F x 400	F.F x 800	F.F x 1600
000110010	F.F x 51	F.F x 102	F.F x 204	F.F x 408	F.F x 816	F.F x 1632
000110011	F.F x 52	F.F x 104	F.F x 208	F.F x 416	F.F x 832	F.F x 1664
000110100	F.F x 53	F.F x 106	F.F x 212	F.F x 424	F.F x 848	F.F x 1696
000110101	F.F x 54	F.F x 108	F.F x 216	F.F x 432	F.F x 864	F.F x 1728
000110110	F.F x 55	F.F x 110	F.F x 220	F.F x 440	F.F x 880	F.F x 1760
000110111	F.F x 56	F.F x 112	F.F x 224	F.F x 448	F.F x 896	F.F x 1792
000111000	F.F x 57	F.F x 114	F.F x 228	F.F x 456	F.F x 912	F.F x 1824
000111001	F.F x 58	F.F x 116	F.F x 232	F.F x 464	F.F x 928	F.F x 1856
000111010	F.F x 59	F.F x 118	F.F x 236	F.F x 472	F.F x 944	F.F x 1888
000111011	F.F x 60	F.F x 120	F.F x 240	F.F x 480	F.F x 960	F.F x 1920
000111100	F.F x 61	F.F x 122	F.F x 244	F.F x 488	F.F x 976	F.F x 1952
000111101	F.F x 62	F.F x 124	F.F x 248	F.F x 496	F.F x 992	F.F x 1984
000111110	F.F x 63	F.F x 126	F.F x 252	F.F x 504	F.F x 1008	F.F x 2016
000111111	F.F x 64	F.F x 128	F.F x 256	F.F x 512	F.F x 1024	F.F x 2048
001000000	F.F x 65	F.F x 130	F.F x 260	F.F x 520	F.F x 1040	F.F x 2080
001000001	F.F x 66	F.F x 132	F.F x 264	F.F x 528	F.F x 1056	F.F x 2112
001000010	F.F x 67	F.F x 134	F.F x 268	F.F x 536	F.F x 1072	F.F x 2144
001000011	F.F x 68	F.F x 136	F.F x 272	F.F x 544	F.F x 1088	F.F x 2176
001000100	F.F x 69	F.F x 138	F.F x 276	F.F x 552	F.F x 1104	F.F x 2208
001000101	F.F x 70	F.F x 140	F.F x 280	F.F x 560	F.F x 1120	F.F x 2240
001000110	F.F x 71	F.F x 142	F.F x 284	F.F x 568	F.F x 1136	F.F x 2272

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
001000111	F.F x 72	F.F x 144	F.F x 288	F.F x 576	F.F x 1152	F.F x 2304
001001000	F.F x 73	F.F x 146	F.F x 292	F.F x 584	F.F x 1168	F.F x 2336
001001001	F.F x 74	F.F x 148	F.F x 296	F.F x 592	F.F x 1184	F.F x 2368
001001010	F.F x 75	F.F x 150	F.F x 300	F.F x 600	F.F x 1200	F.F x 2400
001001011	F.F x 76	F.F x 152	F.F x 304	F.F x 608	F.F x 1216	F.F x 2432
001001100	F.F x 77	F.F x 154	F.F x 308	F.F x 616	F.F x 1232	F.F x 2464
001001101	F.F x 78	F.F x 156	F.F x 312	F.F x 624	F.F x 1248	F.F x 2496
001001110	F.F x 79	F.F x 158	F.F x 316	F.F x 632	F.F x 1264	F.F x 2528
001001111	F.F x 80	F.F x 160	F.F x 320	F.F x 640	F.F x 1280	F.F x 2560
001010000	F.F x 81	F.F x 162	F.F x 324	F.F x 648	F.F x 1296	F.F x 2592
001010001	F.F x 82	F.F x 164	F.F x 328	F.F x 656	F.F x 1312	F.F x 2624
001010010	F.F x 83	F.F x 166	F.F x 332	F.F x 664	F.F x 1328	F.F x 2656
001010011	F.F x 84	F.F x 168	F.F x 336	F.F x 672	F.F x 1344	F.F x 2688
001010100	F.F x 85	F.F x 170	F.F x 340	F.F x 680	F.F x 1360	F.F x 2720
001010101	F.F x 86	F.F x 172	F.F x 344	F.F x 688	F.F x 1376	F.F x 2752
001010110	F.F x 87	F.F x 174	F.F x 348	F.F x 696	F.F x 1392	F.F x 2784
001010111	F.F x 88	F.F x 176	F.F x 352	F.F x 704	F.F x 1408	F.F x 2816
001011000	F.F x 89	F.F x 178	F.F x 356	F.F x 712	F.F x 1424	F.F x 2848
001011001	F.F x 90	F.F x 180	F.F x 360	F.F x 720	F.F x 1440	F.F x 2880
001011010	F.F x 91	F.F x 182	F.F x 364	F.F x 728	F.F x 1456	F.F x 2912
001011011	F.F x 92	F.F x 184	F.F x 368	F.F x 736	F.F x 1472	F.F x 2944
001011100	F.F x 93	F.F x 186	F.F x 372	F.F x 744	F.F x 1488	F.F x 2976
001011101	F.F x 94	F.F x 188	F.F x 376	F.F x 752	F.F x 1504	F.F x 3008
001011110	F.F x 95	F.F x 190	F.F x 380	F.F x 760	F.F x 1520	F.F x 3040
001011111	F.F x 96	F.F x 192	F.F x 384	F.F x 768	F.F x 1536	F.F x 3072
001100000	F.F x 97	F.F x 194	F.F x 388	F.F x 776	F.F x 1552	F.F x 3104
001100001	F.F x 98	F.F x 196	F.F x 392	F.F x 784	F.F x 1568	F.F x 3136
001100010	F.F x 99	F.F x 198	F.F x 396	F.F x 792	F.F x 1584	F.F x 3168
001100011	F.F x 100	F.F x 200	F.F x 400	F.F x 800	F.F x 1600	F.F x 3200
001100100	F.F x 101	F.F x 202	F.F x 404	F.F x 808	F.F x 1616	F.F x 3232
001100101	F.F x 102	F.F x 204	F.F x 408	F.F x 816	F.F x 1632	F.F x 3264
001100110	F.F x 103	F.F x 206	F.F x 412	F.F x 824	F.F x 1648	F.F x 3296
001100111	F.F x 104	F.F x 208	F.F x 416	F.F x 832	F.F x 1664	F.F x 3328

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
001101000	F.F x 105	F.F x 210	F.F x 420	F.F x 840	F.F x 1680	F.F x 3360
001101001	F.F x 106	F.F x 212	F.F x 424	F.F x 848	F.F x 1696	F.F x 3392
001101010	F.F x 107	F.F x 214	F.F x 428	F.F x 856	F.F x 1712	F.F x 3424
001101011	F.F x 108	F.F x 216	F.F x 432	F.F x 864	F.F x 1728	F.F x 3456
001101100	F.F x 109	F.F x 218	F.F x 436	F.F x 872	F.F x 1744	F.F x 3488
001101101	F.F x 110	F.F x 220	F.F x 440	F.F x 880	F.F x 1760	F.F x 3520
001101110	F.F x 111	F.F x 222	F.F x 444	F.F x 888	F.F x 1776	F.F x 3552
001101111	F.F x 112	F.F x 224	F.F x 448	F.F x 896	F.F x 1792	F.F x 3584
001110000	F.F x 113	F.F x 226	F.F x 452	F.F x 904	F.F x 1808	F.F x 3616
001110001	F.F x 114	F.F x 228	F.F x 456	F.F x 912	F.F x 1824	F.F x 3648
001110010	F.F x 115	F.F x 230	F.F x 460	F.F x 920	F.F x 1840	F.F x 3680
001110011	F.F x 116	F.F x 232	F.F x 464	F.F x 928	F.F x 1856	F.F x 3712
001110100	F.F x 117	F.F x 234	F.F x 468	F.F x 936	F.F x 1872	F.F x 3744
001110101	F.F x 118	F.F x 236	F.F x 472	F.F x 944	F.F x 1888	F.F x 3776
001110110	F.F x 119	F.F x 238	F.F x 476	F.F x 952	F.F x 1904	F.F x 3808
001110111	F.F x 120	F.F x 240	F.F x 480	F.F x 960	F.F x 1920	F.F x 3840
001111000	F.F x 121	F.F x 242	F.F x 484	F.F x 968	F.F x 1936	F.F x 3872
001111001	F.F x 122	F.F x 244	F.F x 488	F.F x 976	F.F x 1952	F.F x 3904
001111010	F.F x 123	F.F x 246	F.F x 492	F.F x 984	F.F x 1968	F.F x 3936
001111011	F.F x 124	F.F x 248	F.F x 496	F.F x 992	F.F x 1984	F.F x 3968
001111100	F.F x 125	F.F x 250	F.F x 500	F.F x 1000	F.F x 2000	F.F x 4000
001111101	F.F x 126	F.F x 252	F.F x 504	F.F x 1008	F.F x 2016	F.F x 4032
001111110	F.F x 127	F.F x 254	F.F x 508	F.F x 1016	F.F x 2032	F.F x 4064
001111111	F.F x 128	F.F x 256	F.F x 512	F.F x 1024	F.F x 2048	F.F x 4096
010000000	F.F x 129	F.F x 258	F.F x 516	F.F x 1032	F.F x 2064	F.F x 4128
010000001	F.F x 130	F.F x 260	F.F x 520	F.F x 1040	F.F x 2080	F.F x 4160
010000010	F.F x 131	F.F x 262	F.F x 524	F.F x 1048	F.F x 2096	F.F x 4192
010000011	F.F x 132	F.F x 264	F.F x 528	F.F x 1056	F.F x 2112	F.F x 4224
010000100	F.F x 133	F.F x 266	F.F x 532	F.F x 1064	F.F x 2128	F.F x 4256
010000101	F.F x 134	F.F x 268	F.F x 536	F.F x 1072	F.F x 2144	F.F x 4288
010000110	F.F x 135	F.F x 270	F.F x 540	F.F x 1080	F.F x 2160	F.F x 4320
010000111	F.F x 136	F.F x 272	F.F x 544	F.F x 1088	F.F x 2176	F.F x 4352
010001000	F.F x 137	F.F x 274	F.F x 548	F.F x 1096	F.F x 2192	F.F x 4384

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
010001001	F.F x 138	F.F x 276	F.F x 552	F.F x 1104	F.F x 2208	F.F x 4416
010001010	F.F x 139	F.F x 278	F.F x 556	F.F x 1112	F.F x 2224	F.F x 4448
010001011	F.F x 140	F.F x 280	F.F x 560	F.F x 1120	F.F x 2240	F.F x 4480
010001100	F.F x 141	F.F x 282	F.F x 564	F.F x 1128	F.F x 2256	F.F x 4512
010001101	F.F x 142	F.F x 284	F.F x 568	F.F x 1136	F.F x 2272	F.F x 4544
010001110	F.F x 143	F.F x 286	F.F x 572	F.F x 1144	F.F x 2288	F.F x 4576
010001111	F.F x 144	F.F x 288	F.F x 576	F.F x 1152	F.F x 2304	F.F x 4608
010010000	F.F x 145	F.F x 290	F.F x 580	F.F x 1160	F.F x 2320	F.F x 4640
010010001	F.F x 146	F.F x 292	F.F x 584	F.F x 1168	F.F x 2336	F.F x 4672
010010010	F.F x 147	F.F x 294	F.F x 588	F.F x 1176	F.F x 2352	F.F x 4704
010010011	F.F x 148	F.F x 296	F.F x 592	F.F x 1184	F.F x 2368	F.F x 4736
010010100	F.F x 149	F.F x 298	F.F x 596	F.F x 1192	F.F x 2384	F.F x 4768
010010101	F.F x 150	F.F x 300	F.F x 600	F.F x 1200	F.F x 2400	F.F x 4800
010010110	F.F x 151	F.F x 302	F.F x 604	F.F x 1208	F.F x 2416	F.F x 4832
010010111	F.F x 152	F.F x 304	F.F x 608	F.F x 1216	F.F x 2432	F.F x 4864
010011000	F.F x 153	F.F x 306	F.F x 612	F.F x 1224	F.F x 2448	F.F x 4896
010011001	F.F x 154	F.F x 308	F.F x 616	F.F x 1232	F.F x 2464	F.F x 4928
010011010	F.F x 155	F.F x 310	F.F x 620	F.F x 1240	F.F x 2480	F.F x 4960
010011011	F.F x 156	F.F x 312	F.F x 624	F.F x 1248	F.F x 2496	F.F x 4992
010011100	F.F x 157	F.F x 314	F.F x 628	F.F x 1256	F.F x 2512	F.F x 5024
010011101	F.F x 158	F.F x 316	F.F x 632	F.F x 1264	F.F x 2528	F.F x 5056
010011110	F.F x 159	F.F x 318	F.F x 636	F.F x 1272	F.F x 2544	F.F x 5088
010011111	F.F x 160	F.F x 320	F.F x 640	F.F x 1280	F.F x 2560	F.F x 5120
010100000	F.F x 161	F.F x 322	F.F x 644	F.F x 1288	F.F x 2576	F.F x 5152
010100001	F.F x 162	F.F x 324	F.F x 648	F.F x 1296	F.F x 2592	F.F x 5184
010100010	F.F x 163	F.F x 326	F.F x 652	F.F x 1304	F.F x 2608	F.F x 5216
010100011	F.F x 164	F.F x 328	F.F x 656	F.F x 1312	F.F x 2624	F.F x 5248
010100100	F.F x 165	F.F x 330	F.F x 660	F.F x 1320	F.F x 2640	F.F x 5280
010100101	F.F x 166	F.F x 332	F.F x 664	F.F x 1328	F.F x 2656	F.F x 5312
010100110	F.F x 167	F.F x 334	F.F x 668	F.F x 1336	F.F x 2672	F.F x 5344
010100111	F.F x 168	F.F x 336	F.F x 672	F.F x 1344	F.F x 2688	F.F x 5376
010101000	F.F x 169	F.F x 338	F.F x 676	F.F x 1352	F.F x 2704	F.F x 5408
010101001	F.F x 170	F.F x 340	F.F x 680	F.F x 1360	F.F x 2720	F.F x 5440

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
010101010	F.F x 171	F.F x 342	F.F x 684	F.F x 1368	F.F x 2736	F.F x 5472
010101011	F.F x 172	F.F x 344	F.F x 688	F.F x 1376	F.F x 2752	F.F x 5504
010101100	F.F x 173	F.F x 346	F.F x 692	F.F x 1384	F.F x 2768	F.F x 5536
010101101	F.F x 174	F.F x 348	F.F x 696	F.F x 1392	F.F x 2784	F.F x 5568
010101110	F.F x 175	F.F x 350	F.F x 700	F.F x 1400	F.F x 2800	F.F x 5600
010101111	F.F x 176	F.F x 352	F.F x 704	F.F x 1408	F.F x 2816	F.F x 5632
010110000	F.F x 177	F.F x 354	F.F x 708	F.F x 1416	F.F x 2832	F.F x 5664
010110001	F.F x 178	F.F x 356	F.F x 712	F.F x 1424	F.F x 2848	F.F x 5696
010110010	F.F x 179	F.F x 358	F.F x 716	F.F x 1432	F.F x 2864	F.F x 5728
010110011	F.F x 180	F.F x 360	F.F x 720	F.F x 1440	F.F x 2880	F.F x 5760
010110100	F.F x 181	F.F x 362	F.F x 724	F.F x 1448	F.F x 2896	F.F x 5792
010110101	F.F x 182	F.F x 364	F.F x 728	F.F x 1456	F.F x 2912	F.F x 5824
010110110	F.F x 183	F.F x 366	F.F x 732	F.F x 1464	F.F x 2928	F.F x 5856
010110111	F.F x 184	F.F x 368	F.F x 736	F.F x 1472	F.F x 2944	F.F x 5888
010111000	F.F x 185	F.F x 370	F.F x 740	F.F x 1480	F.F x 2960	F.F x 5920
010111001	F.F x 186	F.F x 372	F.F x 744	F.F x 1488	F.F x 2976	F.F x 5952
010111010	F.F x 187	F.F x 374	F.F x 748	F.F x 1496	F.F x 2992	F.F x 5984
010111011	F.F x 188	F.F x 376	F.F x 752	F.F x 1504	F.F x 3008	F.F x 6016
010111100	F.F x 189	F.F x 378	F.F x 756	F.F x 1512	F.F x 3024	F.F x 6048
010111101	F.F x 190	F.F x 380	F.F x 760	F.F x 1520	F.F x 3040	F.F x 6080
010111110	F.F x 191	F.F x 382	F.F x 764	F.F x 1528	F.F x 3056	F.F x 6112
010111111	F.F x 192	F.F x 384	F.F x 768	F.F x 1536	F.F x 3072	F.F x 6144
011000000	F.F x 193	F.F x 386	F.F x 772	F.F x 1544	F.F x 3088	F.F x 6176
011000001	F.F x 194	F.F x 388	F.F x 776	F.F x 1552	F.F x 3104	F.F x 6208
011000010	F.F x 195	F.F x 390	F.F x 780	F.F x 1560	F.F x 3120	F.F x 6240
011000011	F.F x 196	F.F x 392	F.F x 784	F.F x 1568	F.F x 3136	F.F x 6272
011000100	F.F x 197	F.F x 394	F.F x 788	F.F x 1576	F.F x 3152	F.F x 6304
011000101	F.F x 198	F.F x 396	F.F x 792	F.F x 1584	F.F x 3168	F.F x 6336
011000110	F.F x 199	F.F x 398	F.F x 796	F.F x 1592	F.F x 3184	F.F x 6368
011000111	F.F x 200	F.F x 400	F.F x 800	F.F x 1600	F.F x 3200	F.F x 6400
011001000	F.F x 201	F.F x 402	F.F x 804	F.F x 1608	F.F x 3216	F.F x 6432
011001001	F.F x 202	F.F x 404	F.F x 808	F.F x 1616	F.F x 3232	F.F x 6464
011001010	F.F x 203	F.F x 406	F.F x 812	F.F x 1624	F.F x 3248	F.F x 6496

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
011001011	F.F x 204	F.F x 408	F.F x 816	F.F x 1632	F.F x 3264	F.F x 6528
011001100	F.F x 205	F.F x 410	F.F x 820	F.F x 1640	F.F x 3280	F.F x 6560
011001101	F.F x 206	F.F x 412	F.F x 824	F.F x 1648	F.F x 3296	F.F x 6592
011001110	F.F x 207	F.F x 414	F.F x 828	F.F x 1656	F.F x 3312	F.F x 6624
011001111	F.F x 208	F.F x 416	F.F x 832	F.F x 1664	F.F x 3328	F.F x 6656
011010000	F.F x 209	F.F x 418	F.F x 836	F.F x 1672	F.F x 3344	F.F x 6688
011010001	F.F x 210	F.F x 420	F.F x 840	F.F x 1680	F.F x 3360	F.F x 6720
011010010	F.F x 211	F.F x 422	F.F x 844	F.F x 1688	F.F x 3376	F.F x 6752
011010011	F.F x 212	F.F x 424	F.F x 848	F.F x 1696	F.F x 3392	F.F x 6784
011010100	F.F x 213	F.F x 426	F.F x 852	F.F x 1704	F.F x 3408	F.F x 6816
011010101	F.F x 214	F.F x 428	F.F x 856	F.F x 1712	F.F x 3424	F.F x 6848
011010110	F.F x 215	F.F x 430	F.F x 860	F.F x 1720	F.F x 3440	F.F x 6880
011010111	F.F x 216	F.F x 432	F.F x 864	F.F x 1728	F.F x 3456	F.F x 6912
011011000	F.F x 217	F.F x 434	F.F x 868	F.F x 1736	F.F x 3472	F.F x 6944
011011001	F.F x 218	F.F x 436	F.F x 872	F.F x 1744	F.F x 3488	F.F x 6976
011011010	F.F x 219	F.F x 438	F.F x 876	F.F x 1752	F.F x 3504	F.F x 7008
011011011	F.F x 220	F.F x 440	F.F x 880	F.F x 1760	F.F x 3520	F.F x 7040
011011100	F.F x 221	F.F x 442	F.F x 884	F.F x 1768	F.F x 3536	F.F x 7072
011011101	F.F x 222	F.F x 444	F.F x 888	F.F x 1776	F.F x 3552	F.F x 7104
011011110	F.F x 223	F.F x 446	F.F x 892	F.F x 1784	F.F x 3568	F.F x 7136
011011111	F.F x 224	F.F x 448	F.F x 896	F.F x 1792	F.F x 3584	F.F x 7168
011100000	F.F x 225	F.F x 450	F.F x 900	F.F x 1800	F.F x 3600	F.F x 7200
011100001	F.F x 226	F.F x 452	F.F x 904	F.F x 1808	F.F x 3616	F.F x 7232
011100010	F.F x 227	F.F x 454	F.F x 908	F.F x 1816	F.F x 3632	F.F x 7264
011100011	F.F x 228	F.F x 456	F.F x 912	F.F x 1824	F.F x 3648	F.F x 7296
011100100	F.F x 229	F.F x 458	F.F x 916	F.F x 1832	F.F x 3664	F.F x 7328
011100101	F.F x 230	F.F x 460	F.F x 920	F.F x 1840	F.F x 3680	F.F x 7360
011100110	F.F x 231	F.F x 462	F.F x 924	F.F x 1848	F.F x 3696	F.F x 7392
011100111	F.F x 232	F.F x 464	F.F x 928	F.F x 1856	F.F x 3712	F.F x 7424
011101000	F.F x 233	F.F x 466	F.F x 932	F.F x 1864	F.F x 3728	F.F x 7456
011101001	F.F x 234	F.F x 468	F.F x 936	F.F x 1872	F.F x 3744	F.F x 7488
011101010	F.F x 235	F.F x 470	F.F x 940	F.F x 1880	F.F x 3760	F.F x 7520
011101011	F.F x 236	F.F x 472	F.F x 944	F.F x 1888	F.F x 3776	F.F x 7552

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
011101100	F.F x 237	F.F x 474	F.F x 948	F.F x 1896	F.F x 3792	F.F x 7584
011101101	F.F x 238	F.F x 476	F.F x 952	F.F x 1904	F.F x 3808	F.F x 7616
011101110	F.F x 239	F.F x 478	F.F x 956	F.F x 1912	F.F x 3824	F.F x 7648
011101111	F.F x 240	F.F x 480	F.F x 960	F.F x 1920	F.F x 3840	F.F x 7680
011110000	F.F x 241	F.F x 482	F.F x 964	F.F x 1928	F.F x 3856	F.F x 7712
011110001	F.F x 242	F.F x 484	F.F x 968	F.F x 1936	F.F x 3872	F.F x 7744
011110010	F.F x 243	F.F x 486	F.F x 972	F.F x 1944	F.F x 3888	F.F x 7776
011110011	F.F x 244	F.F x 488	F.F x 976	F.F x 1952	F.F x 3904	F.F x 7808
011110100	F.F x 245	F.F x 490	F.F x 980	F.F x 1960	F.F x 3920	F.F x 7840
011110101	F.F x 246	F.F x 492	F.F x 984	F.F x 1968	F.F x 3936	F.F x 7872
011110110	F.F x 247	F.F x 494	F.F x 988	F.F x 1976	F.F x 3952	F.F x 7904
011110111	F.F x 248	F.F x 496	F.F x 992	F.F x 1984	F.F x 3968	F.F x 7936
011111000	F.F x 249	F.F x 498	F.F x 996	F.F x 1992	F.F x 3984	F.F x 7968
011111001	F.F x 250	F.F x 500	F.F x 1000	F.F x 2000	F.F x 4000	F.F x 8000
011111010	F.F x 251	F.F x 502	F.F x 1004	F.F x 2008	F.F x 4016	F.F x 8032
011111011	F.F x 252	F.F x 504	F.F x 1008	F.F x 2016	F.F x 4032	F.F x 8064
011111100	F.F x 253	F.F x 506	F.F x 1012	F.F x 2024	F.F x 4048	F.F x 8096
011111101	F.F x 254	F.F x 508	F.F x 1016	F.F x 2032	F.F x 4064	F.F x 8128
011111110	F.F x 255	F.F x 510	F.F x 1020	F.F x 2040	F.F x 4080	F.F x 8160
011111111	F.F x 256	F.F x 512	F.F x 1024	F.F x 2048	F.F x 4096	F.F x 8192
100000000	F.F x 257	F.F x 514	F.F x 1028	F.F x 2056	F.F x 4112	F.F x 8224
100000001	F.F x 258	F.F x 516	F.F x 1032	F.F x 2064	F.F x 4128	F.F x 8256
100000010	F.F x 259	F.F x 518	F.F x 1036	F.F x 2072	F.F x 4144	F.F x 8288
100000011	F.F x 260	F.F x 520	F.F x 1040	F.F x 2080	F.F x 4160	F.F x 8320
100000100	F.F x 261	F.F x 522	F.F x 1044	F.F x 2088	F.F x 4176	F.F x 8352
100000101	F.F x 262	F.F x 524	F.F x 1048	F.F x 2096	F.F x 4192	F.F x 8384
100000110	F.F x 263	F.F x 526	F.F x 1052	F.F x 2104	F.F x 4208	F.F x 8416
100000111	F.F x 264	F.F x 528	F.F x 1056	F.F x 2112	F.F x 4224	F.F x 8448
100001000	F.F x 265	F.F x 530	F.F x 1060	F.F x 2120	F.F x 4240	F.F x 8480
100001001	F.F x 266	F.F x 532	F.F x 1064	F.F x 2128	F.F x 4256	F.F x 8512
100001010	F.F x 267	F.F x 534	F.F x 1068	F.F x 2136	F.F x 4272	F.F x 8544
100001011	F.F x 268	F.F x 536	F.F x 1072	F.F x 2144	F.F x 4288	F.F x 8576
100001100	F.F x 269	F.F x 538	F.F x 1076	F.F x 2152	F.F x 4304	F.F x 8608

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
100001101	F.F x 270	F.F x 540	F.F x 1080	F.F x 2160	F.F x 4320	F.F x 8640
100001110	F.F x 271	F.F x 542	F.F x 1084	F.F x 2168	F.F x 4336	F.F x 8672
100001111	F.F x 272	F.F x 544	F.F x 1088	F.F x 2176	F.F x 4352	F.F x 8704
100010000	F.F x 273	F.F x 546	F.F x 1092	F.F x 2184	F.F x 4368	F.F x 8736
100010001	F.F x 274	F.F x 548	F.F x 1096	F.F x 2192	F.F x 4384	F.F x 8768
100010010	F.F x 275	F.F x 550	F.F x 1100	F.F x 2200	F.F x 4400	F.F x 8800
100010011	F.F x 276	F.F x 552	F.F x 1104	F.F x 2208	F.F x 4416	F.F x 8832
100010100	F.F x 277	F.F x 554	F.F x 1108	F.F x 2216	F.F x 4432	F.F x 8864
100010101	F.F x 278	F.F x 556	F.F x 1112	F.F x 2224	F.F x 4448	F.F x 8896
100010110	F.F x 279	F.F x 558	F.F x 1116	F.F x 2232	F.F x 4464	F.F x 8928
100010111	F.F x 280	F.F x 560	F.F x 1120	F.F x 2240	F.F x 4480	F.F x 8960
100011000	F.F x 281	F.F x 562	F.F x 1124	F.F x 2248	F.F x 4496	F.F x 8992
100011001	F.F x 282	F.F x 564	F.F x 1128	F.F x 2256	F.F x 4512	F.F x 9024
100011010	F.F x 283	F.F x 566	F.F x 1132	F.F x 2264	F.F x 4528	F.F x 9056
100011011	F.F x 284	F.F x 568	F.F x 1136	F.F x 2272	F.F x 4544	F.F x 9088
100011100	F.F x 285	F.F x 570	F.F x 1140	F.F x 2280	F.F x 4560	F.F x 9120
100011101	F.F x 286	F.F x 572	F.F x 1144	F.F x 2288	F.F x 4576	F.F x 9152
100011110	F.F x 287	F.F x 574	F.F x 1148	F.F x 2296	F.F x 4592	F.F x 9184
100011111	F.F x 288	F.F x 576	F.F x 1152	F.F x 2304	F.F x 4608	F.F x 9216
100100000	F.F x 289	F.F x 578	F.F x 1156	F.F x 2312	F.F x 4624	F.F x 9248
100100001	F.F x 290	F.F x 580	F.F x 1160	F.F x 2320	F.F x 4640	F.F x 9280
100100010	F.F x 291	F.F x 582	F.F x 1164	F.F x 2328	F.F x 4656	F.F x 9312
100100011	F.F x 292	F.F x 584	F.F x 1168	F.F x 2336	F.F x 4672	F.F x 9344
100100100	F.F x 293	F.F x 586	F.F x 1172	F.F x 2344	F.F x 4688	F.F x 9376
100100101	F.F x 294	F.F x 588	F.F x 1176	F.F x 2352	F.F x 4704	F.F x 9408
100100110	F.F x 295	F.F x 590	F.F x 1180	F.F x 2360	F.F x 4720	F.F x 9440
100100111	F.F x 296	F.F x 592	F.F x 1184	F.F x 2368	F.F x 4736	F.F x 9472
100101000	F.F x 297	F.F x 594	F.F x 1188	F.F x 2376	F.F x 4752	F.F x 9504
100101001	F.F x 298	F.F x 596	F.F x 1192	F.F x 2384	F.F x 4768	F.F x 9536
100101010	F.F x 299	F.F x 598	F.F x 1196	F.F x 2392	F.F x 4784	F.F x 9568
100101011	F.F x 300	F.F x 600	F.F x 1200	F.F x 2400	F.F x 4800	F.F x 9600
100101100	F.F x 301	F.F x 602	F.F x 1204	F.F x 2408	F.F x 4816	F.F x 9632
100101101	F.F x 302	F.F x 604	F.F x 1208	F.F x 2416	F.F x 4832	F.F x 9664

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
100101110	F.F x 303	F.F x 606	F.F x 1212	F.F x 2424	F.F x 4848	F.F x 9696
100101111	F.F x 304	F.F x 608	F.F x 1216	F.F x 2432	F.F x 4864	F.F x 9728
100110000	F.F x 305	F.F x 610	F.F x 1220	F.F x 2440	F.F x 4880	F.F x 9760
100110001	F.F x 306	F.F x 612	F.F x 1224	F.F x 2448	F.F x 4896	F.F x 9792
100110010	F.F x 307	F.F x 614	F.F x 1228	F.F x 2456	F.F x 4912	F.F x 9824
100110011	F.F x 308	F.F x 616	F.F x 1232	F.F x 2464	F.F x 4928	F.F x 9856
100110100	F.F x 309	F.F x 618	F.F x 1236	F.F x 2472	F.F x 4944	F.F x 9888
100110101	F.F x 310	F.F x 620	F.F x 1240	F.F x 2480	F.F x 4960	F.F x 9920
100110110	F.F x 311	F.F x 622	F.F x 1244	F.F x 2488	F.F x 4976	F.F x 9952
100110111	F.F x 312	F.F x 624	F.F x 1248	F.F x 2496	F.F x 4992	F.F x 9984
100111000	F.F x 313	F.F x 626	F.F x 1252	F.F x 2504	F.F x 5008	F.F x 10016
100111001	F.F x 314	F.F x 628	F.F x 1256	F.F x 2512	F.F x 5024	F.F x 10048
100111010	F.F x 315	F.F x 630	F.F x 1260	F.F x 2520	F.F x 5040	F.F x 10080
100111011	F.F x 316	F.F x 632	F.F x 1264	F.F x 2528	F.F x 5056	F.F x 10112
100111100	F.F x 317	F.F x 634	F.F x 1268	F.F x 2536	F.F x 5072	F.F x 10144
100111101	F.F x 318	F.F x 636	F.F x 1272	F.F x 2544	F.F x 5088	F.F x 10176
100111110	F.F x 319	F.F x 638	F.F x 1276	F.F x 2552	F.F x 5104	F.F x 10208
100111111	F.F x 320	F.F x 640	F.F x 1280	F.F x 2560	F.F x 5120	F.F x 10240
101000000	F.F x 321	F.F x 642	F.F x 1284	F.F x 2568	F.F x 5136	F.F x 10272
101000001	F.F x 322	F.F x 644	F.F x 1288	F.F x 2576	F.F x 5152	F.F x 10304
101000010	F.F x 323	F.F x 646	F.F x 1292	F.F x 2584	F.F x 5168	F.F x 10336
101000011	F.F x 324	F.F x 648	F.F x 1296	F.F x 2592	F.F x 5184	F.F x 10368
101000100	F.F x 325	F.F x 650	F.F x 1300	F.F x 2600	F.F x 5200	F.F x 10400
101000101	F.F x 326	F.F x 652	F.F x 1304	F.F x 2608	F.F x 5216	F.F x 10432
101000110	F.F x 327	F.F x 654	F.F x 1308	F.F x 2616	F.F x 5232	F.F x 10464
101000111	F.F x 328	F.F x 656	F.F x 1312	F.F x 2624	F.F x 5248	F.F x 10496
101001000	F.F x 329	F.F x 658	F.F x 1316	F.F x 2632	F.F x 5264	F.F x 10528
101001001	F.F x 330	F.F x 660	F.F x 1320	F.F x 2640	F.F x 5280	F.F x 10560
101001010	F.F x 331	F.F x 662	F.F x 1324	F.F x 2648	F.F x 5296	F.F x 10592
101001011	F.F x 332	F.F x 664	F.F x 1328	F.F x 2656	F.F x 5312	F.F x 10624
101001100	F.F x 333	F.F x 666	F.F x 1332	F.F x 2664	F.F x 5328	F.F x 10656
101001101	F.F x 334	F.F x 668	F.F x 1336	F.F x 2672	F.F x 5344	F.F x 10688
101001110	F.F x 335	F.F x 670	F.F x 1340	F.F x 2680	F.F x 5360	F.F x 10720

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
101001111	F.F x 336	F.F x 672	F.F x 1344	F.F x 2688	F.F x 5376	F.F x 10752
101010000	F.F x 337	F.F x 674	F.F x 1348	F.F x 2696	F.F x 5392	F.F x 10784
101010001	F.F x 338	F.F x 676	F.F x 1352	F.F x 2704	F.F x 5408	F.F x 10816
101010010	F.F x 339	F.F x 678	F.F x 1356	F.F x 2712	F.F x 5424	F.F x 10848
101010011	F.F x 340	F.F x 680	F.F x 1360	F.F x 2720	F.F x 5440	F.F x 10880

NOTE: F.F. means Frame Frequency.

When the display frame frequency is 60Hz, PWM frequency is represented at the table below.

Table 111 Example of PWM FREQUENCY Selection

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
000000000	60	120	240	480	960	1920
000000001	120	240	480	960	1920	3840
000000010	180	360	720	1440	2880	5760
000000011	240	480	960	1920	3840	7680
000000100	300	600	1200	2400	4800	9600
000000101	360	720	1440	2880	5760	11520
000000110	420	840	1680	3360	6720	13440
000000111	480	960	1920	3840	7680	15360
000001000	540	1080	2160	4320	8640	17280
000001001	600	1200	2400	4800	9600	19200
000001010	660	1320	2640	5280	10560	21120
000001011	720	1440	2880	5760	11520	23040
000001100	780	1560	3120	6240	12480	24960
000001101	840	1680	3360	6720	13440	26880
000001110	900	1800	3600	7200	14400	28800
000001111	960	1920	3840	7680	15360	30720
000010000	1020	2040	4080	8160	16320	32640
000010001	1080	2160	4320	8640	17280	34560

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
000010010	1140	2280	4560	9120	18240	36480
000010011	1200	2400	4800	9600	19200	38400
000010100	1260	2520	5040	10080	20160	40320
000010101	1320	2640	5280	10560	21120	42240
000010110	1380	2760	5520	11040	22080	44160
000010111	1440	2880	5760	11520	23040	46080
000011000	1500	3000	6000	12000	24000	48000
000011001	1560	3120	6240	12480	24960	49920
000011010	1620	3240	6480	12960	25920	51840
000011011	1680	3360	6720	13440	26880	53760
000011100	1740	3480	6960	13920	27840	55680
000011101	1800	3600	7200	14400	28800	57600
000011110	1860	3720	7440	14880	29760	59520
000011111	1920	3840	7680	15360	30720	61440
000100000	1980	3960	7920	15840	31680	63360
000100001	2040	4080	8160	16320	32640	65280
000100010	2100	4200	8400	16800	33600	67200
000100011	2160	4320	8640	17280	34560	69120
000100100	2220	4440	8880	17760	35520	71040
000100101	2280	4560	9120	18240	36480	72960
000100110	2340	4680	9360	18720	37440	74880
000100111	2400	4800	9600	19200	38400	76800
000101000	2460	4920	9840	19680	39360	78720
000101001	2520	5040	10080	20160	40320	80640
000101010	2580	5160	10320	20640	41280	82560
000101011	2640	5280	10560	21120	42240	84480
000101100	2700	5400	10800	21600	43200	86400
000101101	2760	5520	11040	22080	44160	88320
000101110	2820	5640	11280	22560	45120	90240
000101111	2880	5760	11520	23040	46080	92160
000110000	2940	5880	11760	23520	47040	94080
000110001	3000	6000	12000	24000	48000	96000
000110010	3060	6120	12240	24480	48960	97920

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
000110011	3120	6240	12480	24960	49920	99840
000110100	3180	6360	12720	25440	50880	101760
000110101	3240	6480	12960	25920	51840	103680
000110110	3300	6600	13200	26400	52800	105600
000110111	3360	6720	13440	26880	53760	107520
000111000	3420	6840	13680	27360	54720	109440
000111001	3480	6960	13920	27840	55680	111360
000111010	3540	7080	14160	28320	56640	113280
000111011	3600	7200	14400	28800	57600	115200
000111100	3660	7320	14640	29280	58560	117120
000111101	3720	7440	14880	29760	59520	119040
000111110	3780	7560	15120	30240	60480	120960
000111111	3840	7680	15360	30720	61440	122880
001000000	3900	7800	15600	31200	62400	124800
001000001	3960	7920	15840	31680	63360	126720
001000010	4020	8040	16080	32160	64320	128640
001000011	4080	8160	16320	32640	65280	130560
001000100	4140	8280	16560	33120	66240	132480
001000101	4200	8400	16800	33600	67200	134400
001000110	4260	8520	17040	34080	68160	136320
001000111	4320	8640	17280	34560	69120	138240
001001000	4380	8760	17520	35040	70080	140160
001001001	4440	8880	17760	35520	71040	142080
001001010	4500	9000	18000	36000	72000	144000
001001011	4560	9120	18240	36480	72960	145920
001001100	4620	9240	18480	36960	73920	147840
001001101	4680	9360	18720	37440	74880	149760
001001110	4740	9480	18960	37920	75840	151680
001001111	4800	9600	19200	38400	76800	153600
001010000	4860	9720	19440	38880	77760	155520
001010001	4920	9840	19680	39360	78720	157440
001010010	4980	9960	19920	39840	79680	159360
001010011	5040	10080	20160	40320	80640	161280

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
001010100	5100	10200	20400	40800	81600	163200
001010101	5160	10320	20640	41280	82560	165120
001010110	5220	10440	20880	41760	83520	167040
001010111	5280	10560	21120	42240	84480	168960
001011000	5340	10680	21360	42720	85440	170880
001011001	5400	10800	21600	43200	86400	172800
001011010	5460	10920	21840	43680	87360	174720
001011011	5520	11040	22080	44160	88320	176640
001011100	5580	11160	22320	44640	89280	178560
001011101	5640	11280	22560	45120	90240	180480
001011110	5700	11400	22800	45600	91200	182400
001011111	5760	11520	23040	46080	92160	184320
001100000	5820	11640	23280	46560	93120	186240
001100001	5880	11760	23520	47040	94080	188160
001100010	5940	11880	23760	47520	95040	190080
001100011	6000	12000	24000	48000	96000	192000
001100100	6060	12120	24240	48480	96960	193920
001100101	6120	12240	24480	48960	97920	195840
001100110	6180	12360	24720	49440	98880	197760
001100111	6240	12480	24960	49920	99840	199680
001101000	6300	12600	25200	50400	100800	201600
001101001	6360	12720	25440	50880	101760	203520
001101010	6420	12840	25680	51360	102720	205440
001101011	6480	12960	25920	51840	103680	207360
001101100	6540	13080	26160	52320	104640	209280
001101101	6600	13200	26400	52800	105600	211200
001101110	6660	13320	26640	53280	106560	213120
001101111	6720	13440	26880	53760	107520	215040
001110000	6780	13560	27120	54240	108480	216960
001110001	6840	13680	27360	54720	109440	218880
001110010	6900	13800	27600	55200	110400	220800
001110011	6960	13920	27840	55680	111360	222720
001110100	7020	14040	28080	56160	112320	224640

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
001110101	7080	14160	28320	56640	113280	226560
001110110	7140	14280	28560	57120	114240	228480
001110111	7200	14400	28800	57600	115200	230400
001111000	7260	14520	29040	58080	116160	232320
001111001	7320	14640	29280	58560	117120	234240
001111010	7380	14760	29520	59040	118080	236160
001111011	7440	14880	29760	59520	119040	238080
001111100	7500	15000	30000	60000	120000	240000
001111101	7560	15120	30240	60480	120960	241920
001111110	7620	15240	30480	60960	121920	243840
001111111	7680	15360	30720	61440	122880	245760
010000000	7740	15480	30960	61920	123840	247680
010000001	7800	15600	31200	62400	124800	249600
010000010	7860	15720	31440	62880	125760	251520
010000011	7920	15840	31680	63360	126720	253440
010000100	7980	15960	31920	63840	127680	255360
010000101	8040	16080	32160	64320	128640	257280
010000110	8100	16200	32400	64800	129600	259200
010000111	8160	16320	32640	65280	130560	261120
010001000	8220	16440	32880	65760	131520	263040
010001001	8280	16560	33120	66240	132480	264960
010001010	8340	16680	33360	66720	133440	266880
010001011	8400	16800	33600	67200	134400	268800
010001100	8460	16920	33840	67680	135360	270720
010001101	8520	17040	34080	68160	136320	272640
010001110	8580	17160	34320	68640	137280	274560
010001111	8640	17280	34560	69120	138240	276480
010010000	8700	17400	34800	69600	139200	278400
010010001	8760	17520	35040	70080	140160	280320
010010010	8820	17640	35280	70560	141120	282240
010010011	8880	17760	35520	71040	142080	284160
010010100	8940	17880	35760	71520	143040	286080
010010101	9000	18000	36000	72000	144000	288000

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
010010110	9060	18120	36240	72480	144960	289920
010010111	9120	18240	36480	72960	145920	291840
010011000	9180	18360	36720	73440	146880	293760
010011001	9240	18480	36960	73920	147840	295680
010011010	9300	18600	37200	74400	148800	297600
010011011	9360	18720	37440	74880	149760	299520
010011100	9420	18840	37680	75360	150720	301440
010011101	9480	18960	37920	75840	151680	303360
010011110	9540	19080	38160	76320	152640	305280
010011111	9600	19200	38400	76800	153600	307200
010100000	9660	19320	38640	77280	154560	309120
010100001	9720	19440	38880	77760	155520	311040
010100010	9780	19560	39120	78240	156480	312960
010100011	9840	19680	39360	78720	157440	314880
010100100	9900	19800	39600	79200	158400	316800
010100101	9960	19920	39840	79680	159360	318720
010100110	10020	20040	40080	80160	160320	320640
010100111	10080	20160	40320	80640	161280	322560
010101000	10140	20280	40560	81120	162240	324480
010101001	10200	20400	40800	81600	163200	326400
010101010	10260	20520	41040	82080	164160	328320
010101011	10320	20640	41280	82560	165120	330240
010101100	10380	20760	41520	83040	166080	332160
010101101	10440	20880	41760	83520	167040	334080
010101110	10500	21000	42000	84000	168000	336000
010101111	10560	21120	42240	84480	168960	337920
010110000	10620	21240	42480	84960	169920	339840
010110001	10680	21360	42720	85440	170880	341760
010110010	10740	21480	42960	85920	171840	343680
010110011	10800	21600	43200	86400	172800	345600
010110100	10860	21720	43440	86880	173760	347520
010110101	10920	21840	43680	87360	174720	349440
010110110	10980	21960	43920	87840	175680	351360

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
010110111	11040	22080	44160	88320	176640	353280
010111000	11100	22200	44400	88800	177600	355200
010111001	11160	22320	44640	89280	178560	357120
010111010	11220	22440	44880	89760	179520	359040
010111011	11280	22560	45120	90240	180480	360960
010111100	11340	22680	45360	90720	181440	362880
010111101	11400	22800	45600	91200	182400	364800
010111110	11460	22920	45840	91680	183360	366720
010111111	11520	23040	46080	92160	184320	368640
011000000	11580	23160	46320	92640	185280	370560
011000001	11640	23280	46560	93120	186240	372480
011000010	11700	23400	46800	93600	187200	374400
011000011	11760	23520	47040	94080	188160	376320
011000100	11820	23640	47280	94560	189120	378240
011000101	11880	23760	47520	95040	190080	380160
011000110	11940	23880	47760	95520	191040	382080
011000111	12000	24000	48000	96000	192000	384000
011001000	12060	24120	48240	96480	192960	385920
011001001	12120	24240	48480	96960	193920	387840
011001010	12180	24360	48720	97440	194880	389760
011001011	12240	24480	48960	97920	195840	391680
011001100	12300	24600	49200	98400	196800	393600
011001101	12360	24720	49440	98880	197760	395520
011001110	12420	24840	49680	99360	198720	397440
011001111	12480	24960	49920	99840	199680	399360
011010000	12540	25080	50160	100320	200640	401280
011010001	12600	25200	50400	100800	201600	403200
011010010	12660	25320	50640	101280	202560	405120
011010011	12720	25440	50880	101760	203520	407040
011010100	12780	25560	51120	102240	204480	408960
011010101	12840	25680	51360	102720	205440	410880
011010110	12900	25800	51600	103200	206400	412800
011010111	12960	25920	51840	103680	207360	414720

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
011011000	13020	26040	52080	104160	208320	416640
011011001	13080	26160	52320	104640	209280	418560
011011010	13140	26280	52560	105120	210240	420480
011011011	13200	26400	52800	105600	211200	422400
011011100	13260	26520	53040	106080	212160	424320
011011101	13320	26640	53280	106560	213120	426240
011011110	13380	26760	53520	107040	214080	428160
011011111	13440	26880	53760	107520	215040	430080
011100000	13500	27000	54000	108000	216000	432000
011100001	13560	27120	54240	108480	216960	433920
011100010	13620	27240	54480	108960	217920	435840
011100011	13680	27360	54720	109440	218880	437760
011100100	13740	27480	54960	109920	219840	439680
011100101	13800	27600	55200	110400	220800	441600
011100110	13860	27720	55440	110880	221760	443520
011100111	13920	27840	55680	111360	222720	445440
011101000	13980	27960	55920	111840	223680	447360
011101001	14040	28080	56160	112320	224640	449280
011101010	14100	28200	56400	112800	225600	451200
011101011	14160	28320	56640	113280	226560	453120
011101100	14220	28440	56880	113760	227520	455040
011101101	14280	28560	57120	114240	228480	456960
011101110	14340	28680	57360	114720	229440	458880
011101111	14400	28800	57600	115200	230400	460800
011110000	14460	28920	57840	115680	231360	462720
011110001	14520	29040	58080	116160	232320	464640
011110010	14580	29160	58320	116640	233280	466560
011110011	14640	29280	58560	117120	234240	468480
011110100	14700	29400	58800	117600	235200	470400
011110101	14760	29520	59040	118080	236160	472320
011110110	14820	29640	59280	118560	237120	474240
011110111	14880	29760	59520	119040	238080	476160
011111000	14940	29880	59760	119520	239040	478080

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
011111001	15000	30000	60000	120000	240000	480000
011111010	15060	30120	60240	120480	240960	481920
011111011	15120	30240	60480	120960	241920	483840
011111100	15180	30360	60720	121440	242880	485760
011111101	15240	30480	60960	121920	243840	487680
011111110	15300	30600	61200	122400	244800	489600
011111111	15360	30720	61440	122880	245760	491520
100000000	15420	30840	61680	123360	246720	493440
100000001	15480	30960	61920	123840	247680	495360
100000010	15540	31080	62160	124320	248640	497280
100000011	15600	31200	62400	124800	249600	499200
100000100	15660	31320	62640	125280	250560	501120
100000101	15720	31440	62880	125760	251520	503040
100000110	15780	31560	63120	126240	252480	504960
100000111	15840	31680	63360	126720	253440	506880
100001000	15900	31800	63600	127200	254400	508800
100001001	15960	31920	63840	127680	255360	510720
100001010	16020	32040	64080	128160	256320	512640
100001011	16080	32160	64320	128640	257280	514560
100001100	16140	32280	64560	129120	258240	516480
100001101	16200	32400	64800	129600	259200	518400
100001110	16260	32520	65040	130080	260160	520320
100001111	16320	32640	65280	130560	261120	522240
100010000	16380	32760	65520	131040	262080	524160
100010001	16440	32880	65760	131520	263040	526080
100010010	16500	33000	66000	132000	264000	528000
100010011	16560	33120	66240	132480	264960	529920
100010100	16620	33240	66480	132960	265920	531840
100010101	16680	33360	66720	133440	266880	533760
100010110	16740	33480	66960	133920	267840	535680
100010111	16800	33600	67200	134400	268800	537600
100011000	16860	33720	67440	134880	269760	539520
100011001	16920	33840	67680	135360	270720	541440

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
100011010	16980	33960	67920	135840	271680	543360
100011011	17040	34080	68160	136320	272640	545280
100011100	17100	34200	68400	136800	273600	547200
100011101	17160	34320	68640	137280	274560	549120
100011110	17220	34440	68880	137760	275520	551040
100011111	17280	34560	69120	138240	276480	552960
100100000	17340	34680	69360	138720	277440	554880
100100001	17400	34800	69600	139200	278400	556800
100100010	17460	34920	69840	139680	279360	558720
100100011	17520	35040	70080	140160	280320	560640
100100100	17580	35160	70320	140640	281280	562560
100100101	17640	35280	70560	141120	282240	564480
100100110	17700	35400	70800	141600	283200	566400
100100111	17760	35520	71040	142080	284160	568320
100101000	17820	35640	71280	142560	285120	570240
100101001	17880	35760	71520	143040	286080	572160
100101010	17940	35880	71760	143520	287040	574080
100101011	18000	36000	72000	144000	288000	576000
100101100	18060	36120	72240	144480	288960	577920
100101101	18120	36240	72480	144960	289920	579840
100101110	18180	36360	72720	145440	290880	581760
100101111	18240	36480	72960	145920	291840	583680
100110000	18300	36600	73200	146400	292800	585600
100110001	18360	36720	73440	146880	293760	587520
100110010	18420	36840	73680	147360	294720	589440
100110011	18480	36960	73920	147840	295680	591360
100110100	18540	37080	74160	148320	296640	593280
100110101	18600	37200	74400	148800	297600	595200
100110110	18660	37320	74640	149280	298560	597120
100110111	18720	37440	74880	149760	299520	599040
100111000	18780	37560	75120	150240	300480	600960
100111001	18840	37680	75360	150720	301440	602880
100111010	18900	37800	75600	151200	302400	604800

	PWM Frequency[Hz]					
BL_DIMMSTEP [2:0]	**000**	**001**	**010**	**011**	**100**	**101**
Dimming Step No.	**1024**	**512**	**256**	**128**	**64**	**32**
100111011	18960	37920	75840	151680	303360	606720
100111100	19020	38040	76080	152160	304320	608640
100111101	19080	38160	76320	152640	305280	610560
100111110	19140	38280	76560	153120	306240	612480
100111111	19200	38400	76800	153600	307200	614400
101000000	19260	38520	77040	154080	308160	616320
101000001	19320	38640	77280	154560	309120	618240
101000010	19380	38760	77520	155040	310080	620160
101000011	19440	38880	77760	155520	311040	622080
101000100	19500	39000	78000	156000	312000	624000
101000101	19560	39120	78240	156480	312960	625920
101000110	19620	39240	78480	156960	313920	627840
101000111	19680	39360	78720	157440	314880	629760
101001000	19740	39480	78960	157920	315840	631680
101001001	19800	39600	79200	158400	316800	633600
101001010	19860	39720	79440	158880	317760	635520
101001011	19920	39840	79680	159360	318720	637440
101001100	19980	39960	79920	159840	319680	639360
101001101	20040	40080	80160	160320	320640	641280
101001110	20100	40200	80400	160800	321600	643200
101001111	20160	40320	80640	161280	322560	645120
101010000	20220	40440	80880	161760	323520	647040
101010001	20280	40560	81120	162240	324480	648960
101010010	20340	40680	81360	162720	325440	650880
101010011	20400	40800	81600	163200	326400	652800

5.2.4.3 BL_MODE_IN_SLP

This register is used to select the state of PWM when driver IC is sleep in mode.

Table 112 BL_MODE_IN_SLP

BL_MODE_IN_SLP	State of PWM
0	Low
1	High

Status	Default Value
Initial	BL_MODE_IN_SLP = 0

Table 113 State of PWM

Pin	State					
	Hard Reset	SW Reset	SLPIN		SPLOUT	
			Display On	Display Off	Display On	Display Off
BC	Low	Low	Fixed as BL_MODE_IN_SLP		Active	Low

5.2.4.4 BL_DRV_EN

This register is used to enable the LED driver IC when the IC needs the chip enable signal.

Table 114 BL_DRV_EN

BL_DRV_EN	State of BC_CTL Pin
0	Low
1	High

Status	Default Value
Initial	BL_DRV_EN = 0

5.2.4.5 DT [2:0]

This register is used to select the transition time of the manual dimming function.

Table 115 DT [2:0]

DT[2:0]	Transition Time	Dimming Step
000	16 frames	16
001	24 frames	24
010	32 frames	32
011	40 frames	40
100	48 frames	48
101	56 frames	56
110	64 frames	64
111	72 frames	72

Transition Time of Manual Dimming Function

$$\text{Transition\_time} = (\text{DT [2:0]} + 2) \times 8 \times \frac{1}{\text{Display\_Frequency}}$$

Status	Default Value
Initial	DT[2:0] = 001

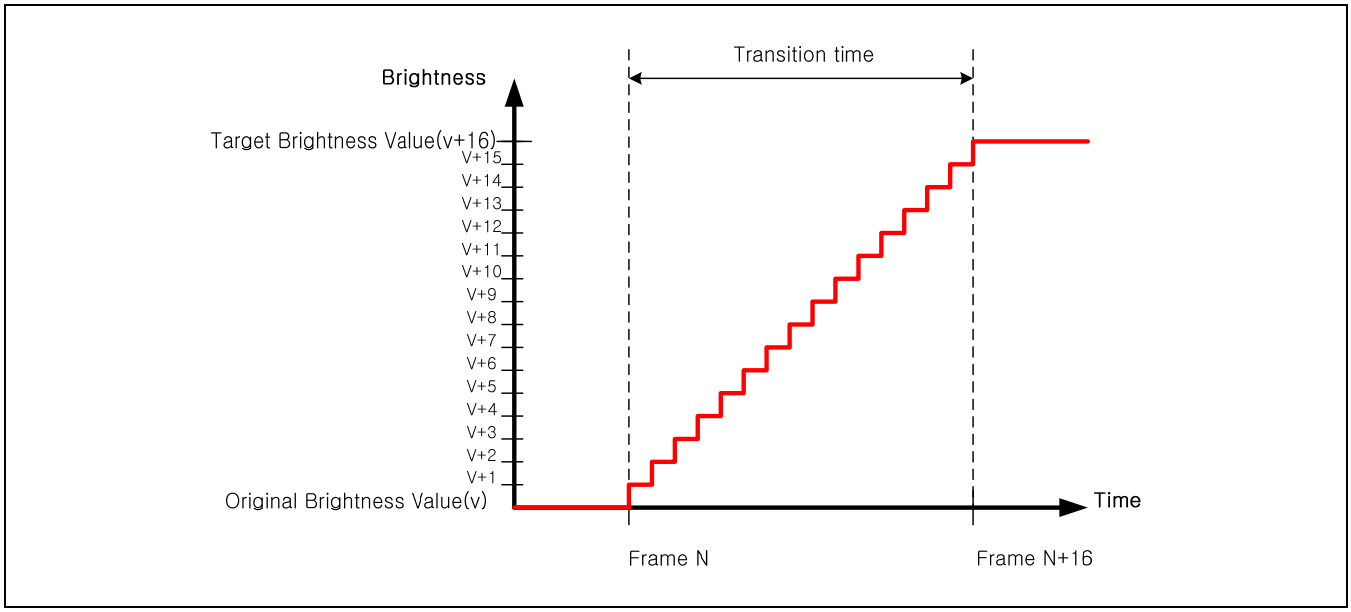


Figure 185 Example of Dimming Function (DT[2:0] = 000)

5.2.5 MTPCTL (D0H)

D0h	MTPCTL (MTP control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	0	0	D0
Parameter	1	1	↑	0	MTP_ MODE	MTP_ EX	0	MTP_ SEL	MTP_ WRB	MTP_ ERB	MTP_ LOAD	0E

This command is used to control MTP.
MTP initial operation is advanced after set both MTP Test Key Command is enable.

5.2.5.1 MTP_MODE

: Set the 2nd booster operating condition.

- MTP_MODE = 0: The 2nd booster operates as a user-specified condition. VGH/VGL voltages are generated as a designated level by BT [2:0] setting.
- MTP_MODE = 1: Available BT [2:0] settings are limited only '010'.

MTP_MODE	MTP operation mode
0	All BT[2:0] settings are available (Normal operating condition)
1	Setting of BT[2:0] is limited. (An MTP-programming / erasing condition)

NOTE: Do not execute MTP programming / erasing operation when MTP_MODE = 0.

5.2.5.2 MTP_EX

: Select MTP power supply source.

- When MTP_EX = 0, Internally generated VGH voltage is used as a MTP-programming / erasing potential.
- If MTP_EX = 1, External power should be applied for programming / erasing MTP via VGH pad.

MTP_EX	Erase / Initial / Program supply
0	Used internally generated VGH
1	Needed external power supply

NOTE: MTP_EX register is valid only in case that MTP_MODE = 1. Do not access MTP_EX register when MTP_MODE = 0.

5.2.5.3 MTP_SEL

: This command is to select MTP value or register value.

- MTP_SEL = “0”: select ID1[7:0],ID2[7:0],ID3[7:0], VCMOC_PO, VCMOC[4:0], VMLOC_PO, VMLOC[3:0], GVDOC_PO, GVDOC[3:0] from pre-register value.
- MTP_SEL = “1”: select ID1[7:0],ID2[7:0],ID3[7:0], VCMOC_PO, VCMOC[4:0], VMLOC_PO, VMLOC[3:0], GVDOC_PO, GVDOC[3:0] from post-register(loaded data from MTP) value.

5.2.5.4 MTP_WRB

: This command is used to MTP programming

- MTP_WRB = “0”: MTP writing enable.
- MTP_WRB = “1”: MTP writing disable.

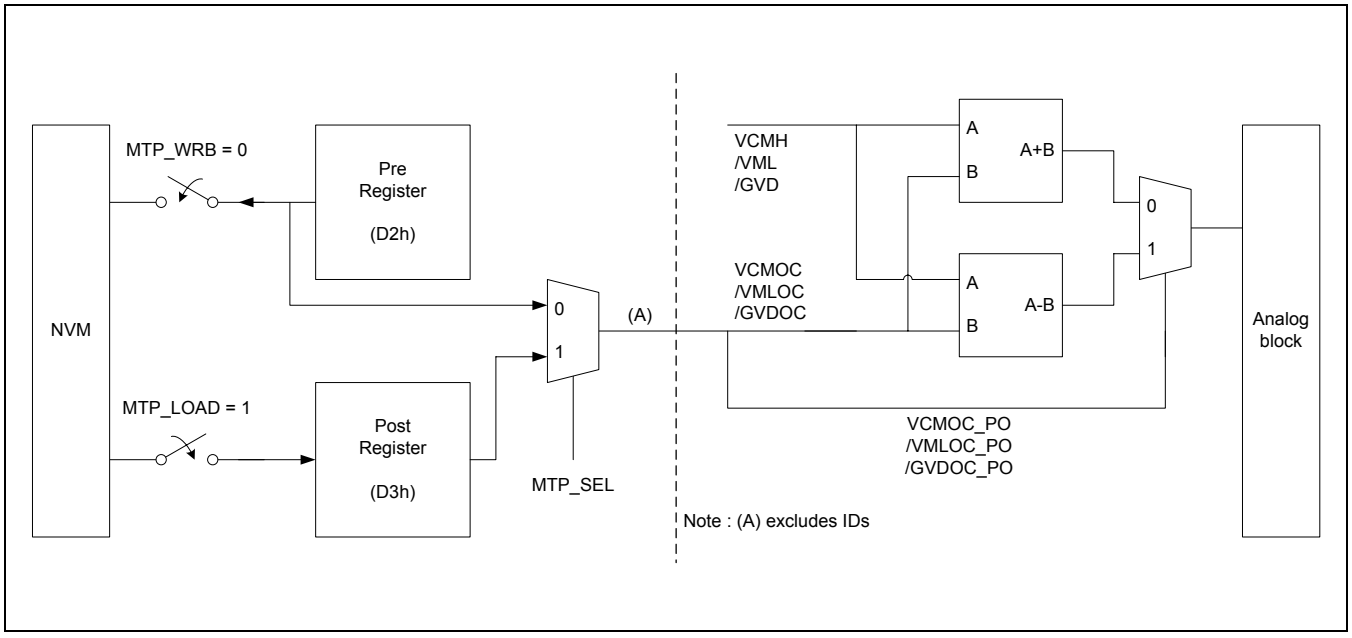


Figure 186 MTP Access Block Diagram

5.2.5.5 MTP_ERB

: This command is a setting for using MTP Data Initialization or Erase.

- Setting MTP_ERB = “0”: MTP Data Initialization or Erase Enable.
- Setting MTP_ERB = “1”: MTP Data Initialization or Erase Disable.

5.2.5.6 MTP_LOAD

: This command is a setting for using MTP data load from MTP to post-register.

- Setting MTP_LOAD = “0”: MTP data load disable.
- Setting MTP_LOAD = “1”: MTP data load enable.

Status	Default Value
Initial	MTP_MODE = 0, MTP_EX=0, MTP_SEL=1, MTP_WRB=1, MTP_ERB=1, MTP_LOAD=0

5.2.6 MTPWR (D2H)

D2h	MTPWR											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	1	0	D2
1st Parameter	1	↑	1	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	00
2nd Parameter	1	↑	1	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	00
3rd Parameter	1	↑	1	ID3 [7]	ID3 [6]	ID3 [5]	ID3 [4]	ID3 [3]	ID3 [2]	ID3 [1]	ID3 [0]	00
4th Parameter	1	↑	1	0	0	VCMOC_PO	VCMOC [4]	VCMOC [3]	VCMOC [2]	VCMOC [1]	VCMOC [0]	00
5th Parameter	1	↑	1	0	0	0	VMLOC_PO	VMLOC [3]	VMLOC [2]	VMLOC [1]	VMLOC [0]	00
6th Parameter	1	↑	1	0	0	0	GVDOC_PO	GVDOC [3]	GVDOC [2]	GVDOC [1]	GVDOC [0]	00

This command is the pre-register that will be written to MTP.

5.2.6.1 ID1 [7:0]

This byte is the LCD module's manufacturer.

5.2.6.2 ID2 [7:0]

This byte is the LCD module / driver version ID.

5.2.6.3 ID3 [7:0]

This byte is the LCD module/driver.

Status	Default Value
Intial	ID1 = 00 / ID2 = 00 / ID3 = 00

5.2.6.4 VCMOC_PO/VCMOC [4:0]

VCMOC[4:0] contains VCM Offset data. This MTP data and VCM register determine VCOMH level.
TOTAL_VCM[6:0] = VCM[6:0](NVCMH or IPVCMH) + VCMOC_PO/VCMOC[4:0]

Table 116 VCMOC_PO/VCMOC [4:0]

VCMOC_PO, VCMOC [4:0]	VCM_OFFSET	VCMOC_PO, VCMOC [4:0]	VCM_OFFSET
000000	0	100000	0
000001	+1	100001	-1
000010	+2	100010	-2
000011	+3	100011	-3
000100	+4	100100	-4
000101	+5	100101	-5
000110	+6	100110	-6
000111	+7	100111	-7
001000	+8	101000	-8
001001	+9	101001	-9
001010	+10	101010	-10
001011	+11	101011	-11
001100	+12	101100	-12
001101	+13	101101	-13
001110	+14	101110	-14

VCMOC_PO, VCMOC [4:0]	VCM_OFFSET	VCMOC_PO, VCMOC [4:0]	VCM_OFFSET
001111	+15	101111	-15
010000	+16	110000	-16
010001	+17	110001	-17
010010	+18	110010	-18
010011	+19	110011	-19
010100	+20	110100	-20
010101	+21	110101	-21
010110	+22	110110	-22
010111	+23	110111	-23
011000	+24	111000	-24
011001	+25	111001	-25
011010	+26	111010	-26
011011	+27	111011	-27
011100	+28	111100	-28
011101	+29	111101	-29
011110	+30	111110	-30
011111	+31	111111	-31

NOTE: TOTAL_VCM[6:0] cannot be set to the value above “1111111” or below “0000000,” that is, 128 ≥ VCM[6:0] + VCMOC_PO/VCMOC[4:0] ≥ 0.

For example, if VCM[6:0] = “1001101”(4.0V and VCMOC_PO/VCMOC[4:0] = 100011 are selected, then VCM_OFFSET is “-3,” which results in VCOM high level voltage = 3.94V from NVCMH[6:0]/NPIVCMH[6:0] table.

Status	Default Value
Initial	VCMOC_PO=0, VCMOC[4:0] = 00000

5.2.6.5 VMLOC_PO/VMLOC [3:0]

VMLOC [3:0] contain VCOM amplitude Offset data. This MTP data and VML register determine VCOML amplitude. TOTAL_VML [6:0] = VML [6:0](NVML or PIVML) + VMLOC_PO/VMLOC[3:0].

Table 117 VMLOC_PO/VMLOC [3:0]

VMLOC_PO / VMLOC [3:0]	VML_OFFSET	VMLOC_PO / VMLOC [3:0]	VML_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10
01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

NOTE: TOTAL_VML[6:0] cannot be set to the value above “1110101” or below “0000000,” that is, 117 ≥ VML[6:0] + VMLOC_PO/VMLOC[3:0] ≥ 0.

For example, if VML[6:0] = 0101011 and VMLOC_PO/VMLOC[3:0] = 10001 are selected, then VML_OFFSET is “-1,” and therefore TOTAL_VML[6:0] is “0101010,” which results in VCOM amplitude voltage = 4.125V from NVML[6:0]/PIVML[6:0] table.

Status	Default Value
Initial	VMLOC_PO=0, VMLOC[3:0] = 0000

5.2.6.6 GVDOC_PO/GVDOC [3:0]

GVDOC [3:0] contains GVD Offset data. This MTP data and GVD register determine GVDD level.
TOTAL_GVD [6:0] = GVD [6:0](NGVD or PIGVD) + GVDOC_PO/GVDOC[3:0].

Table 118 GVDOC_PO/GVDOC[3:0]

GVDOC_PO / GVDOC [3:0]	GVD_OFFSET	GVDOC_PO / GVDOC [3:0]	GVD_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10
01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

NOTE: TOTAL_GVD[6:0] cannot be set to the value above “1111111” or below “0000000,” that is, 127 ≥ GVD[6:0] + GVDOC_PO/GVDOC[3:0] ≥ 0.

For example, if GVD[6:0] = 0101011 and GVDOC_PO/GVDOC[3:0] = 10010 are selected, then MTP_OFFSET is “-2,” and therefore TOTAL_GVD[6:0] is “0101001,” which results in GVDD voltage = 3.28V from NGVD[6:0]/PIGVD[6:0] table.

Status	Default Value
Initial	GVDOC_PO=0, GVDOC[3:0] = 0000

5.2.7 MTPRD (D3H)

D3h	MTPRD											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	1	1	D3
1st Parameter	1	↑	1	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	xx
2nd Parameter	1	↑	1	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	xx
3rd Parameter	1	↑	1	ID3 [7]	ID3 [6]	ID3 [5]	ID3 [4]	ID3 [3]	ID3 [2]	ID3 [1]	ID3 [0]	xx
4th Parameter	1	↑	1	1	0	VCMOC_PO	VCMOC [4]	VCMOC [3]	VCMOC [2]	VCMOC [1]	VCMOC [0]	xx
5th Parameter	1	↑	1	0	1	0	VMLOC_PO-	VMLOC [3]	VMLOC [2]	VMLOC [1]	VMLOC [0]	xx
6th Parameter	1	↑	1	1	1	0	GVDOC_PO	GVDOC [3]	GVDOC [2]	GVDOC [1]	GVDOC [0]	xx

NOTE:

1. After MTP program, MTPRD result is like upper table. In case of MTP Initialization or Erase, the result has all "0" value.

2. When SPI, this command is not supported.

5.2.7.1 ID1 [7:0]

This read byte identifies the LCD module's manufacturer.

5.2.7.2 ID2 [7:0]

This read byte identifies the LCD module / driver version ID.

5.2.7.3 ID3 [7:0]

This read byte identifies the LCD module/driver.

5.2.7.4 VCMOC_PO/VCMOC [4:0]

This is to read VCMOC_PO/VCMOC[4:0]

5.2.7.5 VMLOC_PO/VMLOC [3:0]

This is to read VMLOC_PO/VMLOC[3:0]

5.2.7.6 GVDOC_PO/GVDOC [3:0]

This is to read GVDOC_PO/GVDOC[3:0]

5.2.8 DSTB (DFH)

DFh	DSTB											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	1	1	DF
Parameter	1	1	↑	0	0	0	0	0	0	0	DSTB	00

When DSTB = 1, the S6D05A1 enters the deep standby mode, where the power supply for the internal logic is off to save more power than the sleep mode. The GRAM data and the instruction sets are prohibited during the deep standby mode and they must be reset after releasing from the deep standby mode.

Table 119 DSTB

DSTB	State
0	Deep Standby Off
1	Deep Standby In

Status	Default Value
Initial	DSTB = 0

5.2.9 MDDICTL : MDDI CONTROL (EAH)

EAh	MDDICTL											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	1	0	EA
Parameter	1	1	↑	0	0	0	0	0	0	MDDI_ SLP	VWAK E_EN	00

5.2.9.1 MDDI_SLP/VWAKE_EN

- **MDDI_SLP:** When MDDI_SLP is high, MDDI Operating State is STOP state.
  To release STOP state, input reset(RESX) signal.
- **VWAKE_EN:** When VWAKE_EN is 1, client initiated wake-up is enabled

Status	Default Value
Initial	MDDI_SLP=0 VWAKE_EN=0

5.2.10 MDDILIK: MDDI LINK WAKE-UP START POSITION (EBH)

EBh	MDDILIK											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	1	1	EB
1st Parameter	1	1	↑	WKL [9]	WKL [8]	WKL [7]	WKL [6]	WKL [5]	WKL [4]	WKL [3]	WKL [2]	00
2nd Parameter	1	1	↑	WKL [1]	WKL [0]	WKF [3]	WKF [2]	WKF [1]	WKF [0]	0	0	00

5.2.10.1 WKL [9:0] / WKF [3:0]

- WKL[9:0]: The registers for defining at which number of line the client-initiated wakeup would start. If WKL is updated to '000h', client-initiated wakeup starts automatically at the first line after vertical front porch. The range of WKL is from '000h' to '3DBh'.
- WKF[3:0]: The registers for defining after which number of frame the client-initiated wake up would start. If WKF is updated to '0000' client-initiated wake up starts at the start of next frame, and if '1111', wake up starts after 16th frame.

Setting of WKF and WKL works together for client-initiated wake up.
For example, If WKF is '0011' and WKL is '003h', VBP is ‘03h’,
Wake up starts at the first display line of third frame.

Status	Default Value
Initial	WKL[9:0]=00_0000_0000 WKF[3:0]=0000

5.2.11 PASSWD1 (F0H)

F0h	Password command for level 2(except DSTB and MTP)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	0	F0
1st Parameter	1	1	↑	TEST_KEY1[15]	TEST_KEY1[14]	TEST_KEY1[13]	TEST_KEY1[12]	TEST_KEY1[11]	TEST_KEY1[10]	TEST_KEY1[9]	TEST_KEY1[8]	A5
2nd Parameter	1	1	↑	TEST_KEY1[7]	TEST_KEY1[6]	TEST_KEY1[5]	TEST_KEY1[4]	TEST_KEY1[3]	TEST_KEY1[2]	TEST_KEY1[1]	TEST_KEY1[0]	A5

When the Parameter (TEST_KEY[15:0]) of this command is inputted by 5A5Ah, this command enable Level2 command input(except DSTB and MTP).

Status	Default Value
Initial	TEST_KEY1[15:8]=8’b10100101(A5h) TEST_KEY1[7:0]=8’b10100101(A5h)

5.2.12 PASSWD2 (F1H)

F1h	Password command for level 2(DSTB, MTP only)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	1	F1
1st Parameter	1	1	↑	TEST_KEY2[15]	TEST_KEY2[14]	TEST_KEY2[13]	TEST_KEY2[12]	TEST_KEY2[11]	TEST_KEY2[10]	TEST_KEY2[9]	TEST_KEY2[8]	A5
2nd Parameter	1	1	↑	TEST_KEY2[7]	TEST_KEY2[6]	TEST_KEY2[5]	TEST_KEY2[4]	TEST_KEY2[3]	TEST_KEY2[2]	TEST_KEY2[1]	TEST_KEY2[0]	A5

When the Parameter (TEST_KEY[15:0]) of this command is inputted by 5A5Ah, this command enable DSTB and MTP command input.

Status	Default Value
Initial	TEST_KEY2[15:8]=8'b10100101(A5h) TEST_KEY2[7:0]=8'b10100101(A5h)

5.2.13 DISCTL (F2H)

F2h	DISCTL (Display Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	1	0	F2
1st Parameter	1	1	↑	0	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	3B
2nd Parameter	1	1	↑	0	NHW [6]	NHW [5]	NHW [4]	NHW [3]	NHW [2]	NHW [1]	NHW [0]	40
3rd Parameter	1	1	↑	0	0	0	0	PIINV	IINV	PINV	NINV	03
4th Parameter	1	1	↑	NVBP [7]	NVBP [6]	NVBP [5]	NVBP [4]	NVBP [3]	NVBP [2]	NVBP [1]	NVBP [0]	08
5th Parameter	1	1	↑	NVFP [7]	NVFP [6]	NVFP [5]	NVFP [4]	NVFP [3]	NVFP [2]	NVFP [1]	NVFP [0]	08
6th Parameter	1	1	↑	0	0	0	0	1	0	0	0	08
7th Parameter	1	1	↑	0	0	0	0	1	0	0	0	08
8th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
9th Parameter	1	1	↑	0	0	0	0	1	0	0	0	08
10th Parameter	1	1	↑	0	0	TE_INV	0	1	0	0	0	08
11th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
12th Parameter	1	1	↑	0	0	0	0	0	SM	GS	REV	00
13th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
14th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
15th Parameter	1	1	↑	0	PIHW [6]	PIHW [5]	PIHW [4]	PIHW [3]	PIHW [2]	PIHW [1]	PIHW [0]	40
16th Parameter	1	1	↑	PIVB P [7]	PIVB P [6]	PIVB P [5]	PIVB P [4]	PIVB P [3]	PIVB P [2]	PIVB P [1]	PIVB P [0]	08
17th Parameter	1	1	↑	PIVF P [7]	PIVF P [6]	PIVF P [5]	PIVF P [4]	PIVF P [3]	PIVF P [2]	PIVF P [1]	PIVF P [0]	08
18th Parameter	1	1	↑	RGB_ NVBP [7]	RGB_ NVBP [6]	RGB_ NVBP [5]	RGB_ NVBP [4]	RGB_ NVBP [3]	RGB_ NVBP [2]	RGB_ NVBP [1]	RGB_ NVBP [0]	08
19th Parameter	1	1	↑	RGB_ NVFP [7]	RGB_ NVFP [6]	RGB_ NVFP [5]	RGB_ NVFP [4]	RGB_ NVFP [3]	RGB_ NVFP [2]	RGB_ NVFP [1]	RGB_ NVFP [0]	08

5.2.13.1 NL [5:0]

: Set the display duty. The total number of scan line can be set.

Table 120 NL [5:0]

NL[5:0]	Total number of scan line
000000	Setting disabled
…	
000010	
011101	240
011110	248
…	…
111010	472
111011	480
111100~111111	Setting disabled

Status	Default Value
Initial	NL[5:0] = 111011 (480)

NOTE: ML (MADCTL D4) setting low when Display size < 480.

5.2.13.2 NHW [7:0] /PIHW [7:0]

: Set the horizontal clock (CL1) period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. In the case of MPU interface mode.

Table 121 NHW [6:0] / PIHW [6:0]

*HW[6:0]	Number of INCLK
0000000~0101100	Setting disabled
0101101	45
0101110	46
…	…
1111101	125
1111110	126
1111111	127

NOTE: OSCK is the internal oscillator clock. INCLK is the divided clock of the OSCK for Display Control. INCLK = OSCK / 8.

Status	Default Value
Initial	NHW[6:0]=1000000 (64) PIHW[6:0]=1000000 (64)

5.2.13.3 NINV / PINV / IINV / PIINV

: Select the panel driving method in the Normal mode / Partial mode / Idle mode / Partial-Idle mode respectively. Either frame inversion method or line inversion method can be selected.

Table 122 NINV / PINV / IINV / PIINV

*INV	Panel driving method
0	Frame inversion
1	Line inversion

Status	Default Value
Initial	NINV, PINV = 1 IINV, PIINV = 0

NOTE: Non-display area is (porch + non display area) when partial mode.

5.2.13.4 NVBP [7:0] / PIVBP [7:0]

: Set the vertical back-porch period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. Use in the case of MPU interface mode and in the self-refresh mode of external RGB interface mode(SELF_REF=1).

Table 123 NVBP [7.0] / PIVBP [7.0]

*VBP[7:0]	Number of Horizontal Line
00000000	Setting disable
00000001	Setting disable
00000010	Setting disable
00000011	Setting disable
00000100	4
…	…
11111101	253
11111110	254
11111111	255

Status	Default Value
Initial	*BP[7:0] = 00001000 (8)

NOTE: Refer to the frame frequency adjusting function (4.4.2)'s formula and example in case of self refresh mode.

5.2.13.5 NVFP [7:0]/ PIVFP [7:0]

: Set the vertical front-porch period in the Normal mode, Partial mode, Idle mode / Partial-Idle mode, respectively. Use in the case of MPU interface mode and in self-refresh mode of external RGB interface mode (SELF_REF=1).

Table 124 NVFP[7:0]/PIVFP[7:0]

*VFP[7:0]	Number of Horizontal Line
00000000	Setting disable
00000001	Setting disable
00000010	2
…	…
11111101	253
11111110	254
11111111	255

Status	Default Value
Initial	*FP[7:0] = 00001000 (8)

5.2.13.6 RGB_NVBP[7:0]

: Set the vertical back-porch period in the Normal mode, Idle mode. Use in the case of external RGB interface mode (SELF_REF=0).

5.2.13.7 RGB_NVFP[7:0]

: Set the vertical front-porch period in the Normal mode, Idle mode. Use in the case of external RGB interface mode (SELF_REF=0).

5.2.13.8 TE_INV

: When TE_INV=1, TE signal is inverted. Default value is 0.

5.2.13.9 SM/GS/REV

- SM: Select the division drive method of the gate driver. When SM=0, even/odd division is selected; SM =1, upper/lower division drive is selected by (total gate line)/2 and (total gate line)/2. Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.
- GS: Set the order of Gate Clock generation. When GS = 0 (NL=6'b111011, SCN=5'b00000, SM=0), the order of GATE_ON is from G1 to G480, and then GS = 1 (NL=6'b111011, SCN=5'b00000,SM=0), from G480 to G1. Gate start position and Gate scan order are changed by GS/NL/SCN/SM.

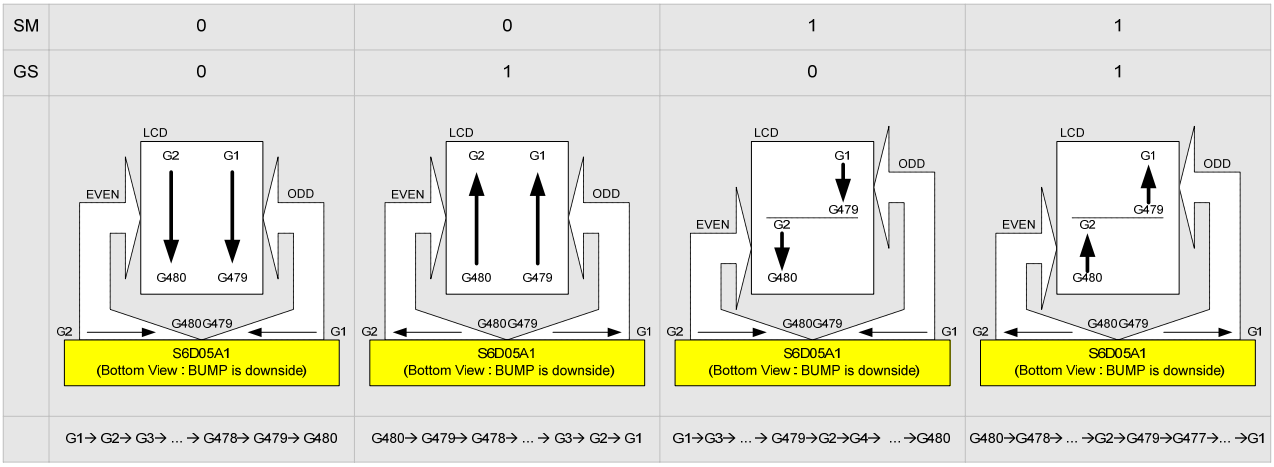


Figure 187 Gate Clock Generation Order Selection Using GS and SM (NL=6'b111011, SCN=5'b00000)

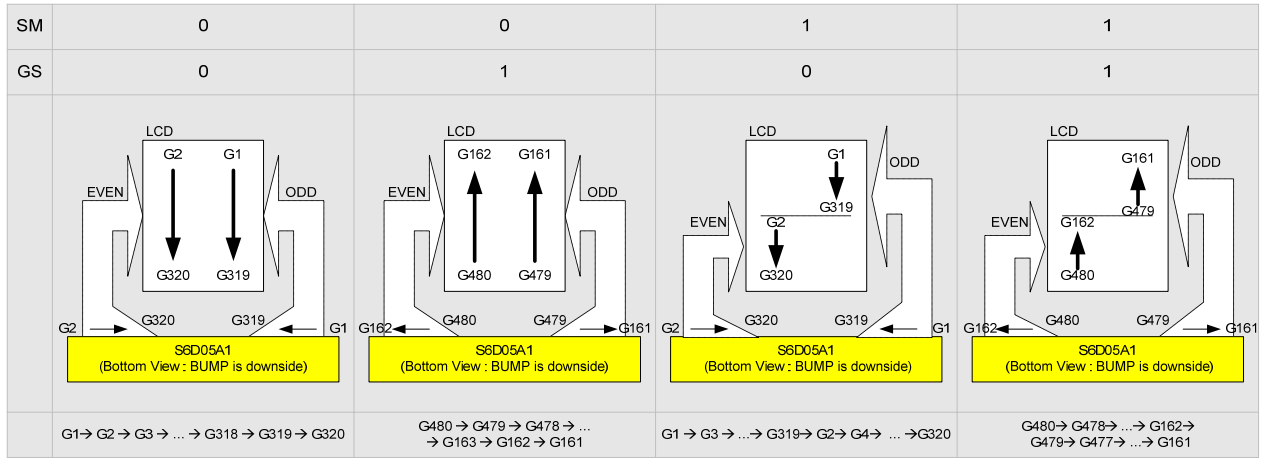


Figure 188 Gate Clock Generation Order Selection Using GS and SM (NL=6'b100111, SCN=5'b00000)

- REV: Display all character and graphics display sections with reversal when REV=1.

Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

Table 125 REV

REV	Liquid Crystal Type	GRAM Data	Display Area	
			Positive	Negative
0	Normally black	8'b000000 : 8'b111111	V255 : V0	V0 : V255
1	Normally white	8'b000000 : 8'b111111	V0 : V255	V255 : V0

Status	Default Value
Initial	GS=0 SM=0 REV = 0

5.2.14 MANPWRSEQ (F3H)

F3h	MANPWRSEQ (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	1	1	F3
1st Parameter	1	1	↑	0	0	0	0	0	0	DISP_SEL	APON	03
2nd Parameter	1	1	↑	VCL_EN	VGL_EN	VGH_EN	0	AVDD11_EN	VCI1_2ND_EN	VCI1_1ST_EN	0	00
3rd Parameter	1	1	↑	0	0	0	GATE_ON	VCIVCI1_EN	OPA_EN	0	AVDD21_EN	00
4th Parameter	1	1	↑	0	0	AVDD22_EN	AVDD12_EN	0	VGHFREE1_EN	VGHFREE2_EN	VGLFREE_EN	00
5th Parameter	1	1	↑	0	0	0	0	0	0	D[1]	D[0]	00

5.2.14.1 DISP_SEL

: This is the command for the selection of display control method.

- When DISP_SEL=0, DISPON/DISPOFF commands are no operation.
- When DISP_SEL=1, D[1:0] commands are no operation.

DISP_SEL	Display Control Command
0	D[1:0]
1	DISPON, DISPOFF

Status	Default Value
Initial	DISP_SEL = 1

5.2.14.2 APON

: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the automatic boosting sequence starter is halted and the booster circuits are operated independently by AVDD_EN, VGH_EN, VGL_EN and VCL_EN bits. In case of APON=1, booster circuits are operated automatically and sequentially.

Status	Default Value
Initial	APON = 1

5.2.14.3 VCI1_1ST_EN/VCI1_2ND_EN

: Internal VCI1 generation amplifier operation control bit. When VCI1_1ST_EN=0, VCI1 voltage is not generated. VCI1_2ND_EN signal is to strengthen the VCI1 amp's current driving capability.

Status	Default Value
Initial	VCI1_1ST_EN = 0, VCI1_2ND_EN = 0

5.2.14.4 AVDD11_EN/AVDD12_EN

: This is an operation-starting bit for the booster circuit1 for source driver. In case of AVDD11_EN =AVDD12_EN= 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the AVDD11_EN =AVDD12_EN= 1

Status	Default Value
Initial	AVDD11_EN = 0, AVDD12_EN=0

5.2.14.5 AVDD21_EN/AVDD22_EN

: This is an operation-starting bit for the booster circuit1 for 2nd/3rd booster, VCOM driver, VCOMH and GVDD Amp. In case of AVDD21_EN =AVDD22_EN= 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the AVDD21_EN =AVDD22_EN= 1

Status	Default Value
Initial	AVDD21_EN = 0, AVDD22_EN=0

5.2.14.6 VGH_EN

: This is an operation-starting bit for the booster circuit 2(VGH). In case of VGH_EN, the circuit is stopped and vice versa. For further information about timing for adjusting to the VGH_EN= 1.

Status	Default Value
Initial	VGH_EN = 0

5.2.14.7 VGHFREE1_EN

: This is a schottky diode free mode bit for the booster circuit 2(VGH). Reardless of external schottky diode, this command is to be ordered according to the setup flow of power.

Status	Default Value
Initial	VGHFREE1_EN = 0

5.2.14.8 VGHFREE2_EN

: This is a schottky diode free mode bit for the booster circuit 2(VGH). Reardless of external schottky diode, this command is to be ordered according to the setup flow of power.

Status	Default Value
Initial	VGHFREE2_EN = 0

5.2.14.9 VGL_EN

: This is an operation-starting bit for the booster circuit 2(VGL). In case of VGL_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the VGL_EN = 1.

Status	Default Value
Initial	VGL_EN = 0

5.2.14.10 VGLFREE_EN

: This is a schottky diode free mode bit for the booster circuit 2(VGL). Reardless of external schottky diode, this command is to be ordered according to the setup flow of power.

Status	Default Value
Initial	VGLFREE_EN = 0

5.2.14.11 VCL_EN

: This is an operation-starting bit for the booster circuit 3(VCL). In case of VCL_EN = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the VCL_EN= 1.

Status	Default Value
Initial	VCL_EN = 0

5.2.14.12 VCIVCI1_EN

: Set VCI1 output equal to VCI. VCI1 output is internally connected to VCI via switching circuit when VCIVCI1_EN=1

Status	Default Value
Initial	VCIVCI1_EN =0

5.2.14.13 OPA_EN

: This is an operation-starting bit for GVDD/VCOMH/VCOML amplifiers. In case of OPA_EN = 0, the amplifier circuits are stopped. On the other hand, the operation of the amplifiers is getting started when OPA_EN = 1.

Status	Default Value
Initial	OPA_EN = 0

5.2.14.14 GATE_ON

: This is a gate on/off control signal. All gate outputs are set to be gate off level when GATE_ON = 0.
When GATE_ON = 1, gate driver is working: G1 to G480 output is either VGH or VGL level.
When APON = 1, GATE_ON setting is ignored.

Status	Default Value
Initial	GATE_ON = 0

5.2.14.15 D[1:0]

D: When APON = 0 and DISP_SEL = 0, Display Status is controled by D [1:0] and GATE_ON, Please refer Following Table,

Table 126 D [1:0]

Register		Chip Operation			Display Status
D	GATE_ON	SOURCE	VCOM	GATE	
00	X	AVSS	AVSS	AVSS	Halt
01	0	AVSS	AVSS	VGL	Halt
01	1	AVSS	AVSS	Operate	Blank Display
10	0	Operate (Same Phase of VCOM)	Operate	VGL	Halt
10	1	Operate (Same Phase of VCOM)	Operate	Operate	Blank Display
11	0	Operate (GRAM Data)	Operate	VGL	Halt
11	1	Operate (GRAM Data)	Operate	Operate	GRAM Display

Status	Default Value
Initial	GATE_ON=0 D[1:0]=00

When APON = 1 and DISP_SEL = 1, Please refer Following Table for Display Control
In this condition, D[1:0] and GATE_ON setting is ignored.

Table 127 Display Control and Chip Operation, when DISP_SEL is High,

Register				Chip Operation			Display Status	Boosting Status
SLP IN	SLP OUT	DISP ON	DISP OFF	SOURCE	VCOM	GATE		
ON	OFF	X	X	AVSS	AVSS	AVSS	Halt	OFF
OFF	ON	OFF	ON	AVSS	AVSS	AVSS	Halt	ON
OFF	ON	ON	OFF	Operate (GRAM Data)	Operate	Operate	GRAM Display	ON

NOTE: APON=1&DISP_SEL=0, APON=0&DISP_SEL=1 is a setting disable condition.

5.2.15 PWRCTL (F4H)

F4h	PWRCTL (Power Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	0	0	F4
1st Parameter	1	1	↑	0	0	0	0	VC [3]	VC [2]	VC [1]	VC [0]	00
2nd Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
3rd Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
4th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
5th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
6th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
7th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
8th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
9th Parameter	1	1	↑	0	0	NDC 3 [1]	NDC 3 [0]	NDC 2 [1]	NDC 2 [0]	NDC 1 [1]	NDC 1 [0]	04
10th Parameter	1	1	↑	0	NGV D [6]	NGV D [5]	NGV D [4]	NGV D [3]	NGV D [2]	NGV D [1]	NGV D [0]	00
11th Parameter	1	1	↑	0	0	0	0	0	NBT [2]	NBT [1]	NBT [0]	02
12th Parameter	1	1	↑	0	0	PIDC 3 [1]	PIDC 3 [0]	PIDC 2 [1]	PIDC 2 [0]	PIDC 1 [1]	PIDC 1 [0]	04
13th Parameter	1	1	↑	0	PIGV D [6]	PIGV D [5]	PIGV D [4]	PIGV D [3]	PIGV D [2]	PIGV D [1]	PIGV D [0]	00
14th Parameter	1	1	↑	0	0	0	0	0	PIBT [2]	PIBT [1]	PIBT [0]	02

5.2.15.1 VC [3:0]

: This register is used to set the VCI1 voltage. These bits set the VCI1 voltage up to 3V as the nominal output (upper limit value may depend on VCI voltage)

Table 128 VC [3:0]

VC3	VC2	VC1	VC0	VCI1
0	0	0	0	2.10
0	0	0	1	2.16
0	0	1	0	2.22
0	0	1	1	2.28
0	1	0	0	2.34
0	1	0	1	2.40
0	1	1	0	2.46
0	1	1	1	2.52
1	0	0	0	2.58
1	0	0	1	2.64
1	0	1	0	2.70
1	0	1	1	2.76
1	1	0	0	2.82
1	1	0	1	2.88
1	1	1	0	2.94
1	1	1	1	3.00

NOTE: Do not set any higher VCI1 level than VCI -0.15V.

Status	Default Value
Initial	VC[3:0] = 0000

5.2.15.2 NDC3 [1:0] / PIDC3 [1:0]

: The operating frequency in the booster circuit 3 is selected. PIDC3 is applied in Idle Partial mode.

Table 129 NDC3 [1:0] / PIDC3 [1:0]

NDC31/ PIDC31	NDC30/ PIDC30	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK3)
0	0	1:2
0	1	1:1
1	0	1:0.5
1	1	1:0.25

NOTE: DCCLK3 is pumping clock for booster circuit 3

Status	Default Value
Initial	NDC3[1:0], PIDC3[1:0] = 00

5.2.15.3 NDC2 [1:0] / PIDC2 [1:0]

: The operating frequency in the booster circuit 2 is selected. PIDC2 is applied in Idle Partial mode.

Table 130 NDC2 [1:0] / PIDC2 [1:0]

NDC21/PIDC21	DC20/PIDC20	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK2)
0	0	1:2
0	1	1:1
1	0	1:0.5
1	1	1:0.25

NOTE: DCCLK2 is pumping clock for booster circuit 2

Status	Default Value
Initial	NDC2[1:0], PIDC2[1:0] = 01

5.2.15.4 NDC1 [1:0] / PIDC1 [1:0]

: The operating frequency in the booster circuit1 is selected. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption. PIDC1 is applied in Idle Partial mode.

Table 131 NDC1 [1:0] / PIDC1 [1:0]

NDC11/PIDC11	NDC10/PIDC10	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK1)
0	0	1:2
0	1	1:1
1	0	1:0.5
1	1	1:0.25

NOTE: DCCLK1 is pumping clock for booster circuit 1. f(1H) is horizontal frequency (1 raster-row)

Status	Default Value
Initial	NDC1[1:0], PIDC1[1:0] = 00

5.2.15.5 PIBT [2:0] / NBT [2:0]

: The output factor of booster is switched. Adjust scale factor of the booster circuit by the voltage used. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.
PIBT is applied in Idle Partial mode.

Table 132 PIBT [2:0] / NBT [2:0]

PIBT1 / NBT2	PIBT1 / NBT1	PIBT0 / NBT0	VGH	VGL	Notes*	
0	0	0	5 X VCI1	-3X VCI1	13.75V	-8.25V
0	0	1	5 X VCI1	-4X VCI1	13.75V	-11V
0	1	0	6 X VCI1	-3X VCI1	16.5V	-8.25V
0	1	1	6 X VCI1	-4X VCI1	16.5V	-11V
1	0	0	6 X VCI1	-5X VCI1	16.5V	-13.75V
1	0	1	7 X VCI1	-4X VCI1	19.25V	-11V
1	1	0	Setting disabled			
1	1	1	Setting disabled			

NOTE: The values in table above are example of nominal upper-limit by register setting when VCI1=2.75V..

Status	Default Value
Initial	PIBT[2:0], NBT[2:0] = 010

5.2.15.6 NGVD [6:0]

This register is used to set the amplifying factor of the GVDD voltage on Normal Mode (the voltage for the Gamma voltage). It allows ranging from 2.46V to 5.00V.

Table 133 NGVD[6:0] (VCIR=2.0V, Unit [V])

NGVD [6:0]	GVDD Voltage	NGVD [6:0]	GVDD Voltage	NGVD [6:0]	GVDD Voltage	NGVD [6:0]	GVDD Voltage
0000000	2.46V	0100000	3.10V	1000000	3.74V	1100000	4.38V
0000001	2.48V	0100001	3.12V	1000001	3.76V	1100001	4.40V
0000010	2.50V	0100010	3.14V	1000010	3.78V	1100010	4.42V
0000011	2.52V	0100011	3.16V	1000011	3.80V	1100011	4.44V
0000100	2.54V	0100100	3.18V	1000100	3.82V	1100100	4.46V
0000101	2.56V	0100101	3.20V	1000101	3.84V	1100101	4.48V
0000110	2.58V	0100110	3.22V	1000110	3.86V	1100110	4.50V
0000111	2.60V	0100111	3.24V	1000111	3.88V	1100111	4.52V
0001000	2.62V	0101000	3.26V	1001000	3.90V	1101000	4.54V
0001001	2.64V	0101001	3.28V	1001001	3.92V	1101001	4.56V
0001010	2.66V	0101010	3.30V	1001010	3.94V	1101010	4.58V
0001011	2.68V	0101011	3.32V	1001011	3.96V	1101011	4.60V
0001100	2.70V	0101100	3.34V	1001100	3.98V	1101100	4.62V
0001101	2.72V	0101101	3.36V	1001101	4.00V	1101101	4.64V
0001110	2.74V	0101110	3.38V	1001110	4.02V	1101110	4.66V
0001111	2.76V	0101111	3.40V	1001111	4.04V	1101111	4.68V
0010000	2.78V	0110000	3.42V	1010000	4.06V	1110000	4.70V
0010001	2.80V	0110001	3.44V	1010001	4.08V	1110001	4.72V
0010010	2.82V	0110010	3.46V	1010010	4.10V	1110010	4.74V
0010011	2.84V	0110011	3.48V	1010011	4.12V	1110011	4.76V
0010100	2.86V	0110100	3.50V	1010100	4.14V	1110100	4.78V
0010101	2.88V	0110101	3.52V	1010101	4.16V	1110101	4.80V
0010110	2.90V	0110110	3.54V	1010110	4.18V	1110110	4.82V
0010111	2.92V	0110111	3.56V	1010111	4.20V	1110111	4.84V
0011000	2.94V	0111000	3.58V	1011000	4.22V	1111000	4.86V
0011001	2.96V	0111001	3.60V	1011001	4.24V	1111001	4.88V
0011010	2.98V	0111010	3.62V	1011010	4.26V	1111010	4.90V
0011011	3.00V	0111011	3.64V	1011011	4.28V	1111011	4.92V

NGVD [6:0]	GVDD Voltage	NGVD [6:0]	GVDD Voltage	NGVD [6:0]	GVDD Voltage	NGVD [6:0]	GVDD Voltage
0011100	3.02V	0111100	3.66V	1011100	4.30V	1111100	4.94V
0011101	3.04V	0111101	3.68V	1011101	4.32V	1111101	4.96V
0011110	3.06V	0111110	3.70V	1011110	4.34V	1111110	4.98V
0011111	3.08V	0111111	3.72V	1011111	4.36V	1111111	5.00V

NOTE: Don't set any higher GVDD level than AVDD-0.3V

Status	Default Value
Initial	NGVD[6:0] = 0000000

- PIGVD [6:0] : Set the amplifying factor of the GVDD voltage on partial idle mode.

Table 134 PIGVD[6:0] (VCIR=2.0V, Unit [V])

PIGVD [6:0]	GVDD Voltage	PIGVD [6:0]	GVDD Voltage	PIGVD [6:0]	GVDD Voltage	PIGVD [6:0]	GVDD Voltage
0000000	2.46V	0100000	3.10V	1000000	3.74V	1100000	4.38V
0000001	2.48V	0100001	3.12V	1000001	3.76V	1100001	4.40V
0000010	2.50V	0100010	3.14V	1000010	3.78V	1100010	4.42V
0000011	2.52V	0100011	3.16V	1000011	3.80V	1100011	4.44V
0000100	2.54V	0100100	3.18V	1000100	3.82V	1100100	4.46V
0000101	2.56V	0100101	3.20V	1000101	3.84V	1100101	4.48V
0000110	2.58V	0100110	3.22V	1000110	3.86V	1100110	4.50V
0000111	2.60V	0100111	3.24V	1000111	3.88V	1100111	4.52V
0001000	2.62V	0101000	3.26V	1001000	3.90V	1101000	4.54V
0001001	2.64V	0101001	3.28V	1001001	3.92V	1101001	4.56V
0001010	2.66V	0101010	3.30V	1001010	3.94V	1101010	4.58V
0001011	2.68V	0101011	3.32V	1001011	3.96V	1101011	4.60V
0001100	2.70V	0101100	3.34V	1001100	3.98V	1101100	4.62V
0001101	2.72V	0101101	3.36V	1001101	4.00V	1101101	4.64V
0001110	2.74V	0101110	3.38V	1001110	4.02V	1101110	4.66V
0001111	2.76V	0101111	3.40V	1001111	4.04V	1101111	4.68V
0010000	2.78V	0110000	3.42V	1010000	4.06V	1110000	4.70V
0010001	2.80V	0110001	3.44V	1010001	4.08V	1110001	4.72V
0010010	2.82V	0110010	3.46V	1010010	4.10V	1110010	4.74V
0010011	2.84V	0110011	3.48V	1010011	4.12V	1110011	4.76V

PIGVD [6:0]	GVDD Voltage	PIGVD [6:0]	GVDD Voltage	PIGVD [6:0]	GVDD Voltage	PIGVD [6:0]	GVDD Voltage
0010100	2.86V	0110100	3.50V	1010100	4.14V	1110100	4.78V
0010101	2.88V	0110101	3.52V	1010101	4.16V	1110101	4.80V
0010110	2.90V	0110110	3.54V	1010110	4.18V	1110110	4.82V
0010111	2.92V	0110111	3.56V	1010111	4.20V	1110111	4.84V
0011000	2.94V	0111000	3.58V	1011000	4.22V	1111000	4.86V
0011001	2.96V	0111001	3.60V	1011001	4.24V	1111001	4.88V
0011010	2.98V	0111010	3.62V	1011010	4.26V	1111010	4.90V
0011011	3.00V	0111011	3.64V	1011011	4.28V	1111011	4.92V
0011100	3.02V	0111100	3.66V	1011100	4.30V	1111100	4.94V
0011101	3.04V	0111101	3.68V	1011101	4.32V	1111101	4.96V
0011110	3.06V	0111110	3.70V	1011110	4.34V	1111110	4.98V
0011111	3.08V	0111111	3.72V	1011111	4.36V	1111111	5.00V

NOTE: Don’t set any higher GVDD level than AVDD-0.3V

Status	Default Value
Initial	PIGVD[6:0] = 0000000

5.2.16 VCMCTL (F5H)

F5h	VCMCTL (VCOM Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	0	1	F5
1st Parameter	1	1	↑	0	0	0	0	0	0	0	VCOMG	00
2nd Parameter	1	1	↑	0	NVCMH6	NVCMH5	NVCMH4	NVCMH3	NVCMH2	NVCMH1	NVCMH0	00
3rd Parameter	1	1	↑	0	NVML6	NVML5	NVML4	NVML3	NVML2	NVML1	NVML0	00
4th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
5th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
6th Parameter	1	1	↑	0	0	0	0	0	VCIR[2]	VCIR[1]	VCIR[0]	04
7th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
8th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
9th Parameter	1	1	↑	0	0	0	0	0	NVC_BLK	0	0	04
10th Parameter	1	1	↑	0	0	0	0	0	PIVC_BLK	0	0	00
11th Parameter	1	1	↑	0	PIVCMH6	PIVCMH5	PIVCMH4	PIVCMH3	PIVCMH2	PIVCMH1	PIVCMH0	00
12th Parameter	1	1	↑	0	PIVML6	PIVML5	PIVML4	PIVML3	PIVML2	PIVML1	PIVML0	00

5.2.16.1 VCOMG

When VCOMG = 1, low level of VCOM signal is to be fixed at VSSA. Therefore, the amplitude of VCOM signal is determined as |VCOMH – VSSA| regardless of VML setting.

Status	Default Value
Initial	VCOMG = 0

5.2.16.2 NVCMH [6:0], PIVCMH [6:0]

Set the VCOMH voltage (a high level voltage at the Vcom alternating drive), It allows ranging from 2.46V to 5.00V.

Table 135 NVCMH [6:0] Setting (VCIR=2.0V, Unit [V])

NVCMH [6:0]	VCOMH Voltage	NVCMH [6:0]	VCOMH Voltage	NVCMH [6:0]	VCOMH Voltage	NVCMH [6:0]	VCOMH Voltage
0000000	2.46V	0100000	3.10V	1000000	3.74V	1100000	4.38V
0000001	2.48V	0100001	3.12V	1000001	3.76V	1100001	4.40V
0000010	2.50V	0100010	3.14V	1000010	3.78V	1100010	4.42V
0000011	2.52V	0100011	3.16V	1000011	3.80V	1100011	4.44V
0000100	2.54V	0100100	3.18V	1000100	3.82V	1100100	4.46V
0000101	2.56V	0100101	3.20V	1000101	3.84V	1100101	4.48V
0000110	2.58V	0100110	3.22V	1000110	3.86V	1100110	4.50V
0000111	2.60V	0100111	3.24V	1000111	3.88V	1100111	4.52V
0001000	2.62V	0101000	3.26V	1001000	3.90V	1101000	4.54V
0001001	2.64V	0101001	3.28V	1001001	3.92V	1101001	4.56V
0001010	2.66V	0101010	3.30V	1001010	3.94V	1101010	4.58V
0001011	2.68V	0101011	3.32V	1001011	3.96V	1101011	4.60V
0001100	2.70V	0101100	3.34V	1001100	3.98V	1101100	4.62V
0001101	2.72V	0101101	3.36V	1001101	4.00V	1101101	4.64V
0001110	2.74V	0101110	3.38V	1001110	4.02V	1101110	4.66V
0001111	2.76V	0101111	3.40V	1001111	4.04V	1101111	4.68V
0010000	2.78V	0110000	3.42V	1010000	4.06V	1110000	4.70V
0010001	2.80V	0110001	3.44V	1010001	4.08V	1110001	4.72V
0010010	2.82V	0110010	3.46V	1010010	4.10V	1110010	4.74V
0010011	2.84V	0110011	3.48V	1010011	4.12V	1110011	4.76V
0010100	2.86V	0110100	3.50V	1010100	4.14V	1110100	4.78V
0010101	2.88V	0110101	3.52V	1010101	4.16V	1110101	4.80V
0010110	2.90V	0110110	3.54V	1010110	4.18V	1110110	4.82V
0010111	2.92V	0110111	3.56V	1010111	4.20V	1110111	4.84V

NVCMH [6:0]	VCOMH Voltage	NVCMH [6:0]	VCOMH Voltage	NVCMH [6:0]	VCOMH Voltage	NVCMH [6:0]	VCOMH Voltage
0011000	2.94V	0111000	3.58V	1011000	4.22V	1111000	4.86V
0011001	2.96V	0111001	3.60V	1011001	4.24V	1111001	4.88V
0011010	2.98V	0111010	3.62V	1011010	4.26V	1111010	4.90V
0011011	3.00V	0111011	3.64V	1011011	4.28V	1111011	4.92V
0011100	3.02V	0111100	3.66V	1011100	4.30V	1111100	4.94V
0011101	3.04V	0111101	3.68V	1011101	4.32V	1111101	4.96V
0011110	3.06V	0111110	3.70V	1011110	4.34V	1111110	4.98V
0011111	3.08V	0111111	3.72V	1011111	4.36V	1111111	5.00V

NOTE: Don't set any higher VCOM high level than AVDD-0.3V. VCOMH voltage should be higher than VCI.

Status	Default Value
Initial	NVCMH[6:0] = 0000000

- PIVCMH[6:0] : Set the amplifying factor of the VCOMH voltage on partial idle mode.

Table 136 PIVCMH[6:0] Setting (VCIR=2.0V, Unit [V])

PIVCMH [6:0]	VCOMH Voltage	PIVCMH [6:0]	VCOMH Voltage	PIVCMH [6:0]	VCOMH Voltage	PIVCMH [6:0]	VCOMH Voltage
0000000	2.46V	0100000	3.10V	1000000	3.74V	1100000	4.38V
0000001	2.48V	0100001	3.12V	1000001	3.76V	1100001	4.40V
0000010	2.50V	0100010	3.14V	1000010	3.78V	1100010	4.42V
0000011	2.52V	0100011	3.16V	1000011	3.80V	1100011	4.44V
0000100	2.54V	0100100	3.18V	1000100	3.82V	1100100	4.46V
0000101	2.56V	0100101	3.20V	1000101	3.84V	1100101	4.48V
0000110	2.58V	0100110	3.22V	1000110	3.86V	1100110	4.50V
0000111	2.60V	0100111	3.24V	1000111	3.88V	1100111	4.52V
0001000	2.62V	0101000	3.26V	1001000	3.90V	1101000	4.54V
0001001	2.64V	0101001	3.28V	1001001	3.92V	1101001	4.56V
0001010	2.66V	0101010	3.30V	1001010	3.94V	1101010	4.58V
0001011	2.68V	0101011	3.32V	1001011	3.96V	1101011	4.60V
0001100	2.70V	0101100	3.34V	1001100	3.98V	1101100	4.62V
0001101	2.72V	0101101	3.36V	1001101	4.00V	1101101	4.64V
0001110	2.74V	0101110	3.38V	1001110	4.02V	1101110	4.66V
0001111	2.76V	0101111	3.40V	1001111	4.04V	1101111	4.68V

PIVCMH [6:0]	VCOMH Voltage	PIVCMH [6:0]	VCOMH Voltage	PIVCMH [6:0]	VCOMH Voltage	PIVCMH [6:0]	VCOMH Voltage
0010000	2.78V	0110000	3.42V	1010000	4.06V	1110000	4.70V
0010001	2.80V	0110001	3.44V	1010001	4.08V	1110001	4.72V
0010010	2.82V	0110010	3.46V	1010010	4.10V	1110010	4.74V
0010011	2.84V	0110011	3.48V	1010011	4.12V	1110011	4.76V
0010100	2.86V	0110100	3.50V	1010100	4.14V	1110100	4.78V
0010101	2.88V	0110101	3.52V	1010101	4.16V	1110101	4.80V
0010110	2.90V	0110110	3.54V	1010110	4.18V	1110110	4.82V
0010111	2.92V	0110111	3.56V	1010111	4.20V	1110111	4.84V
0011000	2.94V	0111000	3.58V	1011000	4.22V	1111000	4.86V
0011001	2.96V	0111001	3.60V	1011001	4.24V	1111001	4.88V
0011010	2.98V	0111010	3.62V	1011010	4.26V	1111010	4.90V
0011011	3.00V	0111011	3.64V	1011011	4.28V	1111011	4.92V
0011100	3.02V	0111100	3.66V	1011100	4.30V	1111100	4.94V
0011101	3.04V	0111101	3.68V	1011101	4.32V	1111101	4.96V
0011110	3.06V	0111110	3.70V	1011110	4.34V	1111110	4.98V
0011111	3.08V	0111111	3.72V	1011111	4.36V	1111111	5.00V

NOTE: Don't set any higher VCOM high level than AVDD-0.3V. VCOMH voltage should be higher than VCI.

Status	Default Value
Initial	PIVCMH[6:0] = 0000000

5.2.16.3 NVML [6:0] , PIVML

Set the Amplitude of the VCOM voltage on Normal Mode. VCOML is adjusted automatically by setting the Amplitude of VCOM voltage.

Table 137 NVML[6:0] Setting (VCIR=2.0V, Unit [V])

NVML [6:0]	Amplitude Voltage	NVML [6:0]	Amplitude Voltage	NVML [6:0]	Amplitude Voltage	NVML [6:0]	Amplitude Voltage
0000000	3.075	0100000	3.875	1000000	4.675	1100000	5.475
0000001	3.100	0100001	3.900	1000001	4.700	1100001	5.500
0000010	3.125	0100010	3.925	1000010	4.725	1100010	5.525
0000011	3.150	0100011	3.950	1000011	4.750	1100011	5.550
0000100	3.175	0100100	3.975	1000100	4.775	1100100	5.575

NVML [6:0]	Amplitude Voltage	NVML [6:0]	Amplitude Voltage	NVML [6:0]	Amplitude Voltage	NVML [6:0]	Amplitude Voltage
0000101	3.200	0100101	4.000	1000101	4.800	1100101	5.600
0000110	3.225	0100110	4.025	1000110	4.825	1100110	5.625
0000111	3.250	0100111	4.050	1000111	4.850	1100111	5.650
0001000	3.275	0101000	4.075	1001000	4.875	1101000	5.675
0001001	3.300	0101001	4.100	1001001	4.900	1101001	5.700
0001010	3.325	0101010	4.125	1001010	4.925	1101010	5.725
0001011	3.350	0101011	4.150	1001011	4.950	1101011	5.750
0001100	3.375	0101100	4.175	1001100	4.975	1101100	5.775
0001101	3.400	0101101	4.200	1001101	5.000	1101101	5.800
0001110	3.425	0101110	4.225	1001110	5.025	1101110	5.825
0001111	3.450	0101111	4.250	1001111	5.050	1101111	5.850
0010000	3.475	0110000	4.275	1010000	5.075	1110000	5.875
0010001	3.500	0110001	4.300	1010001	5.100	1110001	5.900
0010010	3.525	0110010	4.325	1010010	5.125	1110010	5.925
0010011	3.550	0110011	4.350	1010011	5.150	1110011	5.950
0010100	3.575	0110100	4.375	1010100	5.175	1110100	5.975
0010101	3.600	0110101	4.400	1010101	5.200	1110101	6.000
0010110	3.625	0110110	4.425	1010110	5.225	1110110	Setting disable
0010111	3.650	0110111	4.450	1010111	5.250	1110111	Setting disable
0011000	3.675	0111000	4.475	1011000	5.275	1111000	Setting disable
0011001	3.700	0111001	4.500	1011001	5.300	1111001	Setting disable
0011010	3.725	0111010	4.525	1011010	5.325	1111010	Setting disable
0011011	3.750	0111011	4.550	1011011	5.350	1111011	Setting disable
0011100	3.775	0111100	4.575	1011100	5.375	1111100	Setting disable
0011101	3.800	0111101	4.600	1011101	5.400	1111101	Setting disable
0011110	3.825	0111110	4.625	1011110	5.425	1111110	Setting disable
0011111	3.850	0111111	4.650	1011111	5.450	1111111	Setting disable

NOTE: Available setting range of VCOM low level is from VCL+0.5V to 0V. The Amplitude of VCOM cannot exceed 6V.

Status	Default Value
Initial	NVML[6:0] = 0000000

- PIVML[6:0] Set the Amplitude of the VCOM voltage on partial idle mode.

Table 138 PIVML[6:0] Setting (VCIR=2.0V, Unit [V])

PIVML [6:0]	Amplitude Voltage	PIVML [6:0]	Amplitude Voltage	PIVML [6:0]	Amplitude Voltage	PIVML [6:0]	Amplitude Voltage
0000000	3.075	0100000	3.875	1000000	4.675	1100000	5.475
0000001	3.100	0100001	3.900	1000001	4.700	1100001	5.500
0000010	3.125	0100010	3.925	1000010	4.725	1100010	5.525
0000011	3.150	0100011	3.950	1000011	4.750	1100011	5.550
0000100	3.175	0100100	3.975	1000100	4.775	1100100	5.575
0000101	3.200	0100101	4.000	1000101	4.800	1100101	5.600
0000110	3.225	0100110	4.025	1000110	4.825	1100110	5.625
0000111	3.250	0100111	4.050	1000111	4.850	1100111	5.650
0001000	3.275	0101000	4.075	1001000	4.875	1101000	5.675
0001001	3.300	0101001	4.100	1001001	4.900	1101001	5.700
0001010	3.325	0101010	4.125	1001010	4.925	1101010	5.725
0001011	3.350	0101011	4.150	1001011	4.950	1101011	5.750
0001100	3.375	0101100	4.175	1001100	4.975	1101100	5.775
0001101	3.400	0101101	4.200	1001101	5.000	1101101	5.800
0001110	3.425	0101110	4.225	1001110	5.025	1101110	5.825
0001111	3.450	0101111	4.250	1001111	5.050	1101111	5.850
0010000	3.475	0110000	4.275	1010000	5.075	1110000	5.875
0010001	3.500	0110001	4.300	1010001	5.100	1110001	5.900
0010010	3.525	0110010	4.325	1010010	5.125	1110010	5.925
0010011	3.550	0110011	4.350	1010011	5.150	1110011	5.950
0010100	3.575	0110100	4.375	1010100	5.175	1110100	5.975
0010101	3.600	0110101	4.400	1010101	5.200	1110101	6.000
0010110	3.625	0110110	4.425	1010110	5.225	1110110	Setting disable
0010111	3.650	0110111	4.450	1010111	5.250	1110111	Setting disable
0011000	3.675	0111000	4.475	1011000	5.275	1111000	Setting disable
0011001	3.700	0111001	4.500	1011001	5.300	1111001	Setting disable
0011010	3.725	0111010	4.525	1011010	5.325	1111010	Setting disable
0011011	3.750	0111011	4.550	1011011	5.350	1111011	Setting disable
0011100	3.775	0111100	4.575	1011100	5.375	1111100	Setting disable
0011101	3.800	0111101	4.600	1011101	5.400	1111101	Setting disable
0011110	3.825	0111110	4.625	1011110	5.425	1111110	Setting disable
0011111	3.850	0111111	4.650	1011111	5.450	1111111	Setting disable

NOTE: Available setting range of VCOM low level is from VCL+0.5V to 0V. The Amplitude of VCOM cannot exceed 6V.

Status	Default Value
Initial	PIVML[6:0] = 0000000

5.2.16.4 SVCIR [2:0] / VCIR [2:0]

- SVCIR [2:0] : VCI recycling period of Source is sustained for the number of clock cycle which is set on SVCIR [2:0].
- VCIR [2:0] : VCI recycling period of VCOM is sustained for the number of clock cycle which is set on VCIR [2:0].

Table 139 SVCIR [2:0] / VCIR [2:0]

SVCIR2 VCIR2	SVCIR1 VCIR1	SVCIR0 VCIR0	Period of VCIR recycling		
			VCI recycling period. (Synchronized with INCLK)		
			Sn	Vcom 1 (a/b)	Vcom 2 (c/d)
0	0	0	0	0	0
0	0	1	4	2/4	4/2
0	1	0	8	4/8	8/4
0	1	1	12	6/12	12/6
1	0	0	16	8/16	16/8
1	0	1	20	10/20	20/10
1	1	0	24	12/24	24/12
1	1	1	28	14/28	28/14

NOTE: When VCI Recycling is used, VCOMH level must be larger than VCI level.
OSCK is the internal oscillator clock. INCLK is the divided clock of the OSCK for Display Control. INCLK = OSCK / 8.

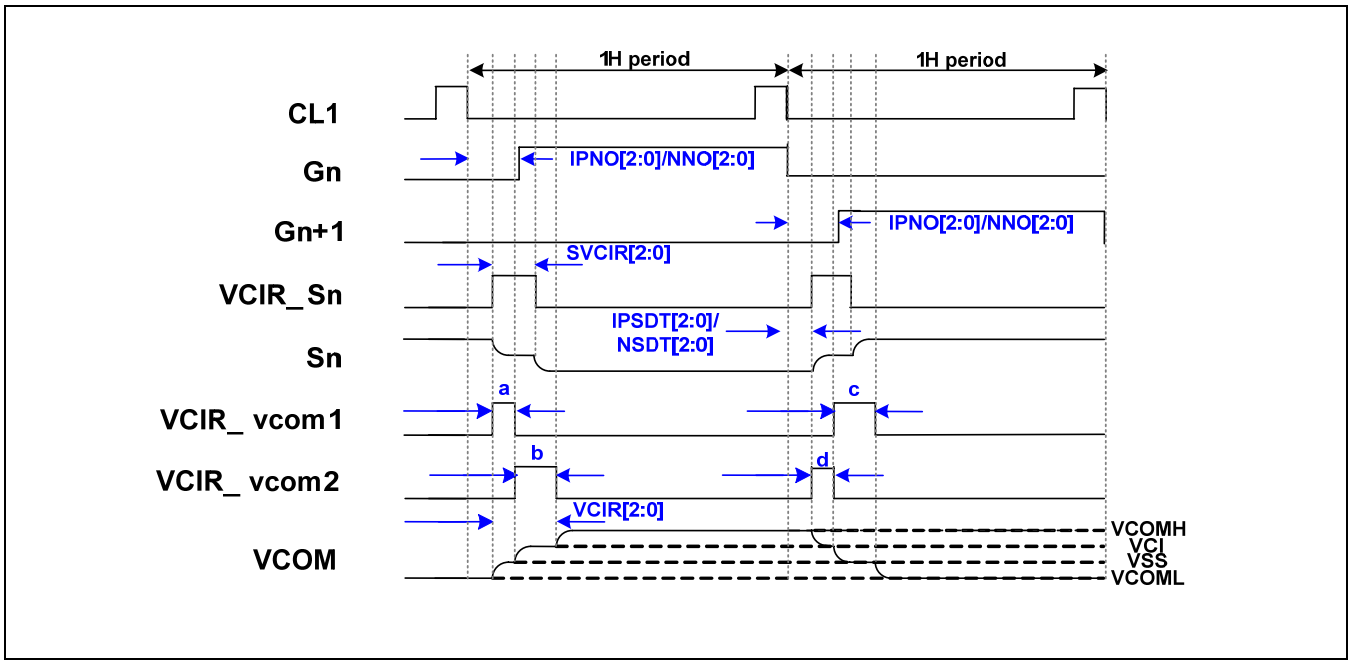


Figure 189 Set Delay From Gate Output To Source Output And VCIR Signal

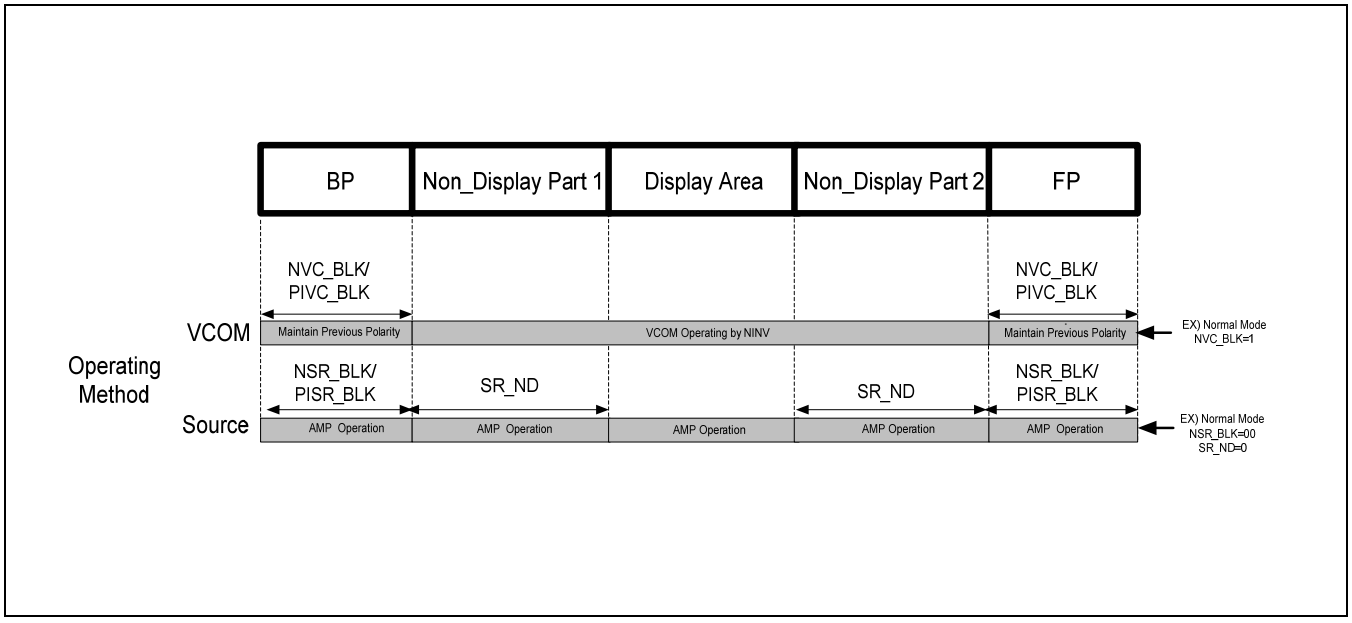


Figure 190 Source/Vcom Operating Example by Releated Registers

Status	Default Value
Initial	VCIR[2:0] = 100 SVCIR[2:0]= 100

5.2.16.5 NVC_BLK/PIVC_BLK

: This register controls VCOM state in porch period.

Table 140 NVC_BLK/PIVC_BLK

VC_BLK	Operation
0	VCOM is continuously toggled every horizontal in porch period.
1	VCOM is continuously toggled every frame in porch period.

Status	Default Value
Initial	NVC_BLK = 1 , PIVC_BLK=0

5.2.17 SRCCTL (F6H)

F6h	SRCCTL (Source Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	1	0	F6
1st Parameter	1	1	↑	0	0	0	0	0	SVCIR[2]	SVCIR[1]	SVCIR[0]	04
2nd Parameter	1	1	↑	0	0	0	SEL_360	0	0	0	SG	00
3rd Parameter	1	1	↑	0	0	0	0	SAP[3]	SAP[2]	SAP[1]	SAP[0]	08
4th Parameter	1	1	↑	0	0	0	0	0	0	OCM[1]	OCM[0]	03
5th Parameter	1	1	↑	0	0	0	0	0	NSDT[2]	NSDT[1]	NSDT[0]	01
6th Parameter	1	1	↑	0	0	0	0	NSR_BLK[1]	NSR_BLK[0]	0	SR_ND	00
7th Parameter	1	1	↑	0	0	0	0	0	PISDT[2]	PISDT[1]	PISDT[0]	01
8th Parameter	1	1	↑	0	0	0	0	PISR_BLK[1]	PISR_BLK[0]	0	0	00

5.2.17.1 SVCIR [2:0]

: This controls the period of source VCI recycling
Refer 5.2.16.4 SVCIR[2:0]/VCIR[2:0] contents.

Status	Default Value
Initial	SVCIR[2:0] = 100

5.2.17.2 SEL_360

: Set the number of active Source Channel

Table 141 SEL_360

SEL_360	Operation
0	S61 ~ S1020 Channel enable
1	S1 ~ S1080 Channel enable

Status	Default Value
Initial	SEL_360 = 0

5.2.17.3 SG

: This controls the gamma symmetric axis.

- SG = 0 : The adjustment register is to adjust X-axis symmetric of the grayscale voltage.
- SG = 1 : The adjustment register is to adjust Y-axis symmetric of the grayscale voltage.

Status	Default Value
Initial	SG = 0

5.2.17.4 NSR_BLK/PISR_BLK

: This register controls source state in porch period.

Table 142 NSR_BLK[1:0]

NSR_BLK	Operation
00	Source is amplifier driving mode in porch period.
01	Source is binary driving mode in porch period.
10	Source is GND in porch period.
11	Source is hi-z in porch period.

Table 143 PISR_BLK[1:0]

PISR_BLK	Operation
00	Source is binary driving mode in porch period.
01	Source is binary driving mode in porch period.
10	Source is GND in porch period.
11	Source is hi-z in porch period.

Status	Default Value
Initial	PISR_BLK[1:0]=00, NSR_BLK[1:0] = 00

5.2.17.5 SR_ND

: This register controls source state in non-display period.

Table 144 SR_ND

SR_ND	Operation
0	Source is amplifier driving mode in non-display period.
1	Source is binary driving mode in non-display period.

Status	Default Value
Initial	SR_ND = 0

5.2.17.6 SAP [3:0]

: Adjust the slew-rate of the operational amplifier for the source driver. If higher SAP[3:0] is set, LCD panel having higher resolution or higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But these bits must be set as adequate value because the amount of fixed current of the operational amplifier is also adjusted. During non-display, when SAP[3:0] =”0000,” operational amplifiers are turned off, so current consumption can be reduced.

Table 145 SAP[3:0]

SAP3	SAP2	SAP1	SAP0	Source Amp. Current Level	Slew rate[us/V]	Delay[us]
0	0	0	0	Amp. Stop	-	-
0	0	0	1	Setting Disable		
0	0	1	0	Setting Disable		
0	0	1	1	Slow 3	5.42	18.31

0	1	0	0	Medium Slow 1	4.22	14.28
0	1	0	1	Medium Slow 2	3.45	11.68
0	1	1	0	Medium Slow 3	3.00	10.15
0	1	1	1	Medium Slow 4	2.67	9.01
1	0	0	0	Medium Fast 1	2.39	8.10
1	0	0	1	Medium Fast 2	2.27	7.64
1	0	1	0	Medium Fast 3	2.11	7.14
1	0	1	1	Medium Fast 4	1.99	6.72
1	1	0	0	Fast1	1.88	6.37
1	1	0	1	Fast2	1.78	6.01
1	1	1	0	Fast3	1.70	5.75
1	1	1	1	Fast4 (the Fastest)	1.64	5.53

Status	Default Value
Initial	SAP[3:0]=1000

NOTE: Panel load (typical case): R=8.8kohm, C=45pF. Where, AVDD=5.5V, GVDD=5.0V

- OCM[1:0]: The control bits to cancel the offset voltage of the source amp. This register supports the line and frame offset cancellation mode.

Table 146 OCM[1:0]

OCM1	OCM0	Source amp. Offset cancellation mode selection
0	0	2 line and 4 frame offset cancellation mode
0	1	1 line and 4 frame offset cancellation mode
1	0	4 frame offset cancellation mode
1	1	POL=”L” fix

NOTE: POL: The register bit for the source amp polarity.

Status	Default Value
Initial	OCM[1:0]=11

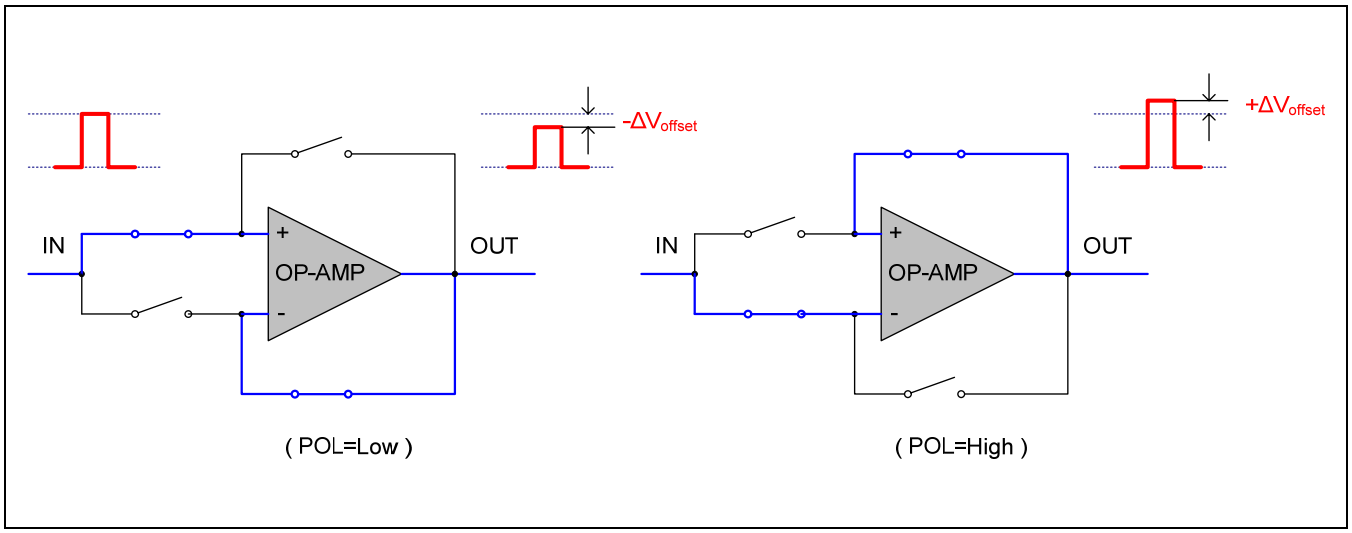


Figure 191 Gamma & Source Driver Offset Cancellation Method

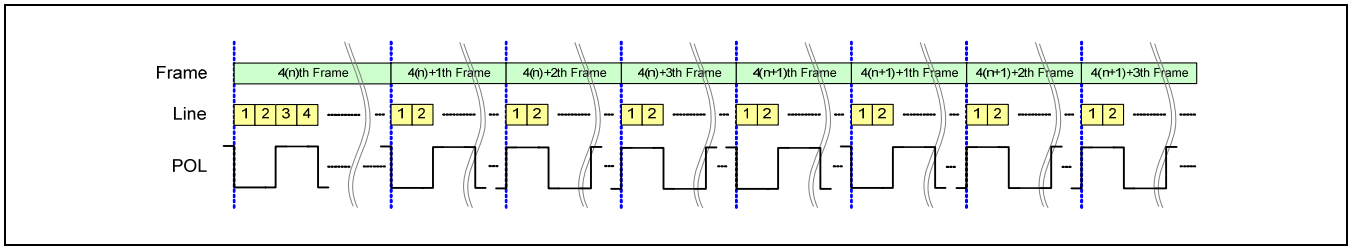


Figure 192 2 Line and 4 Frame Offset Cancellation Mode

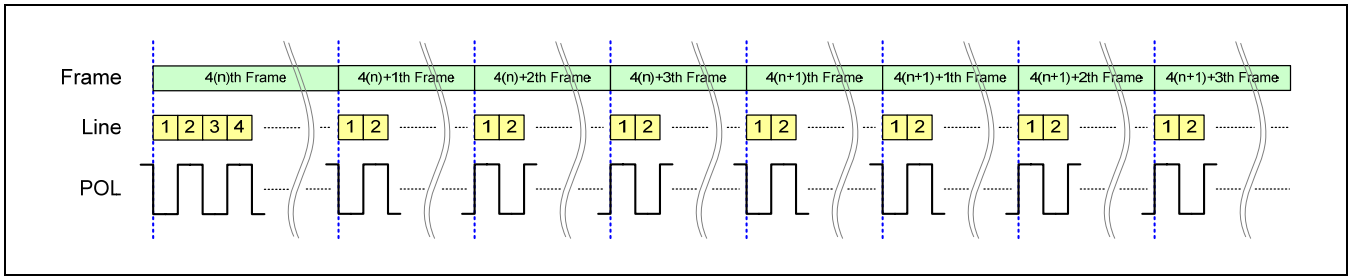


Figure 193 1 Line and 4 Frame Offset Cancellation Mode

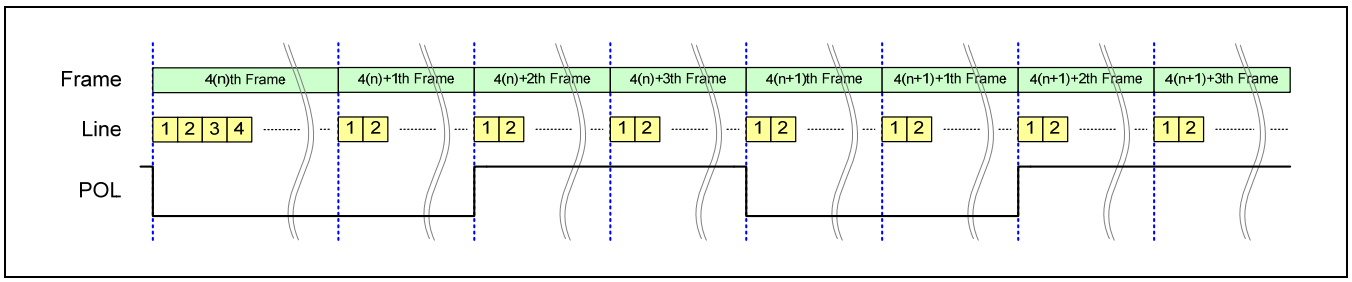


Figure 194 4 Frame Offset Cancellation Mode

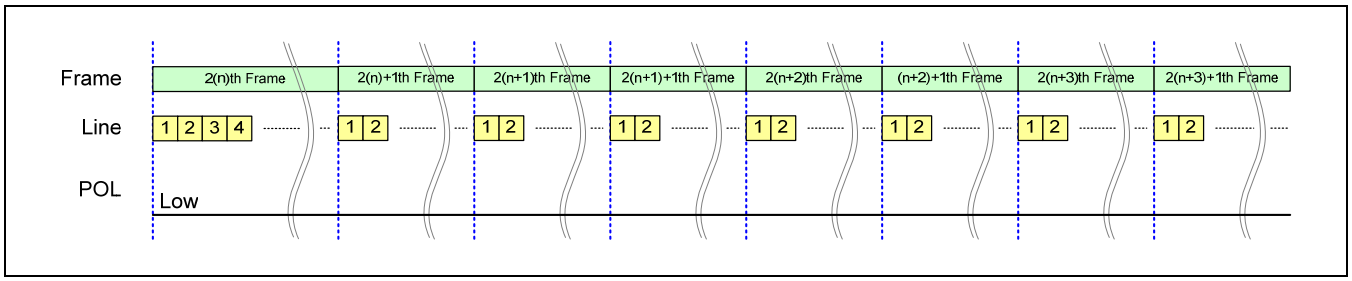


Figure 195 Halt Offset Cancellation Mode

5.2.17.7 PISDT [2:0] / NSDT [2:0]

: This register is used to set delay amount from gate falling(end) to source output. PISDT is applied in Idle Partial mode.

Table 147 NSDT[2:0]/PISDT[2:0]

NSDT2 / PISDT2	NSDT1 / PISDT1	NSDT0 / PISDT0	Delay amount of the source output
			Internal Operation (Synchronized with INCLK)
0	0	0	4
0	0	1	8
0	1	0	12
0	1	1	16
1	0	0	20
1	0	1	24
1	1	0	28
1	1	1	Setting disable

NOTE: INCLK means internal clock for display.
OSCK is the internal oscillator clock. INCLK is the divided clock of the OSCK for Display Control.
In MPU I/F, INCLK = OSCK / 8.
In RGB I/F, INCLK is decided by RGB_DIV.

Status	Default Value
Initial	PISDT[2:0], NSDT[2:0] = 001

5.2.18 IFCTL (F7H)

F7h	IFCTL (Interface Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	1	1	1	F7
1st Parameter	1	1	↑	MY_ EOR	MX_ EOR	MV_ EOR	ML_ EOR	BGR_ EOR	0	0	0	00
2nd Parameter	1	1	↑	IPM [2]	IPM [1]	IPM [0]	MDT [1]	MDT [0]	SELF _REF	DM [1]	DM [0]	80
3rd Parameter	1	1	↑	VPL	HPL	DPL	EPL	ENDI AN	0	0	RIM	10
4th Parameter	1	1	↑	0	0	0	SPR _SEL	0	RGB_ DIV[2]	RGB_ DIV[1]	RGB_ DIV[0]	02
5th Parameter	1	1	↑	0	0	0	0	0	0	0	SDO_ EN	00

5.2.18.1 MY_EOR / MX_EOR / MV_EOR / ML_EOR / BGR_EOR

: Each of these register will be used inside the IC. The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

Status	Default Value
Initial	MY_EOR, MX_EOR, MV_EOR, ML_EOR, BGR_EOR = 0

5.2.18.2 IPM [2:0]

: Select the method of display data expansion.

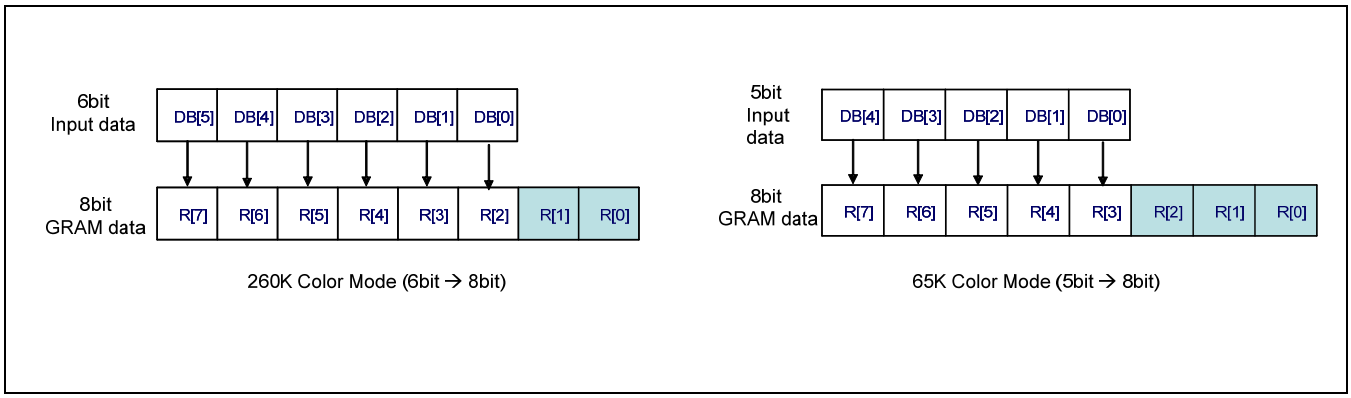


Figure 196 Data Expansion by IPM (Example of Red Color)

5.2.18.3 IPM [2:0]

Table 148 IPM

IPM	6bit → 8bit		5bit → 8bit		
	R[1]	R[0]	R[2]	R[1]	R[0]
000	0	0	DB[4]	0	0
001	0	1	DB[4]	0	1
010	1	0	DB[4]	1	0
011	1	1	DB[4]	1	1
100	DB[5]	DB[4]	DB[4]	DB[4]	DB[3]
101	DB[5]	0	DB[4]	DB[4]	0
110	DB[5]	1	DB[4]	DB[4]	1
111	Not defined		Not defined		

Status	Default Value
Initial	IPM[2:0] = 100

5.2.18.4 MDT [1:0]

: refer to the 3.2 Display Module Data Color Coding section.

Status	Default Value
Initial	MDT[1:0] = 00

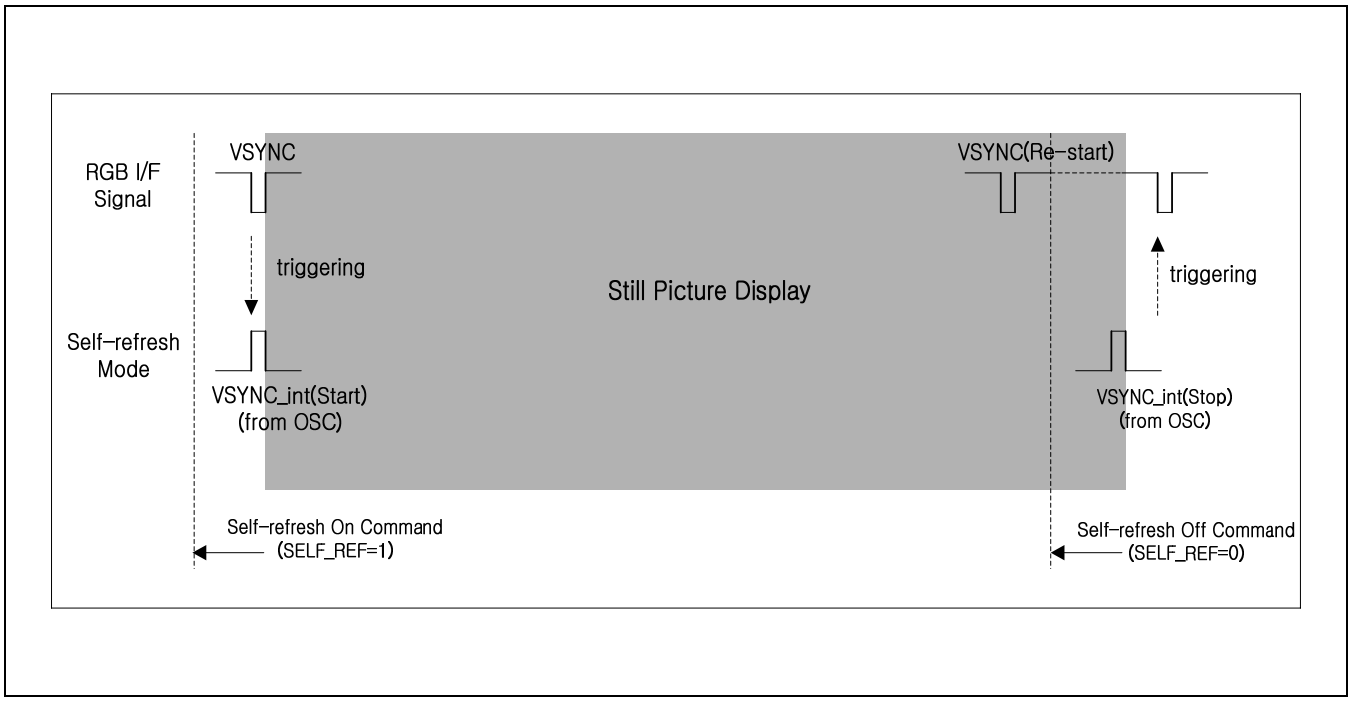
5.2.18.5 SELF_REF

: Specify the Self-refresh On/Off mode in RGB mode.

Table 149 SELF_REF

SELF_REF	Display Operation @RGB Mode
0	External RGB Mode
1	Self-refresh (internal OSC) Mode

Status	Default Value
Initial	SELF_REF = 0



When all the signals from RGB interface do not come into S6D05A1 in the self-refresh mode (SELF_REF=1), signals for still picture display are generated from the internal oscillator. For flicker free display when the mode transition between internal clock mode and external clock mode is done, the display timing is to be synchronized

with vertical sync signal. When the internal clock transits to the external clock, panel can not be refreshed for max 1-frame time in case host does not monitor TE signal from S6D05A1. In the progress of returnning to RGB mode for memory update, initial 1 or 2 frame data can not be displayed. So, up to 3 frame memory update is required for motion picture display

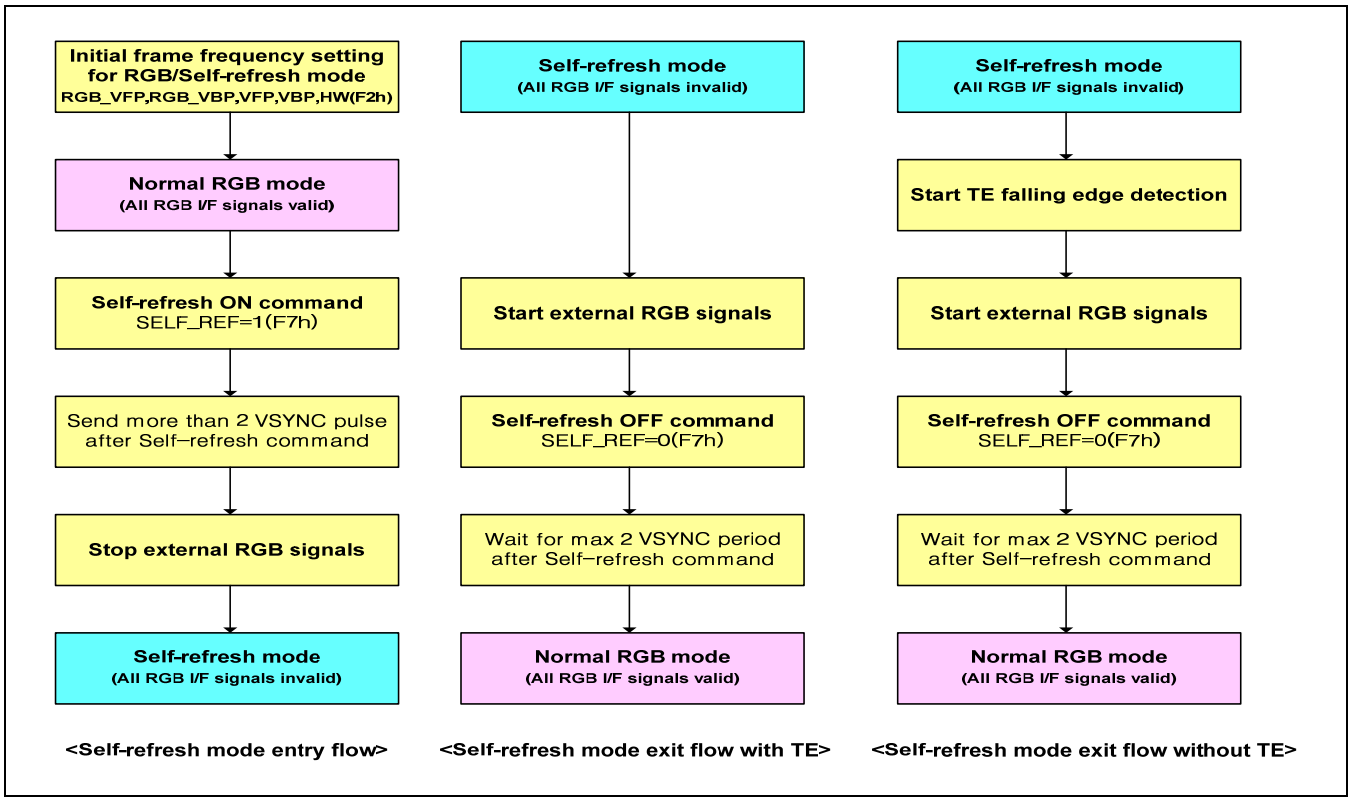


Figure 197 Flow Chart of Entry/Exit for Self-Refresh Mode.

5.2.18.6 DM [1:0]

: Specify the display operation mode. The interface can be set based on the bits of DM. This setting enables switching interface between internal operation and the external display interface.

Table 150 DM[1:0]

DM1	DM0	Display Operation Mode
0	0	CPU interface mode, MIPI command mode, MDDI mode
0	1	RGB interface mode, MIPI video mode
1	0	VSYNC interface mode
1	1	Setting disabled

Status	Default Value
Initial	DM[1:0] = 00

5.2.18.7 ENDIAN

: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

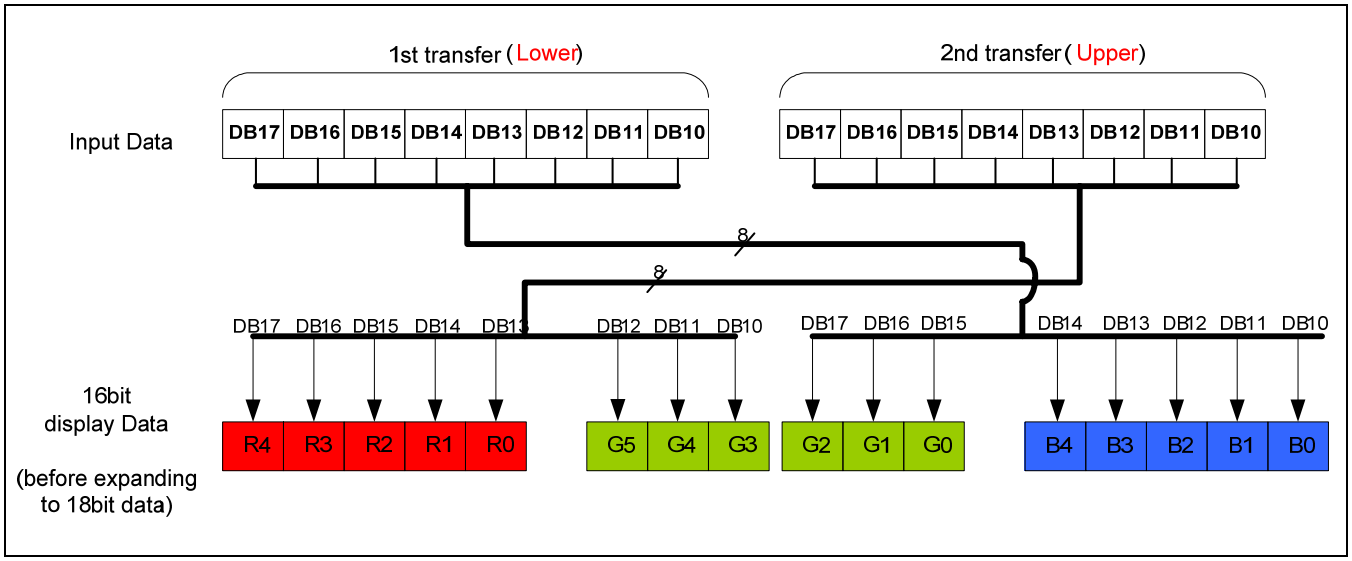


Figure 198 Little Endian (65K 8bit I/F type Ⅱ)

Table 151 ENDIAN

ENDIAN	Data transfer mode
0	Normal (MSB first)
1	Little Endian (LSB first)

NOTE: Little Endian is valid on only 65K 8bit, 9bit I/F mode.

Status	Default Value
Initial	ENDIAN = 0

5.2.18.8 VPL

: Reverses the polarity of the VSYNC signal.

VPL	Operation
0	VSYNC is low active
1	VSYNC is high active

Status	Default Value
Initial	VPL = 0

5.2.18.9 HPL

: Reverses the polarity of the HSYNC signal.

HPL	Operation
0	HSYNC is low active
1	HSYNC is high active

Status	Default Value
Initial	HPL = 0

5.2.18.10 DPL

: Reverses the polarity of the DOTCLK signal.

DPL	Operation
0	Display data is fetched at DOTCLK's rising edge
1	Display data is fetched at DOTCLK's falling edge

Status	Default Value
Initial	DPL = 0

5.2.18.11 EPL

: Set the polarity of ENABLE pad while using RGB interface.

Table 152 Relationship Between EPL, ENABLE and RAM Access

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
0	1	Invalid	Held
1	0	Invalid	Held
1	1	Valid	Updated

Status	Default Value
Initial	EPL = 1

5.2.18.12 RIM

: Specify the RGB interface mode when the RGB interface is used. Specifically, this setting specifies the mode when the bit of DM is set to RGB interface. These bits should be set before display operation through the RGB interface and should not be set during operation.

Table 153 RIM

RIM	RGB Interface Mode
0	24-bit /18-bit / 16-bit RGB interface (one transfer/pixel)
1	8-bit / 6-bit RGB interface (three transfer /pixel)

Status	Default Value
Initial	RIM = 0

You should notice that some display functions, which will be described later, cannot be used according to the display mode shown below.

Table 154 Display Functions and Display Modes

Function	RGB interface	Internal Clock Operation Mode
Partial Display	Cannot be used	Can be used
Rotation	Cannot be used	Can be used
Mirroring	Can be used	Can be used
Window Function	Cannot be used	Can be used

Depending on the external display interface setting, various interfaces can be specified to match the display state. While displaying motion pictures (RGB interface), the data for display can be written in high-speed write mode, which achieves both low power consumption and high-speed access.

5.2.18.13 SPR_SEL

: Select the usage of Short Pulse Rejection (SPR) circuit to Logic input signals.

Table 155 SPR_SEL

SPR_SEL	Description
0	Short pulse rejection circuit is not used
1	Approximately 5ns short pulse rejection

Status	Default Value
Initial	SPR_SEL = 0

5.2.18.14 RGB_DIV [2:0]

- RGB_DIV2-0: Select internal clock in RGB interface mode

Table 156 RGB_DIV[2:0]

RGB_DIV[2:0]	INCLK	
	24/18/16- bit RGB	8/6- bit RGB
000	2 DOTCLK	2 x 3 DOTCLK
001	3 DOTCLK	3 x 3 DOTCLK
010	4 DOTCLK	4 x 3 DOTCLK
011	5 DOTCLK	5 x 3 DOTCLK
100	6 DOTCLK	6 x 3 DOTCLK
101	7 DOTCLK	7 x 3 DOTCLK
110	8 DOTCLK	8 x 3 DOTCLK
111	9 DOTCLK	9 x 3 DOTCLK

NOTE: INCLK means Internal Clock.

Status	Default Value
Initial	RGB_DIV[2:0] = 010

5.2.18.15 SDO_EN

: Set the enable/disable of SDO Pin

Table 157 SDO_EN

SDO_EN	Operation
0	SDO Disable
1	SDO Enable

Status	Default Value
Initial	SDO_EN = 0

5.2.19 PANELCTL (F8H)

F8h	PANELCTL (Panel Control)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	0	0	F8
1st Parameter	1	1	↑	0	PINO [2]	PINO [1]	PINO [0]	0	NNO [2]	NNO [1]	NNO [0]	11
2nd Parameter	1	1	↑	0	0	0	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	00

5.2.19.1 PINO [2:0] / NNO [2:0]

: Set amount of non-overlap for the gate output. PINO[2:0] is applied in Idle Partial mode.

Table 158 PINO[2:0] / NNO[2:0]

PINO2 / NNO2	PINO1 / NNO1	PINO0 / NNO0	Amount of non-overlap * unit : INCLK cycle
0	0	0	4
0	0	1	8
0	1	0	12
0	1	1	16
1	0	0	20
1	0	1	24
1	1	0	28
1	1	1	Setting disable

NOTE: The amount of non-overlap time is defined from starting time of 1H
INCLK means internal clock for display.
OSCK is the internal oscillator clock. INCLK is the divided clock of the OSCK for Display Control.
In MPU I/F, INCLK = OSCK / 8.
In RGB I/F, INCLK is decided by RGB_DIV.

Status	Default Value
Initial	PINO[2:0], NNO[2:0] = 001

5.2.19.2 SCN [4:0]

- SCN [4:0]: Set the scanning start position of the gate driver

Table 159 SCN Bits and Drive Duty

SCN[4:0]	Start Position	
	GS=0	GS=1
00000	G1	G480
00001	G9	G472
00010	G17	G464
:	:	:
11101	233	248
11110	241	240
11111	Setting Disable	Setting Disable

NOTE: Ensure that NL+SCN ≤ 480 Line

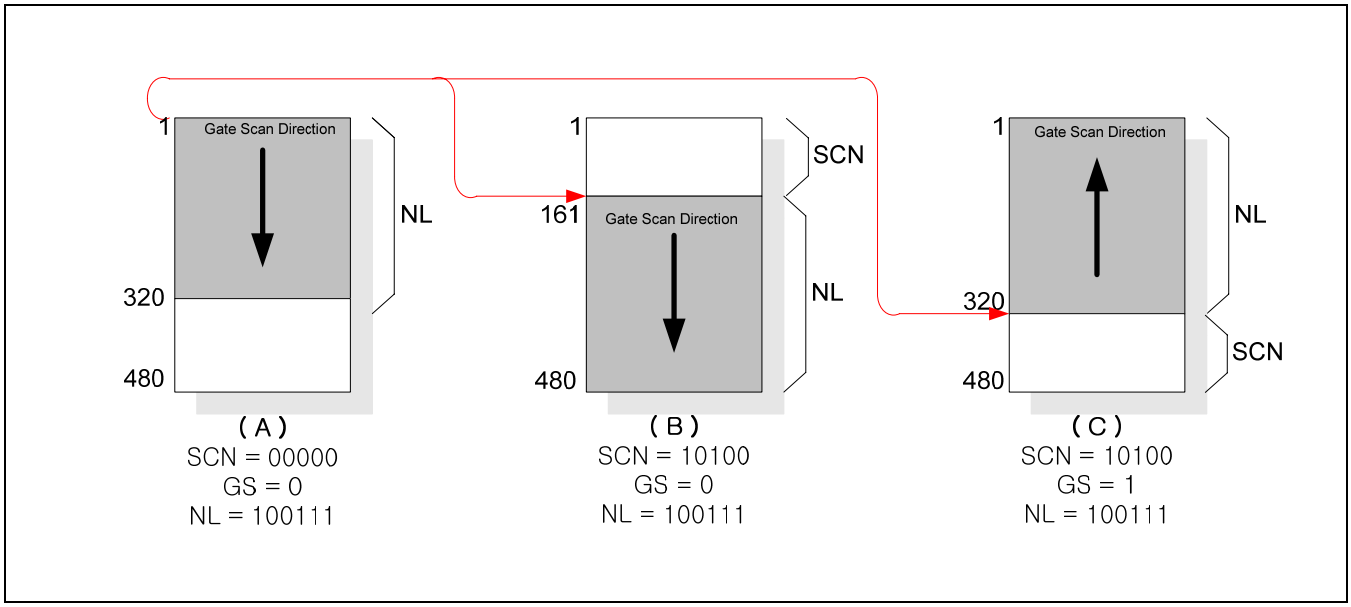


Figure 199 Gate Scan Position Control

Status	Default Value
Initial	SCN[4:0] = 00000

5.2.20 GAMMASEL (F9H)

F9h	GAMMASEL(Gamma Selection)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	0	1	F9
Parameter	1	1	↑	0	0	NGF [1]	NGF [0]	0	R_ GMA	G_ GMA	B_ GMA	27

5.2.20.1 NGF [1:0]

: Set the negative polarity gamma register to positive polarity gamma register or user setting value. Refer to the section 4.2.5.4.

- NGF[1:0] = 00 : negative polarity gamma is applied by the same data as positive polarity gamma register.
- NGF[1:0] = 01 : negative polarity gamma is applied by the negative polarity gamma register.
- NGF[1:0] = 10 : RFN/OSN=RFP/OSP, PKN#[5:0]=PKP(10-#)[5:0], GLN[1:0]=GLP[0:1]
- NGF[1:0] = 11 : Setting disable

Status	Default Value
Initial	NGF[1:0]=10

5.2.20.2 R_GMA,G_GMA,B_GMA

: These register selects the RGB seperate gamma register. Refer to the section 4.2

R_GMA	G_GMA	B_GMA	Selected gamma preset register
1	0	0	Red gamma preset register is selected.
0	1	0	Green gamma preset register is selected.
0	0	1	Blue gamma preset register is selected.
1	1	1	Red, Green, Blue gamma preset register is selected.
others			Setting disable

Status	Default Value
Initial	R_GMA=1, G_GMA=1, B_GMA=1

5.2.21 PGAMMACTL (FAH)

FAh	PGAMMACTL (Positive Gamma Control Register)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	0	FA
1st Parameter	1	1	↑	0	0	RFP5	RFP4	RFP3	RFP2	RFP1	RFP0	00
2nd Parameter	1	1	↑	0	0	OSP5	OSP4	OSP3	OSP2	OSP1	OSP0	00
3rd Parameter	1	1	↑	0	0	PKP05	PKP04	PKP03	PKP02	PKP01	PKP00	00
4th Parameter	1	1	↑	0	0	PKP15	PKP14	PKP13	PKP12	PKP11	PKP10	00
5th Parameter	1	1	↑	0	0	PKP25	PKP24	PKP23	PKP22	PKP21	PKP20	00
6th Parameter	1	1	↑	0	0	PKP35	PKP34	PKP33	PKP32	PKP31	PKP30	00
7th Parameter	1	1	↑	0	0	PKP45	PKP44	PKP43	PKP42	PKP41	PKP40	00
8th Parameter	1	1	↑	0	0	PKP55	PKP54	PKP53	PKP52	PKP51	PKP50	00
9th Parameter	1	1	↑	0	0	PKP65	PKP64	PKP63	PKP62	PKP61	PKP60	00
10th Parameter	1	1	↑	0	0	PKP75	PKP74	PKP73	PKP72	PKP71	PKP70	00
11th Parameter	1	1	↑	0	0	PKP85	PKP84	PKP83	PKP82	PKP81	PKP80	00
12th Parameter	1	1	↑	0	0	PKP95	PKP94	PKP93	PKP92	PKP91	PKP90	00
13th Parameter	1	1	↑	0	0	PKP105	PKP104	PKP103	PKP102	PKP101	PKP100	00
14th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
15th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
16th Parameter	1	1	↑	0	0	0	0	0	0	GLP1	GLP0	00

This command is used to set the gamma preset register for positive.

Table 160 Gamma Preset for Positive

Status	Default Value
Initial	RFP[5:0] : 000000 , OSP[5:0] : 000000 PKP0[5:0] : 000000 , PKP1[5:0] : 000000 PKP2[5:0] : 000000 , PKP3[5:0] : 000000 PKP4[5:0] : 000000 , PKP5[5:0] : 000000 PKP6[5:0] : 000000 , PKP7[5:0] : 000000 PKP8[5:0] : 000000 , PKP9[5:0] : 000000 PKP10[5:0] : 000000 , GLP[1:0] : 00

5.2.22 NGAMMACTL (FBH)

FBh	NGAMMACTL (Negative Gamma Control Register)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	1	0	FB
1st Parameter	1	1	↑	0	0	RFN5	RFN4	RFN3	RFN2	RFN1	RFN0	00
2nd Parameter	1	1	↑	0	0	OSN5	OSN4	OSN3	OSN2	OSN1	OSN0	00
3rd Parameter	1	1	↑	0	0	PKN05	PKN04	PKN03	PKN02	PKN01	PKN00	00
4th Parameter	1	1	↑	0	0	PKN15	PKN14	PKN13	PKN12	PKN11	PKN10	00
5th Parameter	1	1	↑	0	0	PKN25	PKN24	PKN23	PKN22	PKN21	PKN20	00
6th Parameter	1	1	↑	0	0	PKN35	PKN34	PKN33	PKN32	PKN31	PKN30	00
7th Parameter	1	1	↑	0	0	PKN45	PKN44	PKN43	PKN42	PKN41	PKN40	00
8th Parameter	1	1	↑	0	0	PKN55	PKN54	PKN53	PKN52	PKN51	PKN50	00
9th Parameter	1	1	↑	0	0	PKN65	PKN64	PKN63	PKN62	PKN61	PKN60	00
10th Parameter	1	1	↑	0	0	PKN75	PKN74	PKN73	PKN72	PKN71	PKN70	00
11th Parameter	1	1	↑	0	0	PKN85	PKN84	PKN83	PKN82	PKN81	PKN80	00
12th Parameter	1	1	↑	0	0	PKN95	PKN94	PKN93	PKN92	PKN91	PKN90	00
13th Parameter	1	1	↑	0	0	PKN105	PKN104	PKN103	PKN102	PKN101	PKN100	00
14th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
15th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
16th Parameter	1	1	↑	0	0	0	0	0	0	GLN1	GLN0	00

This command is used to set the gamma preset register for negative.

Table 161 Gamma Preset for Negative

Status	Default Value
Initial	RFN[5:0] : 000000 , OSN[5:0] : 000000 PKN0[5:0] : 000000 , PKN1[5:0] : 000000 PKN2[5:0] : 000000 , PKN3[5:0] : 000000 PKN4[5:0] : 000000 , PKN5[5:0] : 000000 PKN6[5:0] : 000000 , PKN7[5:0] : 000000 PKN8[5:0] : 000000 , PKN9[5:0] : 000000 PKN10[5:0] : 000000 ,GLN[1:0] : 00

6 APPENDIX

6.1 APPLICATION CIRCUIT

A typical application circuit is shown in following figure.

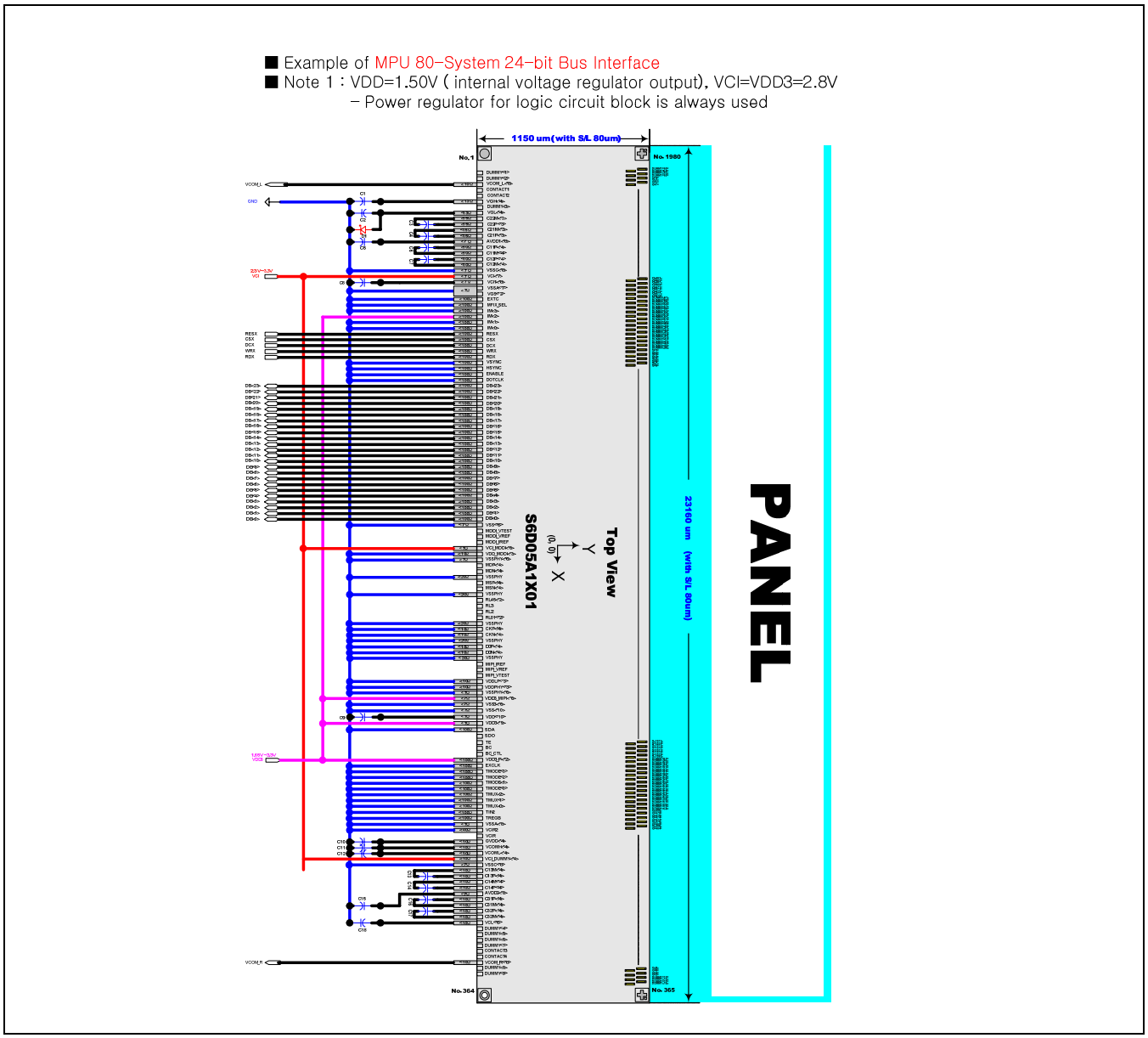


Figure 200 Application Circuit

6.2 EXTERNAL COMPONENT

Table 162 External Components

Name	Device	Value	Connection	Note	
C1	Capacitor	1uF	VGH - GND	Maximum Ratings Voltage	25V
C2	Capacitor	1uF	VGL - GND		16V
C3	Capacitor	1uF	C22M - C22P		25V
C4	Capacitor	1uF	C21M - C21P		16V
C5	Capacitor	1uF	AVDD1 - GND		10V
C6	Capacitor	1uF	C11M - C11P		10V
C7	Capacitor	1uF	C12M - C12P		10V
C8	Capacitor	1uF	VCI1-GND		6V
C9	Capacitor	1uF	VDD-GND		6V
C10	Capacitor	1uF	GVDD - GND		6V
C11	Capacitor	1uF	VCOMH - GND		6V
C12	Capacitor	1uF	VCOML - GND		6V
C13	Capacitor	1uF	C13M - C13P		10V
C14	Capacitor	1uF	C14M - C14P		10V
C15	Capacitor	1uF	AVDD2 - GND		10V
C16	Capacitor	1uF	C31M - C31P		6V
C17	Capacitor	1uF	C32M - C32P		6V
C18	Capacitor	1uF	VCL - GND		6V
C19	Capacitor	1uF	VDDPHY - GND		6V
C20	Capacitor	1uF	VDDLP - GND		6V
C21	Capacitor	1uF	VDD_MDDI - GND		6V
R1	Resistor	100Ω	MDP - MDN		±1%
R2	Resistor	100Ω	MSP - MSN		±1%
D1	Diode	-	VGL(+) – GND(-)	VF < 0.4V (@IF = 20mA, Ta = 25℃) VR > max. 25V	

NOTE: VCIR to GND capacitor is optional for this application. Refer to VCIR description in Table2.

6.3 PAD CENTER COORDINATES

Table 163 Pad Center Coordinates [Unit: um]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
1	DUMMY<1>	-11277.5	-500	661	S<1052>	7161	338	1321	S<392>	-2079	338
2	DUMMY<2>	-11217.5	-500	662	S<1051>	7147	473	1322	S<391>	-2093	473
3	VCOM_L	-11157.5	-500	663	S<1050>	7133	338	1323	S<390>	-2107	338
4	VCOM_L	-11097.5	-500	664	S<1049>	7119	473	1324	S<389>	-2121	473
5	VCOM_L	-11037.5	-500	665	S<1048>	7105	338	1325	S<388>	-2135	338
6	VCOM_L	-10977.5	-500	666	S<1047>	7091	473	1326	S<387>	-2149	473
7	VCOM_L	-10917.5	-500	667	S<1046>	7077	338	1327	S<386>	-2163	338
8	VCOM_L	-10857.5	-500	668	S<1045>	7063	473	1328	S<385>	-2177	473
9	VCOM_L	-10797.5	-500	669	S<1044>	7049	338	1329	S<384>	-2191	338
10	VCOM_L	-10737.5	-500	670	S<1043>	7035	473	1330	S<383>	-2205	473
11	CONTACT1	-10677.5	-500	671	S<1042>	7021	338	1331	S<382>	-2219	338
12	CONTACT2	-10617.5	-500	672	S<1041>	7007	473	1332	S<381>	-2233	473
13	VGH	-10557.5	-500	673	S<1040>	6993	338	1333	S<380>	-2247	338
14	VGH	-10497.5	-500	674	S<1039>	6979	473	1334	S<379>	-2261	473
15	VGH	-10437.5	-500	675	S<1038>	6965	338	1335	S<378>	-2275	338
16	VGH	-10377.5	-500	676	S<1037>	6951	473	1336	S<377>	-2289	473
17	DUMMY<3>	-10317.5	-500	677	S<1036>	6937	338	1337	S<376>	-2303	338
18	VGL	-10257.5	-500	678	S<1035>	6923	473	1338	S<375>	-2317	473
19	VGL	-10197.5	-500	679	S<1034>	6909	338	1339	S<374>	-2331	338
20	VGL	-10137.5	-500	680	S<1033>	6895	473	1340	S<373>	-2345	473
21	VGL	-10077.5	-500	681	S<1032>	6881	338	1341	S<372>	-2359	338
22	C22M	-10017.5	-500	682	S<1031>	6867	473	1342	S<371>	-2373	473
23	C22M	-9957.5	-500	683	S<1030>	6853	338	1343	S<370>	-2387	338
24	C22M	-9897.5	-500	684	S<1029>	6839	473	1344	S<369>	-2401	473
25	C22P	-9837.5	-500	685	S<1028>	6825	338	1345	S<368>	-2415	338
26	C22P	-9777.5	-500	686	S<1027>	6811	473	1346	S<367>	-2429	473
27	C22P	-9717.5	-500	687	S<1026>	6797	338	1347	S<366>	-2443	338
28	C21M	-9657.5	-500	688	S<1025>	6783	473	1348	S<365>	-2457	473
29	C21M	-9597.5	-500	689	S<1024>	6769	338	1349	S<364>	-2471	338
30	C21M	-9537.5	-500	690	S<1023>	6755	473	1350	S<363>	-2485	473
31	C21P	-9477.5	-500	691	S<1022>	6741	338	1351	S<362>	-2499	338
32	C21P	-9417.5	-500	692	S<1021>	6727	473	1352	S<361>	-2513	473
33	C21P	-9357.5	-500	693	S<1020>	6713	338	1353	S<360>	-2527	338
34	AVDD1	-9297.5	-500	694	S<1019>	6699	473	1354	S<359>	-2541	473

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
35	AVDD1	-9237.5	-500	695	S<1018>	6685	338	1355	S<358>	-2555	338
36	AVDD1	-9177.5	-500	696	S<1017>	6671	473	1356	S<357>	-2569	473
37	AVDD1	-9117.5	-500	697	S<1016>	6657	338	1357	S<356>	-2583	338
38	AVDD1	-9057.5	-500	698	S<1015>	6643	473	1358	S<355>	-2597	473
39	AVDD1	-8997.5	-500	699	S<1014>	6629	338	1359	S<354>	-2611	338
40	AVDD1	-8937.5	-500	700	S<1013>	6615	473	1360	S<353>	-2625	473
41	AVDD1	-8877.5	-500	701	S<1012>	6601	338	1361	S<352>	-2639	338
42	C11P	-8817.5	-500	702	S<1011>	6587	473	1362	S<351>	-2653	473
43	C11P	-8757.5	-500	703	S<1010>	6573	338	1363	S<350>	-2667	338
44	C11P	-8697.5	-500	704	S<1009>	6559	473	1364	S<349>	-2681	473
45	C11P	-8637.5	-500	705	S<1008>	6545	338	1365	S<348>	-2695	338
46	C11M	-8577.5	-500	706	S<1007>	6531	473	1366	S<347>	-2709	473
47	C11M	-8517.5	-500	707	S<1006>	6517	338	1367	S<346>	-2723	338
48	C11M	-8457.5	-500	708	S<1005>	6503	473	1368	S<345>	-2737	473
49	C11M	-8397.5	-500	709	S<1004>	6489	338	1369	S<344>	-2751	338
50	C12P	-8337.5	-500	710	S<1003>	6475	473	1370	S<343>	-2765	473
51	C12P	-8277.5	-500	711	S<1002>	6461	338	1371	S<342>	-2779	338
52	C12P	-8217.5	-500	712	S<1001>	6447	473	1372	S<341>	-2793	473
53	C12P	-8157.5	-500	713	S<1000>	6433	338	1373	S<340>	-2807	338
54	C12M	-8097.5	-500	714	S<999>	6419	473	1374	S<339>	-2821	473
55	C12M	-8037.5	-500	715	S<998>	6405	338	1375	S<338>	-2835	338
56	C12M	-7977.5	-500	716	S<997>	6391	473	1376	S<337>	-2849	473
57	C12M	-7917.5	-500	717	S<996>	6377	338	1377	S<336>	-2863	338
58	VSSC	-7857.5	-500	718	S<995>	6363	473	1378	S<335>	-2877	473
59	VSSC	-7797.5	-500	719	S<994>	6349	338	1379	S<334>	-2891	338
60	VSSC	-7737.5	-500	720	S<993>	6335	473	1380	S<333>	-2905	473
61	VSSC	-7677.5	-500	721	S<992>	6321	338	1381	S<332>	-2919	338
62	VSSC	-7617.5	-500	722	S<991>	6307	473	1382	S<331>	-2933	473
63	VSSC	-7557.5	-500	723	S<990>	6293	338	1383	S<330>	-2947	338
64	VSSC	-7497.5	-500	724	S<989>	6279	473	1384	S<329>	-2961	473
65	VSSC	-7437.5	-500	725	S<988>	6265	338	1385	S<328>	-2975	338
66	VCI	-7377.5	-500	726	S<987>	6251	473	1386	S<327>	-2989	473
67	VCI	-7317.5	-500	727	S<986>	6237	338	1387	S<326>	-3003	338
68	VCI	-7257.5	-500	728	S<985>	6223	473	1388	S<325>	-3017	473
69	VCI	-7197.5	-500	729	S<984>	6209	338	1389	S<324>	-3031	338
70	VCI	-7137.5	-500	730	S<983>	6195	473	1390	S<323>	-3045	473

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
71	VCI	-7077.5	-500	731	S<982>	6181	338	1391	S<322>	-3059	338
72	VCI	-7017.5	-500	732	S<981>	6167	473	1392	S<321>	-3073	473
73	VCI1	-6957.5	-500	733	S<980>	6153	338	1393	S<320>	-3087	338
74	VCI1	-6897.5	-500	734	S<979>	6139	473	1394	S<319>	-3101	473
75	VCI1	-6837.5	-500	735	S<978>	6125	338	1395	S<318>	-3115	338
76	VCI1	-6777.5	-500	736	S<977>	6111	473	1396	S<317>	-3129	473
77	VCI1	-6717.5	-500	737	S<976>	6097	338	1397	S<316>	-3143	338
78	VCI1	-6657.5	-500	738	S<975>	6083	473	1398	S<315>	-3157	473
79	VCI1	-6597.5	-500	739	S<974>	6069	338	1399	S<314>	-3171	338
80	VCI1	-6537.5	-500	740	S<973>	6055	473	1400	S<313>	-3185	473
81	VSSA	-6477.5	-500	741	S<972>	6041	338	1401	S<312>	-3199	338
82	VSSA	-6417.5	-500	742	S<971>	6027	473	1402	S<311>	-3213	473
83	VSSA	-6357.5	-500	743	S<970>	6013	338	1403	S<310>	-3227	338
84	VSSA	-6297.5	-500	744	S<969>	5999	473	1404	S<309>	-3241	473
85	VSSA	-6237.5	-500	745	S<968>	5985	338	1405	S<308>	-3255	338
86	VSSA	-6177.5	-500	746	S<967>	5971	473	1406	S<307>	-3269	473
87	VSSA	-6117.5	-500	747	S<966>	5957	338	1407	S<306>	-3283	338
88	VGS	-6057.5	-500	748	S<965>	5943	473	1408	S<305>	-3297	473
89	VGS	-5997.5	-500	749	S<964>	5929	338	1409	S<304>	-3311	338
90	EXTC	-5937.5	-500	750	S<963>	5915	473	1410	S<303>	-3325	473
91	MFIX_SEL	-5877.5	-500	751	S<962>	5901	338	1411	S<302>	-3339	338
92	IM<3>	-5817.5	-500	752	S<961>	5887	473	1412	S<301>	-3353	473
93	IM<2>	-5757.5	-500	753	S<960>	5873	338	1413	S<300>	-3367	338
94	IM<1>	-5697.5	-500	754	S<959>	5859	473	1414	S<299>	-3381	473
95	IM<0>	-5637.5	-500	755	S<958>	5845	338	1415	S<298>	-3395	338
96	RESX	-5577.5	-500	756	S<957>	5831	473	1416	S<297>	-3409	473
97	CSX	-5517.5	-500	757	S<956>	5817	338	1417	S<296>	-3423	338
98	DCX	-5457.5	-500	758	S<955>	5803	473	1418	S<295>	-3437	473
99	WRX	-5397.5	-500	759	S<954>	5789	338	1419	S<294>	-3451	338
100	RDX	-5337.5	-500	760	S<953>	5775	473	1420	S<293>	-3465	473
101	VSYNC	-5277.5	-500	761	S<952>	5761	338	1421	S<292>	-3479	338
102	HSYNC	-5217.5	-500	762	S<951>	5747	473	1422	S<291>	-3493	473
103	ENABLE	-5157.5	-500	763	S<950>	5733	338	1423	S<290>	-3507	338
104	DOTCLK	-5097.5	-500	764	S<949>	5719	473	1424	S<289>	-3521	473
105	DB<23>	-5025	-500	765	S<948>	5705	338	1425	S<288>	-3535	338
106	DB<22>	-4940	-500	766	S<947>	5691	473	1426	S<287>	-3549	473

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
107	DB<21>	-4855	-500	767	S<946>	5677	338	1427	S<286>	-3563	338
108	DB<20>	-4770	-500	768	S<945>	5663	473	1428	S<285>	-3577	473
109	DB<19>	-4685	-500	769	S<944>	5649	338	1429	S<284>	-3591	338
110	DB<18>	-4600	-500	770	S<943>	5635	473	1430	S<283>	-3605	473
111	DB<17>	-4515	-500	771	S<942>	5621	338	1431	S<282>	-3619	338
112	DB<16>	-4430	-500	772	S<941>	5607	473	1432	S<281>	-3633	473
113	DB<15>	-4345	-500	773	S<940>	5593	338	1433	S<280>	-3647	338
114	DB<14>	-4260	-500	774	S<939>	5579	473	1434	S<279>	-3661	473
115	DB<13>	-4175	-500	775	S<938>	5565	338	1435	S<278>	-3675	338
116	DB<12>	-4090	-500	776	S<937>	5551	473	1436	S<277>	-3689	473
117	DB<11>	-4005	-500	777	S<936>	5537	338	1437	S<276>	-3703	338
118	DB<10>	-3920	-500	778	S<935>	5523	473	1438	S<275>	-3717	473
119	DB<9>	-3835	-500	779	S<934>	5509	338	1439	S<274>	-3731	338
120	DB<8>	-3750	-500	780	S<933>	5495	473	1440	S<273>	-3745	473
121	DB<7>	-3665	-500	781	S<932>	5481	338	1441	S<272>	-3759	338
122	DB<6>	-3580	-500	782	S<931>	5467	473	1442	S<271>	-3773	473
123	DB<5>	-3495	-500	783	S<930>	5453	338	1443	S<270>	-3787	338
124	DB<4>	-3410	-500	784	S<929>	5439	473	1444	S<269>	-3801	473
125	DB<3>	-3325	-500	785	S<928>	5425	338	1445	S<268>	-3815	338
126	DB<2>	-3240	-500	786	S<927>	5411	473	1446	S<267>	-3829	473
127	DB<1>	-3155	-500	787	S<926>	5397	338	1447	S<266>	-3843	338
128	DB<0>	-3070	-500	788	S<925>	5383	473	1448	S<265>	-3857	473
129	VSS	-2997.5	-500	789	S<924>	5369	338	1449	S<264>	-3871	338
130	VSS	-2937.5	-500	790	S<923>	5355	473	1450	S<263>	-3885	473
131	VSS	-2877.5	-500	791	S<922>	5341	338	1451	S<262>	-3899	338
132	VSS	-2817.5	-500	792	S<921>	5327	473	1452	S<261>	-3913	473
133	VSS	-2757.5	-500	793	S<920>	5313	338	1453	S<260>	-3927	338
134	VSS	-2697.5	-500	794	S<919>	5299	473	1454	S<259>	-3941	473
135	MDDI_VTEST	-2637.5	-500	795	S<918>	5285	338	1455	S<258>	-3955	338
136	MDDI_VREF	-2577.5	-500	796	S<917>	5271	473	1456	S<257>	-3969	473
137	MDDI_IREF	-2517.5	-500	797	S<916>	5257	338	1457	S<256>	-3983	338
138	VCI_MDDI	-2457.5	-500	798	S<915>	5243	473	1458	S<255>	-3997	473
139	VCI_MDDI	-2397.5	-500	799	S<914>	5229	338	1459	S<254>	-4011	338
140	VCI_MDDI	-2337.5	-500	800	S<913>	5215	473	1460	S<253>	-4025	473
141	VCI_MDDI	-2277.5	-500	801	S<912>	5201	338	1461	S<252>	-4039	338
142	VCI_MDDI	-2217.5	-500	802	S<911>	5187	473	1462	S<251>	-4053	473

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
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144	VDD_MDDI	-2097.5	-500	804	S<909>	5159	473	1464	S<249>	-4081	473
145	VDD_MDDI	-2037.5	-500	805	S<908>	5145	338	1465	S<248>	-4095	338
146	VDD_MDDI	-1977.5	-500	806	S<907>	5131	473	1466	S<247>	-4109	473
147	VSSPHY	-1917.5	-500	807	S<906>	5117	338	1467	S<246>	-4123	338
148	VSSPHY	-1857.5	-500	808	S<905>	5103	473	1468	S<245>	-4137	473
149	VSSPHY	-1797.5	-500	809	S<904>	5089	338	1469	S<244>	-4151	338
150	VSSPHY	-1737.5	-500	810	S<903>	5075	473	1470	S<243>	-4165	473
151	VSSPHY	-1677.5	-500	811	S<902>	5061	338	1471	S<242>	-4179	338
152	VSSPHY	-1617.5	-500	812	S<901>	5047	473	1472	S<241>	-4193	473
153	MDP	-1557.5	-500	813	S<900>	5033	338	1473	S<240>	-4207	338
154	MDP	-1497.5	-500	814	S<899>	5019	473	1474	S<239>	-4221	473
155	MDP	-1437.5	-500	815	S<898>	5005	338	1475	S<238>	-4235	338
156	MDP	-1377.5	-500	816	S<897>	4991	473	1476	S<237>	-4249	473
157	MDN	-1317.5	-500	817	S<896>	4977	338	1477	S<236>	-4263	338
158	MDN	-1257.5	-500	818	S<895>	4963	473	1478	S<235>	-4277	473
159	MDN	-1197.5	-500	819	S<894>	4949	338	1479	S<234>	-4291	338
160	MDN	-1137.5	-500	820	S<893>	4935	473	1480	S<233>	-4305	473
161	VSSPHY	-1077.5	-500	821	S<892>	4921	338	1481	S<232>	-4319	338
162	MSP	-1017.5	-500	822	S<891>	4907	473	1482	S<231>	-4333	473
163	MSP	-957.5	-500	823	S<890>	4893	338	1483	S<230>	-4347	338
164	MSP	-897.5	-500	824	S<889>	4879	473	1484	S<229>	-4361	473
165	MSP	-837.5	-500	825	S<888>	4865	338	1485	S<228>	-4375	338
166	MSN	-777.5	-500	826	S<887>	4851	473	1486	S<227>	-4389	473
167	MSN	-717.5	-500	827	S<886>	4837	338	1487	S<226>	-4403	338
168	MSN	-657.5	-500	828	S<885>	4823	473	1488	S<225>	-4417	473
169	MSN	-597.5	-500	829	S<884>	4809	338	1489	S<224>	-4431	338
170	VSSPHY	-537.5	-500	830	S<883>	4795	473	1490	S<223>	-4445	473
171	RL45	-477.5	-500	831	S<882>	4781	338	1491	S<222>	-4459	338
172	RL45	-417.5	-500	832	S<881>	4767	473	1492	S<221>	-4473	473
173	RL3	-357.5	-500	833	S<880>	4753	338	1493	S<220>	-4487	338
174	RL2	-297.5	-500	834	S<879>	4739	473	1494	S<219>	-4501	473
175	RL01	-237.5	-500	835	S<878>	4725	338	1495	S<218>	-4515	338
176	RL01	-177.5	-500	836	S<877>	4711	473	1496	S<217>	-4529	473
177	VSSPHY	-117.5	-500	837	S<876>	4697	338	1497	S<216>	-4543	338
178	CKP	-57.5	-500	838	S<875>	4683	473	1498	S<215>	-4557	473

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
179	CKP	2.5	-500	839	S<874>	4669	338	1499	S<214>	-4571	338
180	CKP	62.5	-500	840	S<873>	4655	473	1500	S<213>	-4585	473
181	CKP	122.5	-500	841	S<872>	4641	338	1501	S<212>	-4599	338
182	CKN	182.5	-500	842	S<871>	4627	473	1502	S<211>	-4613	473
183	CKN	242.5	-500	843	S<870>	4613	338	1503	S<210>	-4627	338
184	CKN	302.5	-500	844	S<869>	4599	473	1504	S<209>	-4641	473
185	CKN	362.5	-500	845	S<868>	4585	338	1505	S<208>	-4655	338
186	VSSPHY	422.5	-500	846	S<867>	4571	473	1506	S<207>	-4669	473
187	D0P	482.5	-500	847	S<866>	4557	338	1507	S<206>	-4683	338
188	D0P	542.5	-500	848	S<865>	4543	473	1508	S<205>	-4697	473
189	D0P	602.5	-500	849	S<864>	4529	338	1509	S<204>	-4711	338
190	D0P	662.5	-500	850	S<863>	4515	473	1510	S<203>	-4725	473
191	D0N	722.5	-500	851	S<862>	4501	338	1511	S<202>	-4739	338
192	D0N	782.5	-500	852	S<861>	4487	473	1512	S<201>	-4753	473
193	D0N	842.5	-500	853	S<860>	4473	338	1513	S<200>	-4767	338
194	D0N	902.5	-500	854	S<859>	4459	473	1514	S<199>	-4781	473
195	VSSPHY	962.5	-500	855	S<858>	4445	338	1515	S<198>	-4795	338
196	MIPI_IREF	1022.5	-500	856	S<857>	4431	473	1516	S<197>	-4809	473
197	MIPI_VREF	1082.5	-500	857	S<856>	4417	338	1517	S<196>	-4823	338
198	MIPI_VTEST	1142.5	-500	858	S<855>	4403	473	1518	S<195>	-4837	473
199	VDDLP	1202.5	-500	859	S<854>	4389	338	1519	S<194>	-4851	338
200	VDDLP	1262.5	-500	860	S<853>	4375	473	1520	S<193>	-4865	473
201	VDDLP	1322.5	-500	861	S<852>	4361	338	1521	S<192>	-4879	338
202	VDDPHY	1382.5	-500	862	S<851>	4347	473	1522	S<191>	-4893	473
203	VDDPHY	1442.5	-500	863	S<850>	4333	338	1523	S<190>	-4907	338
204	VDDPHY	1502.5	-500	864	S<849>	4319	473	1524	S<189>	-4921	473
205	VSSPHY	1562.5	-500	865	S<848>	4305	338	1525	S<188>	-4935	338
206	VSSPHY	1622.5	-500	866	S<847>	4291	473	1526	S<187>	-4949	473
207	VSSPHY	1682.5	-500	867	S<846>	4277	338	1527	S<186>	-4963	338
208	VSSPHY	1742.5	-500	868	S<845>	4263	473	1528	S<185>	-4977	473
209	VSSPHY	1802.5	-500	869	S<844>	4249	338	1529	S<184>	-4991	338
210	VSSPHY	1862.5	-500	870	S<843>	4235	473	1530	S<183>	-5005	473
211	VDD3_MIPI	1922.5	-500	871	S<842>	4221	338	1531	S<182>	-5019	338
212	VDD3_MIPI	1982.5	-500	872	S<841>	4207	473	1532	S<181>	-5033	473
213	VDD3_MIPI	2042.5	-500	873	S<840>	4193	338	1533	S<180>	-5047	338
214	VDD3_MIPI	2102.5	-500	874	S<839>	4179	473	1534	S<179>	-5061	473

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
215	VDD3_MIPI	2162.5	-500	875	S<838>	4165	338	1535	S<178>	-5075	338
216	VDD3_MIPI	2222.5	-500	876	S<837>	4151	473	1536	S<177>	-5089	473
217	VSS3	2282.5	-500	877	S<836>	4137	338	1537	S<176>	-5103	338
218	VSS3	2342.5	-500	878	S<835>	4123	473	1538	S<175>	-5117	473
219	VSS3	2402.5	-500	879	S<834>	4109	338	1539	S<174>	-5131	338
220	VSS3	2462.5	-500	880	S<833>	4095	473	1540	S<173>	-5145	473
221	VSS3	2522.5	-500	881	S<832>	4081	338	1541	S<172>	-5159	338
222	VSS3	2582.5	-500	882	S<831>	4067	473	1542	S<171>	-5173	473
223	VSS	2642.5	-500	883	S<830>	4053	338	1543	S<170>	-5187	338
224	VSS	2702.5	-500	884	S<829>	4039	473	1544	S<169>	-5201	473
225	VSS	2762.5	-500	885	S<828>	4025	338	1545	S<168>	-5215	338
226	VSS	2822.5	-500	886	S<827>	4011	473	1546	S<167>	-5229	473
227	VSS	2882.5	-500	887	S<826>	3997	338	1547	S<166>	-5243	338
228	VSS	2942.5	-500	888	S<825>	3983	473	1548	S<165>	-5257	473
229	VSS	3002.5	-500	889	S<824>	3969	338	1549	S<164>	-5271	338
230	VSS	3062.5	-500	890	S<823>	3955	473	1550	S<163>	-5285	473
231	VSS	3122.5	-500	891	S<822>	3941	338	1551	S<162>	-5299	338
232	VSS	3182.5	-500	892	S<821>	3927	473	1552	S<161>	-5313	473
233	VDD	3242.5	-500	893	S<820>	3913	338	1553	S<160>	-5327	338
234	VDD	3302.5	-500	894	S<819>	3899	473	1554	S<159>	-5341	473
235	VDD	3362.5	-500	895	S<818>	3885	338	1555	S<158>	-5355	338
236	VDD	3422.5	-500	896	S<817>	3871	473	1556	S<157>	-5369	473
237	VDD	3482.5	-500	897	S<816>	3857	338	1557	S<156>	-5383	338
238	VDD	3542.5	-500	898	S<815>	3843	473	1558	S<155>	-5397	473
239	VDD	3602.5	-500	899	S<814>	3829	338	1559	S<154>	-5411	338
240	VDD	3662.5	-500	900	S<813>	3815	473	1560	S<153>	-5425	473
241	VDD	3722.5	-500	901	S<812>	3801	338	1561	S<152>	-5439	338
242	VDD	3782.5	-500	902	S<811>	3787	473	1562	S<151>	-5453	473
243	VDD3	3842.5	-500	903	S<810>	3773	338	1563	S<150>	-5467	338
244	VDD3	3902.5	-500	904	S<809>	3759	473	1564	S<149>	-5481	473
245	VDD3	3962.5	-500	905	S<808>	3745	338	1565	S<148>	-5495	338
246	VDD3	4022.5	-500	906	S<807>	3731	473	1566	S<147>	-5509	473
247	VDD3	4082.5	-500	907	S<806>	3717	338	1567	S<146>	-5523	338
248	VDD3	4142.5	-500	908	S<805>	3703	473	1568	S<145>	-5537	473
249	VDD3	4202.5	-500	909	S<804>	3689	338	1569	S<144>	-5551	338
250	VDD3	4262.5	-500	910	S<803>	3675	473	1570	S<143>	-5565	473

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
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252	SDA	4395	-500	912	S<801>	3647	473	1572	S<141>	-5593	473
253	SDO	4480	-500	913	S<800>	3633	338	1573	S<140>	-5607	338
254	TE	4565	-500	914	S<799>	3619	473	1574	S<139>	-5621	473
255	BC	4650	-500	915	S<798>	3605	338	1575	S<138>	-5635	338
256	BC_CTL	4735	-500	916	S<797>	3591	473	1576	S<137>	-5649	473
257	VDD3_P	4820	-500	917	S<796>	3577	338	1577	S<136>	-5663	338
258	VDD3_P	4905	-500	918	S<795>	3563	473	1578	S<135>	-5677	473
259	EXCLK	4977.5	-500	919	S<794>	3549	338	1579	S<134>	-5691	338
260	TMODE<3>	5037.5	-500	920	S<793>	3535	473	1580	S<133>	-5705	473
261	TMODE<2>	5097.5	-500	921	S<792>	3521	338	1581	S<132>	-5719	338
262	TMODE<1>	5157.5	-500	922	S<791>	3507	473	1582	S<131>	-5733	473
263	TMODE<0>	5217.5	-500	923	S<790>	3493	338	1583	S<130>	-5747	338
264	TMUX<2>	5277.5	-500	924	S<789>	3479	473	1584	S<129>	-5761	473
265	TMUX<1>	5337.5	-500	925	S<788>	3465	338	1585	S<128>	-5775	338
266	TMUX<0>	5397.5	-500	926	S<787>	3451	473	1586	S<127>	-5789	473
267	TIN2	5457.5	-500	927	S<786>	3437	338	1587	S<126>	-5803	338
268	TREGB	5517.5	-500	928	S<785>	3423	473	1588	S<125>	-5817	473
269	VSSA	5577.5	-500	929	S<784>	3409	338	1589	S<124>	-5831	338
270	VSSA	5637.5	-500	930	S<783>	3395	473	1590	S<123>	-5845	473
271	VSSA	5697.5	-500	931	S<782>	3381	338	1591	S<122>	-5859	338
272	VSSA	5757.5	-500	932	S<781>	3367	473	1592	S<121>	-5873	473
273	VSSA	5817.5	-500	933	S<780>	3353	338	1593	S<120>	-5887	338
274	VSSA	5877.5	-500	934	S<779>	3339	473	1594	S<119>	-5901	473
275	VSSA	5937.5	-500	935	S<778>	3325	338	1595	S<118>	-5915	338
276	VSSA	5997.5	-500	936	S<777>	3311	473	1596	S<117>	-5929	473
277	VCIR2	6057.5	-500	937	S<776>	3297	338	1597	S<116>	-5943	338
278	VCIR	6117.5	-500	938	S<775>	3283	473	1598	S<115>	-5957	473
279	GVDD	6177.5	-500	939	S<774>	3269	338	1599	S<114>	-5971	338
280	GVDD	6237.5	-500	940	S<773>	3255	473	1600	S<113>	-5985	473
281	GVDD	6297.5	-500	941	S<772>	3241	338	1601	S<112>	-5999	338
282	GVDD	6357.5	-500	942	S<771>	3227	473	1602	S<111>	-6013	473
283	VCOMH	6417.5	-500	943	S<770>	3213	338	1603	S<110>	-6027	338
284	VCOMH	6477.5	-500	944	S<769>	3199	473	1604	S<109>	-6041	473
285	VCOMH	6537.5	-500	945	S<768>	3185	338	1605	S<108>	-6055	338
286	VCOMH	6597.5	-500	946	S<767>	3171	473	1606	S<107>	-6069	473

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
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288	VCOML	6717.5	-500	948	S<765>	3143	473	1608	S<105>	-6097	473
289	VCOML	6777.5	-500	949	S<764>	3129	338	1609	S<104>	-6111	338
290	VCOML	6837.5	-500	950	S<763>	3115	473	1610	S<103>	-6125	473
291	VCI_DUMMY	6897.5	-500	951	S<762>	3101	338	1611	S<102>	-6139	338
292	VCI_DUMMY	6957.5	-500	952	S<761>	3087	473	1612	S<101>	-6153	473
293	VCI_DUMMY	7017.5	-500	953	S<760>	3073	338	1613	S<100>	-6167	338
294	VCI_DUMMY	7077.5	-500	954	S<759>	3059	473	1614	S<99>	-6181	473
295	VSSC	7137.5	-500	955	S<758>	3045	338	1615	S<98>	-6195	338
296	VSSC	7197.5	-500	956	S<757>	3031	473	1616	S<97>	-6209	473
297	VSSC	7257.5	-500	957	S<756>	3017	338	1617	S<96>	-6223	338
298	VSSC	7317.5	-500	958	S<755>	3003	473	1618	S<95>	-6237	473
299	VSSC	7377.5	-500	959	S<754>	2989	338	1619	S<94>	-6251	338
300	VSSC	7437.5	-500	960	S<753>	2975	473	1620	S<93>	-6265	473
301	VSSC	7497.5	-500	961	S<752>	2961	338	1621	S<92>	-6279	338
302	VSSC	7557.5	-500	962	S<751>	2947	473	1622	S<91>	-6293	473
303	C13M	7617.5	-500	963	S<750>	2933	338	1623	S<90>	-6307	338
304	C13M	7677.5	-500	964	S<749>	2919	473	1624	S<89>	-6321	473
305	C13M	7737.5	-500	965	S<748>	2905	338	1625	S<88>	-6335	338
306	C13M	7797.5	-500	966	S<747>	2891	473	1626	S<87>	-6349	473
307	C13P	7857.5	-500	967	S<746>	2877	338	1627	S<86>	-6363	338
308	C13P	7917.5	-500	968	S<745>	2863	473	1628	S<85>	-6377	473
309	C13P	7977.5	-500	969	S<744>	2849	338	1629	S<84>	-6391	338
310	C13P	8037.5	-500	970	S<743>	2835	473	1630	S<83>	-6405	473
311	C14M	8097.5	-500	971	S<742>	2821	338	1631	S<82>	-6419	338
312	C14M	8157.5	-500	972	S<741>	2807	473	1632	S<81>	-6433	473
313	C14M	8217.5	-500	973	S<740>	2793	338	1633	S<80>	-6447	338
314	C14M	8277.5	-500	974	S<739>	2779	473	1634	S<79>	-6461	473
315	C14P	8337.5	-500	975	S<738>	2765	338	1635	S<78>	-6475	338
316	C14P	8397.5	-500	976	S<737>	2751	473	1636	S<77>	-6489	473
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514	G<292>	9219	473	1174	S<539>	-21	473	1834	G<285>	-9261	473
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516	G<296>	9191	473	1176	S<537>	-49	473	1836	G<281>	-9289	473
517	G<298>	9177	338	1177	S<536>	-63	338	1837	G<279>	-9303	338
518	G<300>	9163	473	1178	S<535>	-77	473	1838	G<277>	-9317	473
519	G<302>	9149	338	1179	S<534>	-91	338	1839	G<275>	-9331	338
520	G<304>	9135	473	1180	S<533>	-105	473	1840	G<273>	-9345	473
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522	G<308>	9107	473	1182	S<531>	-133	473	1842	G<269>	-9373	473
523	G<310>	9093	338	1183	S<530>	-147	338	1843	G<267>	-9387	338
524	G<312>	9079	473	1184	S<529>	-161	473	1844	G<265>	-9401	473
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526	G<316>	9051	473	1186	S<527>	-189	473	1846	G<261>	-9429	473
527	G<318>	9037	338	1187	S<526>	-203	338	1847	G<259>	-9443	338
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536	G<336>	8911	473	1196	S<517>	-329	473	1856	G<241>	-9569	473
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546	G<356>	8771	473	1206	S<507>	-469	473	1866	G<221>	-9709	473
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550	G<364>	8715	473	1210	S<503>	-525	473	1870	G<213>	-9765	473
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552	G<368>	8687	473	1212	S<501>	-553	473	1872	G<209>	-9793	473
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566	G<396>	8491	473	1226	S<487>	-749	473	1886	G<181>	-9989	473
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571	G<406>	8421	338	1231	S<482>	-819	338	1891	G<171>	-10059	338
572	G<408>	8407	473	1232	S<481>	-833	473	1892	G<169>	-10073	473
573	G<410>	8393	338	1233	S<480>	-847	338	1893	G<167>	-10087	338
574	G<412>	8379	473	1234	S<479>	-861	473	1894	G<165>	-10101	473

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576	G<416>	8351	473	1236	S<477>	-889	473	1896	G<161>	-10129	473
577	G<418>	8337	338	1237	S<476>	-903	338	1897	G<159>	-10143	338
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579	G<422>	8309	338	1239	S<474>	-931	338	1899	G<155>	-10171	338
580	G<424>	8295	473	1240	S<473>	-945	473	1900	G<153>	-10185	473
581	G<426>	8281	338	1241	S<472>	-959	338	1901	G<151>	-10199	338
582	G<428>	8267	473	1242	S<471>	-973	473	1902	G<149>	-10213	473
583	G<430>	8253	338	1243	S<470>	-987	338	1903	G<147>	-10227	338
584	G<432>	8239	473	1244	S<469>	-1001	473	1904	G<145>	-10241	473
585	G<434>	8225	338	1245	S<468>	-1015	338	1905	G<143>	-10255	338
586	G<436>	8211	473	1246	S<467>	-1029	473	1906	G<141>	-10269	473
587	G<438>	8197	338	1247	S<466>	-1043	338	1907	G<139>	-10283	338
588	G<440>	8183	473	1248	S<465>	-1057	473	1908	G<137>	-10297	473
589	G<442>	8169	338	1249	S<464>	-1071	338	1909	G<135>	-10311	338
590	G<444>	8155	473	1250	S<463>	-1085	473	1910	G<133>	-10325	473
591	G<446>	8141	338	1251	S<462>	-1099	338	1911	G<131>	-10339	338
592	G<448>	8127	473	1252	S<461>	-1113	473	1912	G<129>	-10353	473
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598	G<460>	8043	473	1258	S<455>	-1197	473	1918	G<117>	-10437	473
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600	G<464>	8015	473	1260	S<453>	-1225	473	1920	G<113>	-10465	473
601	G<466>	8001	338	1261	S<452>	-1239	338	1921	G<111>	-10479	338
602	G<468>	7987	473	1262	S<451>	-1253	473	1922	G<109>	-10493	473
603	G<470>	7973	338	1263	S<450>	-1267	338	1923	G<107>	-10507	338
604	G<472>	7959	473	1264	S<449>	-1281	473	1924	G<105>	-10521	473
605	G<474>	7945	338	1265	S<448>	-1295	338	1925	G<103>	-10535	338
606	G<476>	7931	473	1266	S<447>	-1309	473	1926	G<101>	-10549	473
607	G<478>	7917	338	1267	S<446>	-1323	338	1927	G<99>	-10563	338
608	G<480>	7903	473	1268	S<445>	-1337	473	1928	G<97>	-10577	473
609	DUMMY<14>	7889	338	1269	S<444>	-1351	338	1929	G<95>	-10591	338
610	DUMMY<15>	7875	473	1270	S<443>	-1365	473	1930	G<93>	-10605	473

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612	DUMMY<17>	7847	473	1272	S<441>	-1393	473	1932	G<89>	-10633	473
613	DUMMY<18>	7833	338	1273	S<440>	-1407	338	1933	G<87>	-10647	338
614	DUMMY<19>	7819	473	1274	S<439>	-1421	473	1934	G<85>	-10661	473
615	DUMMY<20>	7805	338	1275	S<438>	-1435	338	1935	G<83>	-10675	338
616	DUMMY<21>	7791	473	1276	S<437>	-1449	473	1936	G<81>	-10689	473
617	DUMMY<22>	7777	338	1277	S<436>	-1463	338	1937	G<79>	-10703	338
618	DUMMY<23>	7763	473	1278	S<435>	-1477	473	1938	G<77>	-10717	473
619	DUMMY<24>	7749	338	1279	S<434>	-1491	338	1939	G<75>	-10731	338
620	DUMMY<25>	7735	473	1280	S<433>	-1505	473	1940	G<73>	-10745	473
621	DUMMY<26>	7721	338	1281	S<432>	-1519	338	1941	G<71>	-10759	338
622	DUMMY<27>	7707	473	1282	S<431>	-1533	473	1942	G<69>	-10773	473
623	DUMMY<28>	7693	338	1283	S<430>	-1547	338	1943	G<67>	-10787	338
624	DUMMY<29>	7679	473	1284	S<429>	-1561	473	1944	G<65>	-10801	473
625	DUMMY<30>	7665	338	1285	S<428>	-1575	338	1945	G<63>	-10815	338
626	DUMMY<31>	7651	473	1286	S<427>	-1589	473	1946	G<61>	-10829	473
627	DUMMY<32>	7637	338	1287	S<426>	-1603	338	1947	G<59>	-10843	338
628	DUMMY<33>	7623	473	1288	S<425>	-1617	473	1948	G<57>	-10857	473
629	DUMMY<34>	7609	338	1289	S<424>	-1631	338	1949	G<55>	-10871	338
630	DUMMY<35>	7595	473	1290	S<423>	-1645	473	1950	G<53>	-10885	473
631	DUMMY<36>	7581	338	1291	S<422>	-1659	338	1951	G<51>	-10899	338
632	DUMMY<37>	7567	473	1292	S<421>	-1673	473	1952	G<49>	-10913	473
633	S<1080>	7553	338	1293	S<420>	-1687	338	1953	G<47>	-10927	338
634	S<1079>	7539	473	1294	S<419>	-1701	473	1954	G<45>	-10941	473
635	S<1078>	7525	338	1295	S<418>	-1715	338	1955	G<43>	-10955	338
636	S<1077>	7511	473	1296	S<417>	-1729	473	1956	G<41>	-10969	473
637	S<1076>	7497	338	1297	S<416>	-1743	338	1957	G<39>	-10983	338
638	S<1075>	7483	473	1298	S<415>	-1757	473	1958	G<37>	-10997	473
639	S<1074>	7469	338	1299	S<414>	-1771	338	1959	G<35>	-11011	338
640	S<1073>	7455	473	1300	S<413>	-1785	473	1960	G<33>	-11025	473
641	S<1072>	7441	338	1301	S<412>	-1799	338	1961	G<31>	-11039	338
642	S<1071>	7427	473	1302	S<411>	-1813	473	1962	G<29>	-11053	473
643	S<1070>	7413	338	1303	S<410>	-1827	338	1963	G<27>	-11067	338
644	S<1069>	7399	473	1304	S<409>	-1841	473	1964	G<25>	-11081	473
645	S<1068>	7385	338	1305	S<408>	-1855	338	1965	G<23>	-11095	338
646	S<1067>	7371	473	1306	S<407>	-1869	473	1966	G<21>	-11109	473

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648	S<1065>	7343	473	1308	S<405>	-1897	473	1968	G<17>	-11137	473
649	S<1064>	7329	338	1309	S<404>	-1911	338	1969	G<15>	-11151	338
650	S<1063>	7315	473	1310	S<403>	-1925	473	1970	G<13>	-11165	473
651	S<1062>	7301	338	1311	S<402>	-1939	338	1971	G<11>	-11179	338
652	S<1061>	7287	473	1312	S<401>	-1953	473	1972	G<9>	-11193	473
653	S<1060>	7273	338	1313	S<400>	-1967	338	1973	G<7>	-11207	338
654	S<1059>	7259	473	1314	S<399>	-1981	473	1974	G<5>	-11221	473
655	S<1058>	7245	338	1315	S<398>	-1995	338	1975	G<3>	-11235	338
656	S<1057>	7231	473	1316	S<397>	-2009	473	1976	G<1>	-11249	473
657	S<1056>	7217	338	1317	S<396>	-2023	338	1977	DUMMY<62>	-11263	338
658	S<1055>	7203	473	1318	S<395>	-2037	473	1978	DUMMY<63>	-11277	473
659	S<1054>	7189	338	1319	S<394>	-2051	338	1979	DUMMY<64>	-11291	338
660	S<1053>	7175	473	1320	S<393>	-2065	473	1980	DUMMY<65>	-11305	473

6.4 DISPLAY MODULE DEFAULT POSITION

The default position (display driver, glass, filter order, etc) of the display module is always as follow, when MADCTL's (36h) parameter is D0h. The color filter is always RGB (if color filters are used).

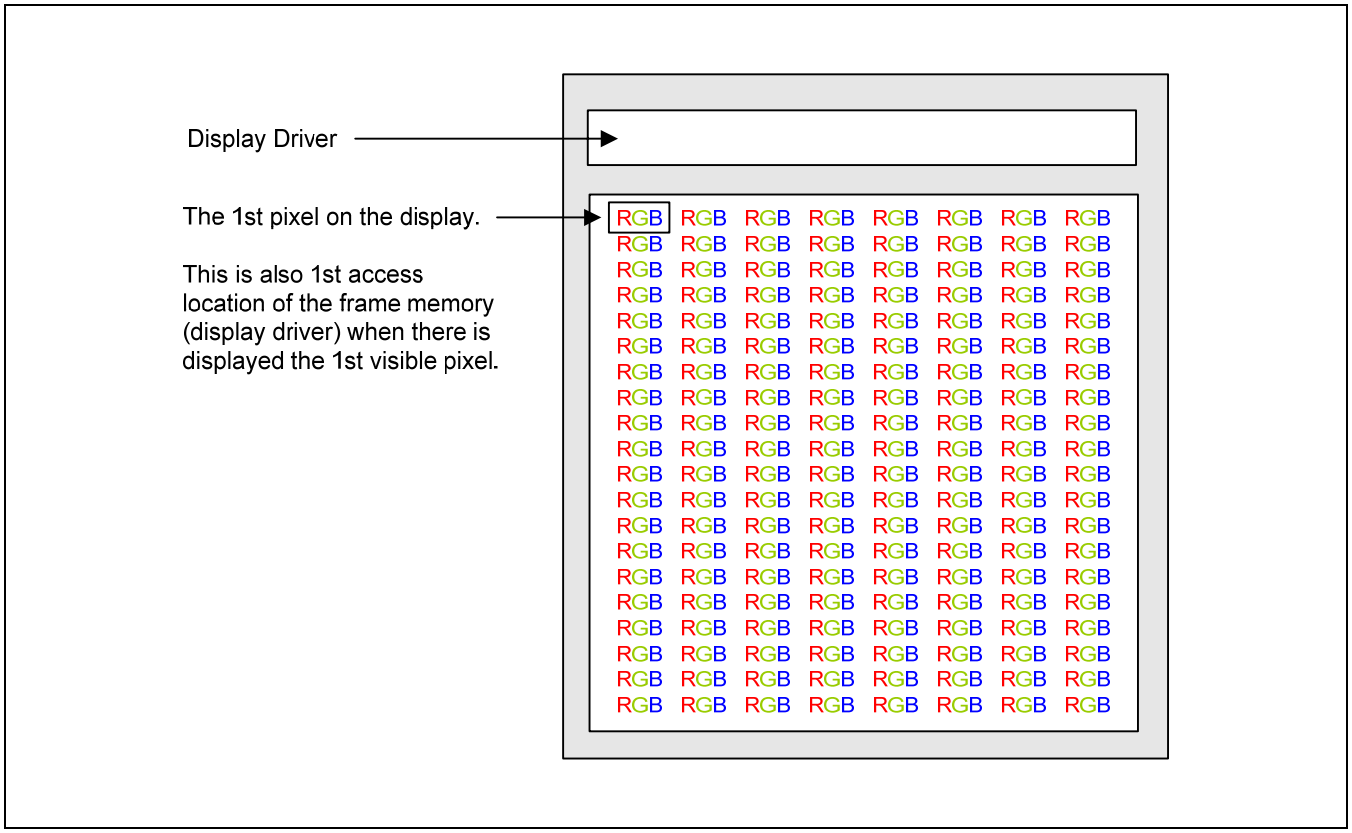

Figure 201 Display Module Default Position