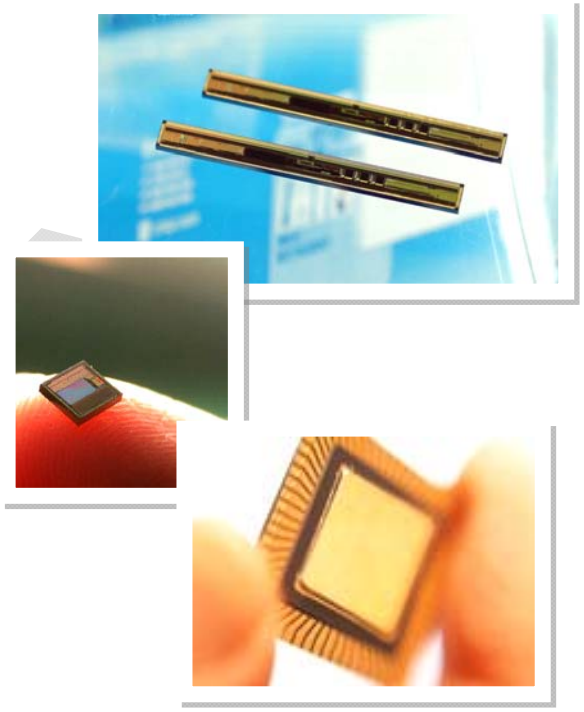
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation



RM68090 Data Sheet

Single Chip Driver with 262K color

for 240RGBx320 a-Si TFT LCD

Revision：0.4

Date：Apr. 27, 2011

Revision History：

Revision	Description Of Change	Date
0.1	New creation	2010/7/2
0.2	Modified descriptions of EPF:16bits Data Format Selection (R05h)	2010/11/09
0.3	(4) IC thickness ; (9.4, 10) Instruction R00h description ; (24.2.3) Tsyncs	2010/12/02
0.4	(a) Modified pin description of VDDI_LED(page 24) (b) Modified pin description of LEDON and LEDPWM(page 26) (c) Add CABC control instructions, RB1h ~ RBFh(page 62 ~ 64) (d) Add Brightness Control ON/OFF sequence(page 116)	2011/04/27

Table of Content

1. General Description

The RM68090 is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, comprising 172,800 bytes RAM for a maximum 240 RGB x 320 dots graphics display, source driver, gate driver and power supply circuit. For efficient data transfer, the RM68090 supports high-speed interface via 8-/9-/16-/18-bit ports as system interface to the microcomputer and high-speed RAM write function. As moving picture interface, the RM68090 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and DB17-0).

Also, the RM68090 incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages.

The RM68090's power management functions such as 8-color display and power operation mode such as deep standby mode, standby mode and sleep mode make this LSI a perfect driver for the medium or small sized portable products with color display systems such as digital cellular phones or hand-held devices with outstanding battery consistency.

2. Features

- A single-chip controller driver incorporating a gate circuit and a power supply circuit for a maximum 240 RGB x 320 dots graphics display on amorphous TFT panel in 262k colors
- System interface
  1. High-speed interface via 8-, 9-, 16-, 18-bit parallel ports
  2. Clock synchronous serial interface
- Moving picture display interface
  1. 6-, 16-, 18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  2. VSYNC interface (System interface + VSYNC)
  3. FMARK interface (System interface + FMARK)
- High-speed RAM write function
- Window address function to specify a rectangular area writing data in the internal RAM
- Write data within a rectangular area in the internal RAM via moving picture interface

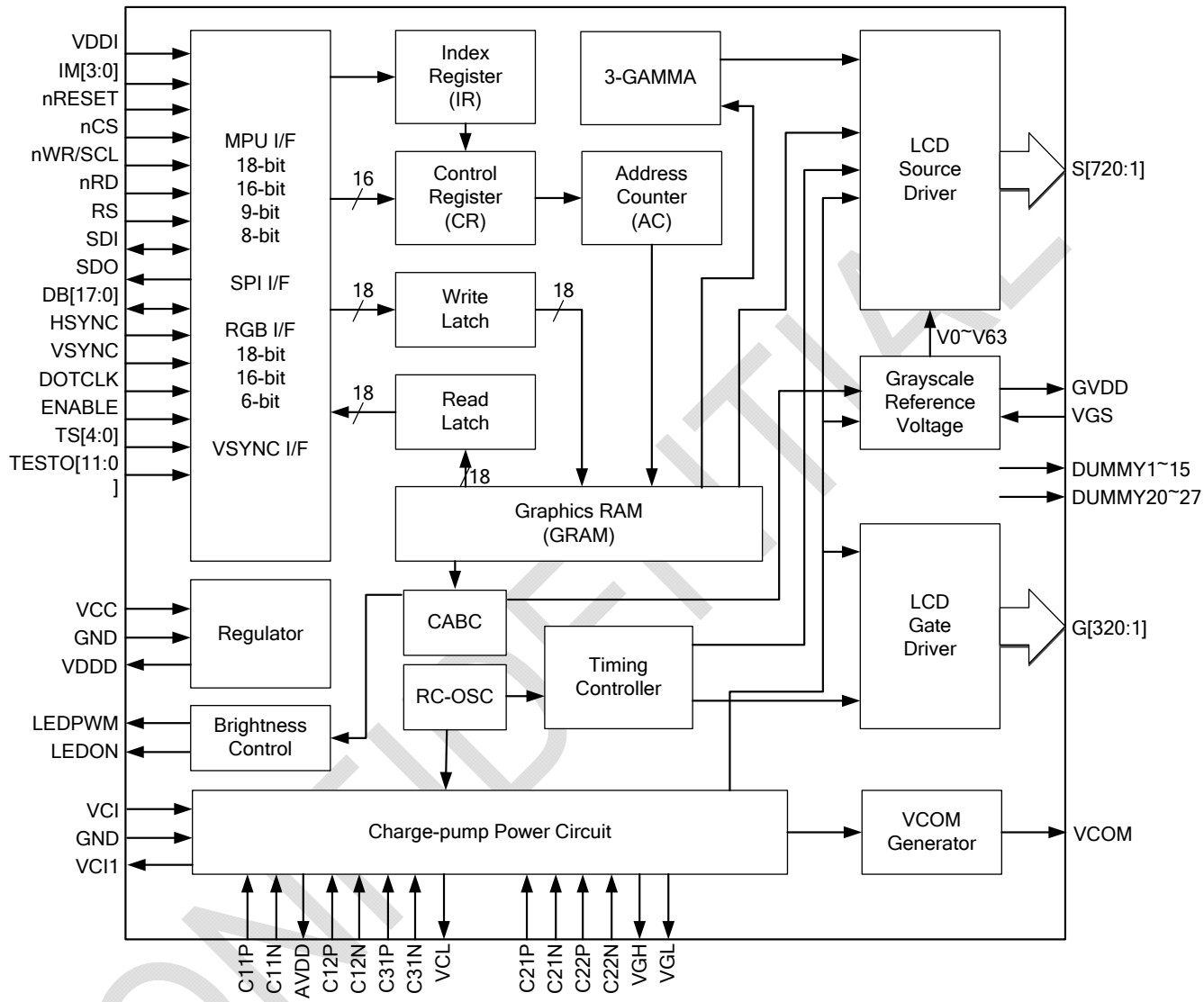
- Reduce data transfer repeat by specifying the area in the RAM to rewrite data
- Support displaying still picture data in RAM area while displaying moving pictures simultaneously
- Resizing function (x 1/2, x 1/4) with remainder consideration
- Abundant color display and drawing functions
  1. Programmable γ-correction function for 262k-color display
  2. Partial display function
- Low power consumption architecture (allowing direct input of interface I/O power supply)
  1. Deep standby mode
  2. Standby mode
  3. Sleep mode
  4. 8-color display function
  5. Input power supply voltages: VDDI = 1.65V~3.3V (interface I/O power supply)
     VCI = 2.5V~3.3V (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
  1. Source driver liquid crystal drive/VCOM power supply: AVDD-GND = 4.5V ~ 6.0V
     VCL-GND = -2.2V ~ -3.0V
     VCI-VCL ≦ 6.0V
  2. Gate drive power supply: VGH-GND = 10.0V ~ 19.8V
     VGL-GND = -4.5V ~ -13.5V
     VGH-VGL ≦ 28.0V
  3. VCOM drive (VCOM power supply): VCOMH = 3.0V ~ (AVDD-0.5)V
     VCOML = (VCL+0.5) V ~ 0V
     VCOMH-VCOML amplitude = 6.0V (max.)
- Liquid crystal power supply startup sequencer
- TFT storage capacitance: Cst only (common VCOM formula)

- 172,800-byte internal RAM
- Internal 720-channel source driver and 320-channel gate driver
- Single-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- Internal reference voltage: to generate GVDD
- Internal NVM: VCOM level adjustment, 6 bits x 3 sets

Table 1 Power Supply Specifications

No.	Item		RM68090
1	TFT data lines		720 output
2	TFT gate lines		320 output
3	TFT display storage capacitance		Cst only (Common VCOM)
4	Liquid crystal drive output	S1~S720	V0~V63 grayscales
		G1~G320	VGH-VGL
		VCOM	Change VCOMH-VCOML amplitude with electronic volume Change VCOMH with electronic volume
5	Input voltage	VDDI (interface voltage)	1.65V~3.30V Power supply to IM0/ID, IM1-3, nRESET, DB17-0, nRD, SDI, SDO, WR/SCL, RS, nCS, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK. Connect to VCC and VCI on the FPC when the electrical potentials are the same.
		VCI (liquid crystal drive power supply voltage)	2.50V~3.30V Connect to VDDI and VCI on the FPC when the electrical potentials are the same.
6	Liquid crystal drive voltages	AVDD	4.5V ~ 6.0V
		VGH	10.0V ~ 19.8V
		VGL	-4.5V ~ -13.5V
		VGH-VGL	Max. 28.0V
		VCL	-2.2V ~ -3.3V
		VCI-VCL	Max. 6.0V
7	Internal step-up circuits	VLOUT1 (AVDD)	VCI1x2
		VLOUT2 (VGH)	VCI1x4, x5, x6
		VLOUT3 (VGL)	VCI1x-3, -4, -5
		VCL	VCI1x-1

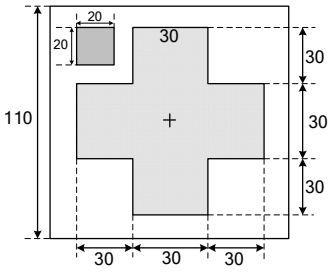
3. Block Diagram



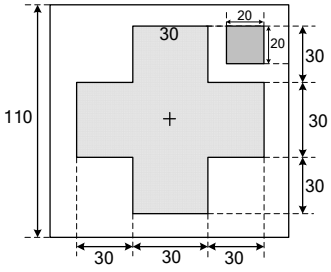
4. Pin Diagram

Alignment Marks

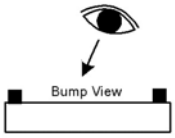
A1

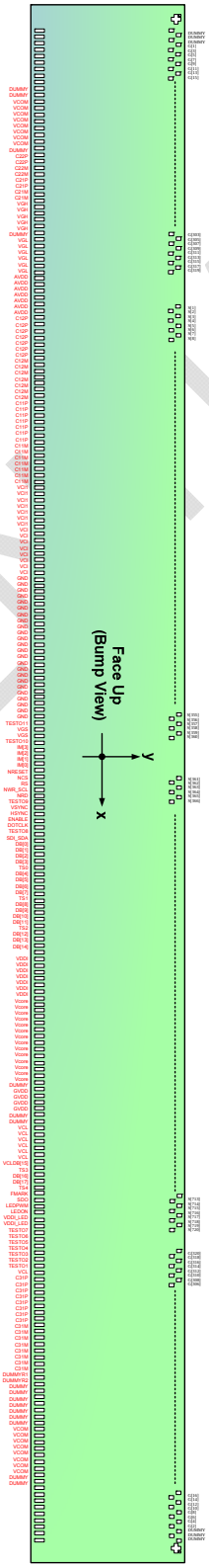


A2



Unit: um





- Chip size: 16.20 mm x 0.72 mm (Include sealing and scribe line)
- Chip thickness: 300 um (typ.)
- PAD coordinates: PAD center
- PAD coordinates origin: Chip center
- Au bump size

4.1.1 14um x 104um: Output Pads to Panel

4.1.2 40um x 56um: Input Pads

- Au bump pitch: See PAD coordinates table
- Au bump height: 12um (typ.)
- Alignment mark

Alignment mark shape	X	Y
Type A	-7480	254
	7480	254

Pad Coordinate (Unit: um)

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-7292.5	-279	61	C11M	-3692.5	-279	121	HSYNC	-92.5	-279	181	Vcore	4232.5	-279
2	DUMMY	-7232.5	-279	62	C11M	-3632.5	-279	122	ENABLE	-32.5	-279	182	Vcore	4292.5	-279
3	VCOM	-7172.5	-279	63	C11M	-3572.5	-279	123	DOTCLK	27.5	-279	183	DUMMY	4352.5	-279
4	VCOM	-7112.5	-279	64	C11M	-3512.5	-279	124	TESTO8	87.5	-279	184	GVDD	4412.5	-279
5	VCOM	-7052.5	-279	65	C11M	-3452.5	-279	125	SDI_SDA	160	-279	185	GVDD	4472.5	-279
6	VCOM	-6992.5	-279	66	C11M	-3392.5	-279	126	DB[0]	245	-279	186	GVDD	4532.5	-279
7	VCOM	-6932.5	-279	67	VCI1	-3332.5	-279	127	DB[1]	330	-279	187	GVDD	4592.5	-279
8	VCOM	-6872.5	-279	68	VCI1	-3272.5	-279	128	DB[2]	415	-279	188	DUMMY	4652.5	-279
9	VCOM	-6812.5	-279	69	VCI1	-3212.5	-279	129	DB[3]	500	-279	189	DUMMY	4712.5	-279
10	VCOM	-6752.5	-279	70	VCI1	-3152.5	-279	130	TS0	572.5	-279	190	VCL	4772.5	-279
11	DUMMY	-6692.5	-279	71	VCI1	-3092.5	-279	131	DB[4]	645	-279	191	VCL	4832.5	-279
12	C22P	-6632.5	-279	72	VCI1	-3032.5	-279	132	DB[5]	730	-279	192	VCL	4892.5	-279
13	C22P	-6572.5	-279	73	VCI1	-2972.5	-279	133	DB[6]	815	-279	193	VCL	4952.5	-279
14	C22M	-6512.5	-279	74	VCI	-2912.5	-279	134	DB[7]	900	-279	194	VCL	5012.5	-279
15	C22M	-6452.5	-279	75	VCI	-2852.5	-279	135	TS1	972.5	-279	195	VCL	5072.5	-279
16	C21P	-6392.5	-279	76	VCI	-2792.5	-279	136	DB[8]	1045	-279	196	VCL	5132.5	-279
17	C21P	-6332.5	-279	77	VCI	-2732.5	-279	137	DB[9]	1130	-279	197	VCL	5192.5	-279
18	C21M	-6272.5	-279	78	VCI	-2672.5	-279	138	DB[10]	1215	-279	198	C31P	5252.5	-279
19	C21M	-6212.5	-279	79	VCI	-2612.5	-279	139	DB[11]	1300	-279	199	C31P	5312.5	-279
20	VGH	-6152.5	-279	80	VCI	-2552.5	-279	140	TS2	1372.5	-279	200	C31P	5372.5	-279
21	VGH	-6092.5	-279	81	VCI	-2492.5	-279	141	DB[12]	1445	-279	201	C31P	5432.5	-279
22	VGH	-6032.5	-279	82	GND	-2432.5	-279	142	DB[13]	1530	-279	202	C31P	5492.5	-279
23	VGH	-5972.5	-279	83	GND	-2372.5	-279	143	DB[14]	1615	-279	203	C31P	5552.5	-279
24	VGH	-5912.5	-279	84	GND	-2312.5	-279	144	DB[15]	1700	-279	204	C31P	5612.5	-279
25	DUMMY	-5852.5	-279	85	GND	-2252.5	-279	145	TS3	1772.5	-279	205	C31P	5672.5	-279
26	VGL	-5792.5	-279	86	GND	-2192.5	-279	146	DB[16]	1845	-279	206	C31M	5732.5	-279
27	VGL	-5732.5	-279	87	GND	-2132.5	-279	147	DB[17]	1930	-279	207	C31M	5792.5	-279
28	VGL	-5672.5	-279	88	GND	-2072.5	-279	148	TS4	2002.5	-279	208	C31M	5852.5	-279
29	VGL	-5612.5	-279	89	GND	-2012.5	-279	149	FMARK	2075	-279	209	C31M	5912.5	-279
30	VGL	-5552.5	-279	90	GND	-1952.5	-279	150	SDO	2160	-279	210	C31M	5972.5	-279
31	VGL	-5492.5	-279	91	GND	-1892.5	-279	151	LEDPWM	2245	-279	211	C31M	6032.5	-279
32	AVDD	-5432.5	-279	92	GND	-1832.5	-279	152	LEDON	2330	-279	212	C31M	6092.5	-279
33	AVDD	-5372.5	-279	93	GND	-1772.5	-279	153	VDDI_LED	2402.5	-279	213	C31M	6152.5	-279
34	AVDD	-5312.5	-279	94	GND	-1712.5	-279	154	VDDI_LED	2462.5	-279	214	DUMMYR1	6212.5	-279
35	AVDD	-5252.5	-279	95	GND	-1652.5	-279	155	TESTO7	2535	-279	215	DUMMYR2	6272.5	-279
36	AVDD	-5192.5	-279	96	GND	-1592.5	-279	156	TESTO6	2620	-279	216	DUMMY	6332.5	-279
37	AVDD	-5132.5	-279	97	GND	-1532.5	-279	157	TESTO5	2705	-279	217	DUMMY	6392.5	-279
38	AVDD	-5072.5	-279	98	GND	-1472.5	-279	158	TESTO4	2790	-279	218	DUMMY	6452.5	-279
39	C12P	-5012.5	-279	99	GND	-1412.5	-279	159	TESTO3	2875	-279	219	DUMMY	6512.5	-279
40	C12P	-4952.5	-279	100	GND	-1352.5	-279	160	TESTO2	2960	-279	220	DUMMY	6572.5	-279
41	C12P	-4892.5	-279	101	GND	-1292.5	-279	161	TESTO1	3032.5	-279	221	DUMMY	6632.5	-279
42	C12P	-4832.5	-279	102	GND	-1232.5	-279	162	VDDI	3092.5	-279	222	DUMMY	6692.5	-279
43	C12P	-4772.5	-279	103	GND	-1172.5	-279	163	VDDI	3152.5	-279	223	VCOM	6752.5	-279
44	C12P	-4712.5	-279	104	GND	-1112.5	-279	164	VDDI	3212.5	-279	224	VCOM	6812.5	-279
45	C12P	-4652.5	-279	105	GND	-1052.5	-279	165	VDDI	3272.5	-279	225	VCOM	6872.5	-279
46	C12M	-4592.5	-279	106	TESTO11	-992.5	-279	166	VDDI	3332.5	-279	226	VCOM	6932.5	-279
47	C12M	-4532.5	-279	107	VGS	-932.5	-279	167	VDDI	3392.5	-279	227	VCOM	6992.5	-279
48	C12M	-4472.5	-279	108	VGS	-872.5	-279	168	VDDI	3452.5	-279	228	VCOM	7052.5	-279
49	C12M	-4412.5	-279	109	TESTO10	-812.5	-279	169	Vcore	3512.5	-279	229	VCOM	7112.5	-279
50	C12M	-4352.5	-279	110	IM[3]	-752.5	-279	170	Vcore	3572.5	-279	230	VCOM	7172.5	-279
51	C12M	-4292.5	-279	111	IM[2]	-692.5	-279	171	Vcore	3632.5	-279	231	DUMMY	7232.5	-279
52	C12M	-4232.5	-279	112	IM[1]	-632.5	-279	172	Vcore	3692.5	-279	232	DUMMY	7292.5	-279
53	C11P	-4172.5	-279	113	IM[0]	-572.5	-279	173	Vcore	3752.5	-279	233	DUMMY	7399	255
54	C11P	-4112.5	-279	114	NRESET	-512.5	-279	174	Vcore	3812.5	-279	234	DUMMY	7385	120
55	C11P	-4052.5	-279	115	NCS	-452.5	-279	175	Vcore	3872.5	-279	235	DUMMY	7371	255
56	C11P	-3992.5	-279	116	RS	-392.5	-279	176	Vcore	3932.5	-279	236	G2	7357	120
57	C11P	-3932.5	-279	117	NWR_SCL	-332.5	-279	177	Vcore	3992.5	-279	237	G4	7343	255
58	C11P	-3872.5	-279	118	NRD	-272.5	-279	178	Vcore	4052.5	-279	238	G6	7329	120
59	C11P	-3812.5	-279	119	TESTO9	-212.5	-279	179	Vcore	4112.5	-279	239	G8	7315	255
60	C11M	-3752.5	-279	120	VSYNC	-152.5	-279	180	Vcore	4172.5	-279	240	G10	7301	120

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
241	G12	7287	255	301	G132	6447	255	361	G252	5607	255	421	S695	4725	255
242	G14	7273	120	302	G134	6433	120	362	G254	5593	120	422	S694	4711	120
243	G16	7259	255	303	G136	6419	255	363	G256	5579	255	423	S693	4697	255
244	G18	7245	120	304	G138	6405	120	364	G258	5565	120	424	S692	4683	120
245	G20	7231	255	305	G140	6391	255	365	G260	5551	255	425	S691	4669	255
246	G22	7217	120	306	G142	6377	120	366	G262	5537	120	426	S690	4655	120
247	G24	7203	255	307	G144	6363	255	367	G264	5523	255	427	S689	4641	255
248	G26	7189	120	308	G146	6349	120	368	G266	5509	120	428	S688	4627	120
249	G28	7175	255	309	G148	6335	255	369	G268	5495	255	429	S687	4613	255
250	G30	7161	120	310	G150	6321	120	370	G270	5481	120	430	S686	4599	120
251	G32	7147	255	311	G152	6307	255	371	G272	5467	255	431	S685	4585	255
252	G34	7133	120	312	G154	6293	120	372	G274	5453	120	432	S684	4571	120
253	G36	7119	255	313	G156	6279	255	373	G276	5439	255	433	S683	4557	255
254	G38	7105	120	314	G158	6265	120	374	G278	5425	120	434	S682	4543	120
255	G40	7091	255	315	G160	6251	255	375	G280	5411	255	435	S681	4529	255
256	G42	7077	120	316	G162	6237	120	376	G282	5397	120	436	S680	4515	120
257	G44	7063	255	317	G164	6223	255	377	G284	5383	255	437	S679	4501	255
258	G46	7049	120	318	G166	6209	120	378	G286	5369	120	438	S678	4487	120
259	G48	7035	255	319	G168	6195	255	379	G288	5355	255	439	S677	4473	255
260	G50	7021	120	320	G170	6181	120	380	G290	5341	120	440	S676	4459	120
261	G52	7007	255	321	G172	6167	255	381	G292	5327	255	441	S675	4445	255
262	G54	6993	120	322	G174	6153	120	382	G294	5313	120	442	S674	4431	120
263	G56	6979	255	323	G176	6139	255	383	G296	5299	255	443	S673	4417	255
264	G58	6965	120	324	G178	6125	120	384	G298	5285	120	444	S672	4403	120
265	G60	6951	255	325	G180	6111	255	385	G300	5271	255	445	S671	4389	255
266	G62	6937	120	326	G182	6097	120	386	G302	5257	120	446	S670	4375	120
267	G64	6923	255	327	G184	6083	255	387	G304	5243	255	447	S669	4361	255
268	G66	6909	120	328	G186	6069	120	388	G306	5229	120	448	S668	4347	120
269	G68	6895	255	329	G188	6055	255	389	G308	5215	255	449	S667	4333	255
270	G70	6881	120	330	G190	6041	120	390	G310	5201	120	450	S666	4319	120
271	G72	6867	255	331	G192	6027	255	391	G312	5187	255	451	S665	4305	255
272	G74	6853	120	332	G194	6013	120	392	G314	5173	120	452	S664	4291	120
273	G76	6839	255	333	G196	5999	255	393	G316	5159	255	453	S663	4277	255
274	G78	6825	120	334	G198	5985	120	394	G318	5145	120	454	S662	4263	120
275	G80	6811	255	335	G200	5971	255	395	G320	5131	255	455	S661	4249	255
276	G82	6797	120	336	G202	5957	120	396	S720	5075	120	456	S660	4235	120
277	G84	6783	255	337	G204	5943	255	397	S719	5061	255	457	S659	4221	255
278	G86	6769	120	338	G206	5929	120	398	S718	5047	120	458	S658	4207	120
279	G88	6755	255	339	G208	5915	255	399	S717	5033	255	459	S657	4193	255
280	G90	6741	120	340	G210	5901	120	400	S716	5019	120	460	S656	4179	120
281	G92	6727	255	341	G212	5887	255	401	S715	5005	255	461	S655	4165	255
282	G94	6713	120	342	G214	5873	120	402	S714	4991	120	462	S654	4151	120
283	G96	6699	255	343	G216	5859	255	403	S713	4977	255	463	S653	4137	255
284	G98	6685	120	344	G218	5845	120	404	S712	4963	120	464	S652	4123	120
285	G100	6671	255	345	G220	5831	255	405	S711	4949	255	465	S651	4109	255
286	G102	6657	120	346	G222	5817	120	406	S710	4935	120	466	S650	4095	120
287	G104	6643	255	347	G224	5803	255	407	S709	4921	255	467	S649	4081	255
288	G106	6629	120	348	G226	5789	120	408	S708	4907	120	468	S648	4067	120
289	G108	6615	255	349	G228	5775	255	409	S707	4893	255	469	S647	4053	255
290	G110	6601	120	350	G230	5761	120	410	S706	4879	120	470	S646	4039	120
291	G112	6587	255	351	G232	5747	255	411	S705	4865	255	471	S645	4025	255
292	G114	6573	120	352	G234	5733	120	412	S704	4851	120	472	S644	4011	120
293	G116	6559	255	353	G236	5719	255	413	S703	4837	255	473	S643	3997	255
294	G118	6545	120	354	G238	5705	120	414	S702	4823	120	474	S642	3983	120
295	G120	6531	255	355	G240	5691	255	415	S701	4809	255	475	S641	3969	255
296	G122	6517	120	356	G242	5677	120	416	S700	4795	120	476	S640	3955	120
297	G124	6503	255	357	G244	5663	255	417	S699	4781	255	477	S639	3941	255
298	G126	6489	120	358	G246	5649	120	418	S698	4767	120	478	S638	3927	120
299	G128	6475	255	359	G248	5635	255	419	S697	4753	255	479	S637	3913	255
300	G130	6461	120	360	G250	5621	120	420	S696	4739	120	480	S636	3899	120

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
481	S635	3885	255	541	S575	3045	255	601	S515	2205	255	661	S455	1365	255
482	S634	3871	120	542	S574	3031	120	602	S514	2191	120	662	S454	1351	120
483	S633	3857	255	543	S573	3017	255	603	S513	2177	255	663	S453	1337	255
484	S632	3843	120	544	S572	3003	120	604	S512	2163	120	664	S452	1323	120
485	S631	3829	255	545	S571	2989	255	605	S511	2149	255	665	S451	1309	255
486	S630	3815	120	546	S570	2975	120	606	S510	2135	120	666	S450	1295	120
487	S629	3801	255	547	S569	2961	255	607	S509	2121	255	667	S449	1281	255
488	S628	3787	120	548	S568	2947	120	608	S508	2107	120	668	S448	1267	120
489	S627	3773	255	549	S567	2933	255	609	S507	2093	255	669	S447	1253	255
490	S626	3759	120	550	S566	2919	120	610	S506	2079	120	670	S446	1239	120
491	S625	3745	255	551	S565	2905	255	611	S505	2065	255	671	S445	1225	255
492	S624	3731	120	552	S564	2891	120	612	S504	2051	120	672	S444	1211	120
493	S623	3717	255	553	S563	2877	255	613	S503	2037	255	673	S443	1197	255
494	S622	3703	120	554	S562	2863	120	614	S502	2023	120	674	S442	1183	120
495	S621	3689	255	555	S561	2849	255	615	S501	2009	255	675	S441	1169	255
496	S620	3675	120	556	S560	2835	120	616	S500	1995	120	676	S440	1155	120
497	S619	3661	255	557	S559	2821	255	617	S499	1981	255	677	S439	1141	255
498	S618	3647	120	558	S558	2807	120	618	S498	1967	120	678	S438	1127	120
499	S617	3633	255	559	S557	2793	255	619	S497	1953	255	679	S437	1113	255
500	S616	3619	120	560	S556	2779	120	620	S496	1939	120	680	S436	1099	120
501	S615	3605	255	561	S555	2765	255	621	S495	1925	255	681	S435	1085	255
502	S614	3591	120	562	S554	2751	120	622	S494	1911	120	682	S434	1071	120
503	S613	3577	255	563	S553	2737	255	623	S493	1897	255	683	S433	1057	255
504	S612	3563	120	564	S552	2723	120	624	S492	1883	120	684	S432	1043	120
505	S611	3549	255	565	S551	2709	255	625	S491	1869	255	685	S431	1029	255
506	S610	3535	120	566	S550	2695	120	626	S490	1855	120	686	S430	1015	120
507	S609	3521	255	567	S549	2681	255	627	S489	1841	255	687	S429	1001	255
508	S608	3507	120	568	S548	2667	120	628	S488	1827	120	688	S428	987	120
509	S607	3493	255	569	S547	2653	255	629	S487	1813	255	689	S427	973	255
510	S606	3479	120	570	S546	2639	120	630	S486	1799	120	690	S426	959	120
511	S605	3465	255	571	S545	2625	255	631	S485	1785	255	691	S425	945	255
512	S604	3451	120	572	S544	2611	120	632	S484	1771	120	692	S424	931	120
513	S603	3437	255	573	S543	2597	255	633	S483	1757	255	693	S423	917	255
514	S602	3423	120	574	S542	2583	120	634	S482	1743	120	694	S422	903	120
515	S601	3409	255	575	S541	2569	255	635	S481	1729	255	695	S421	889	255
516	S600	3395	120	576	S540	2555	120	636	S480	1715	120	696	S420	875	120
517	S599	3381	255	577	S539	2541	255	637	S479	1701	255	697	S419	861	255
518	S598	3367	120	578	S538	2527	120	638	S478	1687	120	698	S418	847	120
519	S597	3353	255	579	S537	2513	255	639	S477	1673	255	699	S417	833	255
520	S596	3339	120	580	S536	2499	120	640	S476	1659	120	700	S416	819	120
521	S595	3325	255	581	S535	2485	255	641	S475	1645	255	701	S415	805	255
522	S594	3311	120	582	S534	2471	120	642	S474	1631	120	702	S414	791	120
523	S593	3297	255	583	S533	2457	255	643	S473	1617	255	703	S413	777	255
524	S592	3283	120	584	S532	2443	120	644	S472	1603	120	704	S412	763	120
525	S591	3269	255	585	S531	2429	255	645	S471	1589	255	705	S411	749	255
526	S590	3255	120	586	S530	2415	120	646	S470	1575	120	706	S410	735	120
527	S589	3241	255	587	S529	2401	255	647	S469	1561	255	707	S409	721	255
528	S588	3227	120	588	S528	2387	120	648	S468	1547	120	708	S408	707	120
529	S587	3213	255	589	S527	2373	255	649	S467	1533	255	709	S407	693	255
530	S586	3199	120	590	S526	2359	120	650	S466	1519	120	710	S406	679	120
531	S585	3185	255	591	S525	2345	255	651	S465	1505	255	711	S405	665	255
532	S584	3171	120	592	S524	2331	120	652	S464	1491	120	712	S404	651	120
533	S583	3157	255	593	S523	2317	255	653	S463	1477	255	713	S403	637	255
534	S582	3143	120	594	S522	2303	120	654	S462	1463	120	714	S402	623	120
535	S581	3129	255	595	S521	2289	255	655	S461	1449	255	715	S401	609	255
536	S580	3115	120	596	S520	2275	120	656	S460	1435	120	716	S400	595	120
537	S579	3101	255	597	S519	2261	255	657	S459	1421	255	717	S399	581	255
538	S578	3087	120	598	S518	2247	120	658	S458	1407	120	718	S398	567	120
539	S577	3073	255	599	S517	2233	255	659	S457	1393	255	719	S397	553	255
540	S576	3059	120	600	S516	2219	120	660	S456	1379	120	720	S396	539	120

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
721	S395	525	255	781	S335	-399	255	841	S275	-1239	255	901	S215	-2079	255
722	S394	511	120	782	S334	-413	120	842	S274	-1253	120	902	S214	-2093	120
723	S393	497	255	783	S333	-427	255	843	S273	-1267	255	903	S213	-2107	255
724	S392	483	120	784	S332	-441	120	844	S272	-1281	120	904	S212	-2121	120
725	S391	469	255	785	S331	-455	255	845	S271	-1295	255	905	S211	-2135	255
726	S390	455	120	786	S330	-469	120	846	S270	-1309	120	906	S210	-2149	120
727	S389	441	255	787	S329	-483	255	847	S269	-1323	255	907	S209	-2163	255
728	S388	427	120	788	S328	-497	120	848	S268	-1337	120	908	S208	-2177	120
729	S387	413	255	789	S327	-511	255	849	S267	-1351	255	909	S207	-2191	255
730	S386	399	120	790	S326	-525	120	850	S266	-1365	120	910	S206	-2205	120
731	S385	385	255	791	S325	-539	255	851	S265	-1379	255	911	S205	-2219	255
732	S384	371	120	792	S324	-553	120	852	S264	-1393	120	912	S204	-2233	120
733	S383	357	255	793	S323	-567	255	853	S263	-1407	255	913	S203	-2247	255
734	S382	343	120	794	S322	-581	120	854	S262	-1421	120	914	S202	-2261	120
735	S381	329	255	795	S321	-595	255	855	S261	-1435	255	915	S201	-2275	255
736	S380	315	120	796	S320	-609	120	856	S260	-1449	120	916	S200	-2289	120
737	S379	301	255	797	S319	-623	255	857	S259	-1463	255	917	S199	-2303	255
738	S378	287	120	798	S318	-637	120	858	S258	-1477	120	918	S198	-2317	120
739	S377	273	255	799	S317	-651	255	859	S257	-1491	255	919	S197	-2331	255
740	S376	259	120	800	S316	-665	120	860	S256	-1505	120	920	S196	-2345	120
741	S375	245	255	801	S315	-679	255	861	S255	-1519	255	921	S195	-2359	255
742	S374	231	120	802	S314	-693	120	862	S254	-1533	120	922	S194	-2373	120
743	S373	217	255	803	S313	-707	255	863	S253	-1547	255	923	S193	-2387	255
744	S372	203	120	804	S312	-721	120	864	S252	-1561	120	924	S192	-2401	120
745	S371	189	255	805	S311	-735	255	865	S251	-1575	255	925	S191	-2415	255
746	S370	175	120	806	S310	-749	120	866	S250	-1589	120	926	S190	-2429	120
747	S369	161	255	807	S309	-763	255	867	S249	-1603	255	927	S189	-2443	255
748	S368	147	120	808	S308	-777	120	868	S248	-1617	120	928	S188	-2457	120
749	S367	133	255	809	S307	-791	255	869	S247	-1631	255	929	S187	-2471	255
750	S366	119	120	810	S306	-805	120	870	S246	-1645	120	930	S186	-2485	120
751	S365	105	255	811	S305	-819	255	871	S245	-1659	255	931	S185	-2499	255
752	S364	91	120	812	S304	-833	120	872	S244	-1673	120	932	S184	-2513	120
753	S363	77	255	813	S303	-847	255	873	S243	-1687	255	933	S183	-2527	255
754	S362	63	120	814	S302	-861	120	874	S242	-1701	120	934	S182	-2541	120
755	S361	49	255	815	S301	-875	255	875	S241	-1715	255	935	S181	-2555	255
756	S360	-49	120	816	S300	-889	120	876	S240	-1729	120	936	S180	-2569	120
757	S359	-63	255	817	S299	-903	255	877	S239	-1743	255	937	S179	-2583	255
758	S358	-77	120	818	S298	-917	120	878	S238	-1757	120	938	S178	-2597	120
759	S357	-91	255	819	S297	-931	255	879	S237	-1771	255	939	S177	-2611	255
760	S356	-105	120	820	S296	-945	120	880	S236	-1785	120	940	S176	-2625	120
761	S355	-119	255	821	S295	-959	255	881	S235	-1799	255	941	S175	-2639	255
762	S354	-133	120	822	S294	-973	120	882	S234	-1813	120	942	S174	-2653	120
763	S353	-147	255	823	S293	-987	255	883	S233	-1827	255	943	S173	-2667	255
764	S352	-161	120	824	S292	-1001	120	884	S232	-1841	120	944	S172	-2681	120
765	S351	-175	255	825	S291	-1015	255	885	S231	-1855	255	945	S171	-2695	255
766	S350	-189	120	826	S290	-1029	120	886	S230	-1869	120	946	S170	-2709	120
767	S349	-203	255	827	S289	-1043	255	887	S229	-1883	255	947	S169	-2723	255
768	S348	-217	120	828	S288	-1057	120	888	S228	-1897	120	948	S168	-2737	120
769	S347	-231	255	829	S287	-1071	255	889	S227	-1911	255	949	S167	-2751	255
770	S346	-245	120	830	S286	-1085	120	890	S226	-1925	120	950	S166	-2765	120
771	S345	-259	255	831	S285	-1099	255	891	S225	-1939	255	951	S165	-2779	255
772	S344	-273	120	832	S284	-1113	120	892	S224	-1953	120	952	S164	-2793	120
773	S343	-287	255	833	S283	-1127	255	893	S223	-1967	255	953	S163	-2807	255
774	S342	-301	120	834	S282	-1141	120	894	S222	-1981	120	954	S162	-2821	120
775	S341	-315	255	835	S281	-1155	255	895	S221	-1995	255	955	S161	-2835	255
776	S340	-329	120	836	S280	-1169	120	896	S220	-2009	120	956	S160	-2849	120
777	S339	-343	255	837	S279	-1183	255	897	S219	-2023	255	957	S159	-2863	255
778	S338	-357	120	838	S278	-1197	120	898	S218	-2037	120	958	S158	-2877	120
779	S337	-371	255	839	S277	-1211	255	899	S217	-2051	255	959	S157	-2891	255
780	S336	-385	120	840	S276	-1225	120	900	S216	-2065	120	960	S156	-2905	120

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
961	S155	-2919	255	1021	S95	-3759	255	1081	S35	-4599	255	1141	G269	-5481	255
962	S154	-2933	120	1022	S94	-3773	120	1082	S34	-4613	120	1142	G267	-5495	120
963	S153	-2947	255	1023	S93	-3787	255	1083	S33	-4627	255	1143	G265	-5509	255
964	S152	-2961	120	1024	S92	-3801	120	1084	S32	-4641	120	1144	G263	-5523	120
965	S151	-2975	255	1025	S91	-3815	255	1085	S31	-4655	255	1145	G261	-5537	255
966	S150	-2989	120	1026	S90	-3829	120	1086	S30	-4669	120	1146	G259	-5551	120
967	S149	-3003	255	1027	S89	-3843	255	1087	S29	-4683	255	1147	G257	-5565	255
968	S148	-3017	120	1028	S88	-3857	120	1088	S28	-4697	120	1148	G255	-5579	120
969	S147	-3031	255	1029	S87	-3871	255	1089	S27	-4711	255	1149	G253	-5593	255
970	S146	-3045	120	1030	S86	-3885	120	1090	S26	-4725	120	1150	G251	-5607	120
971	S145	-3059	255	1031	S85	-3899	255	1091	S25	-4739	255	1151	G249	-5621	255
972	S144	-3073	120	1032	S84	-3913	120	1092	S24	-4753	120	1152	G247	-5635	120
973	S143	-3087	255	1033	S83	-3927	255	1093	S23	-4767	255	1153	G245	-5649	255
974	S142	-3101	120	1034	S82	-3941	120	1094	S22	-4781	120	1154	G243	-5663	120
975	S141	-3115	255	1035	S81	-3955	255	1095	S21	-4795	255	1155	G241	-5677	255
976	S140	-3129	120	1036	S80	-3969	120	1096	S20	-4809	120	1156	G239	-5691	120
977	S139	-3143	255	1037	S79	-3983	255	1097	S19	-4823	255	1157	G237	-5705	255
978	S138	-3157	120	1038	S78	-3997	120	1098	S18	-4837	120	1158	G235	-5719	120
979	S137	-3171	255	1039	S77	-4011	255	1099	S17	-4851	255	1159	G233	-5733	255
980	S136	-3185	120	1040	S76	-4025	120	1100	S16	-4865	120	1160	G231	-5747	120
981	S135	-3199	255	1041	S75	-4039	255	1101	S15	-4879	255	1161	G229	-5761	255
982	S134	-3213	120	1042	S74	-4053	120	1102	S14	-4893	120	1162	G227	-5775	120
983	S133	-3227	255	1043	S73	-4067	255	1103	S13	-4907	255	1163	G225	-5789	255
984	S132	-3241	120	1044	S72	-4081	120	1104	S12	-4921	120	1164	G223	-5803	120
985	S131	-3255	255	1045	S71	-4095	255	1105	S11	-4935	255	1165	G221	-5817	255
986	S130	-3269	120	1046	S70	-4109	120	1106	S10	-4949	120	1166	G219	-5831	120
987	S129	-3283	255	1047	S69	-4123	255	1107	S9	-4963	255	1167	G217	-5845	255
988	S128	-3297	120	1048	S68	-4137	120	1108	S8	-4977	120	1168	G215	-5859	120
989	S127	-3311	255	1049	S67	-4151	255	1109	S7	-4991	255	1169	G213	-5873	255
990	S126	-3325	120	1050	S66	-4165	120	1110	S6	-5005	120	1170	G211	-5887	120
991	S125	-3339	255	1051	S65	-4179	255	1111	S5	-5019	255	1171	G209	-5901	255
992	S124	-3353	120	1052	S64	-4193	120	1112	S4	-5033	120	1172	G207	-5915	120
993	S123	-3367	255	1053	S63	-4207	255	1113	S3	-5047	255	1173	G205	-5929	255
994	S122	-3381	120	1054	S62	-4221	120	1114	S2	-5061	120	1174	G203	-5943	120
995	S121	-3395	255	1055	S61	-4235	255	1115	S1	-5075	255	1175	G201	-5957	255
996	S120	-3409	120	1056	S60	-4249	120	1116	G319	-5131	120	1176	G199	-5971	120
997	S119	-3423	255	1057	S59	-4263	255	1117	G317	-5145	255	1177	G197	-5985	255
998	S118	-3437	120	1058	S58	-4277	120	1118	G315	-5159	120	1178	G195	-5999	120
999	S117	-3451	255	1059	S57	-4291	255	1119	G313	-5173	255	1179	G193	-6013	255
1000	S116	-3465	120	1060	S56	-4305	120	1120	G311	-5187	120	1180	G191	-6027	120
1001	S115	-3479	255	1061	S55	-4319	255	1121	G309	-5201	255	1181	G189	-6041	255
1002	S114	-3493	120	1062	S54	-4333	120	1122	G307	-5215	120	1182	G187	-6055	120
1003	S113	-3507	255	1063	S53	-4347	255	1123	G305	-5229	255	1183	G185	-6069	255
1004	S112	-3521	120	1064	S52	-4361	120	1124	G303	-5243	120	1184	G183	-6083	120
1005	S111	-3535	255	1065	S51	-4375	255	1125	G301	-5257	255	1185	G181	-6097	255
1006	S110	-3549	120	1066	S50	-4389	120	1126	G299	-5271	120	1186	G179	-6111	120
1007	S109	-3563	255	1067	S49	-4403	255	1127	G297	-5285	255	1187	G177	-6125	255
1008	S108	-3577	120	1068	S48	-4417	120	1128	G295	-5299	120	1188	G175	-6139	120
1009	S107	-3591	255	1069	S47	-4431	255	1129	G293	-5313	255	1189	G173	-6153	255
1010	S106	-3605	120	1070	S46	-4445	120	1130	G291	-5327	120	1190	G171	-6167	120
1011	S105	-3619	255	1071	S45	-4459	255	1131	G289	-5341	255	1191	G169	-6181	255
1012	S104	-3633	120	1072	S44	-4473	120	1132	G287	-5355	120	1192	G167	-6195	120
1013	S103	-3647	255	1073	S43	-4487	255	1133	G285	-5369	255	1193	G165	-6209	255
1014	S102	-3661	120	1074	S42	-4501	120	1134	G283	-5383	120	1194	G163	-6223	120
1015	S101	-3675	255	1075	S41	-4515	255	1135	G281	-5397	255	1195	G161	-6237	255
1016	S100	-3689	120	1076	S40	-4529	120	1136	G279	-5411	120	1196	G159	-6251	120
1017	S99	-3703	255	1077	S39	-4543	255	1137	G277	-5425	255	1197	G157	-6265	255
1018	S98	-3717	120	1078	S38	-4557	120	1138	G275	-5439	120	1198	G155	-6279	120
1019	S97	-3731	255	1079	S37	-4571	255	1139	G273	-5453	255	1199	G153	-6293	255
1020	S96	-3745	120	1080	S36	-4585	120	1140	G271	-5467	120	1200	G151	-6307	120

No	Name	X	Y	No	Name	X	Y
1201	G149	-6321	255	1261	G29	-7161	255
1202	G147	-6335	120	1262	G27	-7175	120
1203	G145	-6349	255	1263	G25	-7189	255
1204	G143	-6363	120	1264	G23	-7203	120
1205	G141	-6377	255	1265	G21	-7217	255
1206	G139	-6391	120	1266	G19	-7231	120
1207	G137	-6405	255	1267	G17	-7245	255
1208	G135	-6419	120	1268	G15	-7259	120
1209	G133	-6433	255	1269	G13	-7273	255
1210	G131	-6447	120	1270	G11	-7287	120
1211	G129	-6461	255	1271	G9	-7301	255
1212	G127	-6475	120	1272	G7	-7315	120
1213	G125	-6489	255	1273	G5	-7329	255
1214	G123	-6503	120	1274	G3	-7343	120
1215	G121	-6517	255	1275	G1	-7357	255
1216	G119	-6531	120	1276	DUMMY	-7371	120
1217	G117	-6545	255	1277	DUMMY	-7385	255
1218	G115	-6559	120	1278	DUMMY	-7399	120
1219	G113	-6573	255				
1220	G111	-6587	120				
1221	G109	-6601	255				
1222	G107	-6615	120				
1223	G105	-6629	255				
1224	G103	-6643	120				
1225	G101	-6657	255				
1226	G99	-6671	120				
1227	G97	-6685	255				
1228	G95	-6699	120				
1229	G93	-6713	255				
1230	G91	-6727	120				
1231	G89	-6741	255				
1232	G87	-6755	120				
1233	G85	-6769	255				
1234	G83	-6783	120				
1235	G81	-6797	255				
1236	G79	-6811	120				
1237	G77	-6825	255				
1238	G75	-6839	120				
1239	G73	-6853	255				
1240	G71	-6867	120				
1241	G69	-6881	255				
1242	G67	-6895	120				
1243	G65	-6909	255				
1244	G63	-6923	120				
1245	G61	-6937	255				
1246	G59	-6951	120				
1247	G57	-6965	255				
1248	G55	-6979	120				
1249	G53	-6993	255				
1250	G51	-7007	120				
1251	G49	-7021	255				
1252	G47	-7035	120				
1253	G45	-7049	255				
1254	G43	-7063	120				
1255	G41	-7077	255				
1256	G39	-7091	120				
1257	G37	-7105	255				
1258	G35	-7119	120				
1259	G33	-7133	255				
1260	G31	-7147	120				

5. Pin Function

Table 2 Interface

<table>
<tr><th>Signal</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM3-1,
IM0/ID</td><td>I</td><td>GND or
VDDI</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0
/ID</th><th rowspan="2">Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/
Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-system 8-bit bus interface I</td><td>DB7-0</td><td>DB7-0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80-system 16-bit bus interface I</td><td>DB15-0</td><td>DB15-0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 9-bit bus interface I</td><td>DB8-1</td><td>DB8-0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 18-bit bus interface I</td><td>DB17-10,
DB8-1</td><td>DB17-0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA : In/Out</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA : In/Out</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td></td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80-system 16-bit bus interface II</td><td>DB17-10,
DB8-1</td><td>DB17-10,
DB8-1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80-system 8-bit bus interface II</td><td>DB17-10</td><td>DB17-10</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface II</td><td>DB17-10,
DB8-1</td><td>DB17-0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface II</td><td>DB17-10</td><td>DB17-9</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>ID</td><td>Clock Synchronous Serial interface</td><td colspan="2">SDI : In
SDO : Out</td></tr>
</table></td><td>-</td></tr>
<tr><td>nRESET</td><td>I</td><td>MPU</td><td>Reset signal. Initializes the RM68090 when it is low. Make sure to execute a power-on reset when turning on power supply.
Amplitude: VDDI-GND.</td><td>VDDI</td></tr>
<tr><td>nCS</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: VDDI-GND
Low: the RM68090 is selected and accessible
High: the RM68090 is not selected and not accessible.</td><td>GND</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: VDDI-GND
Low: select Index or status register</td><td>VDDI</td></tr>
</table>

			High: select control register Fix to either VDDI or DGND when not in use	
nWR/SCL	I	MPU	Write strobe signal in 80-system bus interface operation and enables write operation when nWR is low. Synchronous clock signal (SCL) in serial interface operation. Amplitude: VDDI-GND	VDDI
nRD	I	MPU	Read strobe signal in 80-system bus interface operation and enables read operation when nRD is low. Amplitude: VDDI-GND	VDDI
SDI_SDA	I	MPU	Serial data input (SDI) pin in serial interface operation. The data is inputted and latched on the rising edge of the SCL signal. In the 8/9-bit SPI, this pis is a bi-directional data pin. Amplitude: VDDI-GND	GND or VDDI
SDO	I	MPU	Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. Amplitude: VDDI-GND	Open
DB0-DB17	I/O	MPU	18-bit parallel bi-directional data bus for 80-system interface operation. Amplitude: VDDI-GND. 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-DB1 are used. 18-bit I/F: DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation. Amplitude: VDDI-GND. 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB13 and DB11-DB1 are used. 18-bit I/F: DB17-DB0 are used. Unused pins must be fixed to GND level.	GND or VDDI
ENABLE	I	MPU	Data enable signal for RGB interface operation. Amplitude: VDDI-GND. Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit.	GND or VDDI

VSYNC	I	MPU	Frame synchronous signal for RGB interface operation.. Amplitude: VDDI-GND. VSPL = “0”: Active low. VSPL = “1”: Active high.	GND or VDDI
HSYNC	I	MPU	Line synchronous signal for RGB interface operation. Amplitude: VDDI-GND. HSPL = “0”: Active low. HSPL = “1”: Active high.	GND or VDDI
DOTCLK	I	MPU	Dot clock signal for RGB interface operation. The data input timing is on the rising edge of DOTCLK. Amplitude: VDDI-GND. DPL = “0”: Input data on the rising edge of DOTCLK DPL = “1”: Input data on the falling edge of DOTCLK	GND or VDDI
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. (Amplitude: VDDI-GND).	Open

Table 3 Power supply

Signal	I/O	Connect to	Function	When not in use
VDDI	I	Power supply	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)	-
VDDI_LED	I	Power supply	Power supply for LED driver interface. (1.65 ~ 3.3 V)	GND or OPEN
VCI	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.	-
Vcore	I	Stabilizing Capacitor	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization.	-
GND	I	Power supply	System ground level.	-

Table 4 LCD drive

Signal	I/O	Connect to	Function	When not in use
VCI1	O	Stabilizing Capacitor	An internal reference voltage for the step-up circuit1.The amplitude between VCI and GND is determined by the VC[2:0] bits. Make sure to set the VCI1 voltage so that the AVDD, VGH and VGL voltages are set within the respective specification.	-
AVDD	O	Stabilizing Capacitor	Output voltage of 1st step-up circuit (2 x VCI1). Input voltage to 2nd step-up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.	-
VGH	O	Stabilizing Capacitor	Liquid crystal gate driver power supply.	-
VGL	O	Stabilizing Capacitor	Liquid crystal gate driver power supply.	-
VCL	O	Stabilizing Capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = 0.5V ~ -VCI	-
C11P, C11M C12P, C12M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C21P, C21M C22P, C22M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.	-
C31P, C31M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.	-
GVDD	O	Stabilizing Capacitor	High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.	-
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register.	Open
VGS	I	GND or external resistor	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.	-
S1~S720	O	LCD	Liquid crystal application voltages. To change the shift direction of segment signal output, set the SS bit as follows.	Open

			When SS = 0, the data in the RAM address h00000 is outputted from S1. When SS = 1, the data in the RAM address h00000 is outputted from S720.	
G1~G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level	Open

Table 5 Brightness control

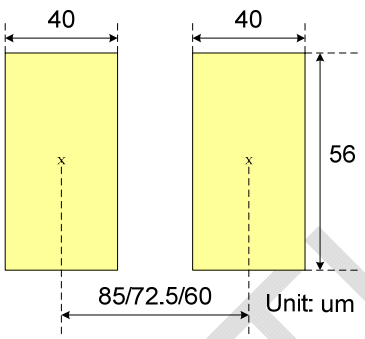
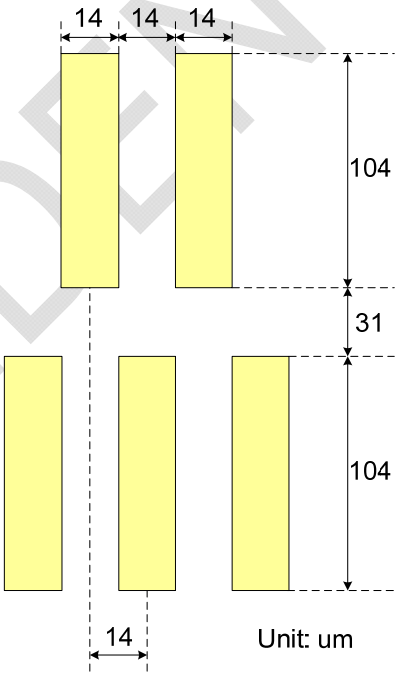
Signal	I/O	Connect to	Function	When not in use
LEDPWM	O	VCI	PWM signal output to control LED driver for LED brightness dimming	Open
LEDON	O	VCI	LED driver control pin to turn on/off the LED backlight	Open

Table 6 Others (test, dummy pins)

Signal	I/O	Connect to	Function	When not in use
DUMMY	-	Open	Dummy pad and no output (no gold bump)	Open
DUMMYR1 DUMMYR2	I	Open	Contact resistance measurement pad. These pads are at GND level. When measuring an ohmic resistance of the contact, do not apply any power.	Open
TESTO1-11	O	Open	Test pins. Leave them open.	Open
TS4-0	I	Open	Test pins (internal pull low). Leave them open.	Open

6. Bump Arrangement

BUMP Size

Input Pad (1~232)	
Output Pad (233~1278)	

7. Function Description

7.1 System Interface

The RM68090 supports 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The RM68090 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information about control register and internal GRAM. The WDR is the register to temporarily store data to be written to control register and internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the RM68090 performs the first read operation from the internal GRAM. Valid data is read out when the RM68090 performs the second and subsequent read operation.

The instruction execution time except that of starting oscillation takes 0 clock cycle to allow writing instructions consecutively.

Table 7 Register Selection (80-system 8/9/16/18-bit Parallel Interface)

nWR	nRD	RS	Function
0	1	0	Write index to IR
1	0	0	Setting disabled
0	1	1	Write to control register or internal GRAM via WDR
1	0	1	Read from internal GRAM and register via RDR

Table 8 Register Selection (Clock synchronous serial interface)

Start byte		
R/W	RS	Function
0	0	Write index to IR
1	0	Setting disabled
0	1	Write to control register or internal GRAM via WDR
1	1	Read from internal GRAM and register via RDR

Table 9 IM Bit Settings and System Interface

IM3	IM2	IM1	IM0	System interface	DB pins	RAM write data	Instruction write transfer
0	0	0	0	80-system 8-bit bus interface I	DB7-0	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	0	0	1	80-system 16-bit bus interface I	DB15-0	Single transfer (16 bits) 2 transfers (1st: 2 bits, 2nd: 16 bits) 2 transfers (1st: 16 bits, 2nd: 2 bits)	Single transfer (16 bits)
0	0	1	0	80-system 9-bit bus interface I	DB8-0	2 transfers (1st: 9 bits, 2nd: 9 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	0	1	1	80-system 18-bit bus interface I	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
0	1	0	0	Setting disabled			
0	1	0	1	3-wire 9-bit data serial interface	SDA	2 transfers (1st: 8 bits, 2nd: 8 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	1	0	4-wire 8-bit data serial interface	SDA	2 transfers (1st: 8 bits, 2nd: 8 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	1	1	Setting disabled			
1	0	0	0	80-system 16-bit bus interface II	DB17-10, DB8-1	Single transfer (16 bits) 2 transfers (1st: 2 bits, 2nd: 16 bits) 2 transfers (1st: 16 bits, 2nd: 2 bits)	Single transfer (16 bits)
1	0	0	1	80-system 8-bit bus interface II	DB17-10	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)

1	0	1	0	80-system 18-bit bus interface II	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
1	0	1	1	80-system 9-bit bus interface II	DB17-9	2 transfers (1st: 9 bits, 2nd: 9 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
1	1	*	*	Clock synchronous serial interface	(SDI, SDO)	2 transfers (1st: 8 bits, 2nd: 8 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)

7.2 External Display Interface (RGB, VSYNC interfaces)

The RM68090 supports RGB interface and VSYNC interface as the external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is written to the internal GRAM via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display interface” section.

The RM68090 allows switching interface by instruction according to the still and/or moving pictures display required. Via the RGB interface, the RM68090 writes all display data to the internal GRAM in order to transfer data only when updating the data and thereby reduce the data transfer and power consumption for moving picture display.

7.3 Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register to set a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As the RM68090 writes data to the internal GRAM, the address in the AC is automatically increased or decreased one step. The window address function enables writing data only within the rectangular area specified in the GRAM.

7.4 Graphics RAM (GRAM)

GRAM is graphics RAM, which can store bit-pattern data of 172,800 (240RGB x 320 x18/8) bytes with 18 bits per pixel.

7.5 Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal driving voltages according to the grayscale data in the γ-correction registers to enable 262k-color display. For details, see the γ-Correction Register section.

7.6 Timing Generator

The timing generator produces timing signals for the operations of internal circuits such as the internal GRAM, source driver, etc. The timing signals for display operations such as RAM read operation and the timing signals for internal operations such as RAM access from the MPU are generated separately in order to avoid mutual interference.

7.7 Oscillator (OSC)

The RM68090 generates the RC oscillation clock by internal RC oscillator circuit. The frame rate is adjusted by the register setting.

7.8 Liquid Crystal Driver Circuit

The liquid crystal driver circuit of the RM68090 consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). The display pattern data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for each LCD module.

7.9 Internal Logic Power Supply Regulator

The internal logic power supply regulator generates internal logic power supply VDD.

8. GRAM Address Map and Read/Write

Table 10 GRAM address and display position on the panel (SS = 0, BGR = 0)

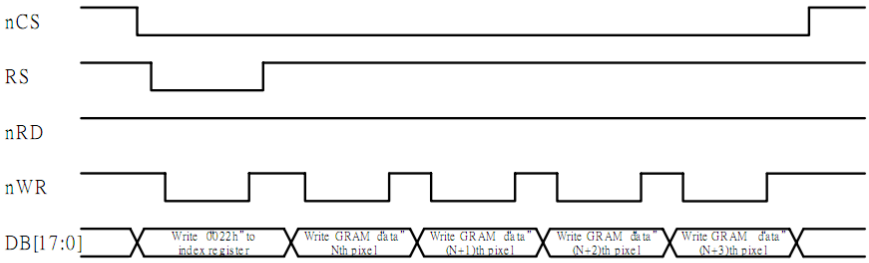
GS=0		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			.....	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G320	h00000			h00001			h00002			h00003			.....	h000EC			h000ED			h000EE			h000EF		
G2	G319	h00100			h00101			h00102			h00103			.....	h001EC			h001ED			h001EE			h001EF		
G3	G318	h00200			h00201			h00202			h00203			.....	h002EC			h002ED			h002EE			h002EF		
G4	G317	H00300			h00301			h00302			h00303			.....	h003EC			h003ED			h003EE			h003EF		
G5	G316	h00400			h00401			h00402			h00403			.....	h004EC			h004ED			h004EE			h004EF		
G6	G315	h00500			h00501			h00502			h00503			.....	h005EC			h005ED			h005EE			h005EF		
G7	G314	h00600			h00601			h00602			h00603			.....	h006EC			h006ED			h006EE			h006EF		
G8	G313	h00700			h00701			h00702			h00703			.....	h007EC			h007ED			h007EE			h007EF		
G9	G312	h00800			h00801			h00802			h00803			.....	h008EC			h008ED			h008EE			h008EF		
G10	G311	h00900			h00901			h00902			h00903			.....	h009EC			h009ED			h009EE			h009EF		
G11	G310	h00A00			h00A01			h00A02			h00A03			.....	h00AEC			h00AED			h00AEE			h00AEF		
G12	G309	h00B00			h00B01			h00B02			h00B03			.....	h00BEC			h00BED			h00BEE			h00BEF		
G13	G308	h00C00			h00C01			h00C02			h00C03			.....	h00CEC			h00CED			h00CEE			h00CEF		
G14	G307	h00D00			h00D01			h00D02			h00D03			.....	h00DEC			h00DED			h00DEE			h00DEF		
G15	G306	h00E00			h00E01			h00E02			h00E03			.....	h00EEC			h00EED			h00EEE			h00EEF		
G16	G305	h00F00			h00F01			h00F02			h00F03			.....	h00FEC			h00FED			h00FEE			h00FEF		
G17	G304	h01000			h01001			h01002			h01003			.....	h010EC			h010ED			h010EE			h010EF		
G18	G303	h01100			h01101			h01102			h01103			.....	h011EC			h011ED			h011EE			h011EF		
G19	G302	h01200			h01201			h01202			h01203			.....	h012EC			h012ED			h012EE			h012EF		
G20	G301	h01300			h01301			h01302			h01303			.....	h013EC			h013ED			h013EE			h013EF		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G305	G16	h13000			h13001			h13002			h13003			.....	h130EC			h130ED			h130EE			h130EF		
G306	G15	h13100			h13101			h13102			h13103			.....	h131EC			h131ED			h131EE			h131EF		
G307	G14	h13200			h13201			h13202			h13203			.....	h132EC			h132ED			h132EE			h132EF		
G308	G13	h13300			h13301			h13302			h13303			.....	h133EC			h133ED			h133EE			h133EF		
G309	G12	h13400			h13401			h13402			h13403			.....	h134EC			h134ED			h134EE			h134EF		
G310	G11	h13500			h13501			h13502			h13503			.....	h135EC			h135ED			h135EE			h135EF		
G311	G10	h13600			h13601			h13602			h13603			.....	h136EC			h136ED			h136EE			h136EF		
G312	G9	h13700			h13701			h13702			h13703			.....	h137EC			h137ED			h137EE			h137EF		
G313	G8	h13800			h13801			h13802			h13803			.....	h138EC			h138ED			h138EE			h138EF		
G314	G7	h13900			h13901			h13902			h13903			.....	h139EC			h139ED			h139EE			h139EF		
G315	G6	h13A00			h13A01			h13A02			h13A03			.....	h13AEC			h13AED			h13AEE			h13AEF		
G316	G5	h13B00			h13B01			h13B02			h13B03			.....	h13BEC			h13BED			h13BEE			h13BEF		
G317	G4	h13C00			h13C01			h13C02			h13C03			.....	h13CEC			h13CED			h13CEE			h13CEF		
G318	G3	h13D00			h13D01			h13D02			h13D03			.....	h13DEC			h13DED			h13DEE			h13DEF		
G319	G2	h13E00			h13E01			h13E02			h13E03			.....	h13EEC			h13EED			h13EEE			h13EEF		
G320	G1	h13F00			h13F01			h13F02			h13F03			.....	h13FEC			h13FED			h13FEE			h13FEF		

Table 11 GRAM address and display position on the panel (SS = 1, BGR = 1)

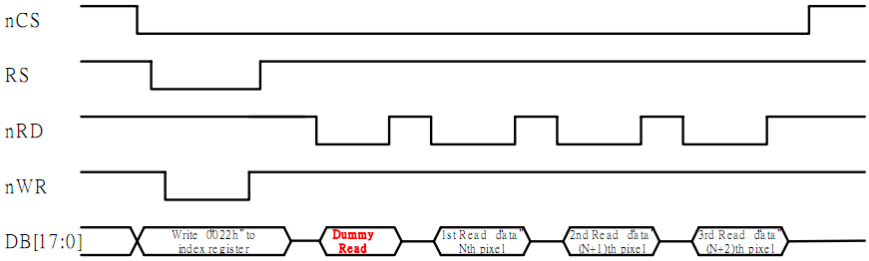
GS=0		S720 S719 S718	S717 S716 S715	S714 S713 S712	S711 S710 S709	.....	S12 S11 S10	S9 S8 S7	S6 S5 S4	S3 S2 S1
GS=0	GS=1	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]	.....	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]
G1	G320	h00000	h00001	h00002	h00003	.....	h000EC	h000ED	h000EE	h000EF
G2	G319	h00100	h00101	h00102	h00103	.....	h001EC	h001ED	h001EE	h001EF
G3	G318	h00200	h00201	h00202	h00203	.....	h002EC	h002ED	h002EE	h002EF
G4	G317	H00300	h00301	h00302	h00303	.....	h003EC	h003ED	h003EE	h003EF
G5	G316	h00400	h00401	h00402	h00403	.....	h004EC	h004ED	h004EE	h004EF
G6	G315	h00500	h00501	h00502	h00503	.....	h005EC	h005ED	h005EE	h005EF
G7	G314	h00600	h00601	h00602	h00603	.....	h006EC	h006ED	h006EE	h006EF
G8	G313	h00700	h00701	h00702	h00703	.....	h007EC	h007ED	h007EE	h007EF
G9	G312	h00800	h00801	h00802	h00803	.....	h008EC	h008ED	h008EE	h008EF
G10	G311	h00900	h00901	h00902	h00903	.....	h009EC	h009ED	h009EE	h009EF
G11	G310	h00A00	h00A01	h00A02	h00A03	.....	h00AEC	h00AED	h00AEE	h00AEF
G12	G309	h00B00	h00B01	h00B02	h00B03	.....	h00BEC	h00BED	h00BEE	h00BEF
G13	G308	h00C00	h00C01	h00C02	h00C03	.....	h00CEC	h00CED	h00CEE	h00CEF
G14	G307	h00D00	h00D01	h00D02	h00D03	.....	h00DEC	h00DED	h00DEE	h00DEF
G15	G306	h00E00	h00E01	h00E02	h00E03	.....	h00EEC	h00EED	h00EEE	h00EEF
G16	G305	h00F00	h00F01	h00F02	h00F03	.....	h00FEC	h00FED	h00FEE	h00FEF
G17	G304	h01000	h01001	h01002	h01003	.....	h010EC	h010ED	h010EE	h010EF
G18	G303	h01100	h01101	h01102	h01103	.....	h011EC	h011ED	h011EE	h011EF
G19	G302	h01200	h01201	h01202	h01203	.....	h012EC	h012ED	h012EE	h012EF
G20	G301	h01300	h01301	h01302	h01303	.....	h013EC	h013ED	h013EE	h013EF
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
G305	G16	h13000	h13001	h13002	h13003	.....	h130EC	h130ED	h130EE	h130EF
G306	G15	h13100	h13101	h13102	h13103	.....	h131EC	h131ED	h131EE	h131EF
G307	G14	h13200	h13201	h13202	h13203	.....	h132EC	h132ED	h132EE	h132EF
G308	G13	h13300	h13301	h13302	h13303	.....	h133EC	h133ED	h133EE	h133EF
G309	G12	h13400	h13401	h13402	h13403	.....	h134EC	h134ED	h134EE	h134EF
G310	G11	h13500	h13501	h13502	h13503	.....	h135EC	h135ED	h135EE	h135EF
G311	G10	h13600	h13601	h13602	h13603	.....	h136EC	h136ED	h136EE	h136EF
G312	G9	h13700	h13701	h13702	h13703	.....	h137EC	h137ED	h137EE	h137EF
G313	G8	h13800	h13801	h13802	h13803	.....	h138EC	h138ED	h138EE	h138EF
G314	G7	h13900	h13901	h13902	h13903	.....	h139EC	h139ED	h139EE	h139EF
G315	G6	h13A00	h13A01	h13A02	h13A03	.....	h13AEC	h13AED	h13AEE	h13AEF
G316	G5	h13B00	h13B01	h13B02	h13B03	.....	h13BEC	h13BED	h13BEE	h13BEF
G317	G4	h13C00	h13C01	h13C02	h13C03	.....	h13CEC	h13CED	h13CEE	h13CEF
G318	G3	h13D00	h13D01	h13D02	h13D03	.....	h13DEC	h13DED	h13DEE	h13DEF
G319	G2	h13E00	h13E01	h13E02	h13E03	.....	h13EEC	h13EED	h13EEE	h13EEF
G320	G1	h13F00	h13F01	h13F02	h13F03	.....	h13FEC	h13FED	h13FEE	h13FEF

i80 18-/16-bit System Bus Interface Timing

(a) Write to GRAM

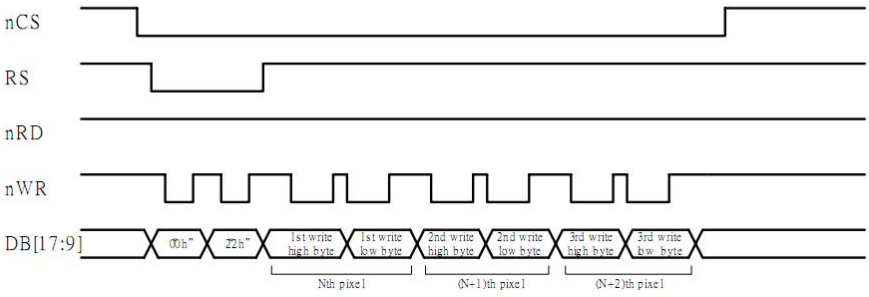


(b) Read from GRAM

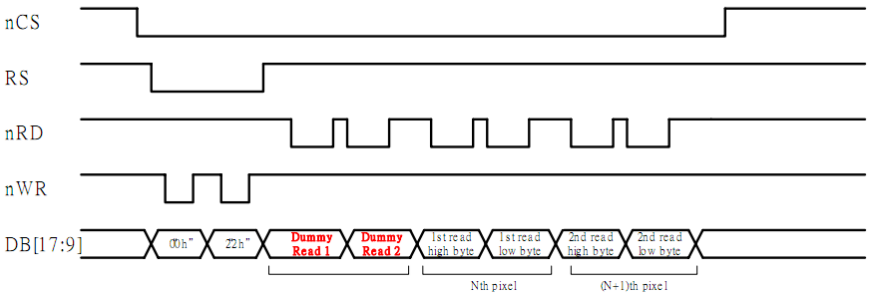


i80 9-/8-bit System Bus Interface Timing

(a) Write to GRAM



(b) Read from GRAM



9. Instruction

9.1 Outline

The RM68090 adopts 18-bit bus architecture in order to interface to high-performance microcomputer in high speed. All the functional blocks of RM68090 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of RM68090. When accessing the RM68090's internal RAM, data is processed in units of 18 bits. The following are the categories of instruction in RM68090.

1. Specify the index of register
2. Display control
3. Power management control
4. Set internal GRAM address
5. Transfer data to and from the internal GRAM
6. γ -correction
7. Window address control
8. Panel display control

The internal GRAM address is updated automatically as data is written to the internal GRAM, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the loading on the microcomputer. The RM68090 writes instructions consecutively by executing the instruction within the cycle when it is written, meanwhile, there is no instruction execution time required.

9.2 Instruction Data Format

The data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface. For more details, please refer to section of "System Interface".

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface.

9.3 Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index R00h to RFFh of the control register or RAM control to be accessed using a binary number from “0000_0000” to “1111_1111”. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

9.4 ID code (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RO	1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	1

The ID code “6809”h is outputted when this register is read.

9.5 Display control

9.5.1 Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shift from S1 to S720.

When SS = “1”, the source driver output shift from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, RGB dots are assigned one to one from S1 to S720.

When SS = “1” and BGR = “1”, RGB dots are assigned one to one from S720 to S1.

When changing the SS or BGR bits, RAM data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See “Scan mode setting”.

9.5.2 LCD Driving Wave Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BC0: Selects the liquid crystal drive waveform VCOM..

BC0 = 0: frame inversion waveform is selected.

BC0 = 1: line inversion waveform is selected.

9.5.3 Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I//D1	I/D0	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the RM68090 writes data to the internal GRAM.
AM = “0”, sets the horizontal direction.
AM = “1”, sets the vertical direction.
When making a window address area, the data is written only within the area in the direction determined by I/D[1:0] and AM.

I/D[1:0]: Either increments or decrements the address counter automatically as the data is written to the GRAM. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]).

ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data within the window address area using high-speed RAM write function. Also see Figure 3 and Figure 4.
ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.
ORG = 1: The origin address “h00000” is moved according to the I/D[1:0] setting.

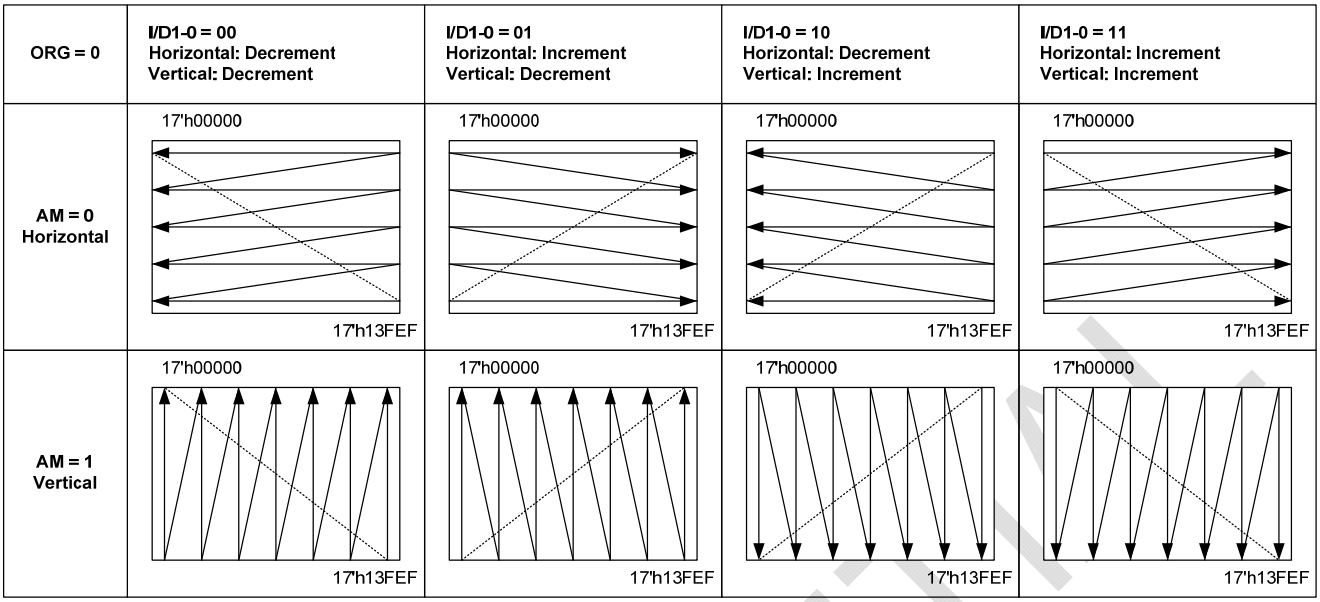


Figure 1 Automatic address update (ORG = 0, AM, ID)

Note: When writing data within the window address area with ORG = 0, any address within the window address area can be designated as the starting point of RAM write operation.

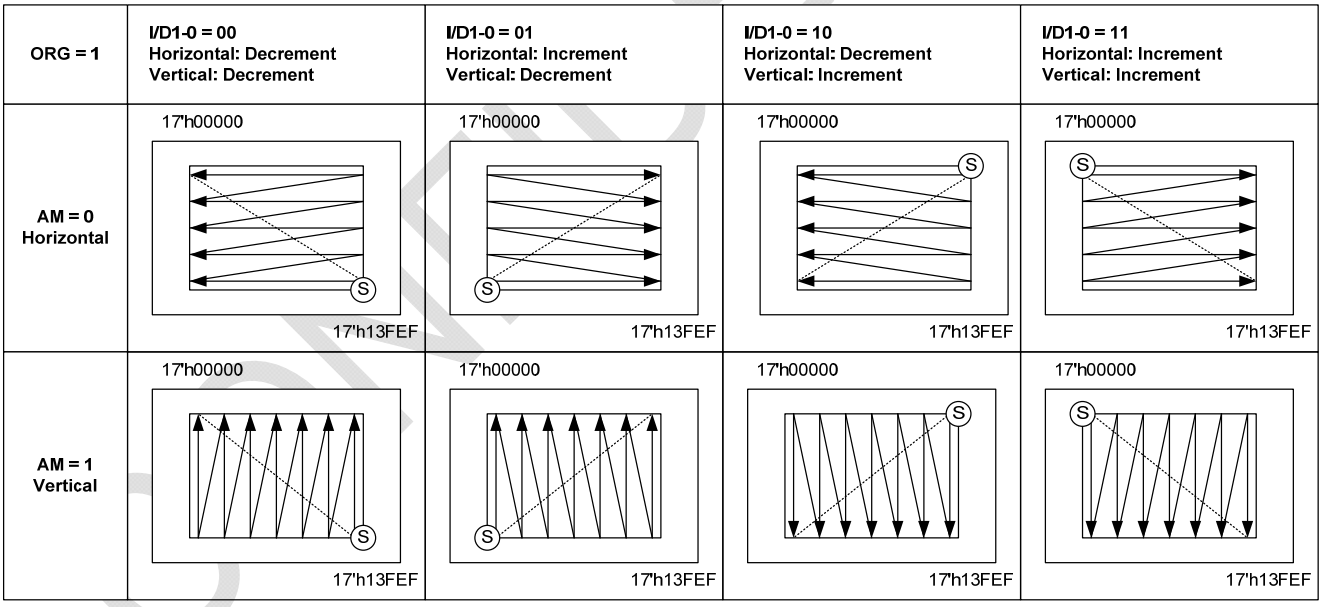


Figure 2 Automatic address update (ORG = 1, AM, ID)

Note: 1. When ORG = 1, make sure to set the address “h00000” in the RAM address set registers (R210h, R21h). Setting other addresses is inhibited. 2. When ORG = 1, the starting point of writing data within the window address area can be set at either corner of the window address area (“S” in circle in the above figure).

BGR: Reverse the order from RGB to BGR in writing 18-bit pixel data in the GRAM.

BGR = 0: Write data in the order of RGB to the GRAM.

BGR = 1: Reverse the order from RGB to BGR in writing data to the GRAM.

BGR = 0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR = 1

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

DFM: In combination with the TRI setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface.

TRI: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 16-bit bus interface operation,

TRI = 0: 16-bit RAM data is transferred in one transfer.

TRI = 1: 18-bit RAM data is transferred in two transfers.

In 8-bit interface operation,

TRI = 0: 16-bit RAM data is transferred in two transfers.

TRI = 1: 18-bit RAM data is transferred in three transfers.

9.5.4 Resizing Control (R04h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RSZ[1:0]: Sets the resizing factor. When the RSZ bits are set for resizing, the RM68023 writes the data according to the resizing factor so that the original image is displayed in horizontal and vertical dimensions contracted according to the factor. See “Resizing function”.

RCH[1:0]: Sets the number of pixels made as the remainder in horizontal direction when resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2’h0 when not using the resizing function (RSZ = 2’h0) or there are no remainder pixels.

RCV[1:0]: Sets the number of pixels made as the remainder in vertical direction when resizing a picture. By specifying the number of remainder pixels with the RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

Table 12 Resizing factor

RSZ[1:0]	Resizing Scale
2'h0	No resizing (x 1)
2'h1	x 1/2
2'h2	Setting disabled
2'h3	x 1/4

Table 13 Remainder Pixels in Horizontal Direction

RCH[1:0]	Number of remainder pixels in horizontal direction
2'h0	0
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Table 14 Remainder Pixels in Vertical Direction

RCV[1:0]	Number of remainder pixels in vertical direction
2'h0	0
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

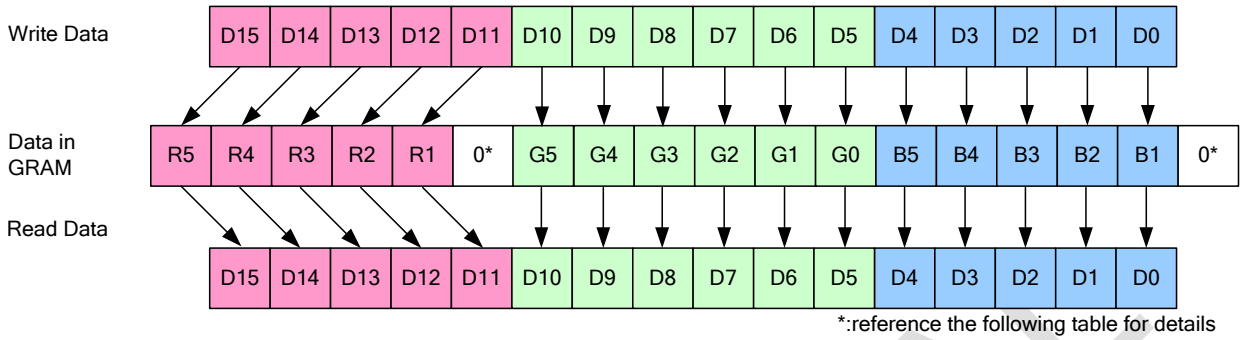
Note: 1 pixel = 1RGB

9.5.5 16bits Data Format Selection (R05h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

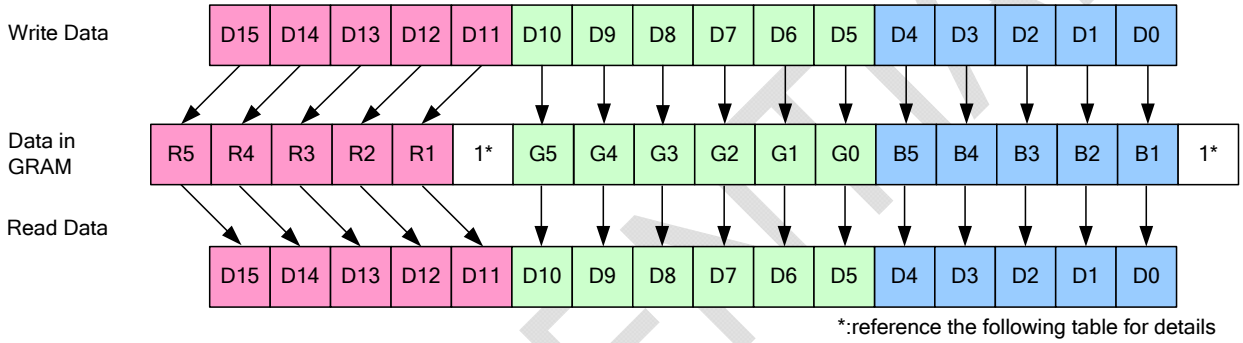
EPF[1:0]: The extension method for transforming 16bits data format to 18bits data format.

EPF[1:0]=00



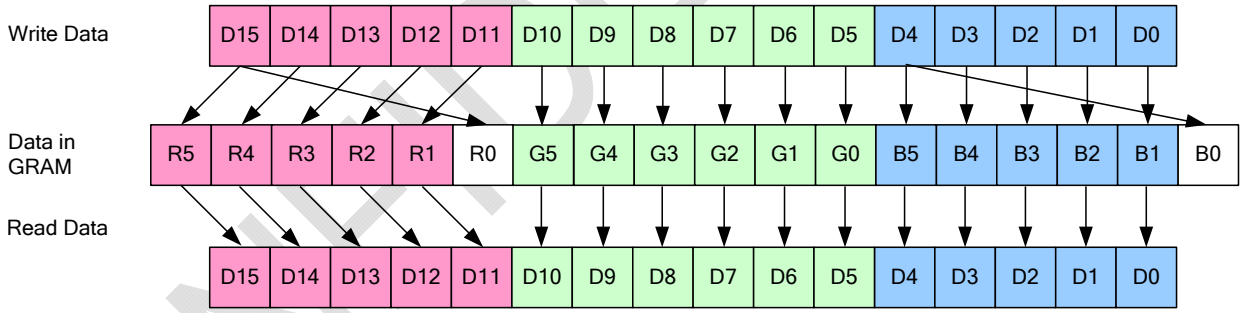
*:reference the following table for details

EPF[1:0]=01

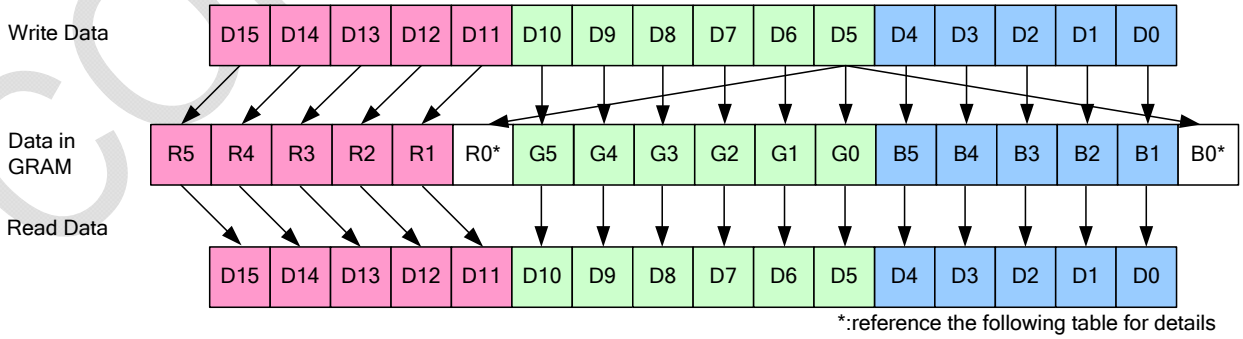


*:reference the following table for details

EPF[1:0]=10



EPF[1:0]=11



*:reference the following table for details

EPF[1:0]	Expand 16-bit pixel data(R,G,B) to 18-bit pixel data(r,g,b)
00	r[5:0] = {R[5:1], 0} (exception : if R[5:1]=5'h1F , r[5:0] = 6'h3F) g[5:0] = G[5:0] b[5:0] = {B[5:1], 0} (exception : if B[5:1]=5'h1F , b[5:0] = 6'h3F)
01	r[5:0] = {R[5:1], 1} (exception : if R[5:1]=5'h00, r[5:0] = 6'h00) g[5:0] = G[5:0] b[5:0] = {B[5:1], 1} (exception : if B[5:1]=5'h00, b[5:0] = 6'h00)
10	r[5:0] = {R[5:1], R[5]} g[5:0] = G[5:0] b[5:0] = {B[5:1], B[5]}
11	r[5:0] = (R[5:1]==G[5:1]) ? {R[5:1], G[0]} : {R[5:1], R[5]} g[5:0] = G[5:0] b[5:0] = (B[5:1]==G[5:1]) ? {B[5:1], G[0]} : {B[5:1], B[5]}

9.5.6 Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: A graphics display is turned on when writing D1 = “1”, and is turned off when writing D1 = “0”. When writing D1 = “0”, the graphics display data is retained in the internal GRAM and the RM68090 displays the data when writing D1 = “1”. When D1 = “0”, i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D1-0 = 2’b01, the RM68090 continues internal display operation. When the display is turned off by setting D1-0 = 2’b00, the RM68090’s internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D[1:0]	BASEE	Source, VCOM Output	Internal Operation
2’h0	*	GND	Halt
2’h1	*	GND	Operation
2’h2	*	Non-lit display	Operation
2’h3	0	Non-lit display	Operation
	1	Base-image display	Operation

Note:

1. The data write operation from the microcomputer is independent on the D[1:0] setting.
2. The D[1:0] setting is valid on both 1st and 2nd displays
3. The non-lit display level from the source output pins is determined by instruction (PTS).

CL: When CL = 1, the RM68090 displays in 8-colors with low power consumption.

CL	Display color
0	262,144
1	8

GON, DTE: The combination of GON and DTE settings set the output level form gate lines (G1 ~ G320).

GON	DTE	G1~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The RM68090 drives liquid crystal with non-lit display level or drives only partial image display areas.

BASEE = 1: A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE[1:0]: PTDE[0] is the display enable bit of partial image 1. PTDE[1] is the display enable bit of partial image 2. When PTDE1/0 = 0, the partial image is turned off and only base image is displayed on the screen.

When PTDE1/0 = 1, the partial image is displayed on the screen. In this case, turn off the base image by setting BASEE = 0.

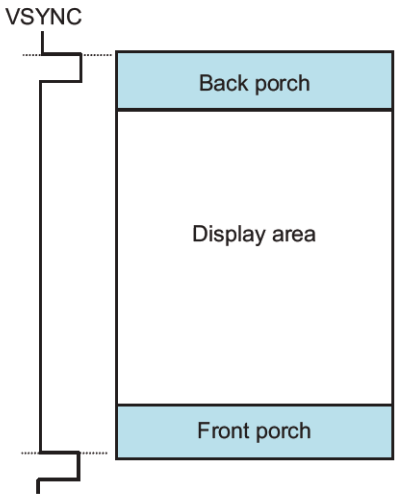
9.5.7 Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP [7:0] / BP [7:0]: Sets the number of lines for a front porch period / back porch period (a blank period following the end of display / (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

FP[7:0] BP[7:0]	Front and Back Porch period (Line periods)
8'h00	Setting disabled
8'h01	Setting disabled
8'h02	2 lines
8'h03	3 lines
8'h04	4 lines
8'h05	5 lines
8'h06	6 lines
8'h07	7 lines
8'h08	8 lines
8'h09	9 lines
8'h0A	10 lines
…	…
8'h7F	127 lines
8'h80	128 lines
8'h81	Setting disabled
…	…
8'hFF	Setting disabled



Note : The output timing to the LCD panel is delayed by two line periods from the synchronous signal (VSYNC) input timing.

9.5.8 Display Control 3 (R09h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC [3:0]: Set the scan cycle when setting PTG[1:0]=”10” to selects interval scan. The scan cycle is defined by from 0 to 29 as table below. The polarity is inverted in the same timing every interval scan cycle.

ISC[3:0]	Scan cycle	Time for interval when (f_{FLM}) = 60Hz
4’h0	0 frames	-
4’h1	0 frames	-
4’h2	3 frames	50 ms
4’h3	5 frames	84 ms
4’h4	7 frames	117 ms
4’h5	9 frames	150 ms
4’h6	11 frames	184 ms
4’h7	13 frames	217 ms
4’h8	15 frames	251 ms
4’h9	17 frames	284 ms
4’hA	19 frames	317 ms
4’hB	21 frames	351 ms
4’hC	23 frames	384 ms
4’hD	25 frames	418 ms
4’hE	27 frames	451 ms
4’hF	29 frames	484 ms

PTG[1:0]: Sets the scan mode in non-display area. The scan mode selected by PTG[1:0] bits is applied in the non-display area when the base image is turned off and the non-display area other than the first and second partial display areas.

PTG1	PTG0	Gate in non-display area	Source in non-display area	VCOM output
0	0	Normal scan	PTS[2:0] setting	VCOMH/VCOML
0	1	Setting disabled	-	-
1	0	Interval scan	PTS[2:0] setting	VCOMH/VCOML
1	1	Setting disabled	-	-

PTS[2:0]: Sets the source output level in non-display area drive period. When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in order to reduce power consumption.

PTS[1:0]	Source / VCOM output in non-display area	
	Frame with gate scan	Frame without gate scan
2’h0	White	V63 / VCOML
2’h1	Black	V0 / VCOML
2’h2	White	GND / GND
2’h3	White	Hi-Z / Hi-Z

9.5.9 Display Control 4 (R0Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE: When FMARKOE = 1, the RM68090 starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits.

FMI[2]	FMI[1]	FMI[0]	FMARK output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

9.5.10 External Display Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM 0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets the interface format in RGB interface.

RIM[1:0]	RGB interface operation	Display color
2'h0	18-bit RGB interface (1 transfer/pixel) via DB17-0	262,144
2'h1	16-bit RGB interface (1 transfer/pixel) via DB17-13 and DB 11-1	65,536
2'h2	6-bit RGB interface (3 transfers/pixel) via DB17-12	262,144
2'h3	Setting disabled	-

Note:

1. Instruction bits are set via system interface.
2. Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting disabled

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

RM	RAM Access Interface
0	System interface / VSYNC interface
1	RGB interface

ENC[2:0]: Sets the RAM write cycle via RGB interface.

ENC[2:0]	RAM Write Cycle (frame periods)
3'h0	1 frame
3'h1	2 frames
3'h2	3 frames
3'h3	4 frames
3'h4	5 frames
3'h5	6 frames
3'h6	7 frames
3'h7	8 frames

9.5.11 Frame Marker Position (R0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is outputted at the start of back porch period for 1H period .

Make sure the setting restriction 9'h000 ≤ FMP ≤ BP+NL+FP.

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1st line
9'h002	2nd line
…	…
9'h175	373rd line
9'h176	374th line
9'h177	375th line

9.5.12 External Display Interface Control 2 (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of DOTCLK pin.

DPL = 0: input data on the rising edge of DOTCLK

DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.

EPL = 0: writes data DB17-0 when ENABLE = “0” and disables data write operation when ENABLE = “1”.

EPL = 1: writes data DB17-0 when ENABLE = “1” and disables data write operation when ENABLE = “0”.

HSPL: Sets the signal polarity of HSYNC pin.

HSPL = 0: low active

HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNC pin.

VSPL = 0: low active

VSPL = 1: high active

9.6 Power Control

9.6.1 Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP: When SLP = 1, the RM68090 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following instruction, Exit sleep mode (SLP = “0”).

STB: When STB = 1, the RM68090 enters the standby mode and the display operation stops except the GRAM power supply to reduce the power consumption. In the standby mode, the GRAM data and instructions cannot be updated except the following instruction, Exit standby mode (STB = “0”).

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = 3’h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Gamma driver amplifiers	Source driver amplifiers
3’h0	Halt operation	Halt operation
3’h1	1.00	1.00
3’h2	1.00	0.75
3’h3	1.00	0.50
3’h4	0.75	1.00
3’h5	0.75	0.75
3’h6	0.75	0.50
3’h7	0.50	0.50

APE: Power supply enable bit.

Set APE = “1” to start the generation of power supply according to the power supply startup sequence.

SAP: Source Driver output control. SAP=0, Source driver is disabled. SAP=1, Source driver is enabled. When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	AVDD	VCL	VGH	VGL
3’h0	VCI1 x 2	-VCI1	VCI1 x 6	-VCI1 x 5
3’h1				-VCI1 x 4
3’h2				-VCI1 x 3
3’h3			VCI1 x 5	-VCI1 x 5
3’h4				-VCI1 x 4
3’h5				-VCI1 x 3
3’h6			VCI1 x 4	-VCI1 x 4
3’h7				-VCI1 x 3

Notes:

1. Connect capacitors where required when using AVDD, VGH, VGL and VCL voltages.
2. Set the following voltages within the respective ranges:

   AVDD = 6.0V (max.)

9.6.2 Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

DC0[2:0] / DC1[2:0]: Selects the operating frequency of the step-up circuit 1 / step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC0[2:0]	Step-up circuit 1: step-up frequency (f_{DCDC1})
3’h0	fbclk
3’h1	fbclk / 2
3’h2	fbclk / 4
3’h3	fbclk / 8
3’h4	fbclk / 16
3’h5	fbclk / 32
3’h6	fbclk / 64
3’h7	Halt Step-up circuit 1

DC1[2:0]	Step-up circuit 2: step-up frequency (f_{DCDC2})
3’h0	fbclk / 4
3’h1	fbclk / 8
3’h2	fbclk / 16
3’h3	fbclk / 32
3’h4	fbclk / 64
3’h5	fbclk / 128
3’h6	fbclk / 256
3’h7	Halt Step-up circuit 2

Note: Make sure the DC0, DC1 setting restriction: $f_{DCDC1} \geq f_{DCDC2}$. “fbclk” is a clock for boost circuit.

VC[2:0]: Sets the output level voltages of VCI1.

VC[2:0]	VCI1 Voltage
3'h0	2.75V
3'h1	2.70V
3'h2	2.65V
3'h3	2.60V
3'h4	2.55V
3'h5	2.50V
3'h6	Disabled
3'h7	VCI(bypass)

9.6.3 Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCIRE: Select the external reference voltage VCI or internal reference voltage VCIR.

VCIRE = 0	External reference voltage VCI (**default**)
VCIRE =1	Internal reference voltage 2.5V

VRH[3:0]: Sets the factor to generate GVDD from VCI.

	VCIRE=0	VCIRE=1
VRH[3:0]	**GVDD Voltage**	**GVDD Voltage**
4'h0	Halt	Halt
4'h1	VCI x 2.00	2.5V x 2.00 = 5.000V
4'h2	VCI x 2.05	2.5V x 2.05 = 5.125V
4'h3	VCI x 2.10	2.5V x 2.10 = 5.250V
4'h4	VCI x 2.20	2.5V x 2.20 = 5.500V
4'h5	VCI x 2.30	2.5V x 2.30 = 5.750V
4'h6	VCI x 2.40	2.5V x 2.40 = 6.000V
4'h7	VCI x 2.40	2.5V x 2.40 = 6.000V
4'h8	VCI x 1.60	2.5V x 1.60 = 4.000V
4'h9	VCI x 1.65	2.5V x 1.65 = 4.125V
4'hA	VCI x 1.70	2.5V x 1.70 = 4.250V
4'hB	VCI x 1.75	2.5V x 1.75 = 4.375V
4'hC	VCI x 1.80	2.5V x 1.80 = 4.500V
4'hD	VCI x 1.85	2.5V x 1.85 = 4.625V
4'hE	VCI x 1.90	2.5V x 1.90 = 4.750V
4'hF	VCI x 1.95	2.5V x 1.95 = 4.875V

Notes:

1. Make sure the VC and VRH setting restrictions: GVDD ≦ (AVDD-0.5)V.
2. When VCI<2.5V, internal reference voltage will be same as VCI.

9.6.4 Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VDV4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0]: Select the factor of GVDD to set the amplitude of VCOM alternating voltage from 0.70 to 1.24 x GVDD

VDV[4:0]	VCOM Amplitude	VDV[4:0]	VCOM Amplitude
5'h0	GVDD x 0.70	5'h10	GVDD x 0.94
5'h1	GVDD x 0.72	5'h11	GVDD x 0.96
5'h2	GVDD x 0.74	5'h12	GVDD x 0.98
5'h3	GVDD x 0.76	5'h13	GVDD x 1.00
5'h4	GVDD x 0.78	5'h14	GVDD x 1.02
5'h5	GVDD x 0.80	5'h15	GVDD x 1.04
5'h6	GVDD x 0.82	5'h16	GVDD x 1.06
5'h7	GVDD x 0.84	5'h17	GVDD x 1.08
5'h8	GVDD x 0.86	5'h18	GVDD x 1.10
5'h9	GVDD x 0.88	5'h19	GVDD x 1.12
5'hA	GVDD x 0.90	5'h1A	GVDD x 1.14
5'hB	GVDD x 0.92	5'h1B	GVDD x 1.16
5'hC	GVDD x 0.94	5'h1C	GVDD x 1.18
5'hD	GVDD x 0.96	5'h1D	GVDD x 1.20
5'hE	GVDD x 0.98	5'h1E	GVDD x 1.22
5'hF	GVDD x 1.00	5'h1F	GVDD x 1.24

9.7 RAM Access Instruction

9.7.1 RAM Address Set (Horizontal Address) (R20h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.7.2 RAM Address Set (Vertical Address) (R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the RM68090 writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note: In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

AD[16:0]	GRAM Data Setting
17'h00000 ~ 17'h000EF	Bitmap data on the 1st line
17'h00100 ~ 17'h001EF	Bitmap data on the 2nd line
17'h00200 ~ 17'h002EF	Bitmap data on the 3rd line
17'h00300 ~ 17'h003EF	Bitmap data on the 4th line
17'h00400 ~ 17'h004EF	Bitmap data on the 5th line
..	..
17'h13C00 ~ 17'h13CEF	Bitmap data on the 317th line
17'h13D00 ~ 17'h13DEF	Bitmap data on the 318th line
17'h13E00 ~ 17'h13EEF	Bitmap data on the 319th line
17'h13F00 ~ 17'h13FEF	Bitmap data on the 320th line

9.7.3 Write Data to GRAM (R22h)

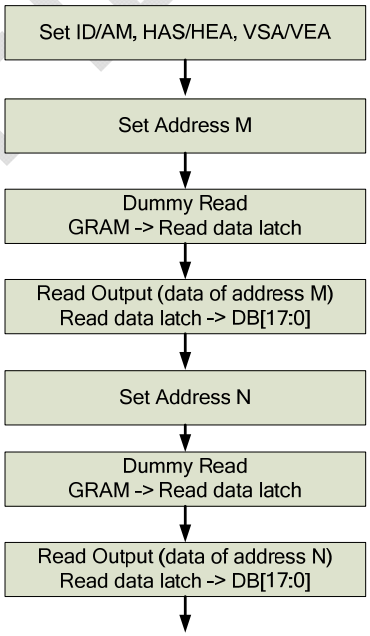
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operation.															

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

9.7.4 Read Data from GRAM (R22h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM read data RD[17:0] is transferred via different data bus in different interface operation.															

Read 18-bit data from GRAM through the read data register (RDR).



9.8 Power Control 7 (R29h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM [5:0]: Set internal VCOMH voltages.

VCM1[5:0]	VCOMH Voltage
6'h00	GVDD x 0.685
6'h01	GVDD x 0.690
6'h02	GVDD x 0.695
6'h03	GVDD x 0.700
6'h04	GVDD x 0.705
6'h05	GVDD x 0.710
6'h06	GVDD x 0.715
6'h07	GVDD x 0.720
6'h08	GVDD x 0.725
6'h09	GVDD x 0.730
6'h0A	GVDD x 0.735
6'h0B	GVDD x 0.740
6'h0C	GVDD x 0.745
6'h0D	GVDD x 0.750
6'h0E	GVDD x 0.755
6'h0F	GVDD x 0.760
6'h10	GVDD x 0.765
6'h11	GVDD x 0.770
6'h12	GVDD x 0.775
6'h13	GVDD x 0.780
6'h14	GVDD x 0.785
6'h15	GVDD x 0.790
6'h16	GVDD x 0.795
6'h17	GVDD x 0.800
6'h18	GVDD x 0.805
6'h19	GVDD x 0.810
6'h1A	GVDD x 0.815
6'h1B	GVDD x 0.820
6'h1C	GVDD x 0.825
6'h1D	GVDD x 0.830
6'h1E	GVDD x 0.835
6'h1F	GVDD x 0.840

VCM1[5:0]	VCOMH Voltage
6'h20	GVDD x 0.845
6'h21	GVDD x 0.850
6'h22	GVDD x 0.855
6'h23	GVDD x 0.860
6'h24	GVDD x 0.865
6'h25	GVDD x 0.870
6'h26	GVDD x 0.875
6'h27	GVDD x 0.880
6'h28	GVDD x 0.885
6'h29	GVDD x 0.890
6'h2A	GVDD x 0.895
6'h2B	GVDD x 0.900
6'h2C	GVDD x 0.905
6'h2D	GVDD x 0.910
6'h2E	GVDD x 0.915
6'h2F	GVDD x 0.920
6'h30	GVDD x 0.925
6'h31	GVDD x 0.930
6'h32	GVDD x 0.935
6'h33	GVDD x 0.940
6'h34	GVDD x 0.945
6'h35	GVDD x 0.950
6'h36	GVDD x 0.955
6'h37	GVDD x 0.960
6'h38	GVDD x 0.965
6'h39	GVDD x 0.970
6'h3A	GVDD x 0.975
6'h3B	GVDD x 0.980
6'h3C	GVDD x 0.985
6'h3D	GVDD x 0.990
6'h3E	GVDD x 0.995
6'h3F	GVDD x 1.000

9.9 Frame Rate and Color Control (R2Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS2	FRS2	FRS1	FRS0
Default		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

FRS[4:0] Set the frame rate when the internal resistor is used for oscillator circuit.

FRS[3:0]	Frame Rate	FRS[3:0]	Frame Rate
0000	30	1000	51
0001	31	1001	56
0010	33	1010	62
0011	35	1011	70 (default)
0100	38	1100	80
0101	40	1101	93
0110	43	1110	Setting Prohibited
0111	47	1111	Setting Prohibited

9.10 γ Control

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R30h	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31h	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32h	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP1[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35h	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R36h	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37h	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38h	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39h	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN1[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3Ch	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3Dh	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

KP5-0[2:0] / KN5-0[2:0] : γ Fine Adjustment Register for positive/negative polarity

PRP1-0[2:0] / PRN1-0[2:0] : γ Gradient Adjustment Register for positive/negative polarity

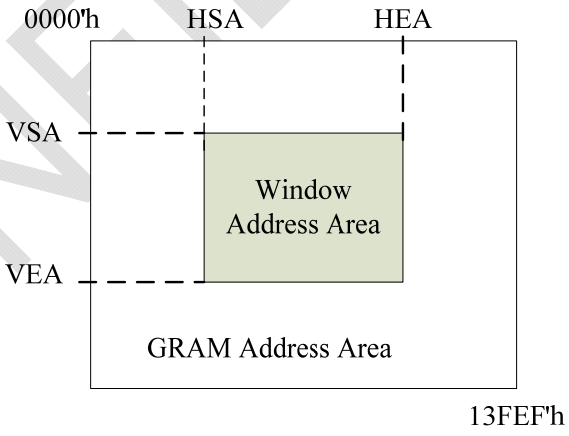
VRP1-0[4:0] / VRN1-0[4:0]: γ Amplitude Adjustment Register for positive/negative polarity

9.11 Window Address Write Control Instruction

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R51h	W	1	0	0	0	0	0	0	0	0	HEA7	HSA6	HSA5	HEA4	HEA3	HEA2	HEA1	HEA0
R52h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R53h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VSA6	VSA5	VEA4	VEA3	VEA2	VEA1	VEA0
R50h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51h			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R52h			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53h			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HAS < HEA ≤ 8'hEF and 8'h01 ≤ HEA – HSA.

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h13F.



Note: The window address range must be within the GRAM address space.

9.12 Base Image Display Control Instruction

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R60h	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

R61h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
R6Ah	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R60h	Default		0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
R61h			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6Ah			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the RM68090 to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	…	…	…
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	…	…	…
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the RM68090 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image
0	Fixed
1	Enable scrolling

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	Number of Lines	NL[5:0]	Number of Lines	NL[5:0]	Number of Lines
6'h00	8 (lines)	6'h0E	112	6'h1C	232
6'h01	16	6'h0F	120	6'h1D	240
6'h02	24	6'h10	128	6'h1E	248
6'h03	32	6'h11	136	6'h1F	256
6'h04	40	6'h12	144	6'h20	264
6'h05	48	6'h13	152	6'h21	272
6'h06	48	6'h14	160	6'h22	280
6'h07	56	6'h15	168	6'h23	288
6'h08	64	6'h16	176	6'h24	296
6'h09	72	6'h17	184	6'h25	304
6'h0A	80	6'h18	192	6'h26	312

6’h0B	88	6’h19	200	6’h27	320
6’h0C	96	6’h1A	216	Others	Setting inhibited
6’h0D	104	6’h1B	224		

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

SCN[5:0]	**Gate Line No (Scan start position)**			
	SM=0		**SM=1**	
	GS=0	**GS=1**	**GS=0**	**GS=1**
6’h00	G1	G320	G1	G320
6’h01	G9	G312	G17	G304
6’h02	G17	G304	G33	G288
6’h03	G25	G296	G49	G272
6’h04	G33	G288	G65	G256
6’h05	G41	G280	G81	G240
6’h06	G49	G272	G97	G224
6’h07	G57	G264	G113	G208
6’h08	G65	G256	G129	G192
6’h09	G73	G248	G145	G176
6’h0A	G81	G240	G161	G160
6’h0B	G89	G232	G177	G144
6’h0C	G97	G224	G193	G128
6’h0D	G105	G216	G209	G112
6’h0E	G113	G208	G225	G96
6’h0F	G121	G200	G241	G80
6’h10	G129	G192	G257	G64
6’h11	G137	G184	G273	G48
6’h12	G145	G176	G289	G32
6’h13	G153	G168	G305	G16
6’h14	G161	G160	G2	G319
6’h15	G169	G152	G18	G303
6’h16	G177	G144	G34	G287
6’h17	G185	G136	G50	G271
6’h18	G193	G128	G66	G255
6’h19	G201	G120	G82	G239
6’h1A	G209	G112	G98	G223
6’h1B	G217	G104	G114	G207
6’h1C	G225	G96	G130	G191
6’h1D	G233	G88	G146	G175
6’h1E	G241	G80	G162	G159
6’h1F	G249	G72	G178	G143
6’h20	G257	G64	G194	G127
6’h21	G265	G56	G210	G111
6’h22	G273	G48	G226	G95
6’h23	G281	G40	G242	G79
6’h24	G289	G32	G258	G63
6’h25	G297	G24	G274	G47
6’h26	G305	G16	G290	G31
6’h27	G313	G8	G306	G15
6’h28~6’h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NDL: Sets the source output level in non-lit display area. NDL bit can keep the non-display area lit on.

NDL	**Non-display area**	
	Positive	**Negative**

0	V63	V0
1	V0	V63

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0]. Make sure VL[8:0] ≤ 320.

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

9.13 Partial Display Control Instruction

9.13.1 Partial Image 1: Display Position (R80h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTDP0[8]	PTDP0[7]	PTDP0[6]	PTDP0[5]	PTDP0[4]	PTDP0[3]	PTDP0[2]	PTDP0[1]	PTDP0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.13.2 Partial Image 1: RAM Address (Start Line Address) (R81h), (End Line Address) (R82h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTSA0[8]	PTSA0[7]	PTSA0[6]	PTSA0[5]	PTSA0[4]	PTSA0[3]	PTSA0[2]	PTSA0[1]	PTSA0[0]
W	1	0	0	0	0	0	0	0	PTEA0[8]	PTEA0[7]	PTEA0[6]	PTEA0[5]	PTEA0[4]	PTEA0[3]	PTEA0[2]	PTEA0[1]	PTEA0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.13.3 Partial Image 2: Display Position (R83h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTDP1[8]	PTDP1[7]	PTDP1[6]	PTDP1[5]	PTDP1[4]	PTDP1[3]	PTDP1[2]	PTDP1[1]	PTDP1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.13.4 Partial Image 2: RAM Address (Start Line Address) (R84h), (End Line Address) (R85h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTSA1[8]	PTSA1[7]	PTSA1[6]	PTSA1[5]	PTSA1[4]	PTSA1[3]	PTSA1[2]	PTSA1[1]	PTSA1[0]
W	1	0	0	0	0	0	0	0	PTEA1[8]	PTEA1[7]	PTEA1[6]	PTEA1[5]	PTEA1[4]	PTEA1[3]	PTEA1[2]	PTEA1[1]	PTEA1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[8:0]: Sets the display position of partial image 1.

PTDP1[8:0]: Sets the display position of partial image 2.

PTSA0[8:0] and PTEA0[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 1. In setting, make sure that PTSA0 ≤ PTEA0.

PTSA1[8:0] and PTEA1[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 2. In setting, make sure that PTSA1 ≤ PTEA1.

9.14 Panel Interface Control Instruction

9.14.1 Panel Interface Control 1 (R90h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the RM68090's display operation is synchronized with internal clock.

DIVI[1:0]: Sets the division ratio of the internal clock frequency.

Frame Frequency Calculation

$$Frame\ frequency = \frac{fosc}{Clocks\ per\ line \times division\ ratio \times (line + BP + FP)}\ [Hz]$$

fosc : RC oscillation frequency
Line : Number of lines to drive the LCD (NL bits)
Division ratio : DIVI
Clocks per line : RTNI

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

RTNI[4:0]	Clocks per line
5'h00~5'h0F	Setting inhibited
5'h10	16 clocks
5'h11	17 clocks
5'h12	18 clocks
5'h13	19 clocks
5'h14	20 clocks

RTNI[4:0]	Clocks per line
5'h15	21 clocks
5'h16	22 clocks
5'h17	23 clocks
5'h18	24 clocks
5'h19	25 clocks
5'h1A	26 clocks

RTNI[4:0]	Clocks per line
5'h1B	27 clocks
5'h1C	28 clocks
5'h1D	29 clocks
5'h1E	30 clocks
5'h1F	31 clocks

9.14.2 Panel Interface Control 2 (R92h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation synchronizing with the internal clock.

NOWI[2:0]	Non-overlap period
3'h0	Setting inhibited
3'h1	1 (internal clock)
3'h2	2
3'h3	3

NOWI[2:0]	Non-overlap period
3'h4	4
3'h5	5
3'h6	6
3'h7	Setting inhibited

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits.

9.14.3 Panel Interface Control 4 (R95h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DIVE[1:0]: Sets the division ratio of DOTCLK when RM68090 display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	Internal operation clock unit (DOTCLK)			
		18-bit, 1 transfer RGB interface	DOTCLK = 5 MHz	6-bit, 3 transfer RGB interface	DOTCLK = 15 MHz
2'h0	Setting inhibited	Setting inhibited	-	Setting inhibited	-
2'h1	1/4	4 DOTCLKs	0.8 us	12 DOTCLKs	0.8 us
2'h2	1/8	8 DOTCLKs	1.6 us	24 DOTCLKs	1.6 us
2'h3	1/16	16 DOTCLKs	3.2 us	48 DOTCLKs	3.2 us

9.14.4 Panel Interface Control 5 (R97h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	NOWE[3]	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

NOWE[3:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

NOWE[3:0]	Non-overlap period
4'h0	Setting inhibited
4'h1	1 (clocks)
4'h2	2
4'h3	3
4'h4	4
4'h5	5
4'h6	6
4'h7	7

NOWE[3:0]	Non-overlap period
4'h8	8
4'h9	9
4'hA	10
4'hB	Disabled
4'hC	Disabled
4'hD	Disabled
4'hE	Disabled
4'hF	Disabled

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) [DOTCLK].

9.15 OTP VCM Control

9.15.1 OTP VCM Programming Control 1 (RA1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_ OTP5	VCM_ OTP4	VCM_ OTP3	VCM_ OTP2	VCM_ OTP1	VCM_ OTP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTP_PGM_EN: OTP programming enable. When program OTP, must set this bit.

OTP data can be programmed 3 times.

VCM_OTP[5:0]: OTP programming data for VCOMH voltage, the voltage refer to VCM[5:0] value.

9.15.2 OTP VCM Status and Enable (RA2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	PGM_ CNT1	PGM_ CNT0	VCM_ D5	VCM _D4	VCM _D3	VCM _D2	VCM _D1	VCM _D0	0	0	0	0	0	0	0	VCM_ EN
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PGM_CNT[1:0]: OTP programmed record. These bits are read only.

OTP_PGM_CNT[1:0]	Description
2'h0	OTP clean
2'h1	OTP programmed 1 time
2'h2	OTP programmed 2 times
2'h3	OTP programmed 3 times

VCM_D[5:0]: OTP VCM data read value. These bits are read only.

VCM_EN: OTP VCM data enable.

VCM_EN=1: Set this bit to enable OTP VCM data to replace R29h VCM value.

VCM_EN=0: Default value, use R29h VCM value.

9.15.3 OTP VCM Programming ID Key (RA5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KEY[15:0]: OTP Programming ID key protection. Before writing OTP programming data RA1h, it must write RA5h with 0xAA55 value first to make OTP programming successfully. If RA5h is not written with 0xAA55, OTP programming will be fail. See OTP Programming flow.

9.16 CABC control

9.16.1 Write Display Brightness Value (RB1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to adjust the brightness value of the display.

DBV[7:0]: control the brightness of manual setting or CABC in RM68051. The PWM output signal, LEDPWM, controls the LED driver IC to decide the display brightness

9.16.2 Read Display Brightness Value (RB2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to return the brightness value of the display.

DBV[7:0] is reset when display is in sleep-in mode.

DBV[7:0] is ‘0’ when bit BCTRL of “Write CTRL Display (B3h)” command is ‘0’.

DBV[7:0] is manual set brightness specified with “Write CTRL Display (B3h)” command when BCTRL bit is ‘1’.

When bit BCTRL of “Write CTRL Display (B3h)” command is ‘1’ and C1/C0 bit of “Write Content Adaptive Brightness Control (B5h)” command are ‘0’, DBV[7:0] output is the brightness value specified with “Write Display Brightness (B1h)” command.

9.16.3 Write CTRL Display Value (RB3h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0

This command is used to set the brightness control mechanism.

BCTRL: Brightness control block on/off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00H)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control.

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1→ 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected

9.16.4 Read CTRL Display Value (RB4h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0

This command is used to read the status of the brightness control mechanism.

9.16.5 Write Content Adaptive Brightness Control Value (RB5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1]	C[0]

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]	Description
2’h0	CABC OFF
2’h1	User Interface Image
2’h2	Still Picture
2’h3	Moving Image

9.16.6 Read Content Adaptive Brightness Control Value (RB6h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1]	C[0]

This command is used to read the status for image content based adaptive brightness control functionality.

9.16.7 Write CABC Minimum Brightness (RBEh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed. This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of “Write CTRL Display (B3h)”), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

9.16.8 Read CABC Minimum Brightness (RBFh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]

This command is used to read the minimum brightness value of the display for CABC function.

9.17 Deep standby control (RE6h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTB: When DSTB = 1, the RM68090 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not kept when the RM68090 enters the deep standby mode, and they would be reset automatically after exiting deep standby mode.

To exit deep standby mode, nCS pin needs to be toggled from low to high 6 times.

10. Instruction List

No.	Register Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	1
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I//D1	I/D0	AM	0	0	0
04h	Resize Control	W	1	0	0	0	0	0	0	RCV1	RCV2	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
05h	16 bits data format control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM 0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

22h	Write Data to GRAM	RAM write data WD[17:0] / read data RD[17:0] is transferred via different data bus in different interface operation.																
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS2	FRS2	FRS1	FRS0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP1[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN1[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HSA6	HSA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VSA6	VSA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
66h	SPI Read/Write Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP0[8]	PTDP0[7]	PTDP0[6]	PTDP0[5]	PTDP0[4]	PTDP0[3]	PTDP0[2]	PTDP0[1]	PTDP0[0]
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA0[8]	PTSA0[7]	PTSA0[6]	PTSA0[5]	PTSA0[4]	PTSA0[3]	PTSA0[2]	PTSA0[1]	PTSA0[0]
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA0[8]	PTEA0[7]	PTEA0[6]	PTEA0[5]	PTEA0[4]	PTEA0[3]	PTEA0[2]	PTEA0[1]	PTEA0[0]

83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP1[8]	PTDP1[7]	PTDP1[6]	PTDP1[5]	PTDP1[4]	PTDP1[3]	PTDP1[2]	PTDP1[1]	PTDP1[0]
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA1[8]	PTSA1[7]	PTSA1[6]	PTSA1[5]	PTSA1[4]	PTSA1[3]	PTSA1[2]	PTSA1[1]	PTSA1[0]
85h	Partial Image 2 Area (End Line	W	1	0	0	0	0	0	0	0	PTEA1[8]	PTEA1[7]	PTEA1[6]	PTEA1[5]	PTEA1[4]	PTEA1[3]	PTEA1[2]	PTEA1[1]	PTEA1[0]
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE[3]	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	0	0	0	0
A1h	OTP VCM Programming Control	W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
A2h	OTP VCM Status and Enable	W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
A5h	OTP Programming ID Key	W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
E6h	Deep stand by mode control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB

11. Interface and Data Format

The RM68090 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The RM68090 can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the RM68090 supports RGB interface and VSYNC interface, which enables data rewrite operation without flicker effect of the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the RM68090 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the RM68090's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The RM68090 operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register (R0Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes:

1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.

12. System Interface

The following are the kinds of system interfaces available with the RM68090. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

IM3	IM2	IM1	IM0	Interfacing Mode with MPU	DB pins	Colors
0	0	0	0	80-system 8-bit bus interface I	DB7-0	262,144
0	0	0	1	80-system 16-bit bus interface I	DB15-0	262,144
0	0	1	0	80-system 9-bit bus interface I	DB8-0	262,144
0	0	1	1	80-system 18-bit bus interface I	DB17-10	262,144
0	1	0	0	Setting disabled		
0	1	0	1	3-wire 9-bit data serial interface	SDA	262,144
0	1	1	0	4-wire 8-bit data serial interface	SDA	65,536
0	1	1	1	Setting disabled		
1	0	0	0	80-system 16-bit bus interface II	DB17-10, DB8-1	262,144
1	0	0	1	80-system 8-bit bus interface II	DB17-10	262,144
1	0	1	0	80-system 18-bit bus interface II	DB17-0	262,144
1	0	1	1	80-system 9-bit bus interface II	DB17-9	262,144
1	1	*	*	Clock synchronous serial interface	(SDI, SDO)	65,536

12.1 80-system 18-bit Bus Interface

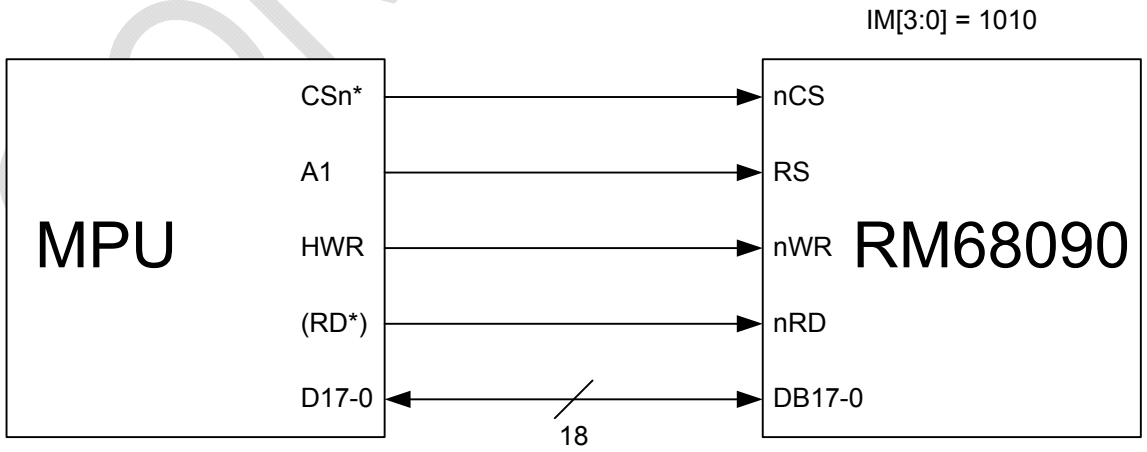


Figure 3 18-bit bus interface for 80-system

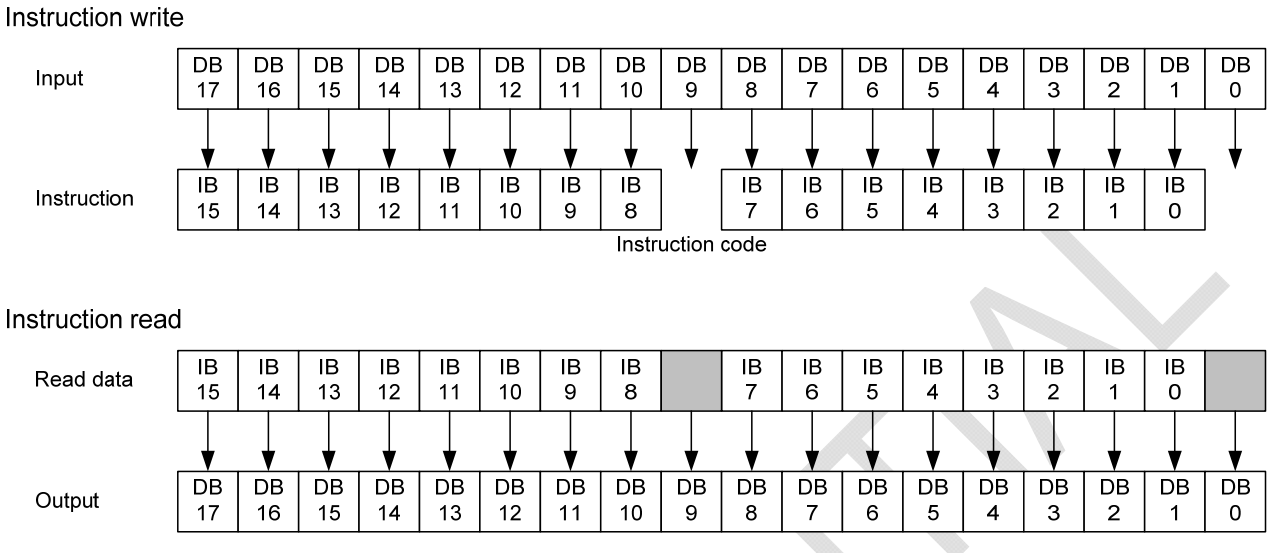


Figure 4 18-bit Interface Data Format (Instruction Write / Instruction Read)

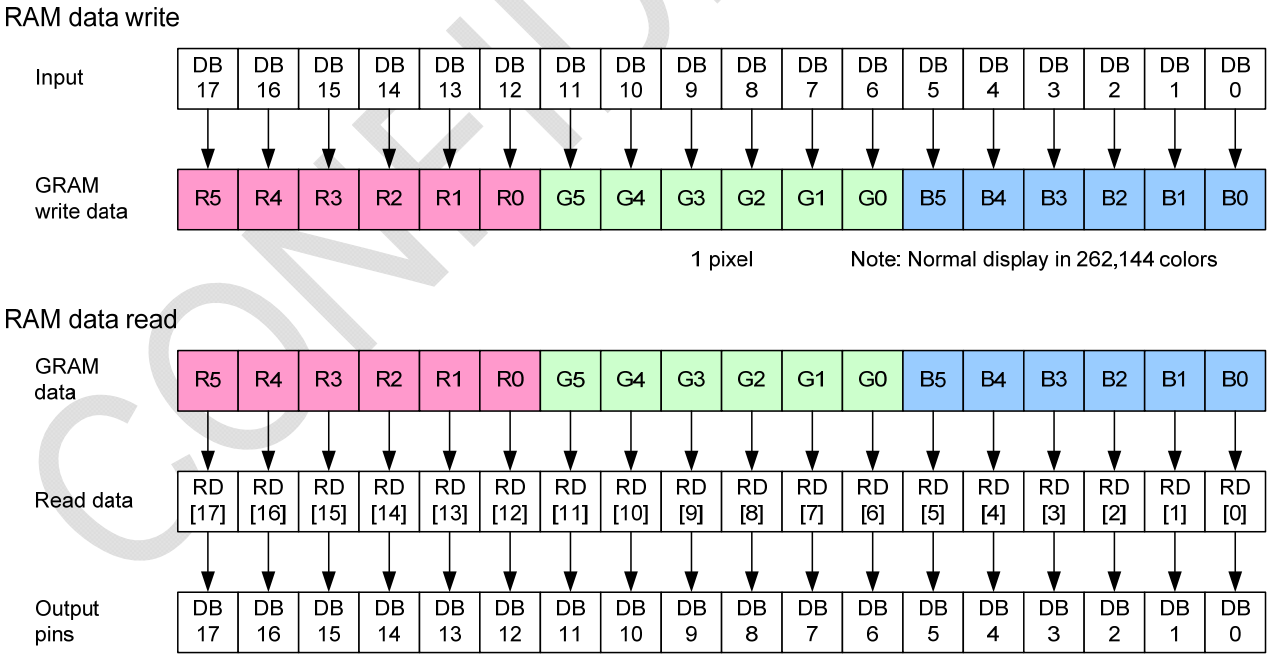


Figure 5 18-bit Interface Data Format (RAM Data Write / RAM Data Read)

12.2 80-system 16-bit Bus Interface

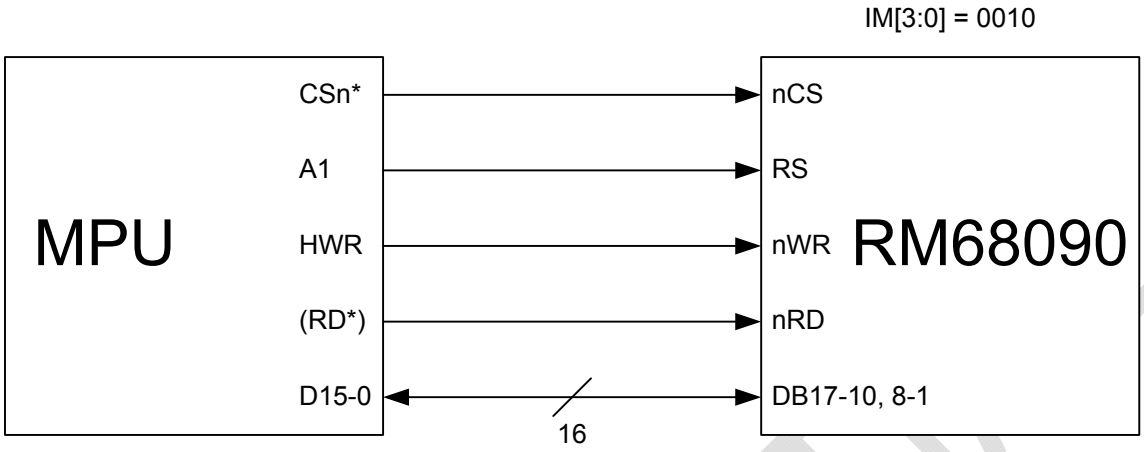


Figure 6 16-bit bus interface for 80-system

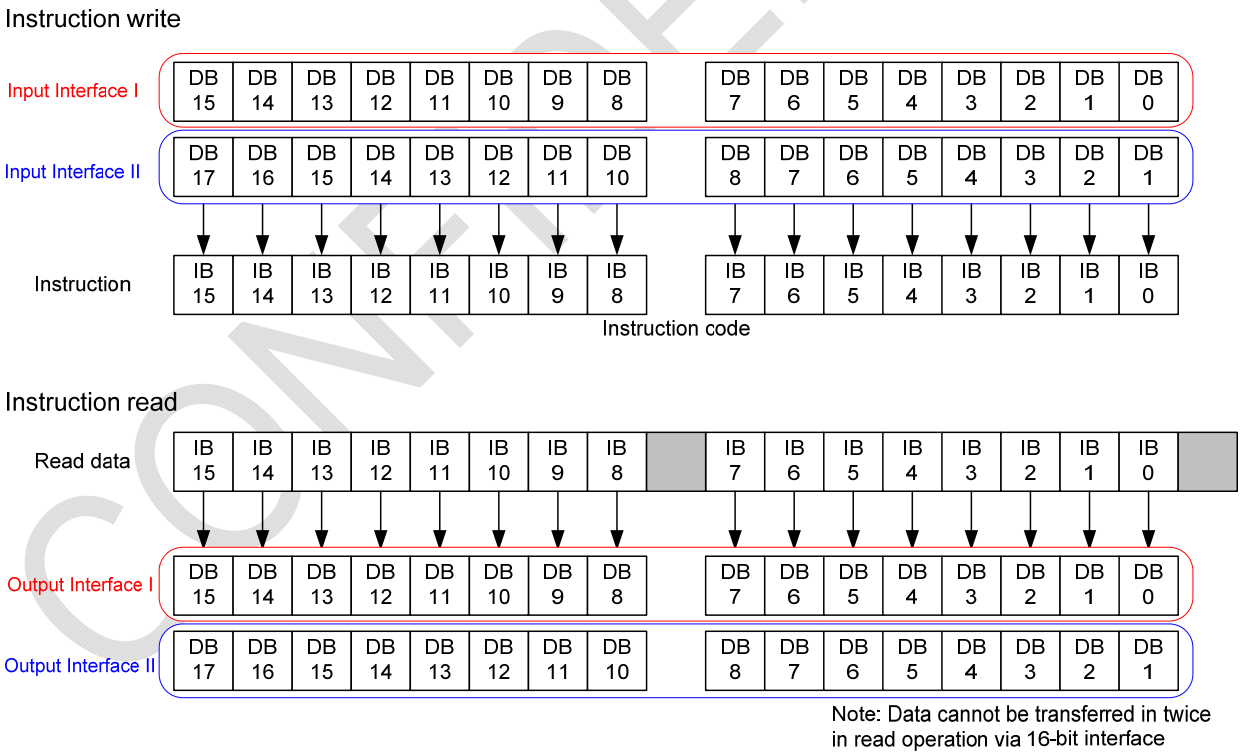


Figure 7 16-bit Interface Data Format (Instruction Write / Instruction Read)

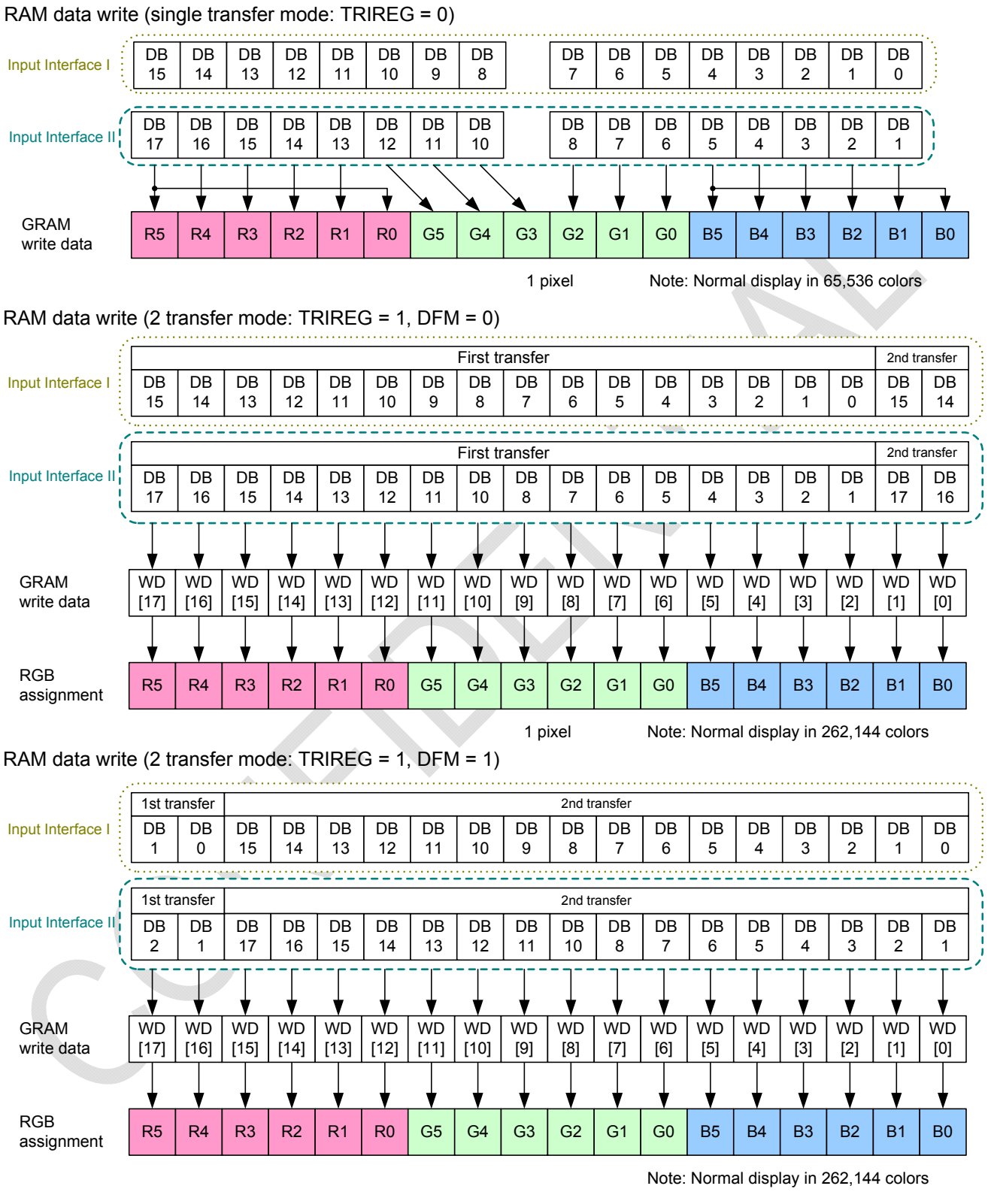


Figure 8 16-bit Interface Data Format (RAM data write)

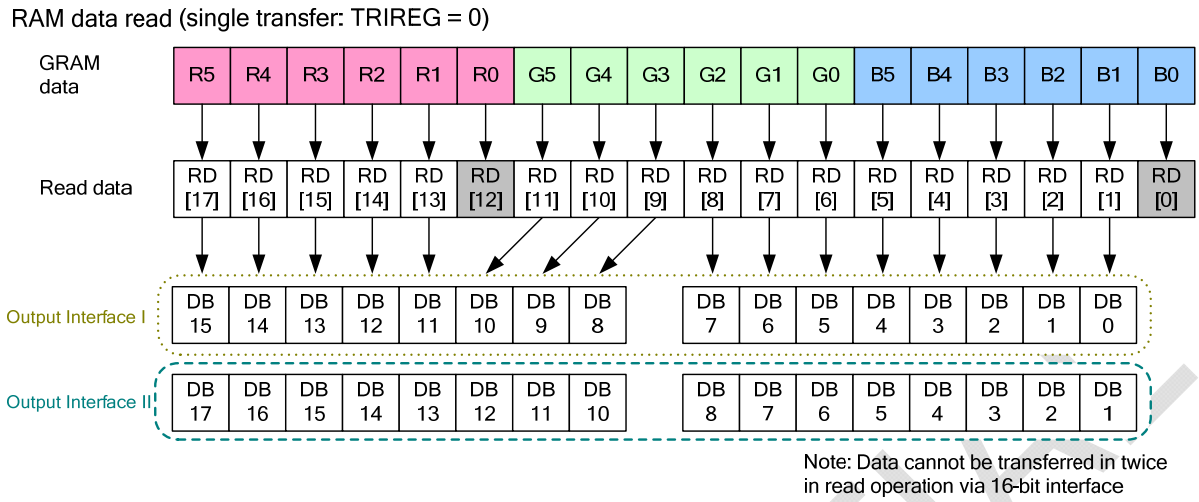


Figure 9 16-bit Interface Data Format (RAM data read)

12.3 80-system 9-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either VDDI or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

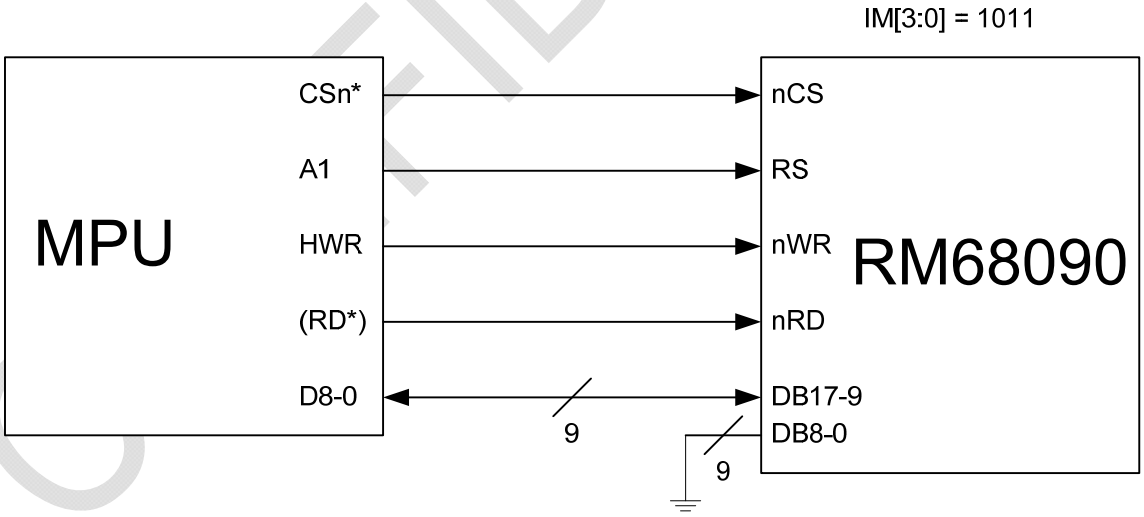


Figure 10 9-bit bus interface for 80-system

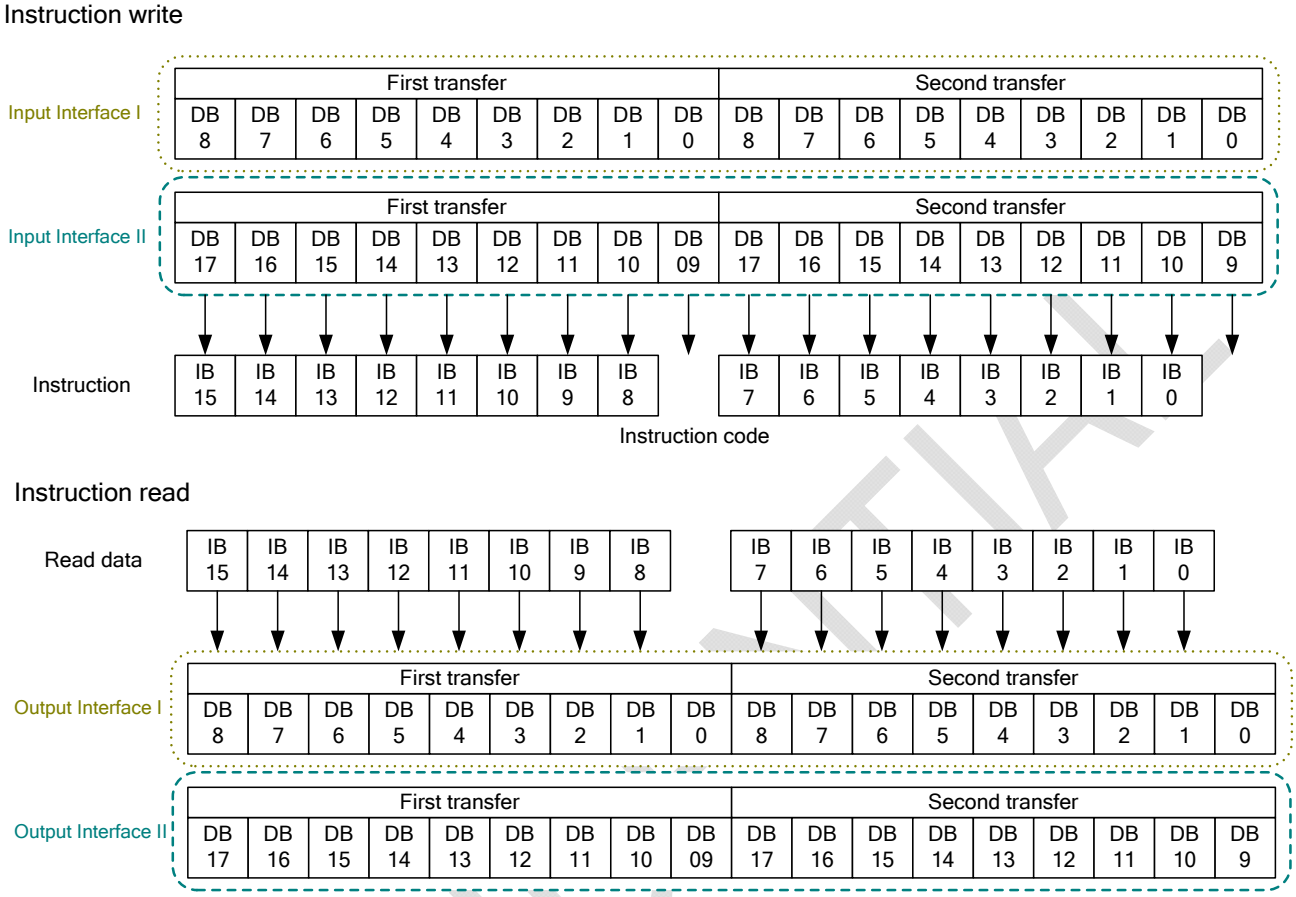
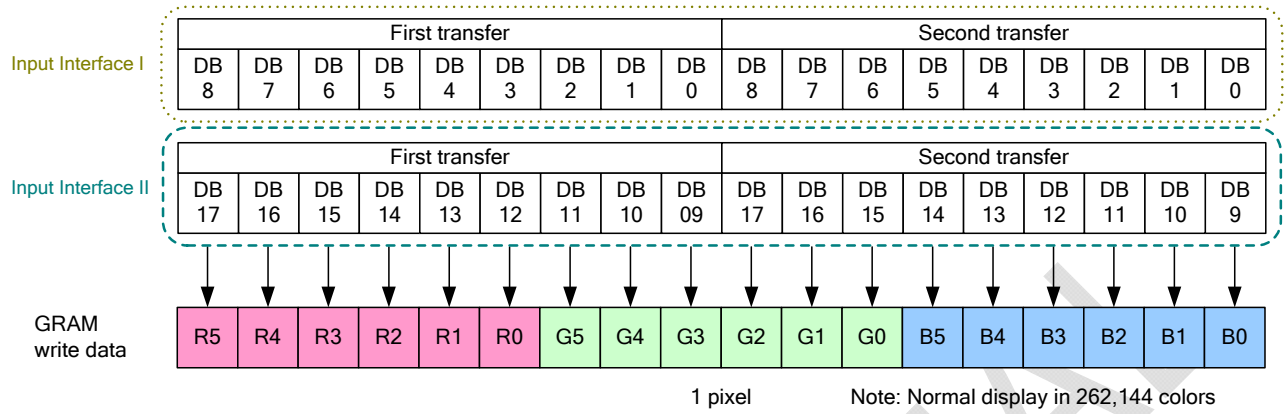


Figure 11 9-bit Interface Data Format (Instruction Write / Device Code Read)

RAM data write



RAM data read

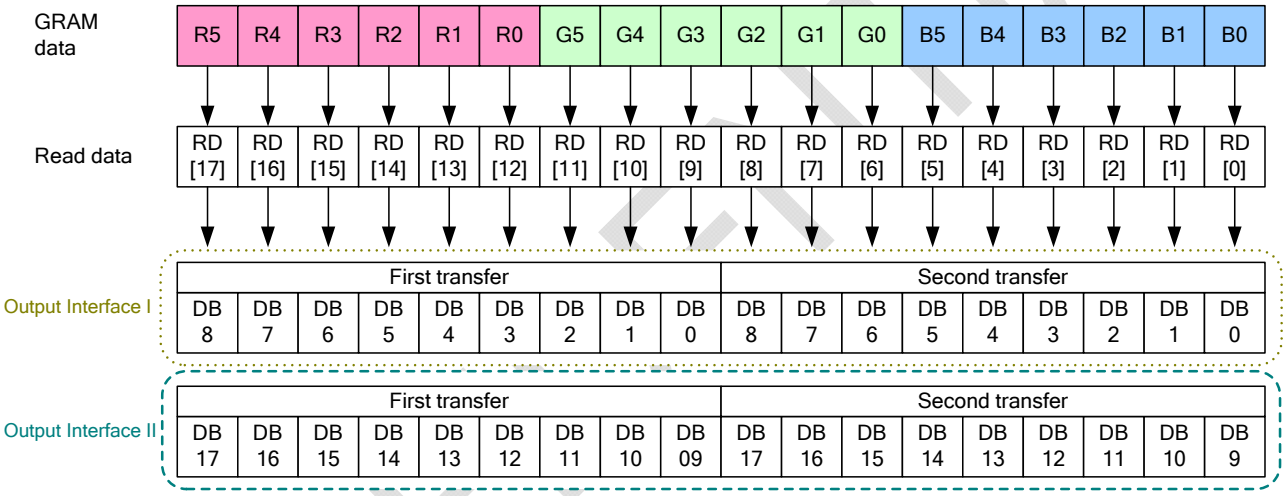


Figure 12 9-bit Interface Data Format (RAM Data Write / RAM Data Read)

12.4 80-system 8-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either VDDI or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

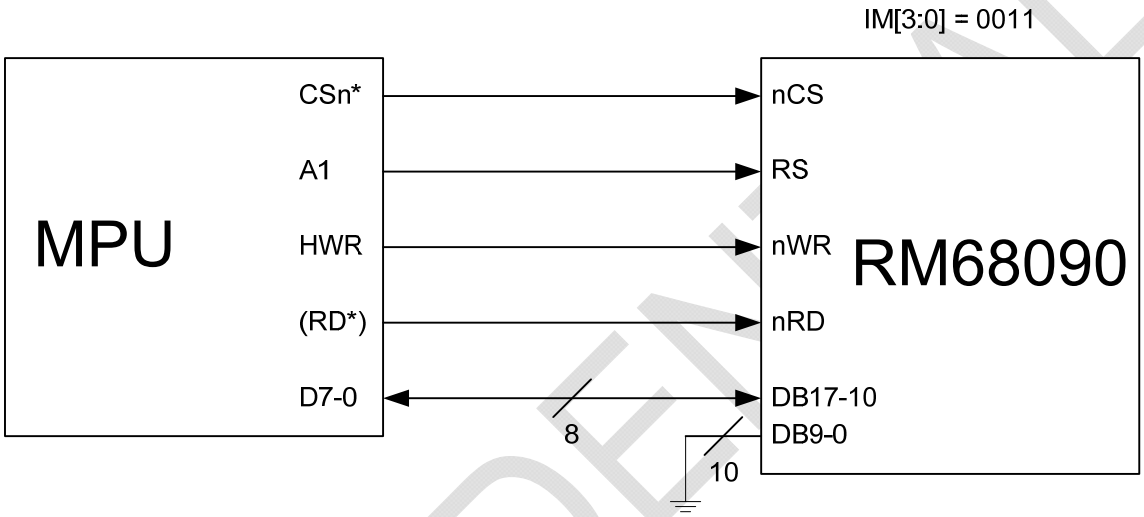


Figure 13 8-bit bus interface for 80-system

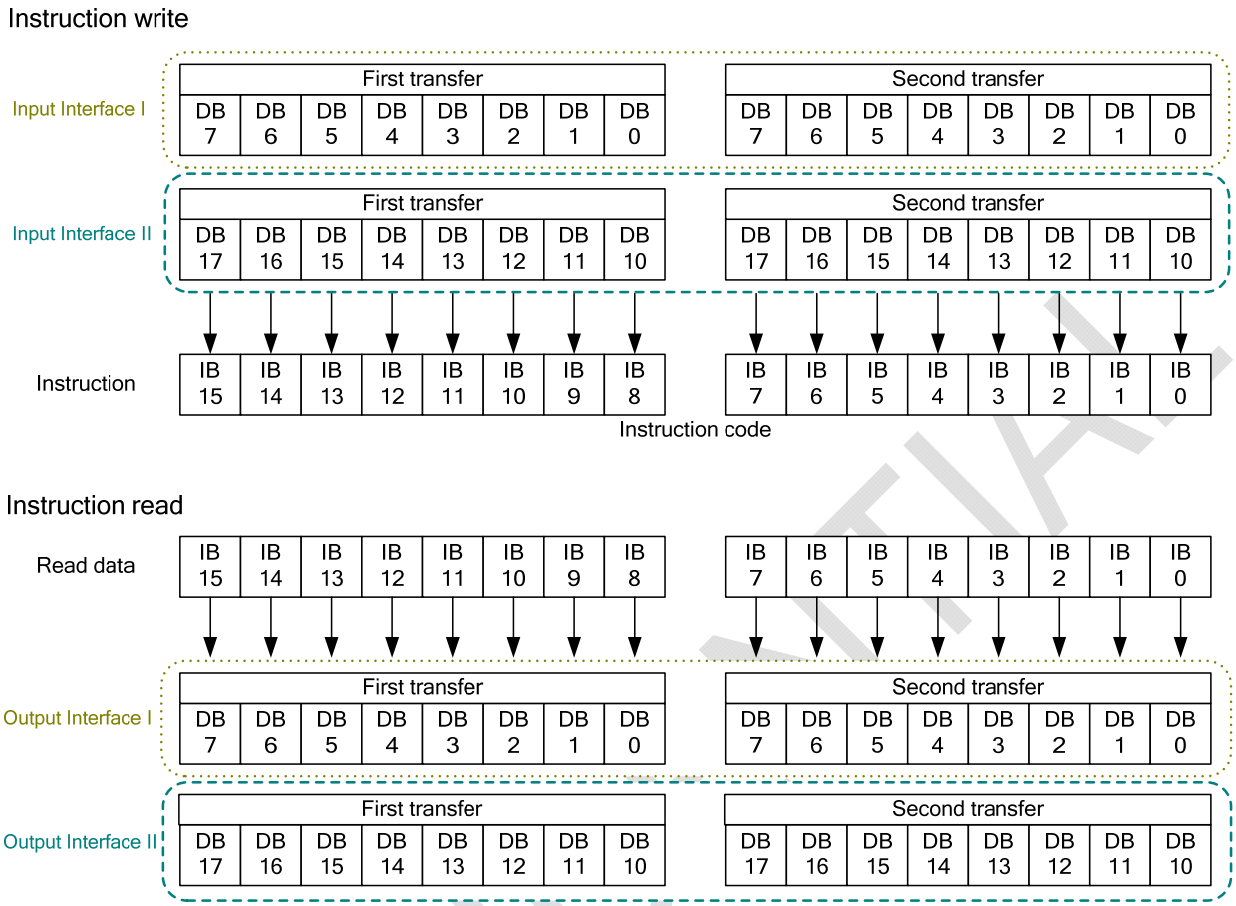
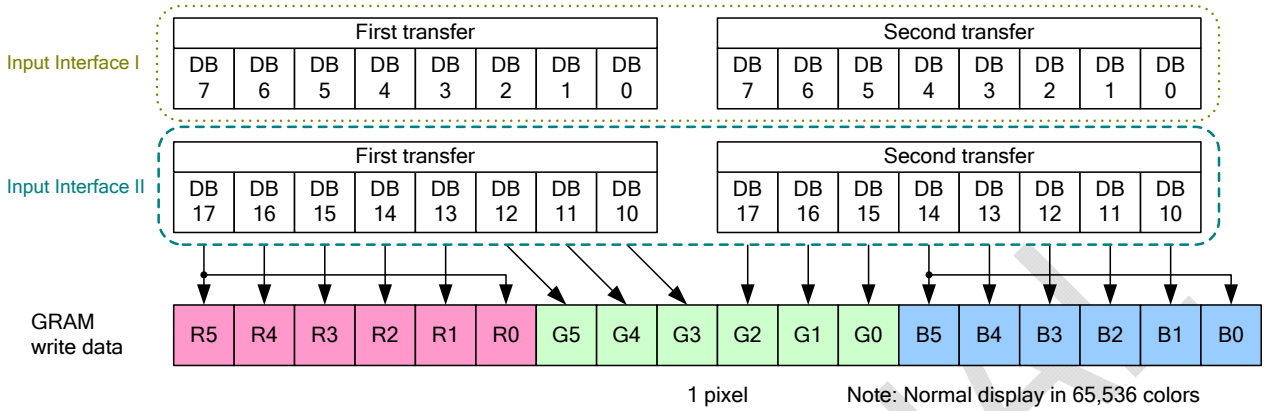
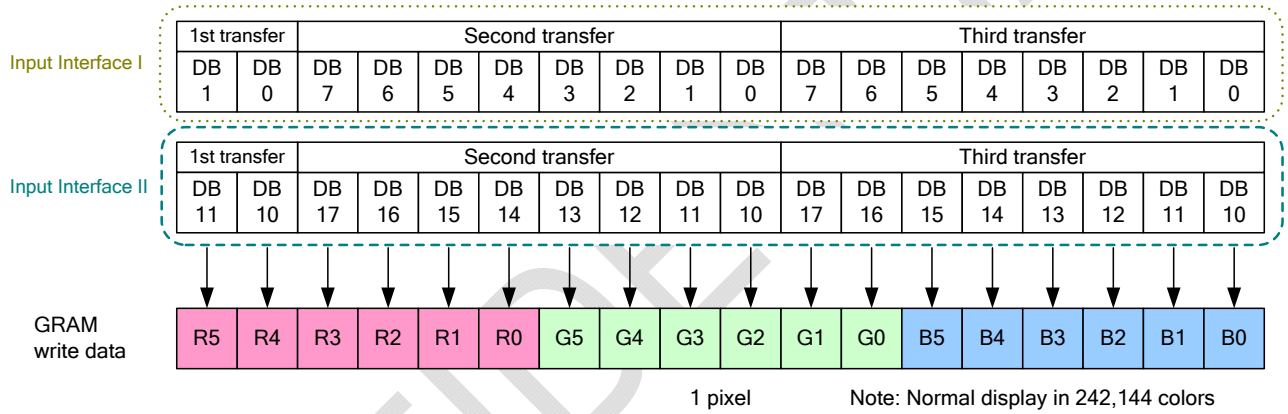


Figure 14 8-bit Interface Data Format (Instruction Write / Device Code Read)

RAM data write (2-transfer mode: TRIREG = 0)



RAM data write (3-transfer mode: TRIREG = 1, DFM = 0)



RAM data write (3-transfer mode: TRIREG = 1, DFM = 1)

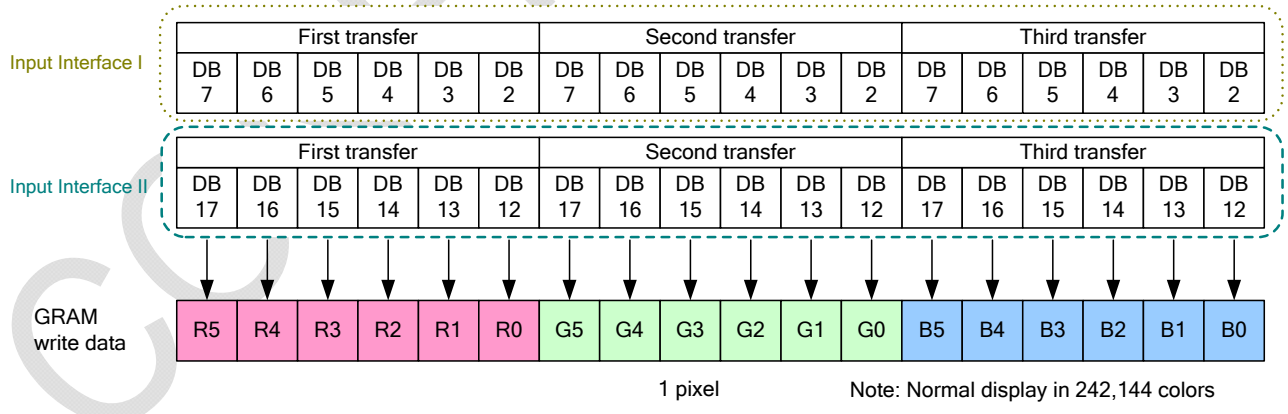


Figure 15 8-bit Interface Data Format (RAM Data Write)

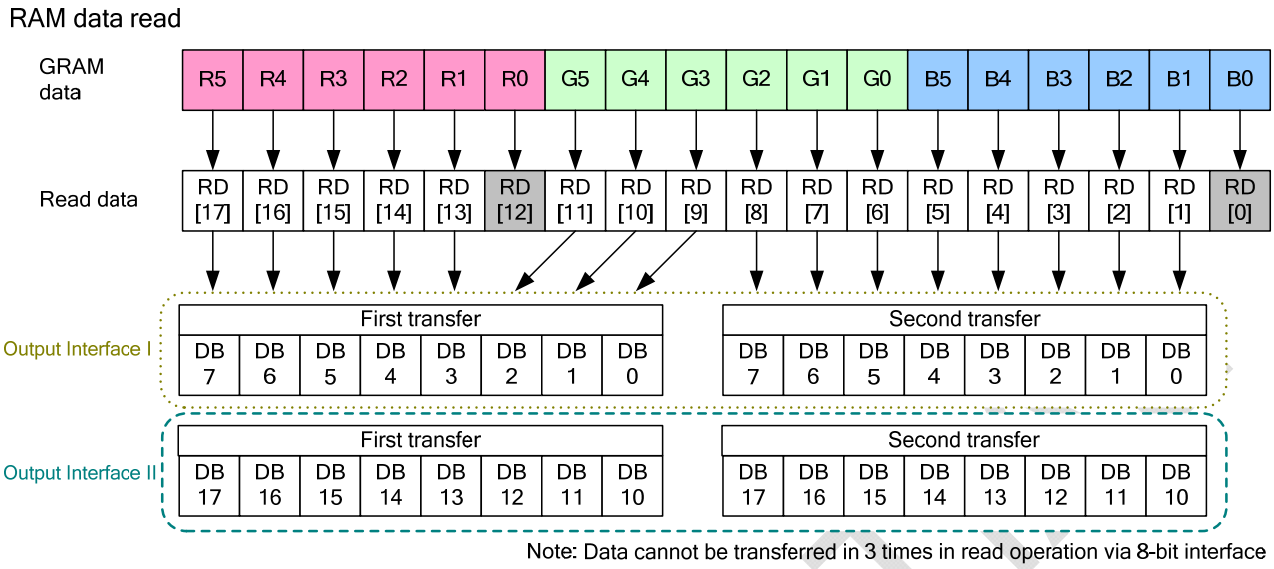


Figure 16 8-bit Interface Data Format (RAM Data Read)

12.5 Serial Interface

The serial interface is selected by setting the IM3/2/1 pins to the GND/VDDI/GND levels, respectively. The data is transferred via chip select line (nCS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either VDDI or GND level.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by RM68090.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, RM68090 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the RM68090 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Table 15 Start Byte Format

Transferred Bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: The ID bit is determined by setting the IM0/ID pin.

Table 16 Functions of RS, R/W bits

RS	R/W	Function
0	0	Set index register
0	1	Read a status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

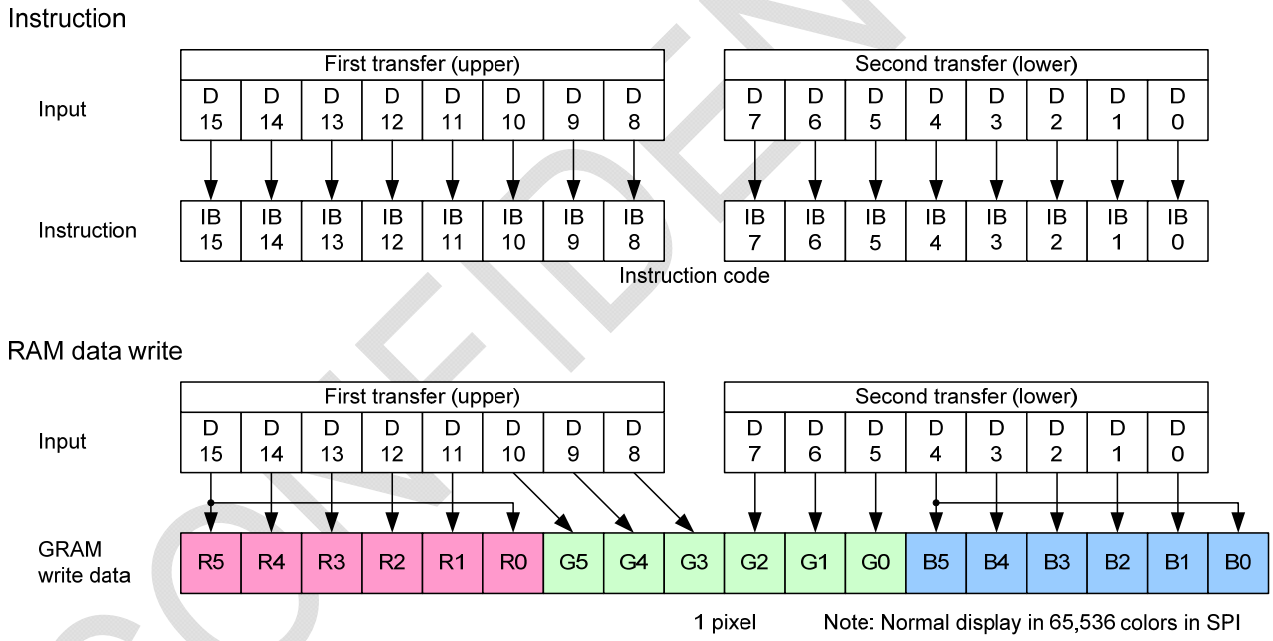
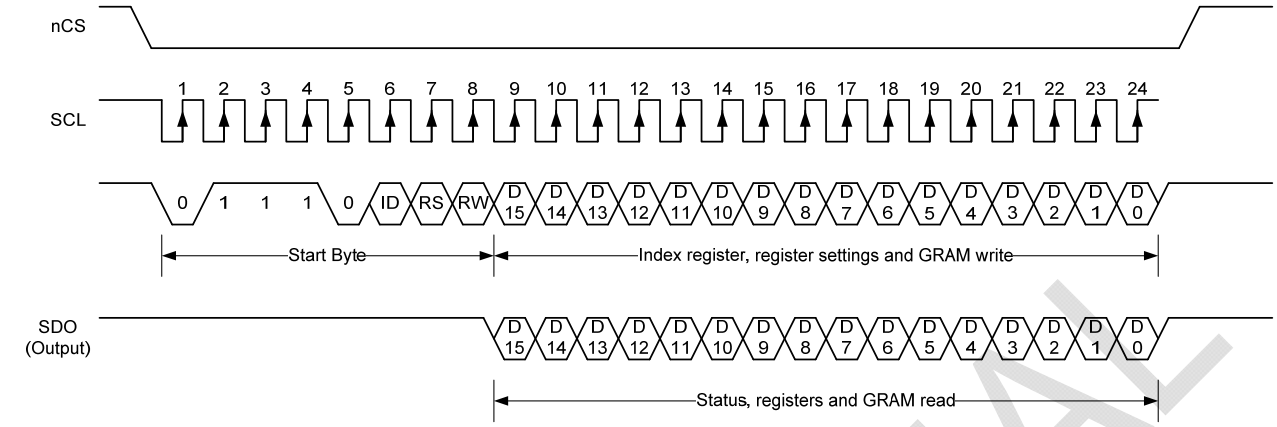
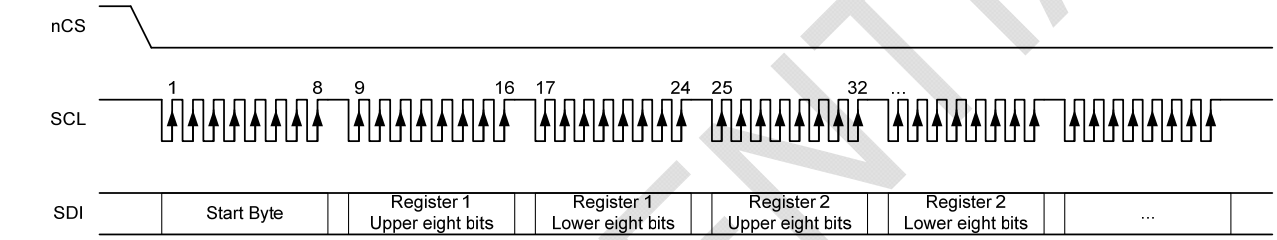


Figure 17 Serial Interface Data Format

(a) Basic data transmission through SPI

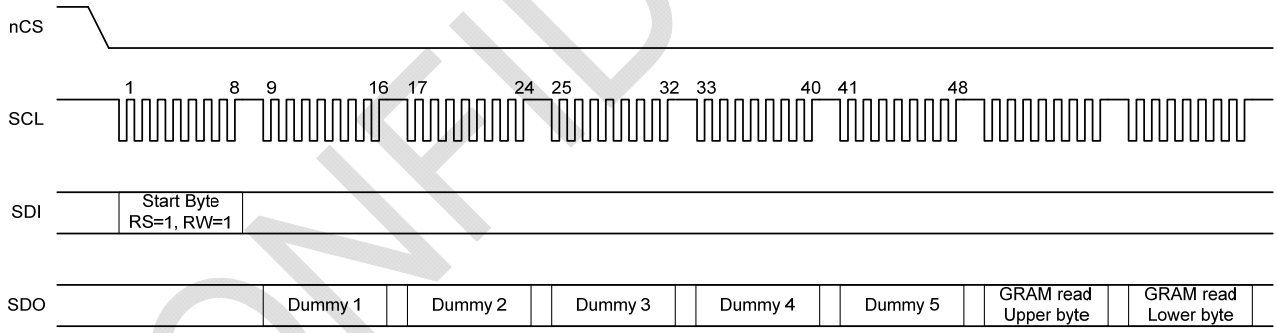


(b) Consecutive transmission through SPI



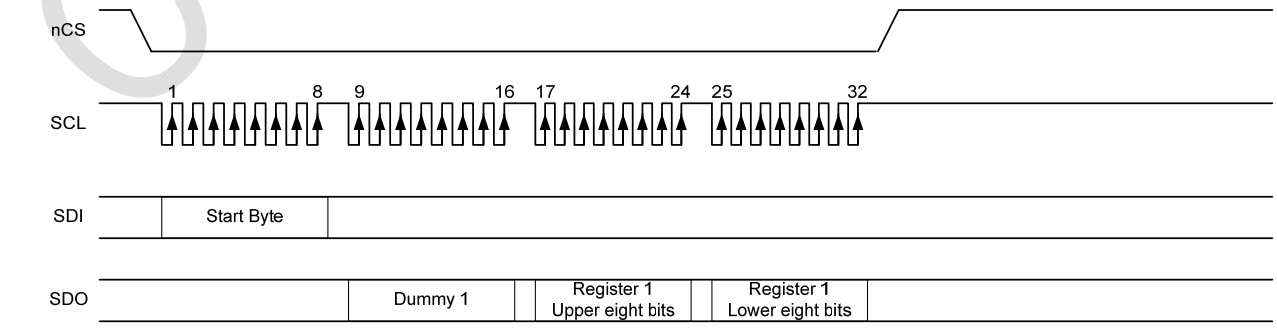
Note: The first byte after Start Byte must be the upper eight bits

(c) GRAM data read transmission (TRI="0")



Note: Five bytes of dummy data are right after the Start Byte

(d) Status/register read transmission



Note: One byte of dummy data is right after the Start Byte

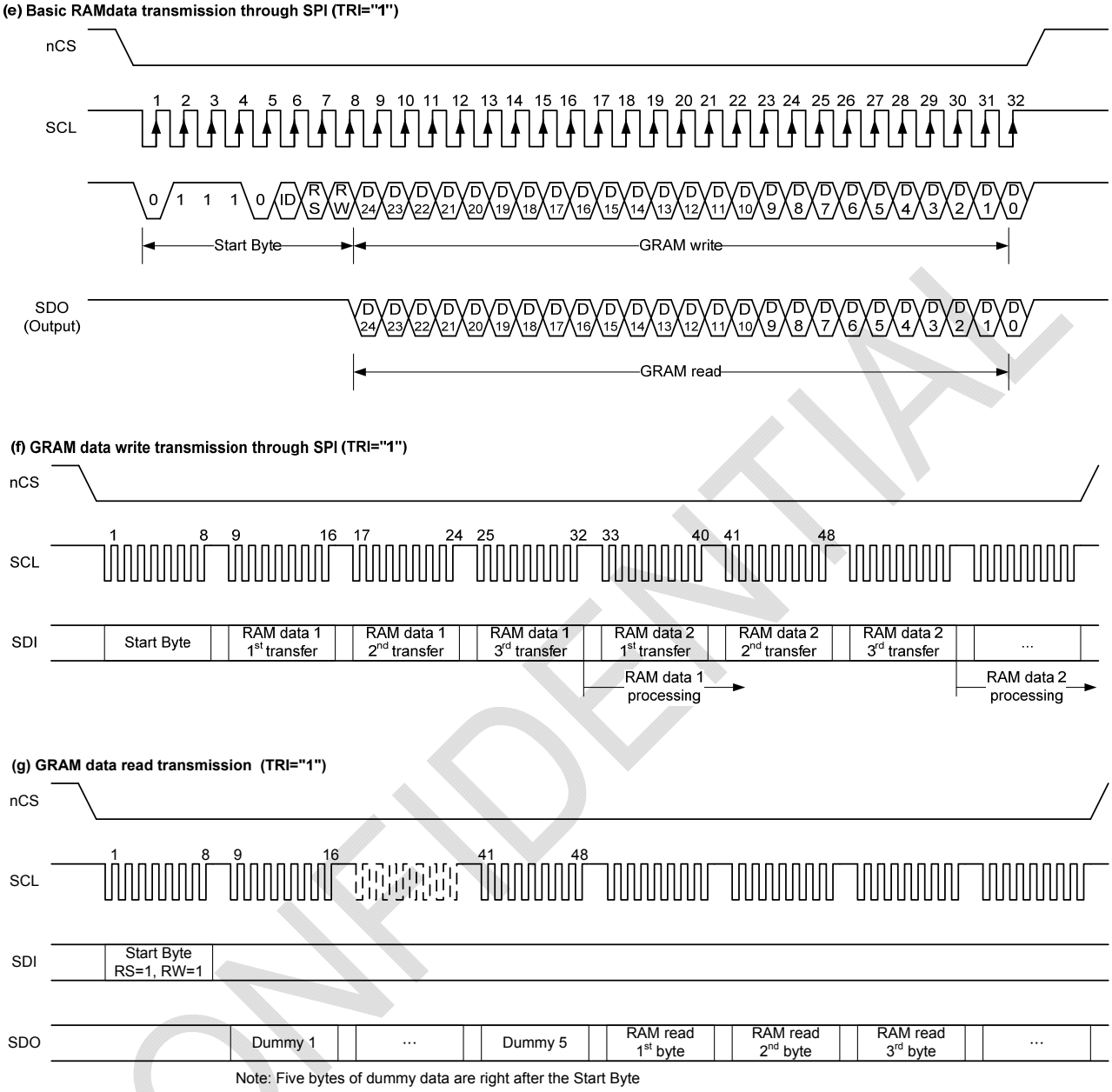


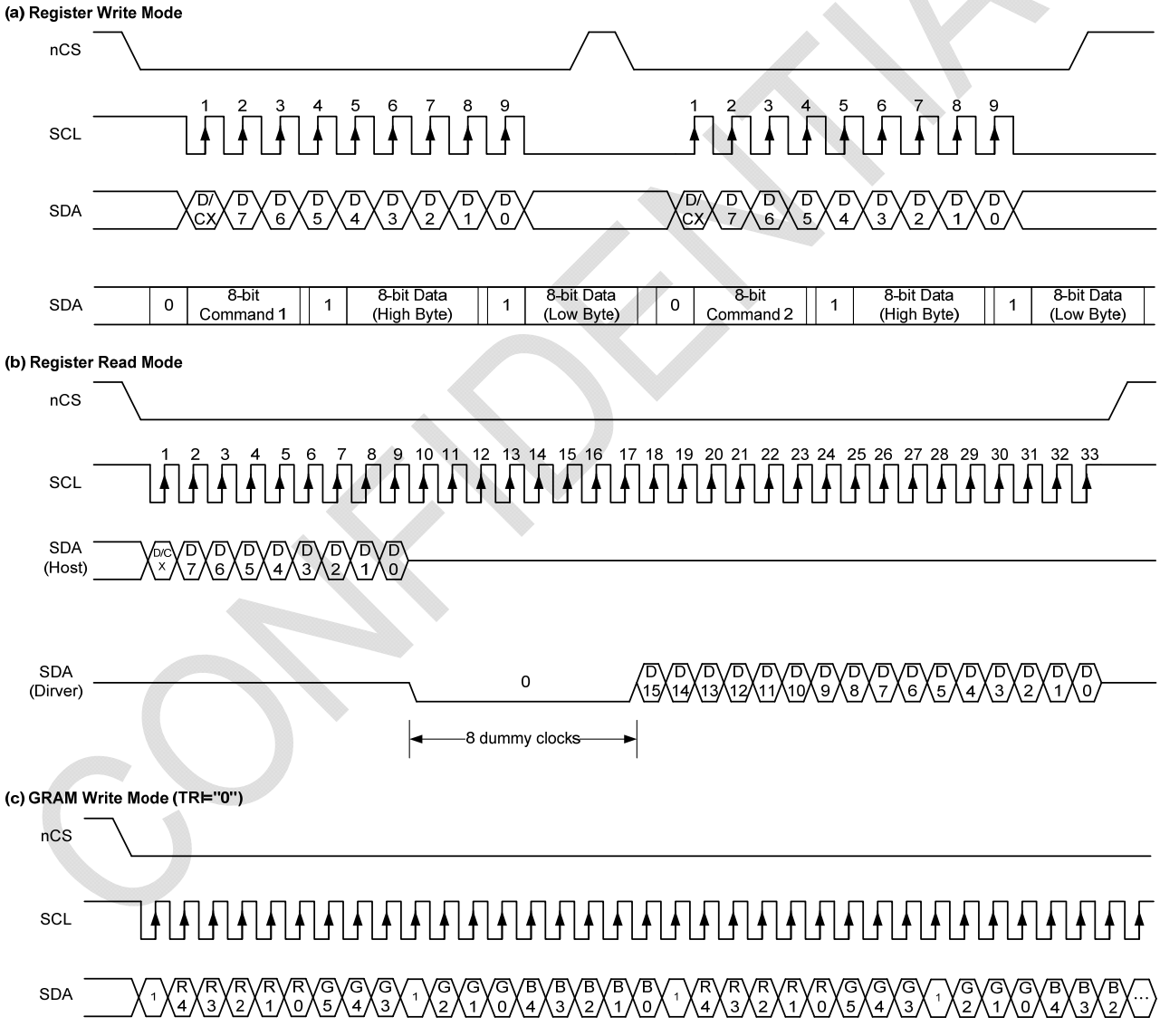
Figure 18 Data Transfer in Serial Interface

12.6 3-wire 9-bit data Serial Interface

This SPI mode uses a 3-wire 9-bit serial interface. The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock and SDA is serial data.

Serial data must be input to SDA in the sequence D/CX, D7 to D0. The RM68090 catches the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. D/CX = "1" indicates that D7 to D0 bits are display RAM data or command parameters. D/CX = "0" indicates that D7 to D0 bits are commands.

When users need to read back the register or GRAM data, the register R66h must be set to “1” first, and then write the register index to read back the register or GRAM data.



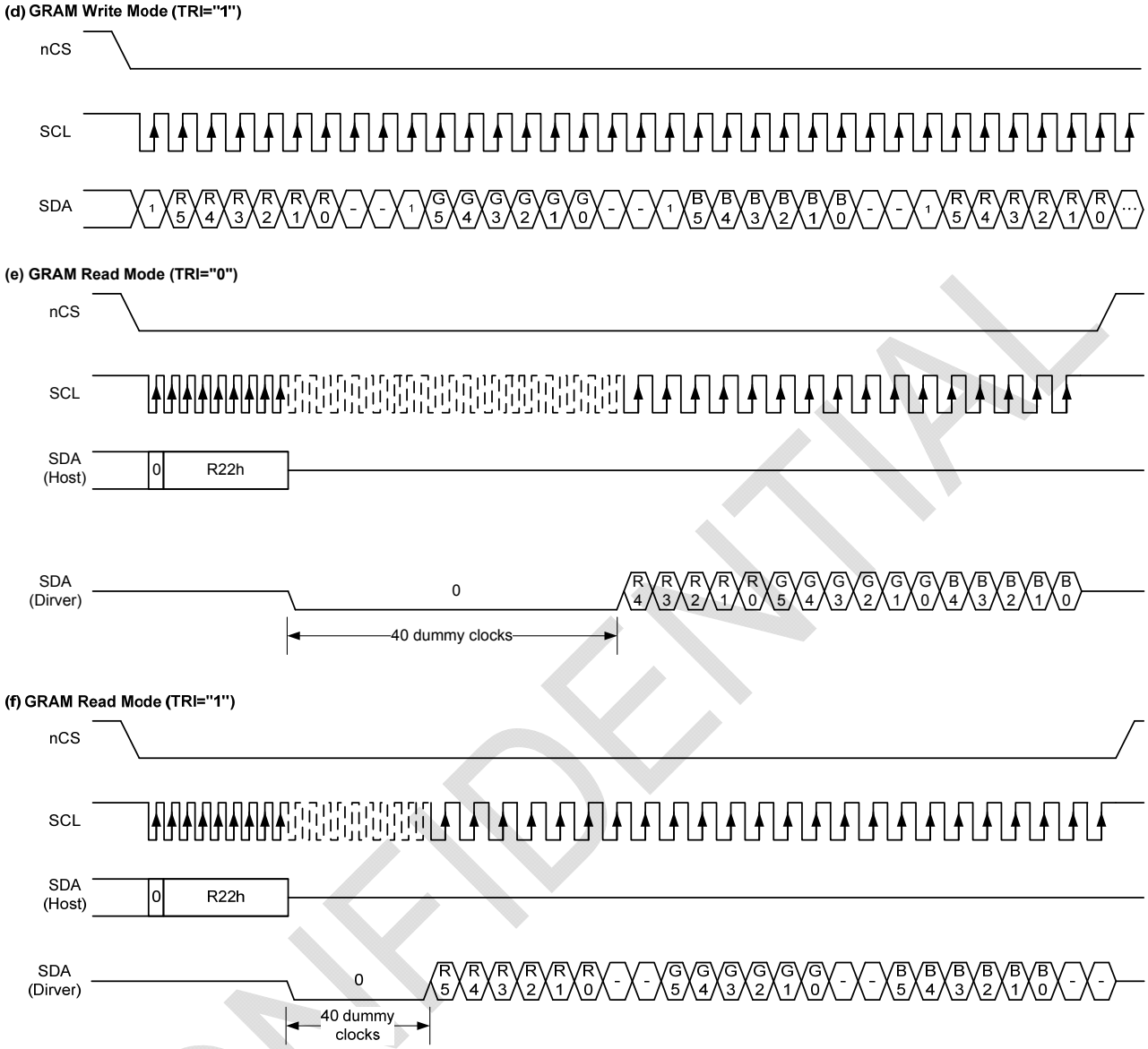
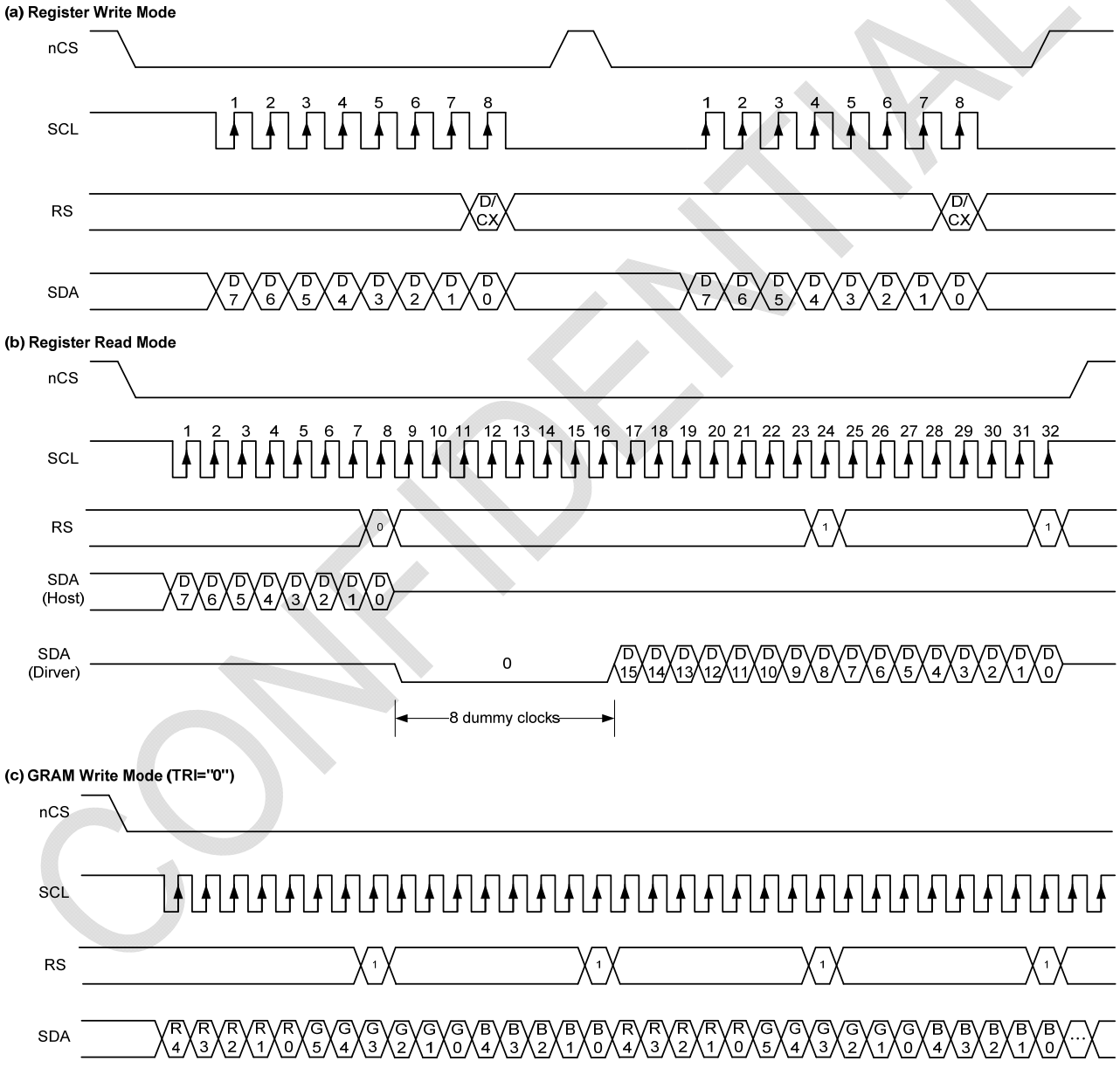


Figure 19 Data Transfer in 3-wire Serial Interface

12.7 4-wire 8-bit data Serial Interface

This SPI mode uses a 4-wire 8-bit serial interface. The chip-select nCS (active low) enables and disables the serial interface. D/CX (input through RS pin) is the command or data select signal, SCL is the serial data clock and SDA is serial data.

Serial data must be input to SDA in the sequence D7 to D0. The RM68090 catches the data at the rising edge of SCL signal. The D/CX signal indicates data/command. D/CX = "1" indicates that D7 to D0 bits are display RAM data or command parameters. D/CX = "0" indicates that D7 to D0 bits are commands.



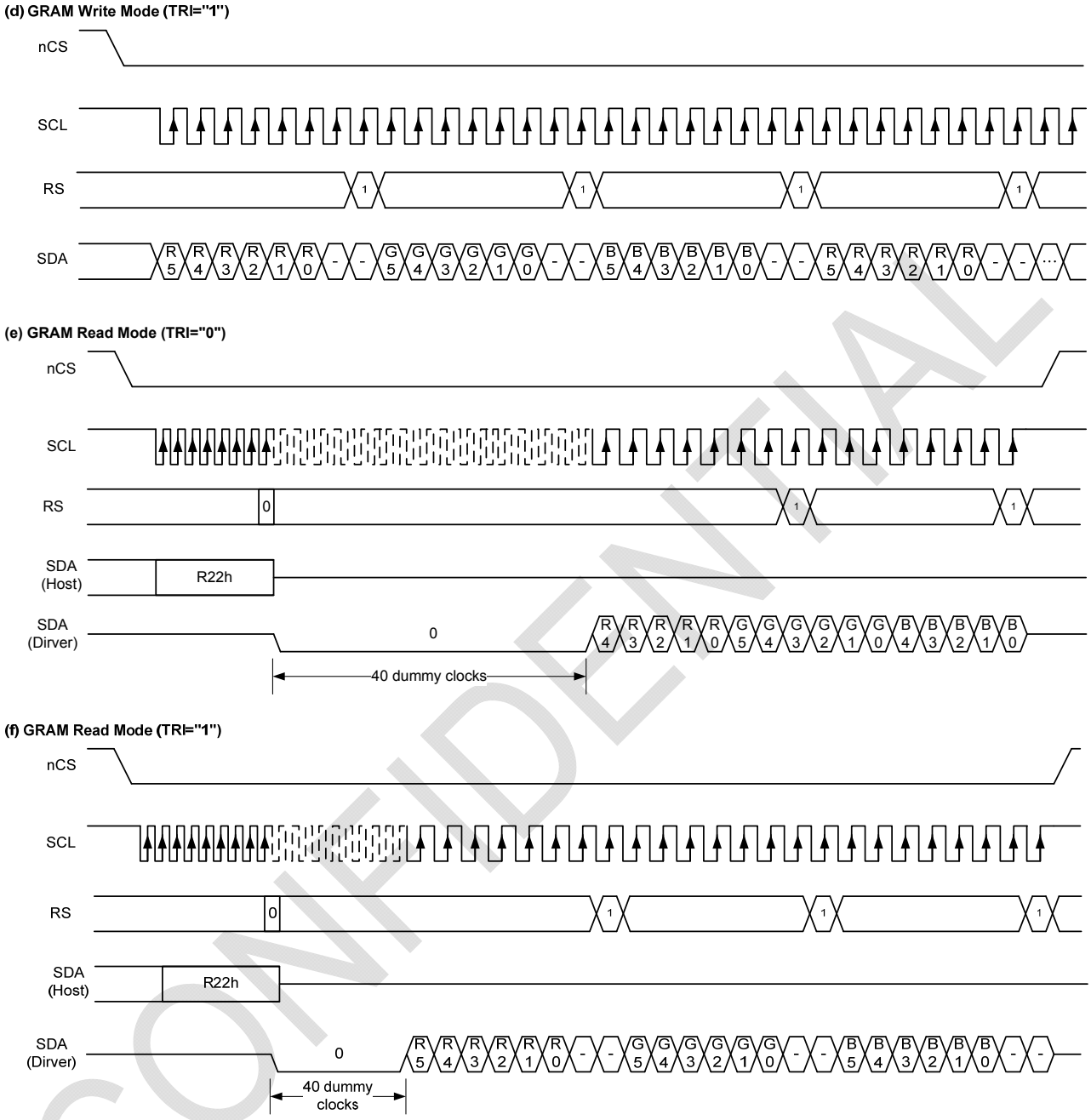


Figure 20 Data Transfer in 4-wire Serial Interface

13. VSYNC Interface

RM68090 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.

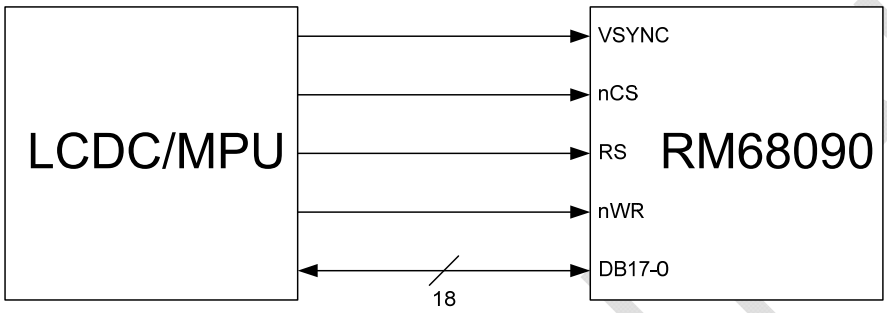


Figure 21 VSYNC Interface connection

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

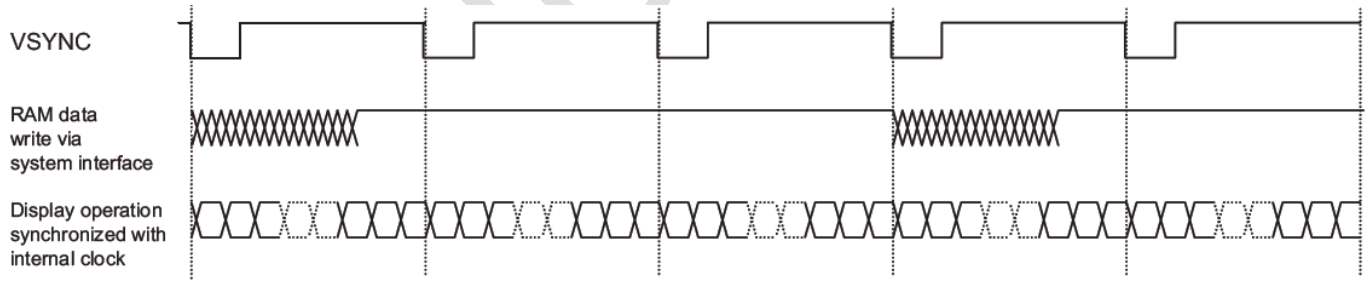


Figure 22 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$\text{Internal clock frequency (fosc)[Hz]} = \text{FrameRate} \times (\text{DisplayLines(NL)} + \text{FrontPorch(FP)} + \text{BackPorch(BP)}) \times \text{ClocksPerLine(RTN)} \times \text{variance}$$

$$\text{RAM Write Speed(min.)[Hz]} > \frac{240 \times \text{DisplayLines(NL)}}{(\text{FrintPorch(FP)} + \text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times 16(\text{clocks}) \times \frac{1}{\text{fosc}}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Panel Size	240 RGB x 320 lines (NL = 6'h27: 320 lines)
Total number of lines (NL)	320 lines
Black/front porch	14/2 lines (BP = 8'h0E, FP = 8'h02)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]

= 60 Hz x (320 + 2 + 14) lines x 16 clocks x 1.1 / 0.9 = 394 kHz

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz]

> 240 x 320 / {((14 + 320 - 2) lines x 16 clocks) x 1/394 kHz} = 5.7 MHz

The above theoretical value is calculated based on the premise that the RM68090 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the RM68090 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes:

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC

interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display and vertical scroll functions are not available in VSYNC interface mode and set the AM bit to “0” to transfer display data.

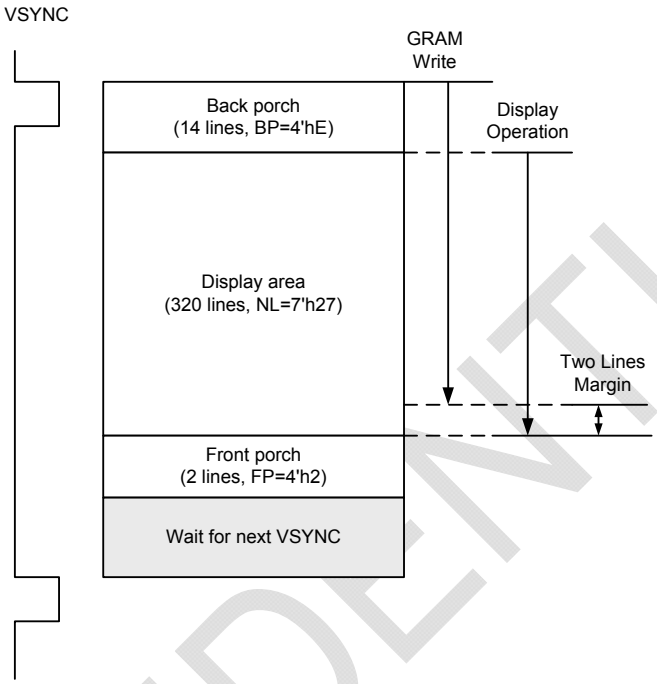


Figure 23 RAM Write Speed Margins

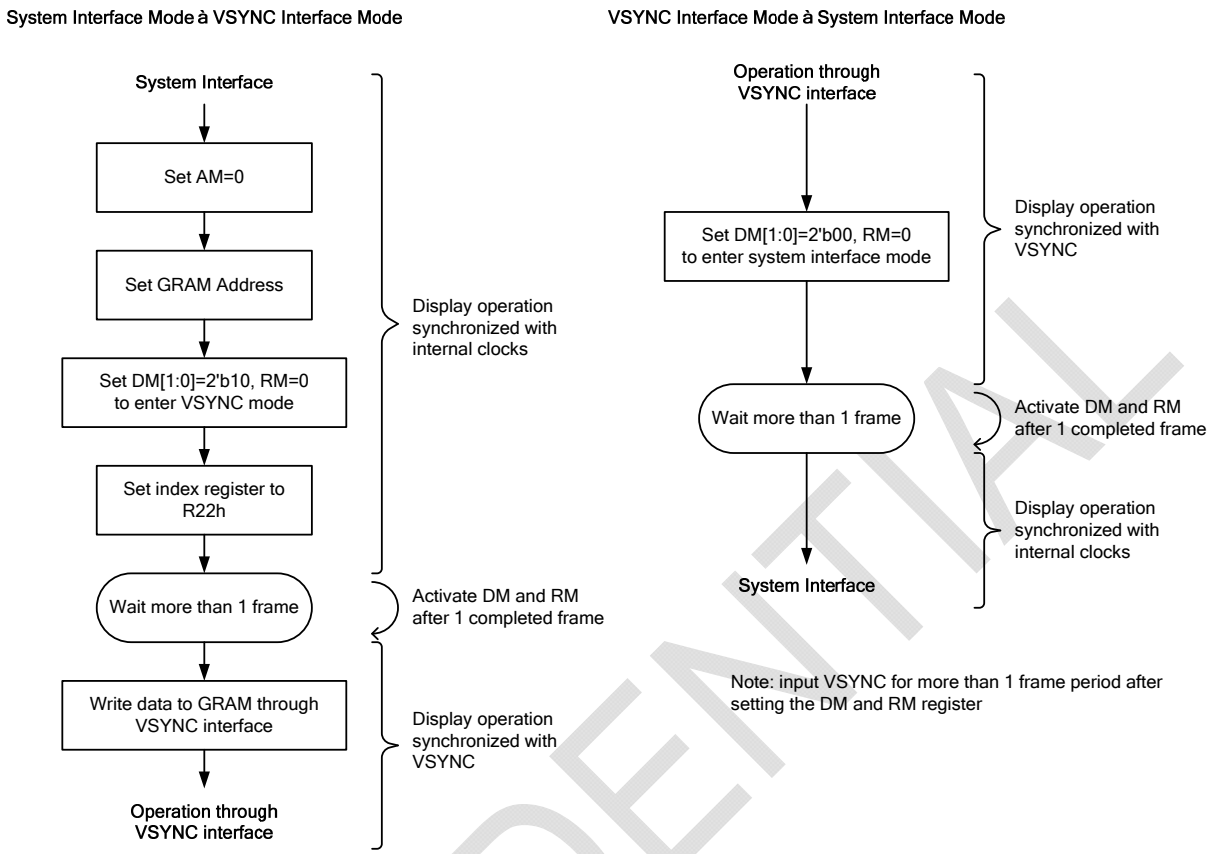


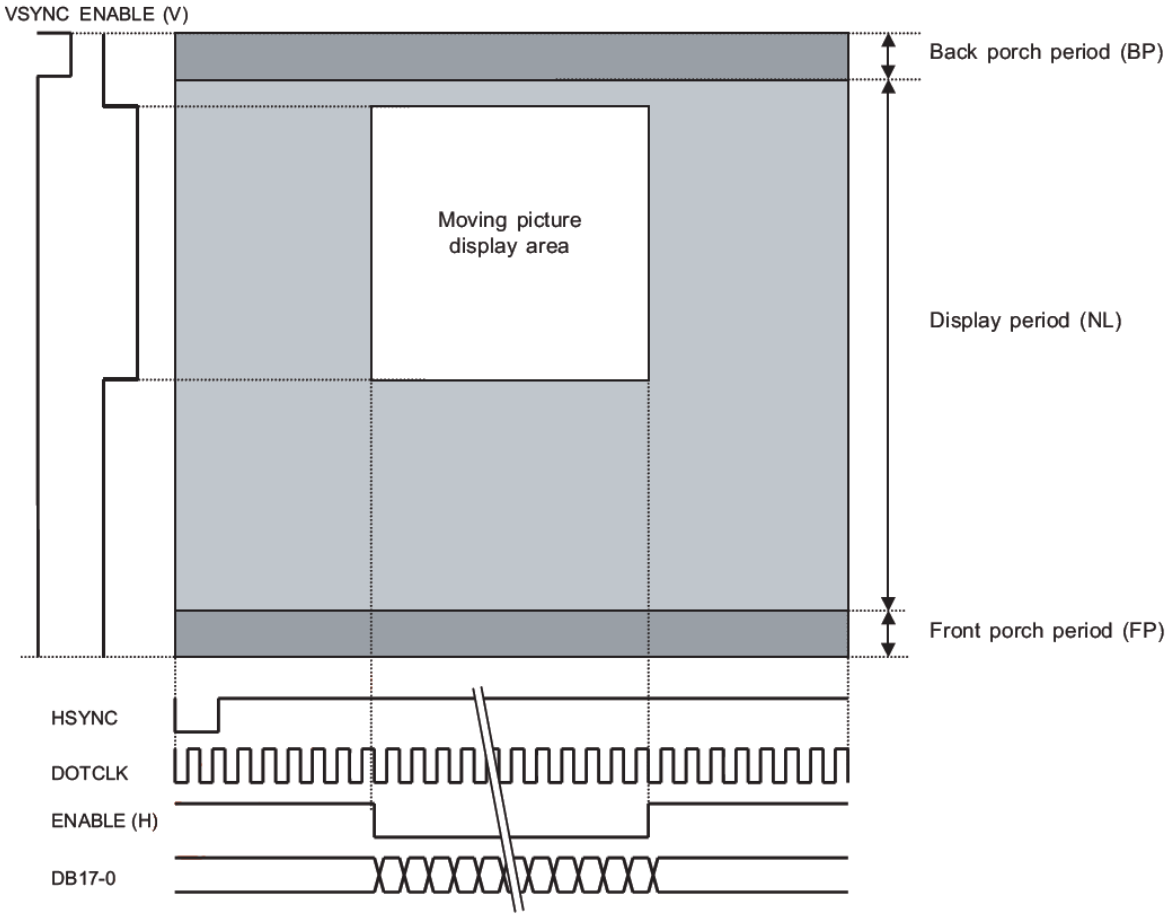
Figure 24 Sequences to Switch between VSYNC and Internal Clock Operation Modes

14. RGB Interface

The RM68090 supports the RGB interface. The interface format is set by RIM[1:0] bits. The internal RAM is accessible via RGB interface.

Table 17 RGB interface

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, DB11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting inhibited	-



Notes: 1. The front porch period continues until next VSYNC input is detected.
2. Make sure to match the VSYNC, HSYNC, and DOTCLK frequencies to the resolution of liquid crystal panel.

Figure 25 Display Operation via RGB Interface

14.1 RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

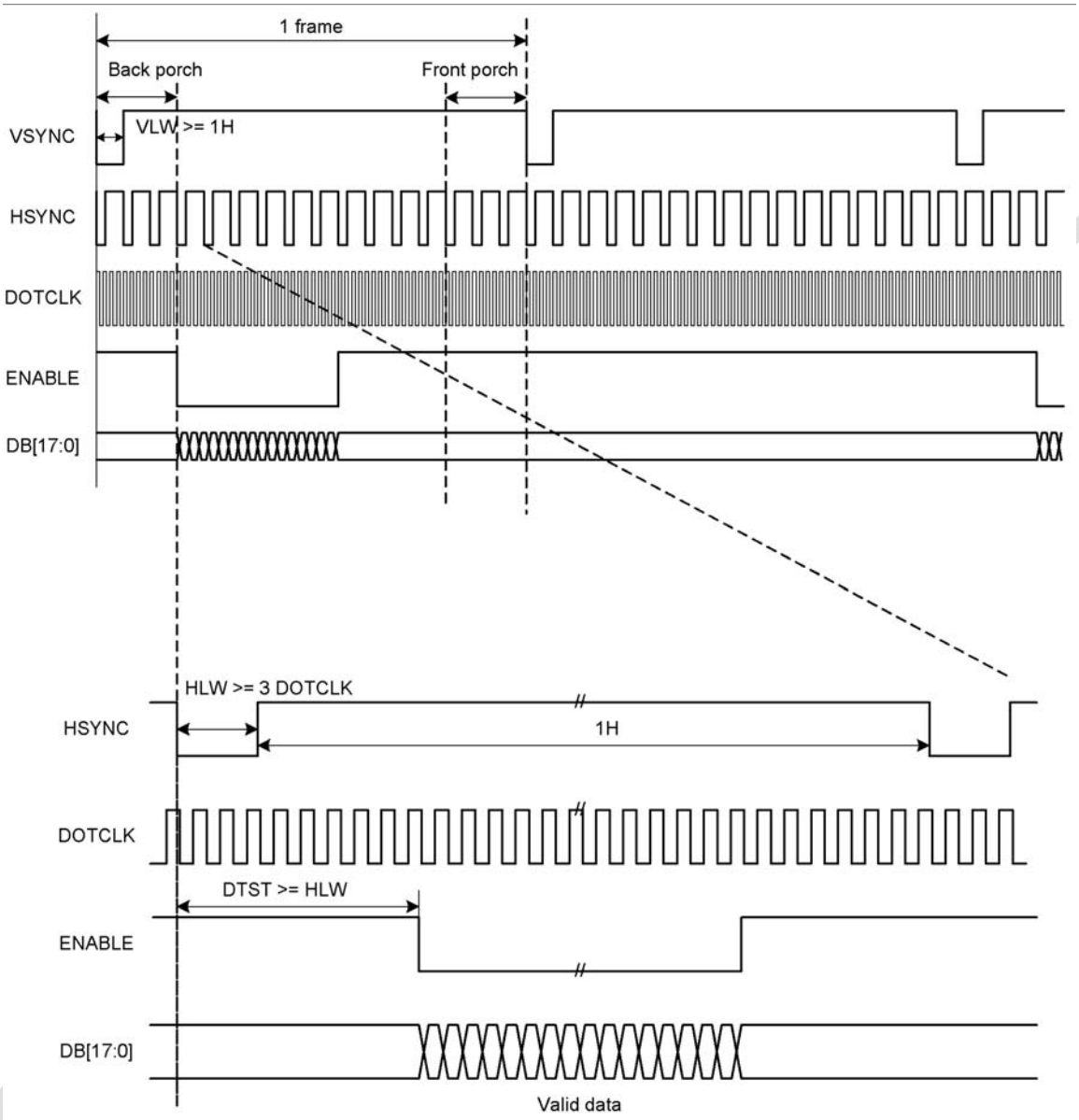


Figure 26 16-/18-bit RGB Interface Timing

Notes:

1. VLW: VSYNC Low period,
2. HLW: HSYNC Low period,
3. DTST: data transfer setup time

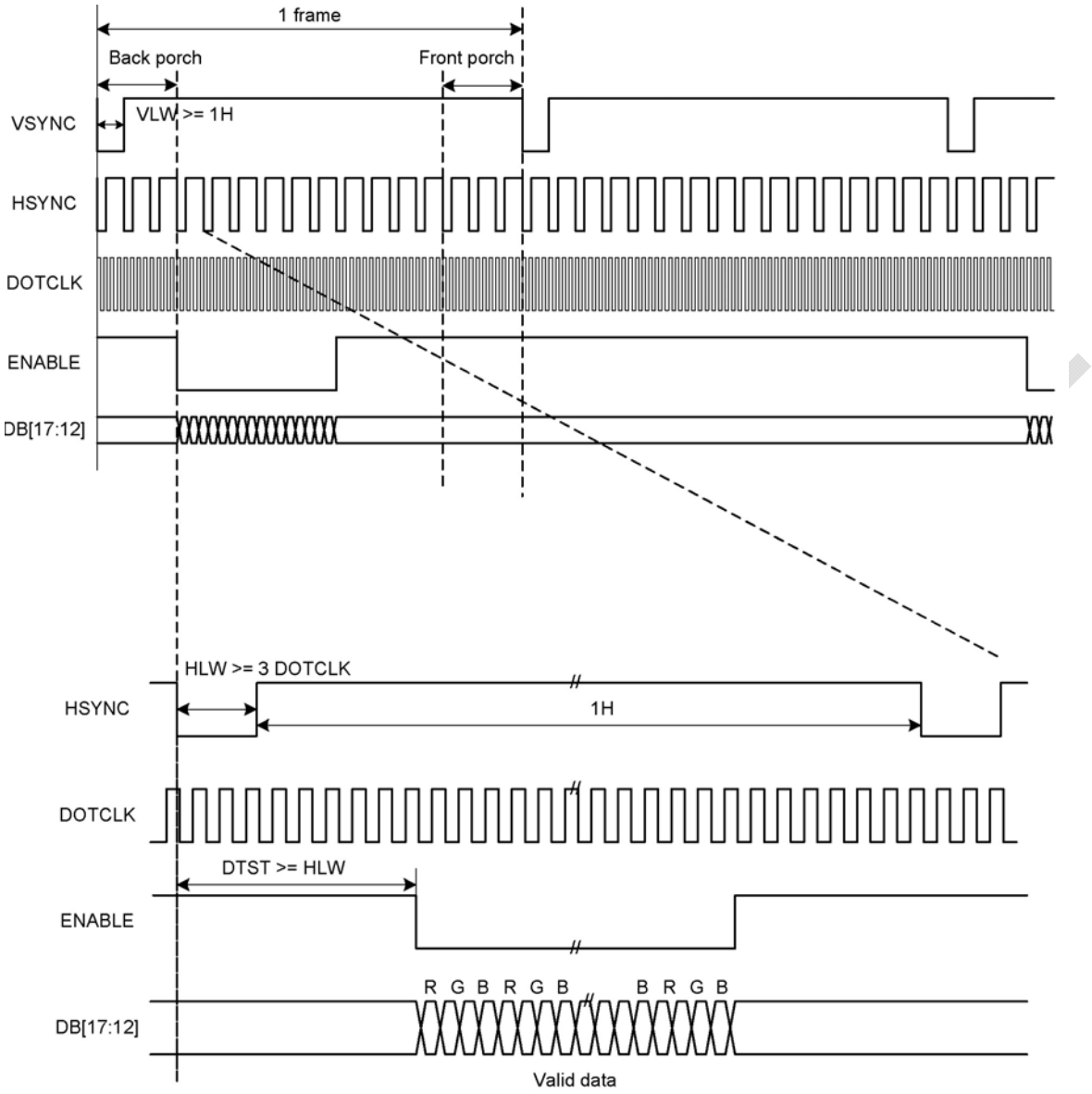


Figure 27 6-bit RGB Interface Timing

Notes:

1. VLW: VSYNC Low period,
2. HLW: HSYNC Low period,
3. DTST: data transfer setup time
4. In 6-bit RGB interface operation, set the VSYNC, HSYNC, ENABLE, DOTCLK cycles so that one pixel is transferred in units of three DOTCLKs via DB17-12.

14.2 Moving Pictures Mode

RM68090 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following advantages in displaying a moving picture.

• The window address function defined the update area of GRAM.

• Only the moving picture area of GRAM is updated.

• When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

14.3 RAM access via system interface in RGB interface operation

RM68090 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = “0”) and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = “1” and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the RM68090 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

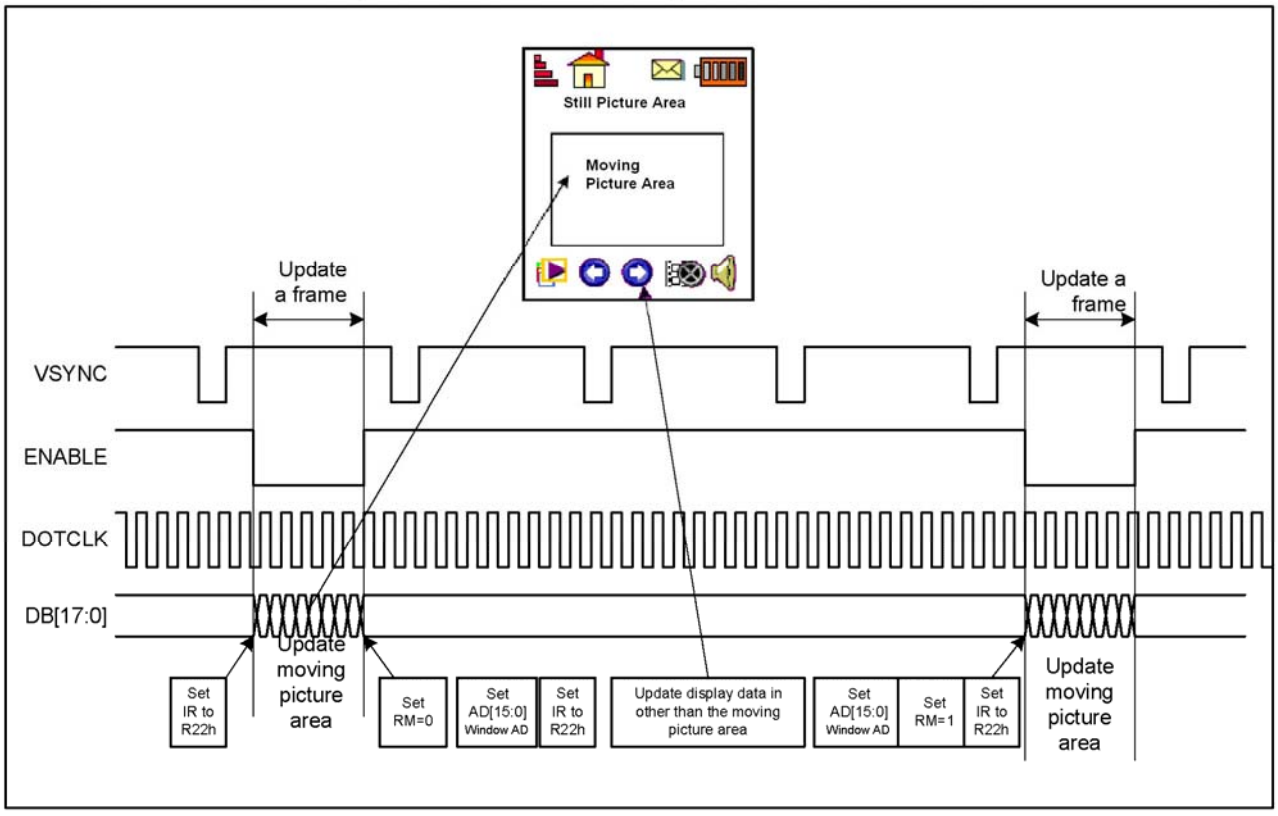


Figure 28 Updating the Still Picture Area while Displaying Moving Picture

14.4 6-bit RGB interface

The 6-bit RGB interface is selected by setting RIM[1:0] = 2'b10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit port while data enable signal (ENABLE) allows RAM access via RGB interface. Unused pins DB11-0 (DB17-6) must be fixed at either VDDI or GND level.

Instruction bits can be transferred only via system interface.

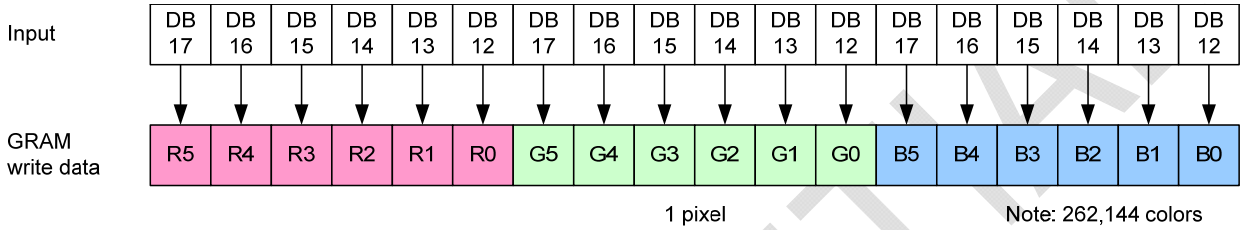


Figure 29 Example of 6-bit RGB Interface and Data Format

14.5 Data Transfer Synchronization in 6-bit Bus Interface Operation

The RM68090 has counters, which indicate the first, second, and third 6-bit transfer via 6-bit RBG interface. The counters are reset on the falling edge of VSYNC so that the data transfer will start from the first 6 bits of 18-bit RGB data from the next frame period. Accordingly, the data transfer via 6-bit interface can restart in correct order from the next frame period even if a mismatch occurs in transferring 6-bit data. This function can minimizes the effect from data transfer mismatch and help the display system return to normal display operation when data is transferred consecutively in moving picture operation.

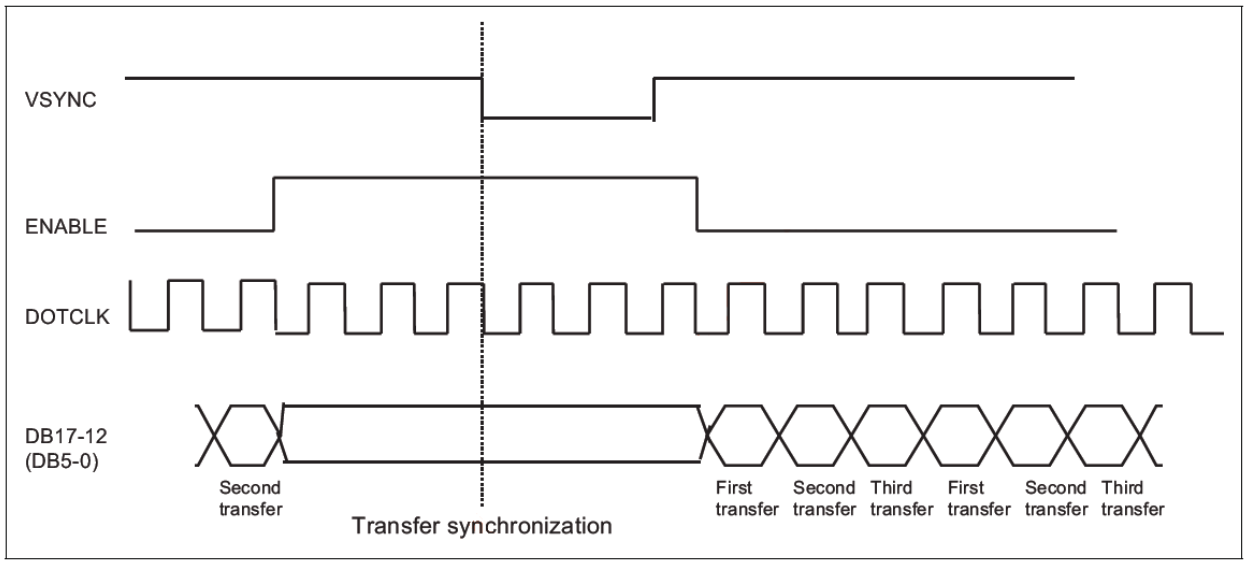


Figure 30 6-bit Transfer Synchronization

14.6 16-bit RGB interface

The 16-bit RGB interface is selected by setting RIM[1:0] = 2'b01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

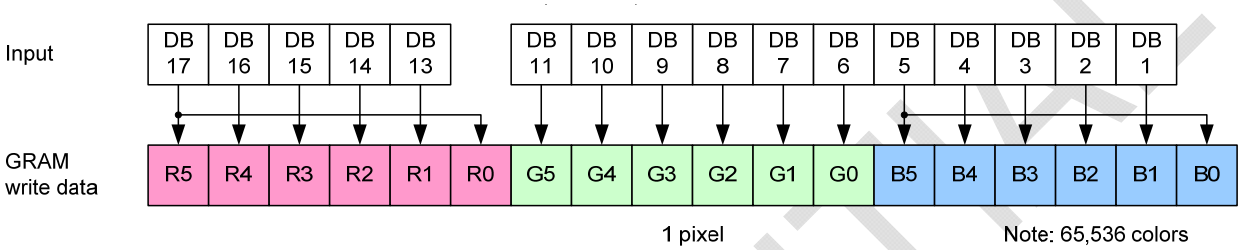


Figure 31 Example of 16-bit RGB Interface and Data Format

14.7 18-bit RGB interface

The 18-bit RGB interface is selected by setting RIM[1:0] = 2'b00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit ports (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

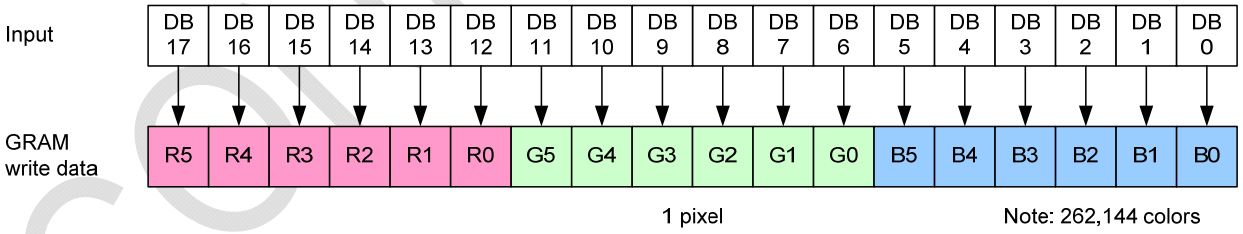


Figure 32 Example of 18-bit RGB Interface and Data Format

14.8 Notes to external display interface operation

1. The following functions are not available in external display interface operation.

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.
3. The period set with the NOWE[1:0] bits (gate output non-overlap period) is not based on the internal clock but based on DOTCLK in RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

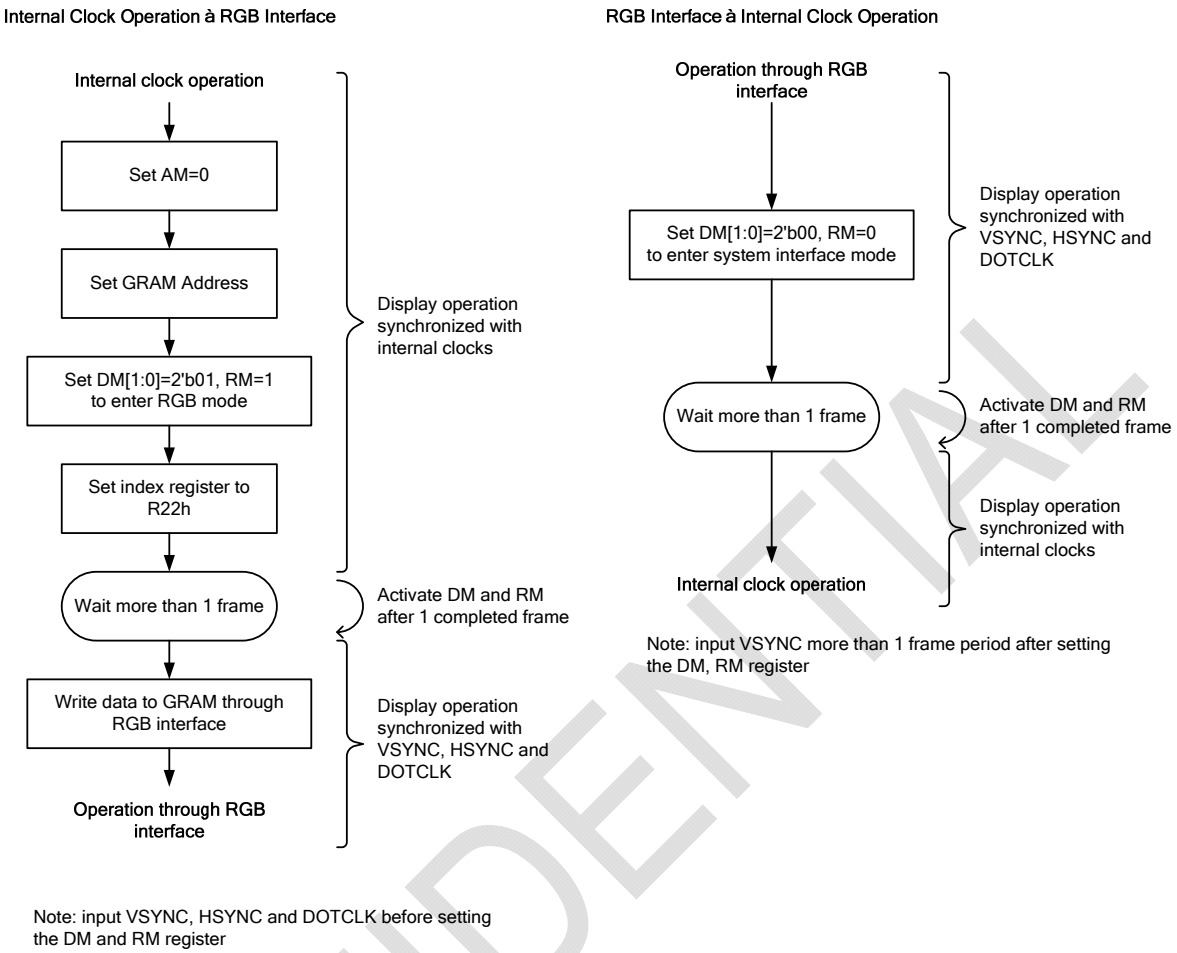


Figure 33 RGB and Internal Clock Operation Mode Switching Sequences

15. Resizing Function

RM68090 supports resizing function (x1/2, x1/4), which is performed when writing image data to GRAM. The resizing function is enabled by setting a window address area and the RSZ bit which represents the resizing factor (x1/2, x1/4) of image. The resizing function allows the system to transfer the original-size image data into the GRAM with resized image data.

Original image data

	0	1	2	3	4	5	6	7
0	(0, 0)	(0, 1)	(0, 2)	(0, 3)	(0, 4)	(0, 5)	(0, 6)	(0, 7)
1	(1, 0)	(1, 1)	(1, 2)	(1, 3)	(1, 4)	(1, 5)	(1, 6)	(1, 7)
2	(2, 0)	(2, 1)	(2, 2)	(2, 3)	(2, 4)	(2, 5)	(2, 6)	(2, 7)
3	(3, 0)	(3, 1)	(3, 2)	(3, 3)	(3, 4)	(3, 5)	(3, 6)	(3, 7)
4	(4, 0)	(4, 1)	(4, 2)	(4, 3)	(4, 4)	(4, 5)	(4, 6)	(4, 7)
5	(5, 0)	(5, 1)	(5, 2)	(5, 3)	(5, 4)	(5, 5)	(5, 6)	(5, 7)
6	(6, 0)	(6, 1)	(6, 2)	(6, 3)	(6, 4)	(6, 5)	(6, 6)	(6, 7)
7	(7, 0)	(7, 1)	(7, 2)	(7, 3)	(7, 4)	(7, 5)	(7, 6)	(7, 7)

½ resizing

RAM data

	0	1	2	3
0	(0, 0)	(0, 2)	(0, 4)	(0, 6)
1	(2, 0)	(2, 2)	(2, 4)	(2, 6)
2	(4, 0)	(4, 2)	(4, 4)	(4, 6)
3	(6, 0)	(6, 2)	(6, 4)	(6, 6)

Figure 34 Data transfer in resizing

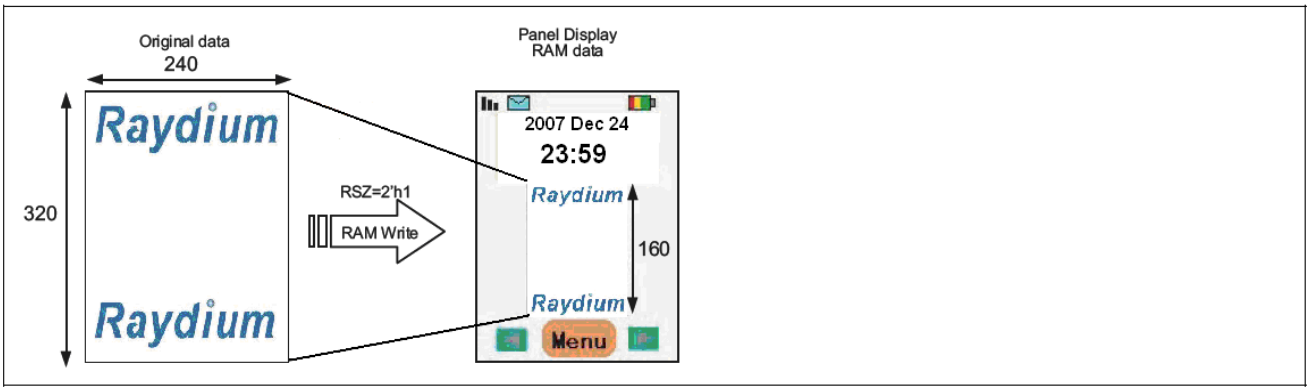
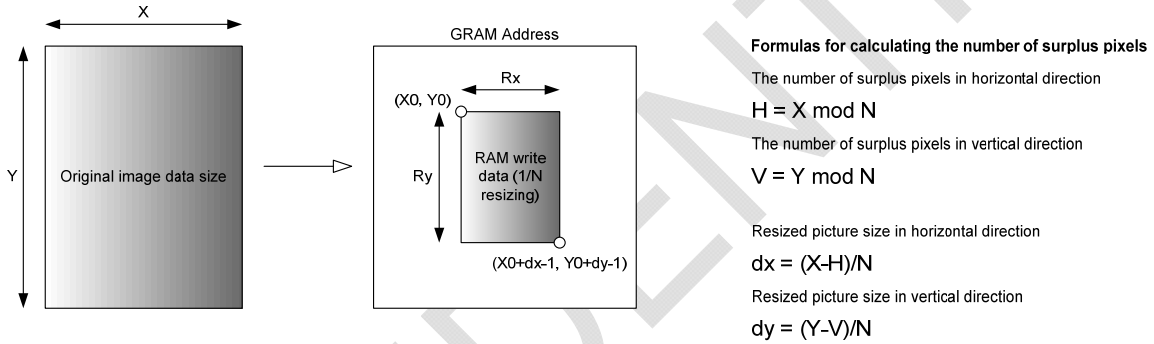


Figure 35 Data transfer, display example in resizing

Table 18

Original image size (X x Y)	Resized image size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
640x480 (VGA)	320x240	160x120
352x288 (CIF)	176x144	88x72
320x240 (QVGA)	160x320	80x60
176x144 (QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44



Original image data number in horizontal direction		X
Original image data number in Vertical direction		Y
Resizing Ration		1/N
Resizing Setting	RSZ	N-1
Remainder pixels in horizontal direction	RCH	H
Remainder pixels in vertical direction	RCV	V
GRAM writing start address	AD	(X0,Y0)
GRAM window setting	HAS	X0
	HEA	X0+dX-1
	VSA	Y0
	VEA	Y0+dY-1

15.1 Example of 1/2 resizing

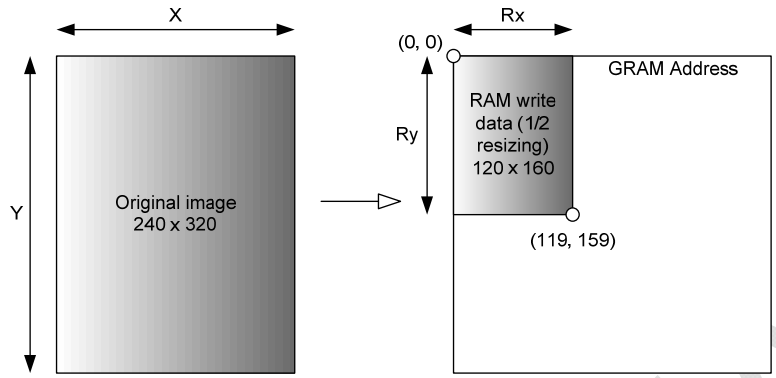


Figure 36 Resizing setting example (x 1/2)

Table 19

Image (before resizing)

Number of data in horizontal direction	X	240
Number of data in vertical direction	Y	320
Resizing ratio	1/N	1/2

Register setting

Resizing setting	RSZ	2'h1
Number of data in horizontal direction	RCV	2'h0
Number of data in vertical direction	RCH	2'h0

RAM writing start address	AD	17'h00000
RAM window address	HSA	8'h00
	HEA	8'h77
	VSA	8'h00
	VEA	8'h9F

15.2 Resizing Instruction

Table 20 Resizing factor

RSZ[1:0]	Contraction factor
2'h0	No resizing (x 1)
2'h1	1/2 resizing (x 1/2)
2'h2	Setting disabled
2'h3	1/4 resizing (x 1/4)

Table 21 Surplus pixels (Vertical direction)

RCV[1:0]	Surplus pixels
2'h0	0
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Table 22 Surplus pixels (Horizontal direction)

RCH[1:0]	Surplus pixels
2'h0	0
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

15.3 Notes to Resizing function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 (R20h, R21h) before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are surplus pixels. Otherwise (if RSZ = 2'h0), set RCH = RCV = 2'h0.

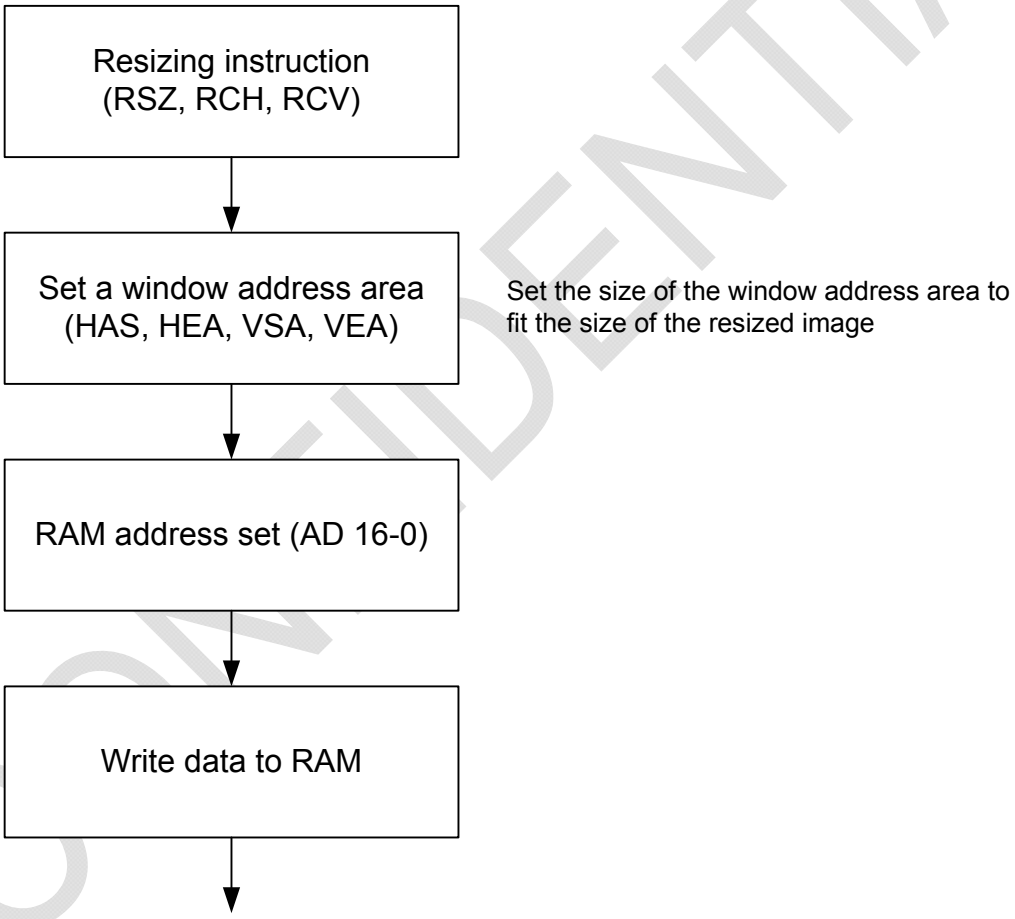


Figure 37 RAM write operation sequence in resizing

16. Partial Display Function

The RM68090 allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Partial image 1 display instruction		Partial image 2 display instruction		Other instruction	
PTDE0	1	PTDE1	1	BASEE	0
PTSA0[8:0]	9’h000	PTSA1[8:0]	9’h020	NL[5:0]	6’h27
PTEA0[8:0]	9’h00F	PTEA1[8:0]	9’h02F		
PTDP0[8:0]	9’h080	PTDP1[8:0]	9’h0C0		

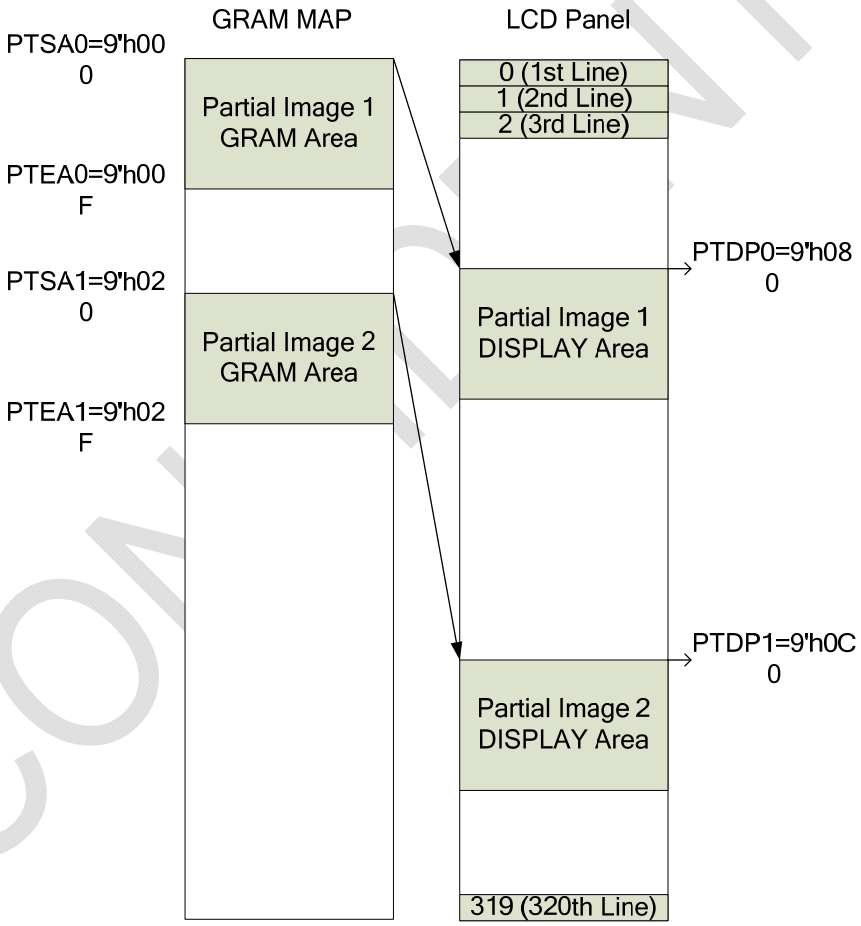


Figure 38 Partial Display example

17. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (increment or decrement, horizontal or vertical, respectively). Setting these bits enables the RM68090 to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

	Window address area setting range	**RAM address area setting range**
Horizontal direction	8'h00 ≤ HSA ≤ HEA ≤ 8'hEF	HSA ≤ AD[7:0] ≤ HEA
Vertical direction	9'h000 ≤ VSA ≤ VEA ≤ 9'h13F	VSA ≤ AD[16:8] ≤ VEA

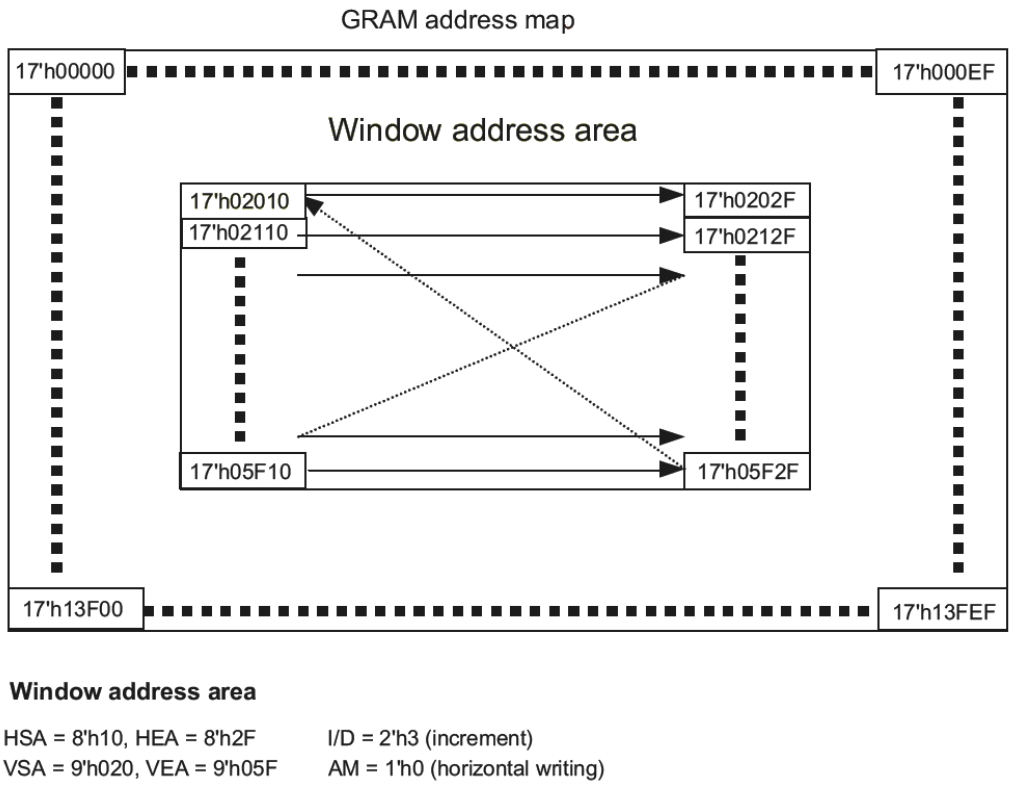


Figure 39 Automatic address update within a Window Address Area

18. γ Correction Function

The RM68090 supports γ-correction function to display in 262,144 colors simultaneously using gradient adjustment, amplitude-adjustment, and fine-adjustment registers. Each register consists of positive-polarity register and negative-polarity register to allow optimal gamma correction setting for the characteristics of the panel by enabling different settings for positive and negative polarities.

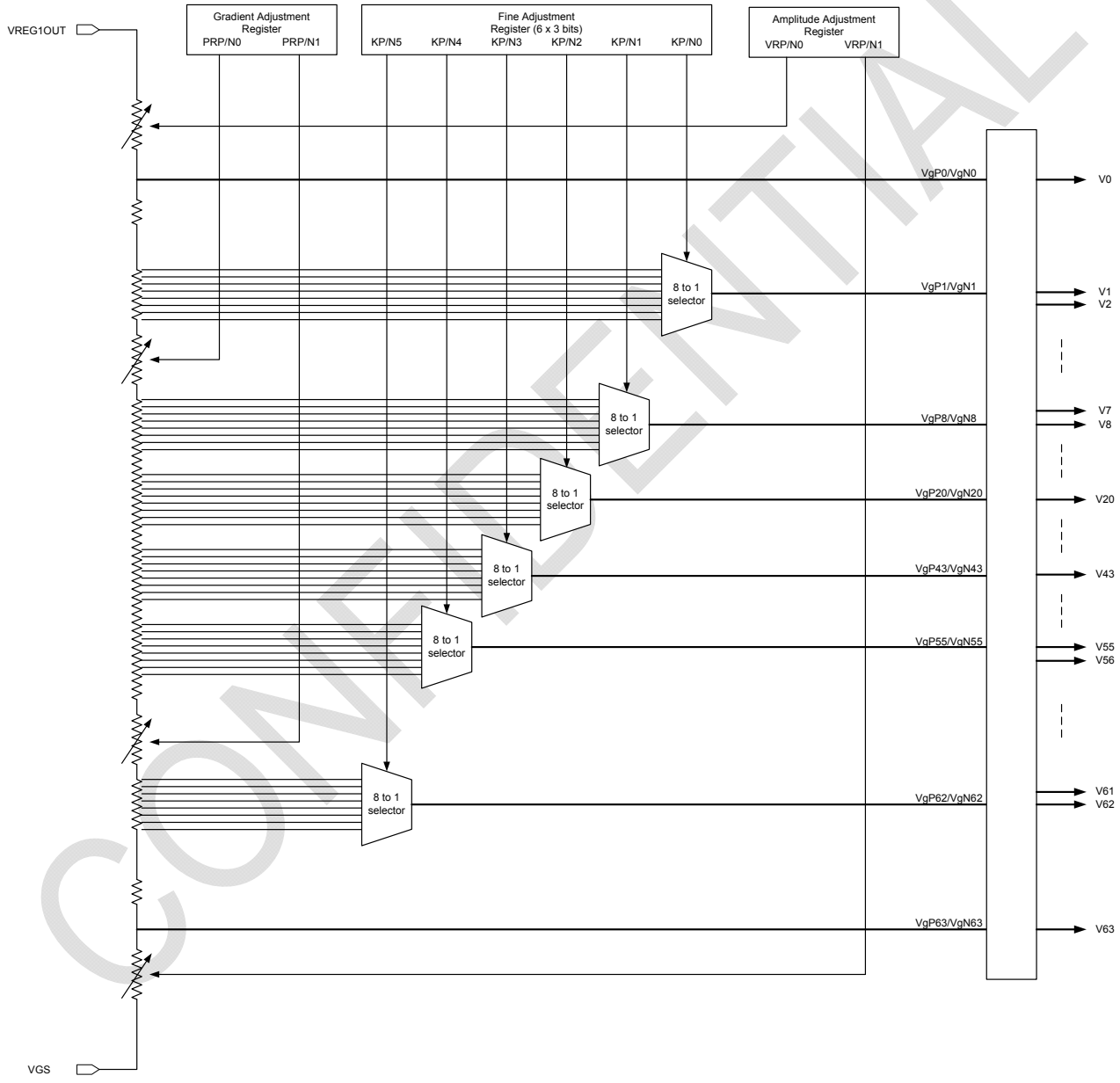


Figure 40 Structure of gamma correction function

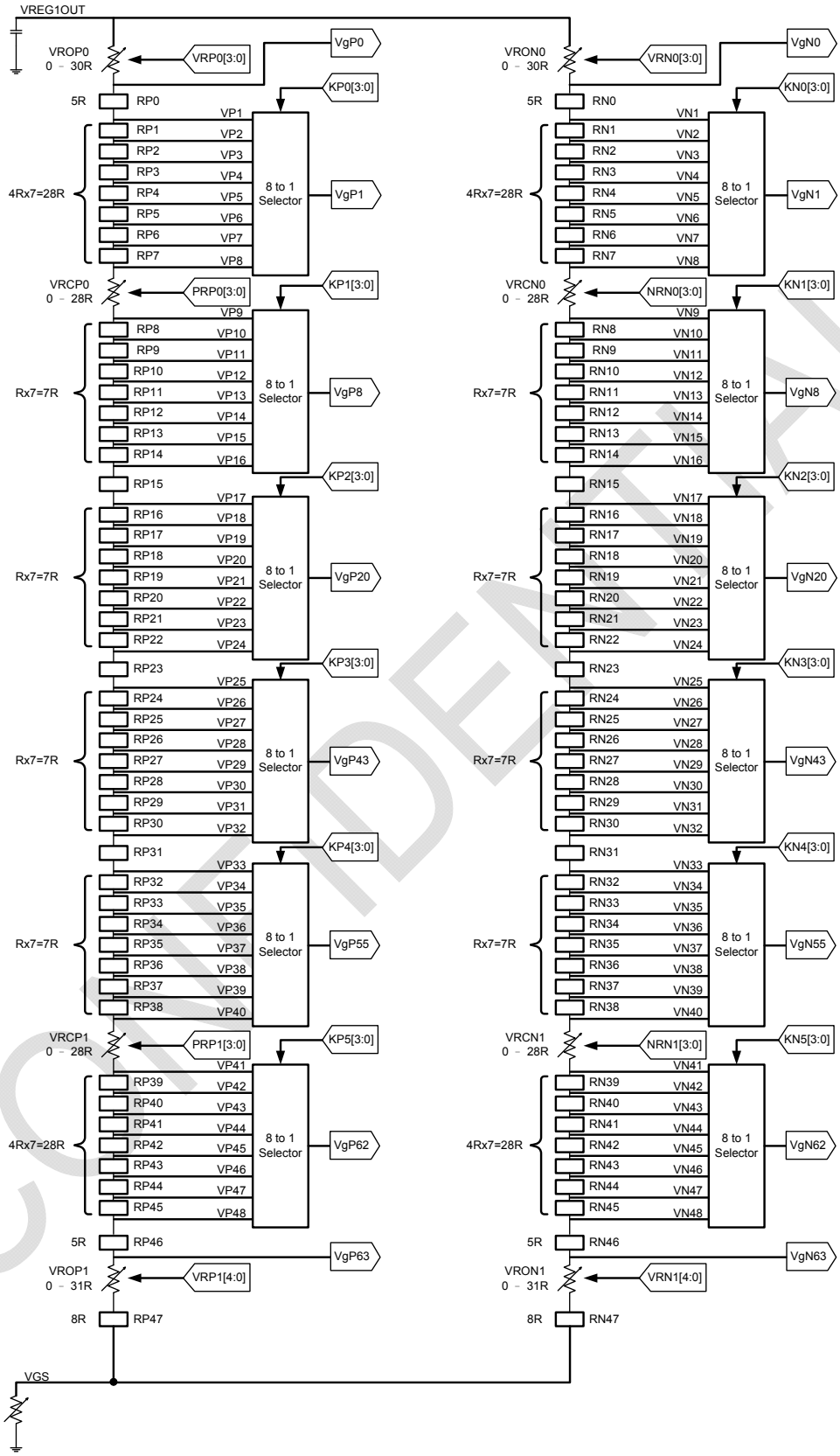


Figure 41 Grayscale Voltage Adjustment

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Register	Positive	Negative	Function
Gradient	PRP0 [2:0]	PRN1 [2:0]	Variable resistor VRCP0, VRCN0
	PRP1 [2:0]	PRN0 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude	VRP0 [4:0]	VRN1 [4:0]	Variable resistor VROP0, VRON0
	VRP1 [4:0]	VRN0 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of V1)
	KP1 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of V8)
	KP2 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of V20)
	KP3 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of V43)
	KP4 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of V55)
	KP5 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of V62)

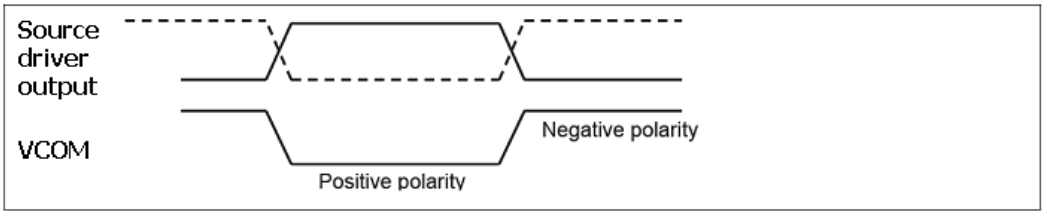


Figure 42 Source output waveform and VCOM polarity relationship

18.1 Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

18.2 Variable resistors

RM68090 uses variable resistors for the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment	
PRP(N)0/1[2:0]	VRCP(N)0/1
3'h0	0R
3'h1	4R
3'h2	8R
3'h3	12R
3'h4	16R
3'h5	20R
3'h6	24R
3'h7	28R

Amplitude adjustment (1)	
VRP(N)0[3:0]	VROP(N)0
4'h0	0R
4'h1	2R
4'h2	4R
…	…
4'hD	26R
4'hE	28R
4'hF	30R

Amplitude adjustment (2)	
VRP(N)0[4:0]	VROP(N)0
5'h00	0R
5'h01	1R
5'h02	2R
…	…
5'h1D	29R
5'h1E	30R
5'h1F	31R

18.3 8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine Adjustment												
KP(N)[2:0]	VgP(N)1		VgP(N)8		VgP(N)20		VgP(N)43		VgP(N)55		VgP(N)62	
	voltage	resistor	voltage	resistor	voltage	resistor	voltage	resistor	voltage	resistor	voltage	resistor
3'h0	VP(N)1	0R	VP(N)9	0R	VP(N)17	0R	VP(N)25	0R	VP(N)33	0R	VP(N)41	0R
3'h1	VP(N)2	4R	VP(N)10	1R	VP(N)18	1R	VP(N)26	1R	VP(N)34	1R	VP(N)42	4R
3'h2	VP(N)3	8R	VP(N)11	2R	VP(N)19	2R	VP(N)27	2R	VP(N)35	2R	VP(N)43	8R
3'h3	VP(N)4	12R	VP(N)12	3R	VP(N)20	3R	VP(N)28	3R	VP(N)36	3R	VP(N)44	12R
3'h4	VP(N)5	16R	VP(N)13	4R	VP(N)21	4R	VP(N)29	4R	VP(N)37	4R	VP(N)45	16R
3'h5	VP(N)6	20R	VP(N)14	5R	VP(N)22	5R	VP(N)30	5R	VP(N)38	5R	VP(N)46	20R
3'h6	VP(N)7	24R	VP(N)15	6R	VP(N)23	6R	VP(N)31	6R	VP(N)39	6R	VP(N)47	24R
3'h7	VP(N)8	28R	VP(N)16	7R	VP(N)24	7R	VP(N)32	7R	VP(N)40	7R	VP(N)48	28R

19. Power-Supply Generating Circuit

19.1 Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the RM68090 and the TFT display application voltage waveforms and electrical potential relationship.

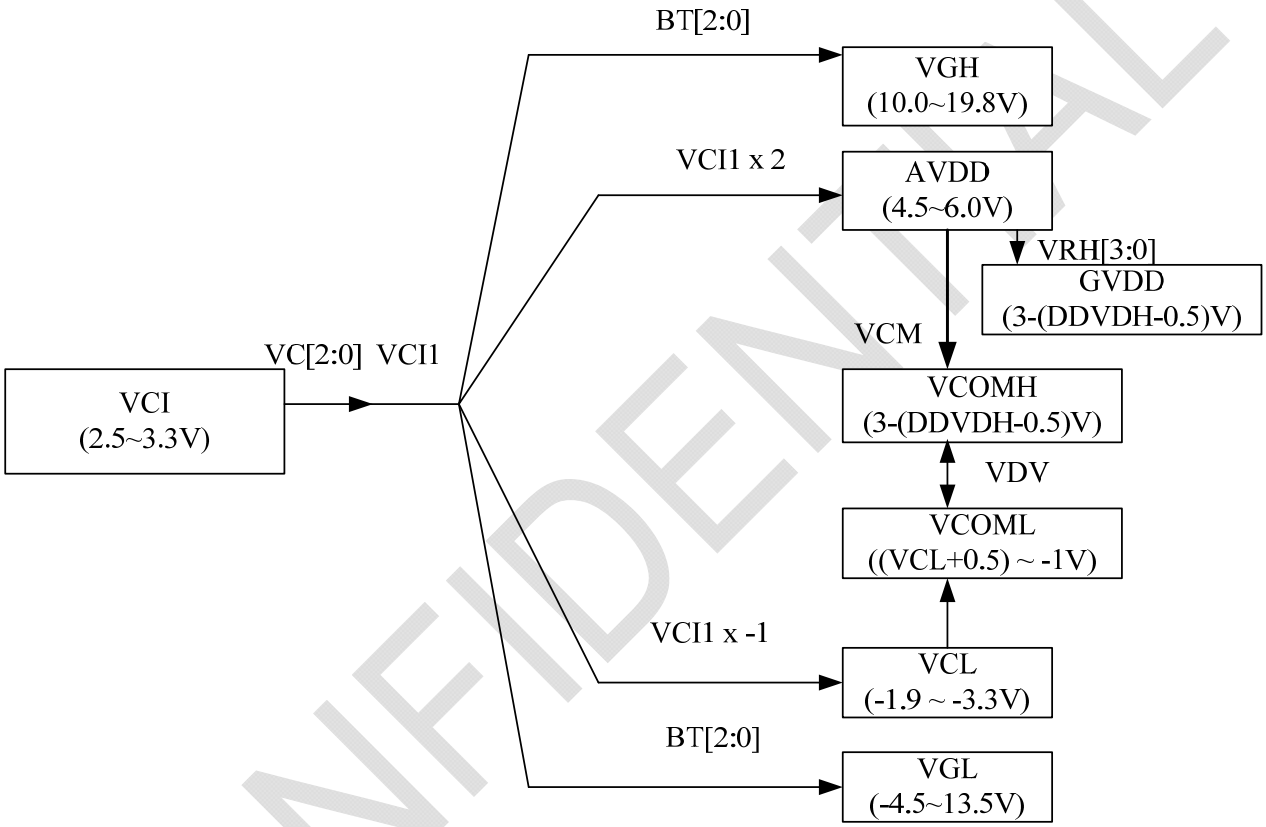


Figure 43 Diagram of voltage generation

Notes:

1. The AVDD, VGH, VGL, and VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. Make sure that output voltage level in operation maintains the following relationship: (AVDD – GVDD) ≥ 0.5V, (VCOML – VCL) > 0.5V. Also make sure VGH-VGL ≤ 28V, VCI-VCL ≤ 6V. When the alternating cycle of VCOM is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

2. In operation, setting voltages within the respective voltage ranges are recommended.

19.2 Liquid crystal application voltage waveform and electrical potential

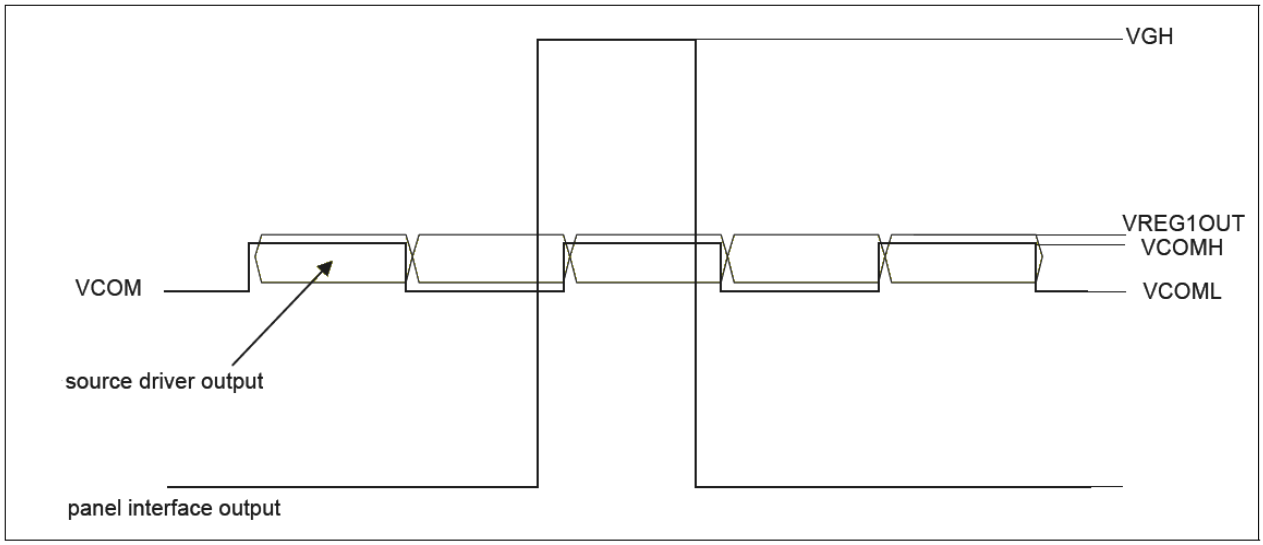


Figure 44 Voltage output to TFT LCD Panel

20. OTP control sequence

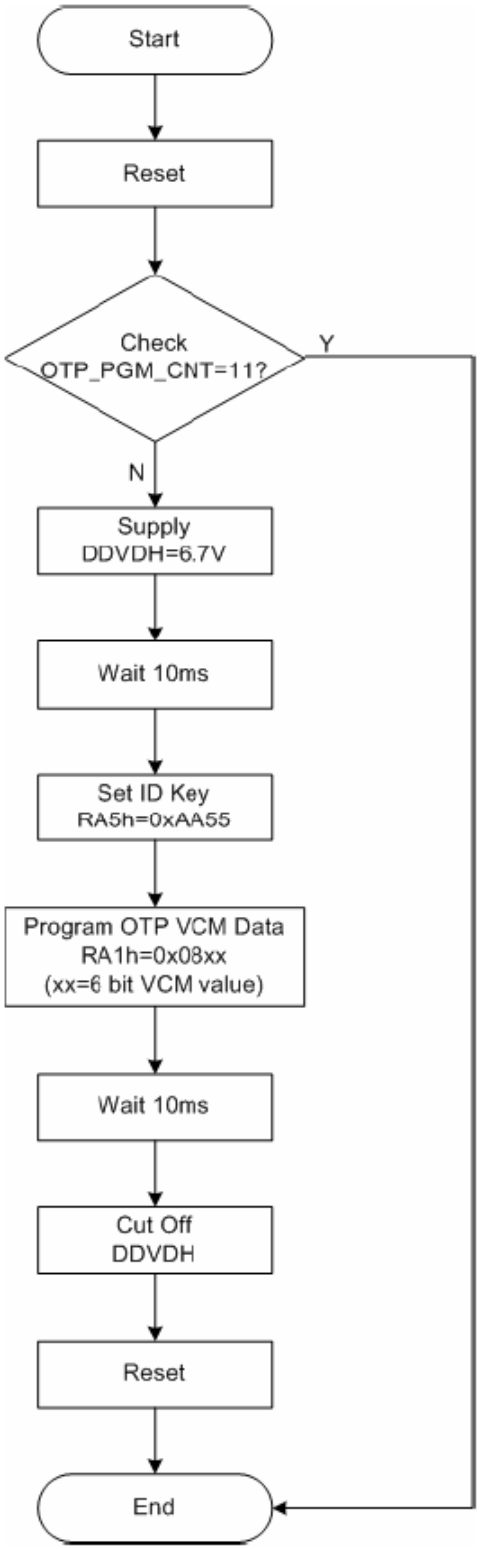
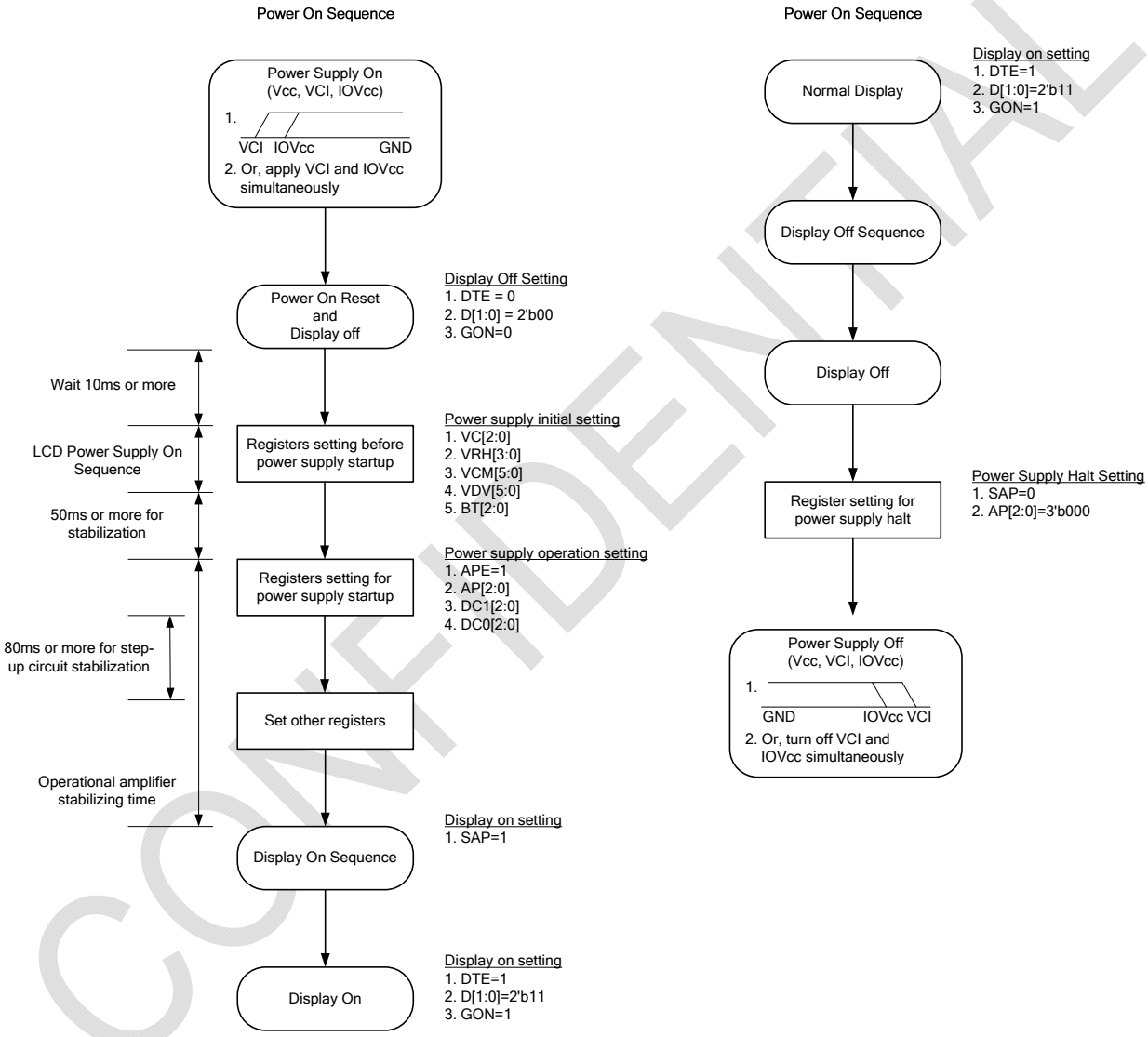


Figure 45 OTP control sequence diagram

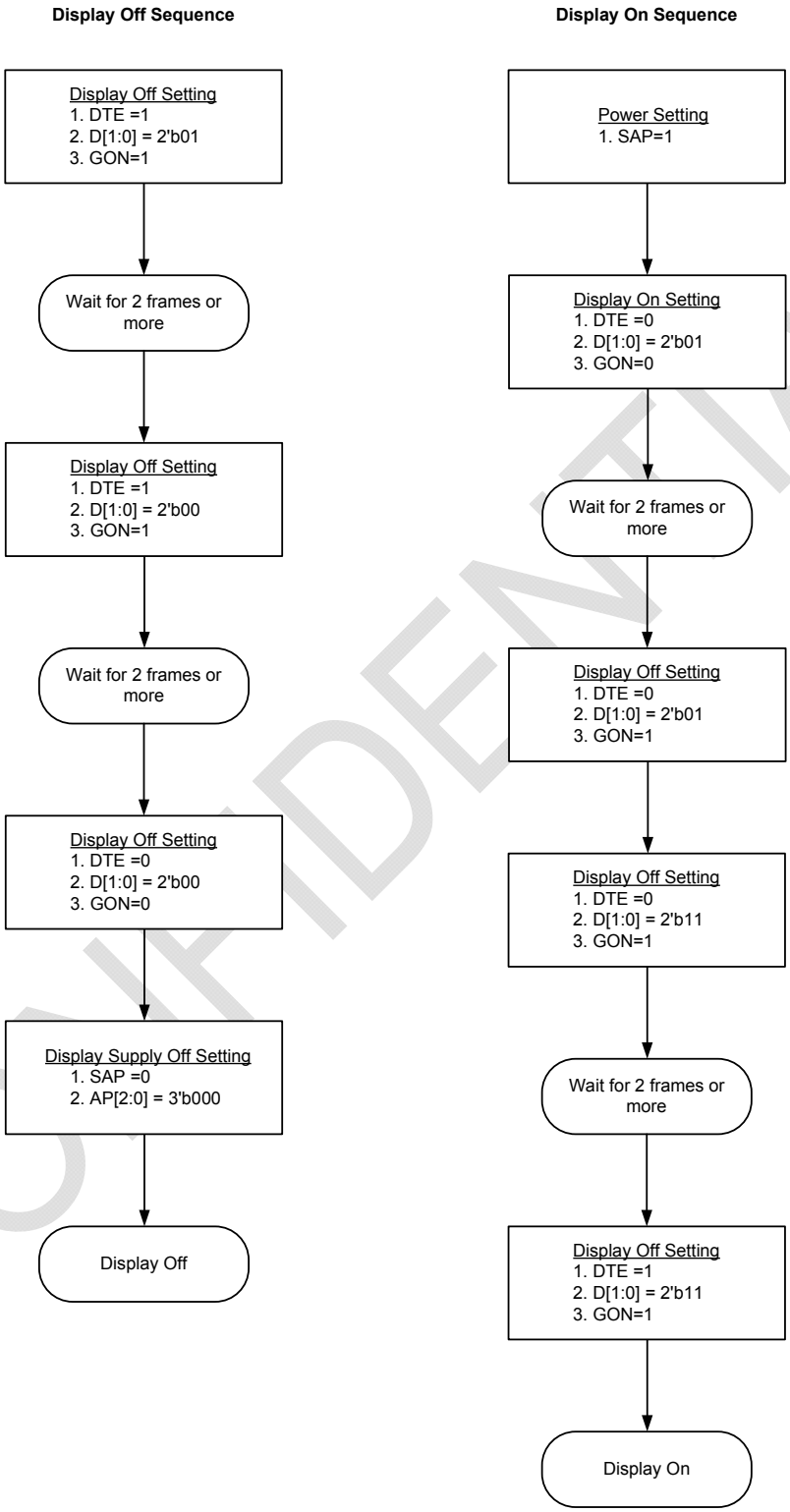
21. Power Supply Instruction Setting

The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences.

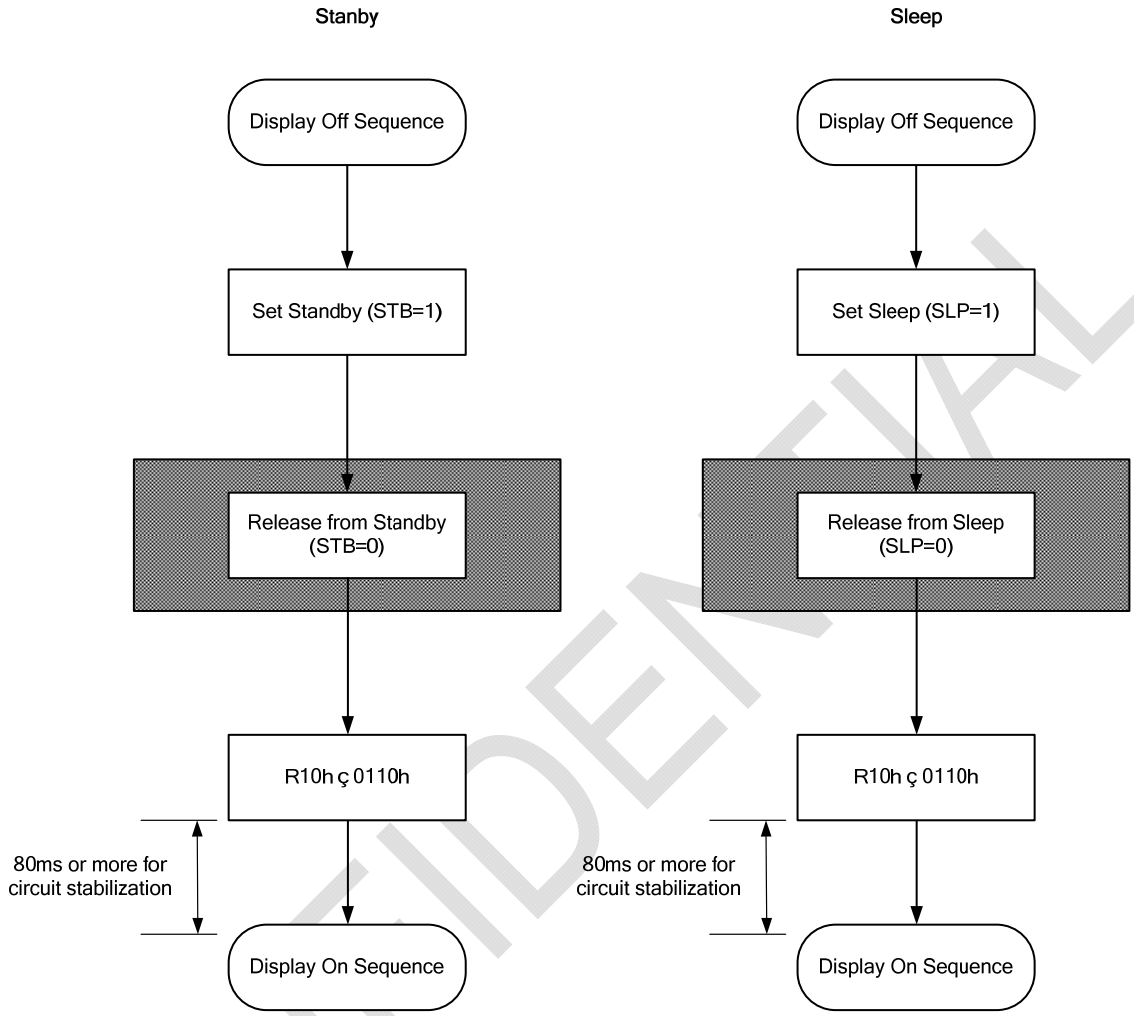
21.1 Power Supply Instruction Setting



21.2 Display On / Off Instruction Setting

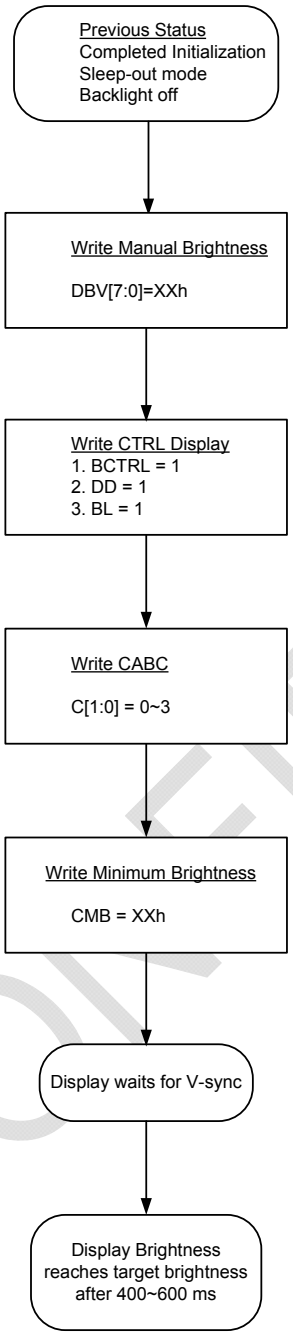


21.3 Sleep mode/Standby mode SET/EXIT sequence

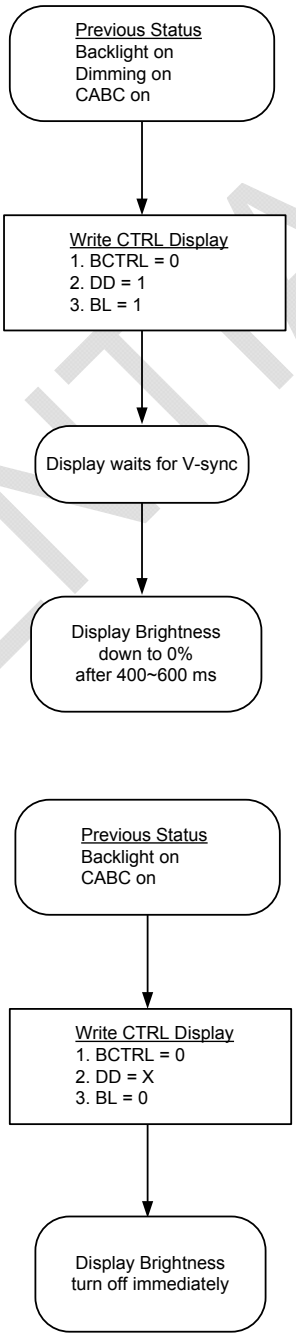


22. Brightness Control ON / OFF sequence

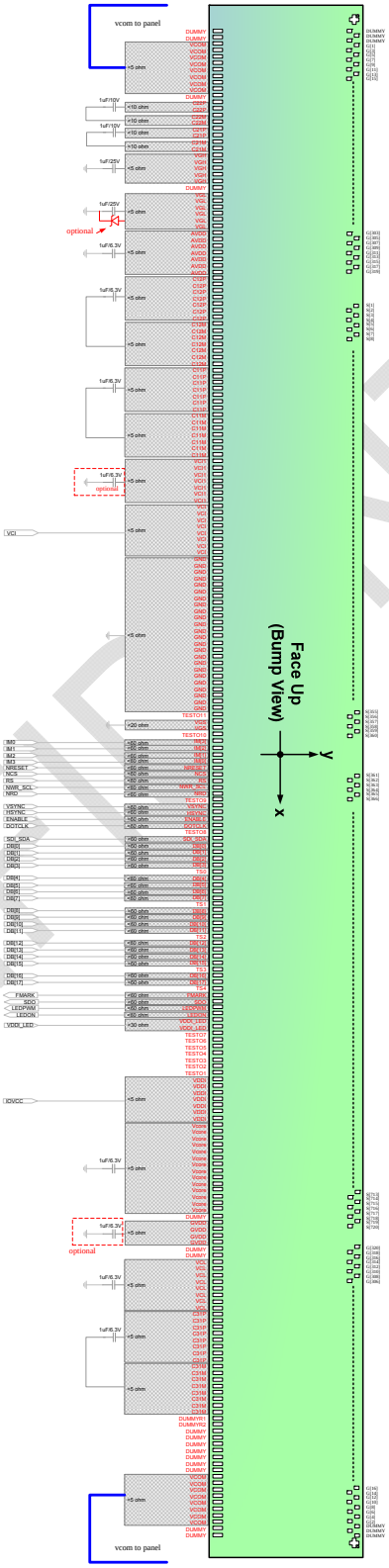
Display Brightness ON Sequence



Display Brightness OFF Sequence



23. Application Circuit



24. Absolute Maximum Ratings

Table 23

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VCI, VDDI	V	-0.3 ~ +4.6	1, 2
Power Supply Voltage 2	VCI – GND	V	-0.3 ~ +4.6	1, 4
Power Supply Voltage 3	AVDD –GND	V	-0.3 ~ +6.0	1, 4
Power Supply Voltage 4	AGND – VCL	V	-0.3 ~ +4.6	1
Power Supply Voltage 5	AVDD – VCL	V	-0.3 ~ +9.0	1, 5
Power Supply Voltage 6	VGH – VGL	V	-0.3 ~ +30.0	1, 5
Input Voltage	Vt	V	-0.3 ~ VDDI + 0.3	1
Operating Temperature	Topr	℃	-40 ~ +85	8, 9
Storage Temperature	Tstg	℃	-55 ~ +110	8, 9

Notes:

1. GND must be maintained.
2. Make sure VCI(high)≥DGND(low), VDDI(high)≥DGND(low).
3. Make sure VCI(high)≥DGND(low).
4. Make sure AVDD(high)≥AGND(low)
5. Make sure AVDD(high) ≥VCL(low).
6. Make sure VGH(high) ≥GND(low)
7. Make sure AGND(high)≥VGL(low).
8. For die and wafer products, specified up to 85℃.
9. This temperature specifications apply to the TCP package.

25. Electrical Characteristics

25.1 DC Electrical Characteristics

(VCI = 2.50V ~ 3.30V, VDDI = 1.65V ~ 3.30V, Ta= -40℃~+85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ	Max.
Input “High” level voltage	V_{IH}	V	VDDI = 1.65V~3.30V	0.85 x VDDI	-	VDDI
Input “Low” level voltage	V_{IL}	V	VDDI = 1.65V~3.30V	-0.3	-	0.15 x VDDI
Output “High” level voltage 1 (DB0-17, FMARK)	V_{OH}	V	VDDI = 1.65V~3.30V IOH = -0.1mA	0.80 x VDDI	-	-
Output “Low” level voltage 1 (DB0-17, FMARK)	V_{OL}	V	VDDI = 1.65V~3.30V IOL = 0.1mA	-	-	0.2 x VDDI
Input/Output leak current	I_{LI}	uA	Vin = 0~VDDI	-0.1	-	0.1
Current Consumption (VDDI-GND)+(VCI-GND) Normal operation mode (262k-colors, display operation)	I_{OP1}	uA	fosc=512kHz (320line drive), VDDI=VCI=2.80V, Ta=25℃, RAM data: 18’h000000	--	TBD	--
Current Consumption (VDDI-GND)+(VCI-GND) Deep standby mode	I_{DST}	uA	VDDI=VCI=2.80V, Ta=25℃	-	30	50
LCD Power Supply Current (AVDD-GND) 262k-color display operation	ILCD	mA	VDDI=VCI=2.80V, AVDD=5.20V, GVDD=4.8V, Frame Rate=70Hz, Ta=25, RAM data: 18’h000000, line-inversion	-	5.5	--
LCD Driving Voltage	AVDD	V	-	4.5	-	6.0
Output Voltage deviation	ΔV_O	mV	-	-	20	-
Maximum output voltage offset	ΔV_Δ	mV	-	-	35	-

25.2 AC Timing Characteristics

25.2.180-System Bus Interface

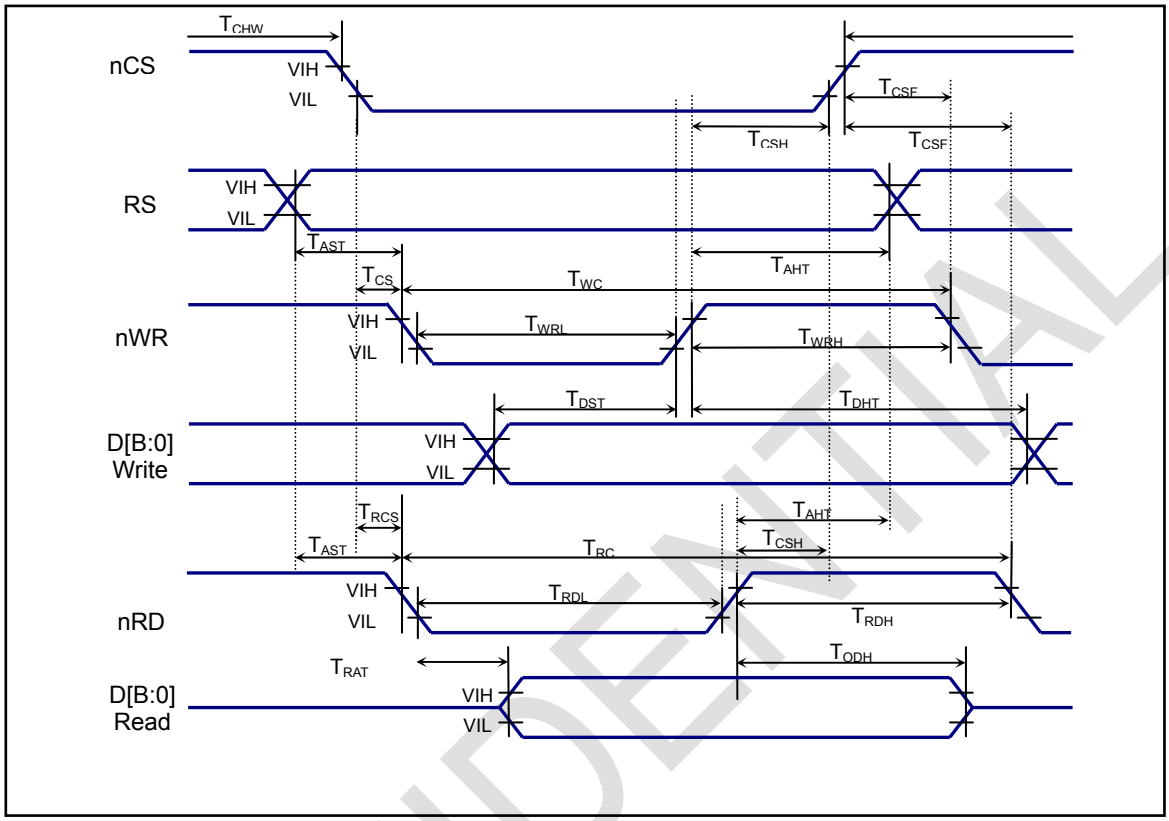


Figure 46 80-system Bus Interface

Normal Write Mode (VDDI = 1.65~3.3V, VCI=2.5~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
RS	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	5		ns	
nCS	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	10		ns	
	T_{RCS}	Chip select setup time (Read)	10		ns	
nWR	T_{CSH}	Chip select hold time	10		ns	
	T_{WC}	Write cycle	75		ns	
	T_{WRH}	Control pulse “H” duration	30		ns	-
	T_{WRL}	Control pulse “L” duration	40		ns	
nRD (ID)	T_{CSH}	Chip select hold time	10		ns	
	T_{RC}	Read cycle	300		ns	-
	T_{RDH}	Control pulse “H” duration	150		ns	
	T_{RDL}	Control pulse “L” duration	150		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	-
	T_{DHT}	Data hold time	15		ns	
	T_{RAT}	Read access time		100	ns	
	T_{ODH}	Output disable time	5		ns	

25.2.2 Clock Synchronous Serial Interface

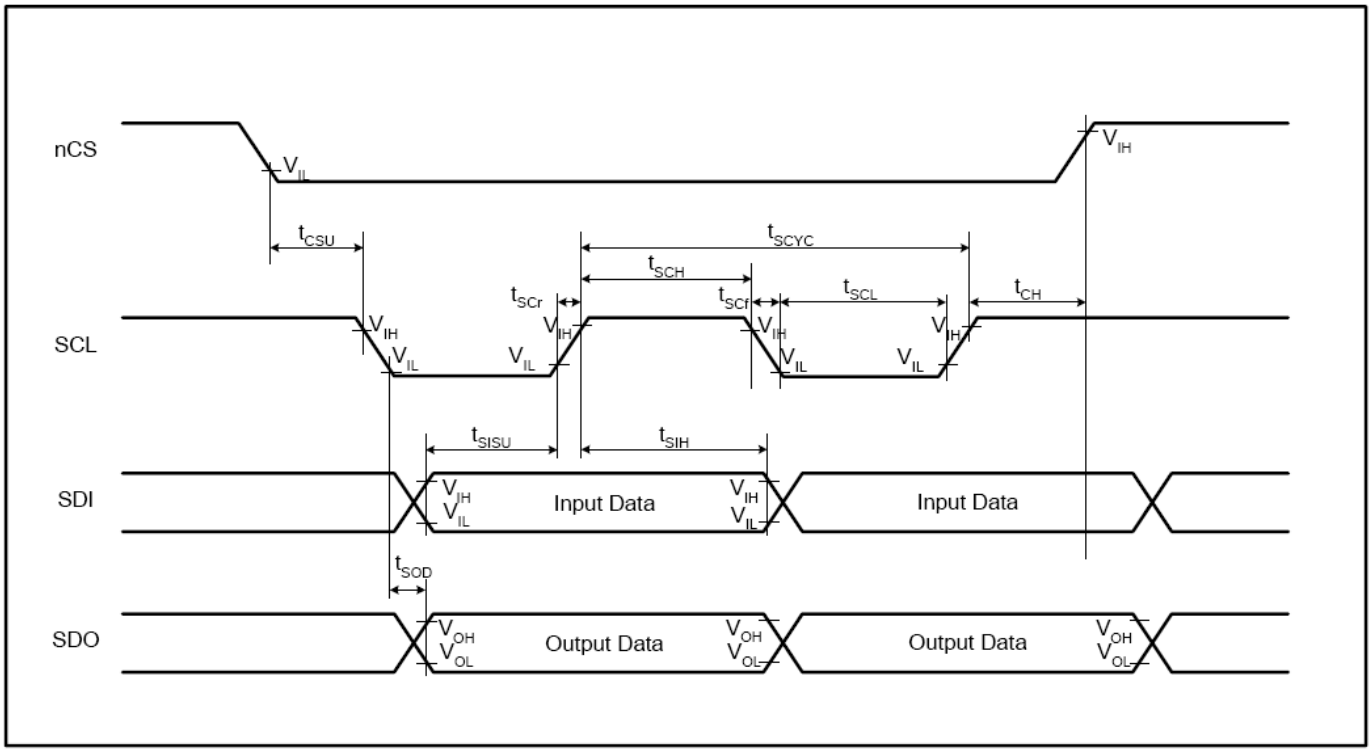


Figure 47 Clock Synchronous Serial Interface

VDDI = 1.65~3.3V, VCI=2.5~3.3V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T_{SCYC}	Clock cycle (Write)	100		ns	-
	T_{SCYC}	Clock cycle (Read)	200		ns	
	T_{SCH}	Clock “H” pulse width (Write)	40		ns	
	T_{SCH}	Clock “H” pulse width (Read)	100		ns	
	T_{SCL}	Clock “L” pulse width (Write)	40		ns	
	T_{SCL}	Clock “L” pulse width (Read)	100		ns	
	T_{SCr}	Clock rise time		5	ns	
	T_{SCf}	Clock fall time		5	ns	
nCS	T_{CSU}	Chip select setup time	10		ns	-
	T_{CH}	Chip select hold time	50		ns	
SDI	T_{SISU}	Data input setup time	20		ns	-
	T_{SIH}	Data input hold time	20		ns	
SDO	T_{SOD}	Data output setup time		100	ns	-
	T_{SOH}	Data output hold time	5		ns	

25.2.3 RGB Interface

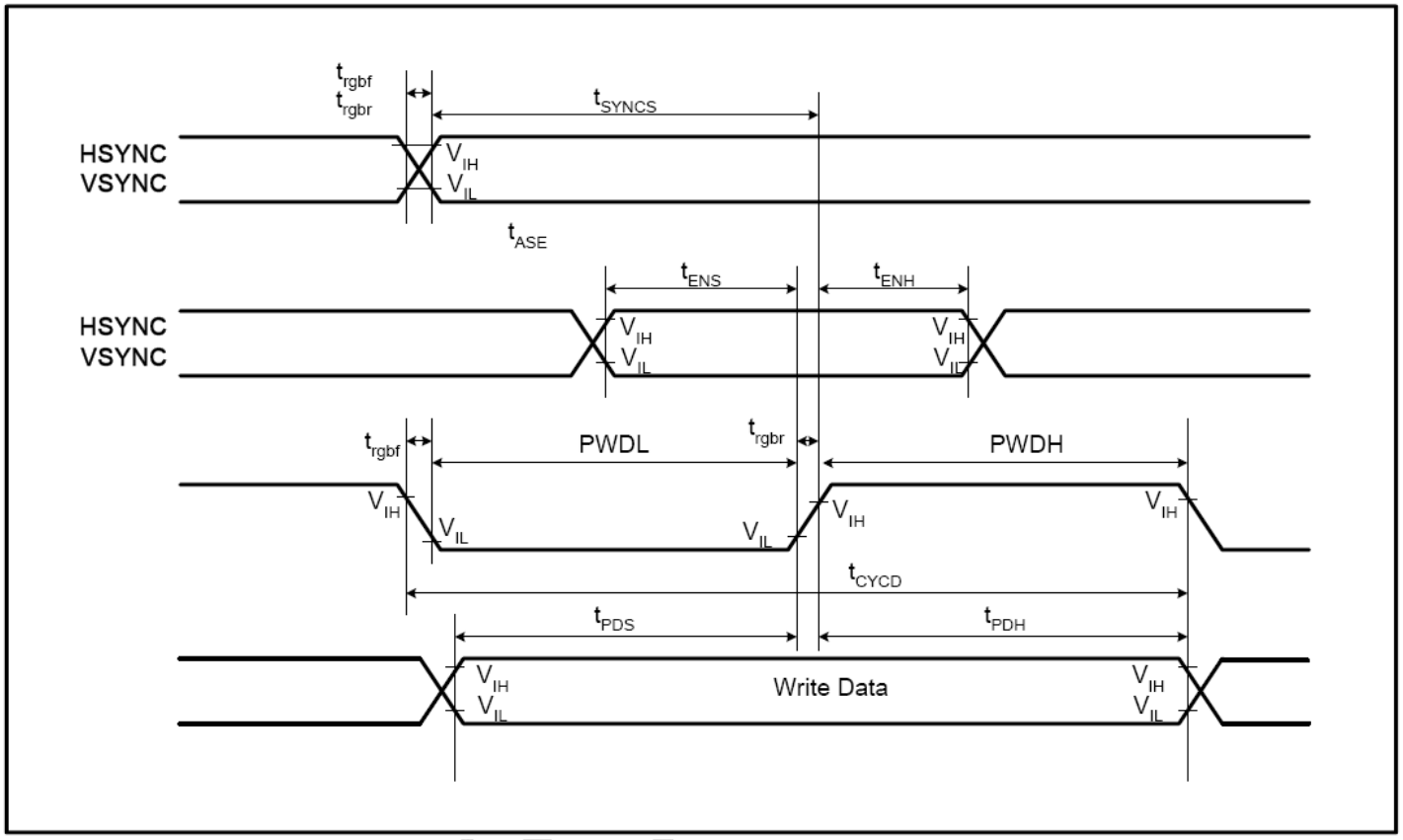


Figure 48 Timing chart for RGB Interface

18/16-bit Bus RGB Interface Mode (VDDI = 1.65~3.3V, VCI=2.5~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
VSYNC	T_{SYNCS}	VSYNC setup time	10		ns	-
	T_{rghr}	VSYNC rise time		25	ns	
	T_{rghf}	VSYNC fall time		25	ns	
HSYNC	T_{SYNCS}	HSYNC setup time	10		ns	-
	T_{rghr}	HSYNC rise time		25	ns	
	T_{rghf}	HSYNC fall time		25	ns	
ENABLE	T_{ENS}	ENABLE setup time	10		ns	-
	T_{ENH}	ENABLE hold time	10		ns	
DB[17:0]	T_{PDS}	Data input setup time	10		ns	-
	T_{PDH}	Data input hold time	40		ns	
DOTCLK	PWDH	DOTCLK “H” pulse width	40		ns	-
	PWDL	DOTCLK “L” pulse width	40		ns	
	T_{CYCD}	DOTCLK clock cycle	150			
	T_{rghr}	DOTCLK rise time		25	ns	
	T_{rghf}	DOTCLK fall time		25	ns	

6-bit Bus RGB Interface Mode (VDDI = 1.65 ~ 3.3V, VCI=2.5~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
VSYNC	T_{SYNCS}	VSYNC setup time	0		ns	-
	T_{rghr}	VSYNC rise time		25	ns	
	T_{rghf}	VSYNC fall time		25	ns	

HSYNC	T_{SYNCS}	HSYNC setup time	0		ns	-
	T_{rghr}	HSYNC rise time		25	ns	
	T_{rghf}	HSYNC fall time		25	ns	
ENABLE	T_{ENS}	ENABLE setup time	10		ns	-
	T_{ENH}	ENABLE hold time	10		ns	
DB[17:0]	T_{PDS}	Data input setup time	10		ns	-
	T_{PDH}	Data input hold time	30		ns	
DOTCLK	PWDH	DOTCLK “H” pulse width	30		ns	-
	PWDL	DOTCLK “L” pulse width	30		ns	
	T_{CYCD}	DOTCLK clock cycle	80			
	T_{rghr}	DOTCLK rise time		25	ns	
	T_{rghf}	DOTCLK fall time		25	ns	

25.3 Reset Timing Characteristics

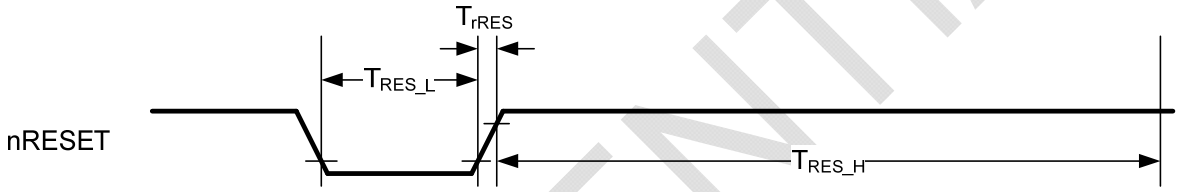


Figure 49 Reset Operation

Reset Timing Characteristics (VCI = 2.5 ~ 3.3 V, VDDI = 1.65 ~ 3.3 V)

Item	Symbol	MIN	MAX	Unit	Description
Reset low-level width	T_{RES_L}	1		ms	-
Reset rise time	T_{rRES}		10	us	-
Reset high-level witdth	T_{RES_H}	50		ms	-

Note: After nRESET releasing, the host processor have to wait 10 milliseconds before sending any command.