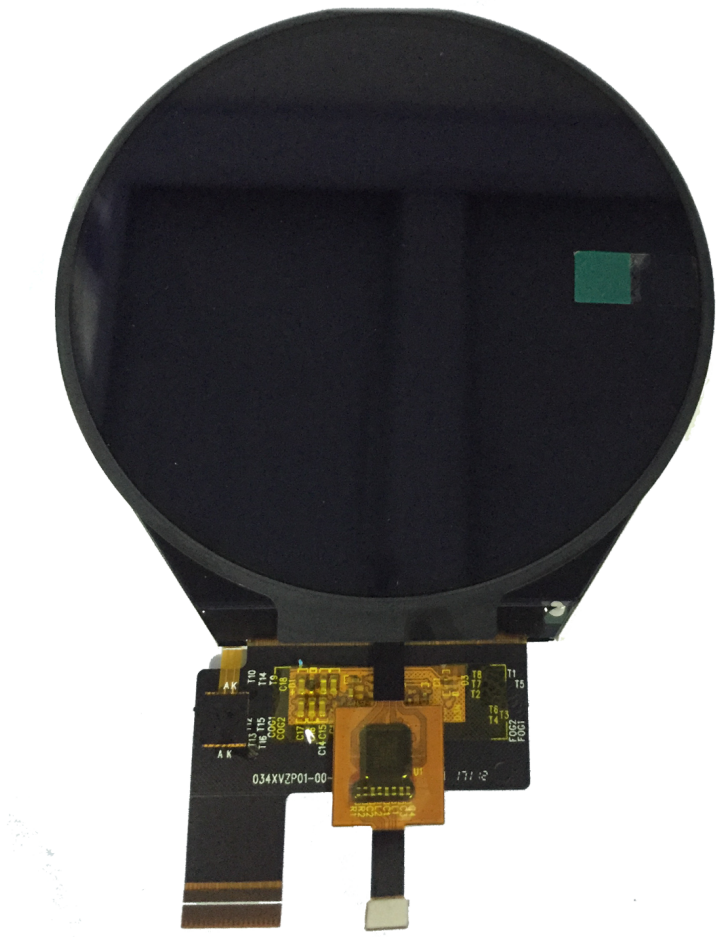
DisplayModule



DM-TFTR34-471

3.4" 800 x 800 Round Free View Touch TFT LCD - I2C,MIPI

Table of Contents

1 General Specifications

Feature		Spec
Display Spec.	Size	3.4 inch
	Resolution	800(RGB) x 800
	Technology Type	a-Si
	Pixel Configuration	R.G.B. Vertical Stripe
	Pixel pitch(um)	109.5*109.5
	Display Mode	SFT
	Surface Treatment	HC
	Viewing Direction	FREE
Mechanical Characteristics	Module (W x H x D) (mm) with CTP	99.0 x 96.6 x 3.98
	Active Area(mm)	87.6*87.6
	With /Without TSP	With CTP
	Matching Connection Type	FPC
	LED Numbers	8 LEDs
	CTP Surface hardness	≥7H
	Weight (g)	TBD
Electrical Characteristics	Interface	MIPI 3 lane
	Color Depth	16.7M
	LCD Driver IC	ILI9881C
	CTP Driver IC	HX8526-E30
	CTP Interface	IIC

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: ± 5%

2 Input/Output Terminals

2.1 LCD Interface

Pin No.	Symbol	I/O	Function	Remark
1	GND	GND	Power Ground	
2	LEDA	P	LED Anode	
3	LEDA	P		
4	LEDK	P	LED Cathode	
5	LEDK	P		
6	GND	GND	Power Ground	
7	VDD(-5V)	P	-5V INPUT	
8	VDD(-5V)	P		
9	GND	GND	Power Ground	
10	VDD(+5V)	P	+5V INPUT	
11	VDD(+5V)	P		
12	GND	GND	Power Ground	
13	IOVCC	P	Power supply 1.8V	
14	IOVCC	P		
15	GND	GND	Power Ground	
16	RESET	I	Global Reset Pin	
17	GND	GND	Power Ground	
18	TE	I	tearing effect output	
19	GND	GND	Power Ground	
20	NC	N	No connect	
21	NC	N		
22	NC	N		
23	GND	GND	Power Ground	
24	LAN2_P	I	MIPI lane 2+	
25	NC	N	No connect	
26	LAN2_N	I	MIPI lane 2-	
27	GND	GND	Power Ground	
28	CLK_P	I	MIPI clock +	
29	NC	N	No connect	

30	CLK_N	I	IMIPI clock -	
31	GND	GND	Power Ground	
32	LAN1_P	I	MIPI lane 1+	
33	NC	N	No connect	
34	LAN1_N	I	MIPI lane 1-	
35	GND	GND	Power Ground	
36	LAN0_P	I	MIPI lane 0+	
37	NC	N	No connect	
38	LAN0_N	I	MIPI lane 0-	
39	GND	GND	Power Ground	

2.2 CTP Interface

Pin	Name
1	VCCA(2.8V)
2	VCCD(1.8V)
3	SCL
4	SDA
5	GND
6	GND
7	TSIX
8	NC
9	NC
10	XRES

3 Absolute Maximum Ratings

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage	IOVCC	-0.3	3.3	V	Note1
Power Supply Voltage	VDD(+5V)	-0.3	6.5		
Power Supply Voltage	VDD(-5V)	-6.5	0.3		
Logic Supply Voltage	VCCIO	-0.3	3.3	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	
Relative Humidity Note2	RH	--	≤95	%	Ta≤40℃
		--	≤85	%	40℃＜Ta≤50℃
		--	≤55	%	50℃＜Ta≤60℃
		--	≤36	%	60℃＜Ta≤70℃
		--	≤24	%	70℃＜Ta≤80℃
Absolute Humidity	AH	--	≤70	g/m³	Ta＞70℃

Table 3 Absolute Maximum Ratings

Note1: Input voltage include R0~R5, G0~G5, B0~B5, Dotclk, Hsync, Vsync, Enable, R/L, U/D.

4 Electrical Characteristics

4.1 LCD characteristics

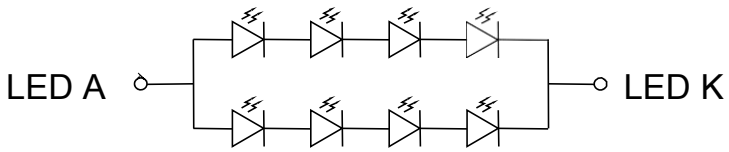
GND=0V,Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Power Supply Voltage		IOVCC	1.75	1.8	3.3	V	
Power Supply Voltage		VDD(+5V)	4.5	5.0	6	V	
Power Supply Voltage		VDD(-5V)	-6	-5.0	-4.5		
Input Signal Voltage	High Level	VIH	0.7*IOVCC	-	IOVCC	V	
	Low Level	VIL	0	-	0.3*IOVCC	V	

Table 4.1 LCD module electrical characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
4.2 Backlight Unit **Ta=25℃**						
Forward Current	I_F	18	20	22	mA	1 LED
Forward Voltage	V_F	-	12.8	-	V	BLH-BLL
Backlight Power Consumption	W_{BL}	-	512	-	mW	8 LEDs
Operating Life Time	-	-	30,000	-	Hrs	For each LED

Note1: Figure below shows the connection of backlight LED.



LED CIRCUIT

(If=40mA / Vf=12.8V TYP)

Note 2: 1LED: V_F =3.2V I_F =20mA

Note 3: I_F is defined for one LED.

Optical performance should be evaluated at Ta=25℃ only.

If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

5 Timing Chart

5.1 MIPI Data to clock Timing Definition

5.1.1 High Speed Mode

High Speed Mode – Clock Channel Timing

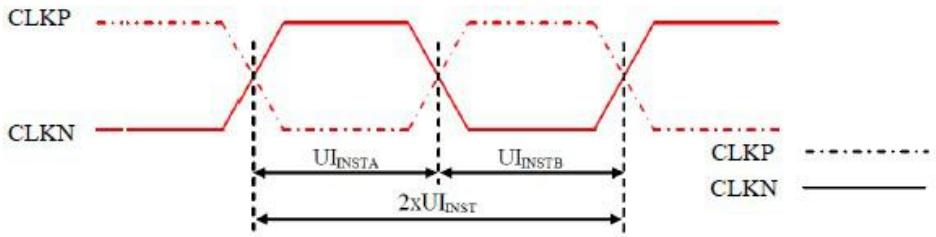


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

High Speed Mode – Data Clock Channel Timing

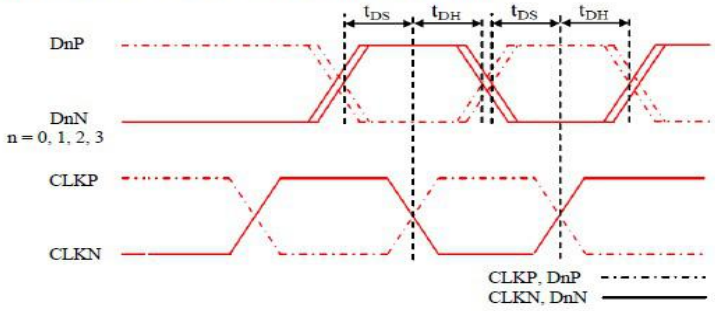


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rising and Falling Timings

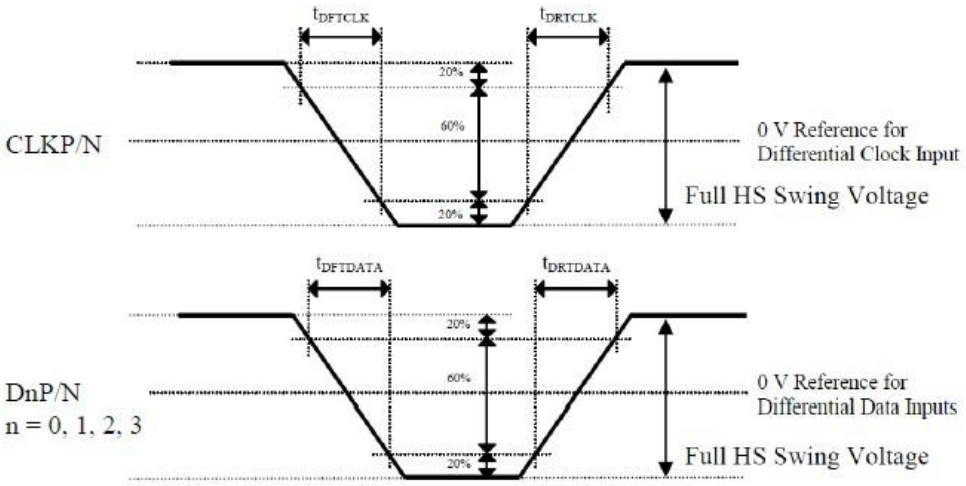


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

5.1.2 Low Speed Mode

Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

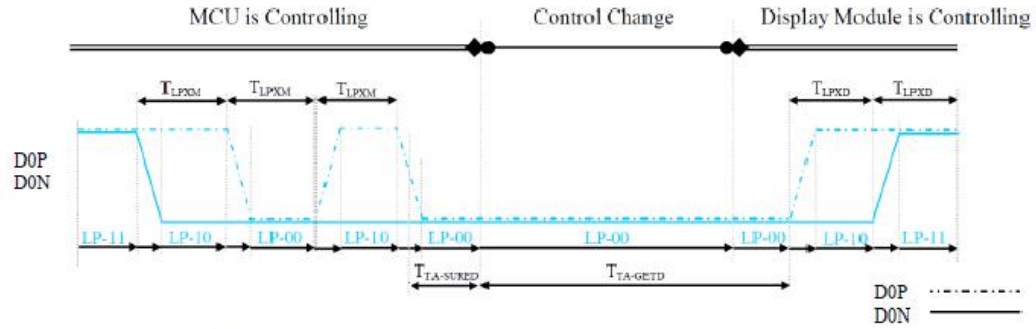


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

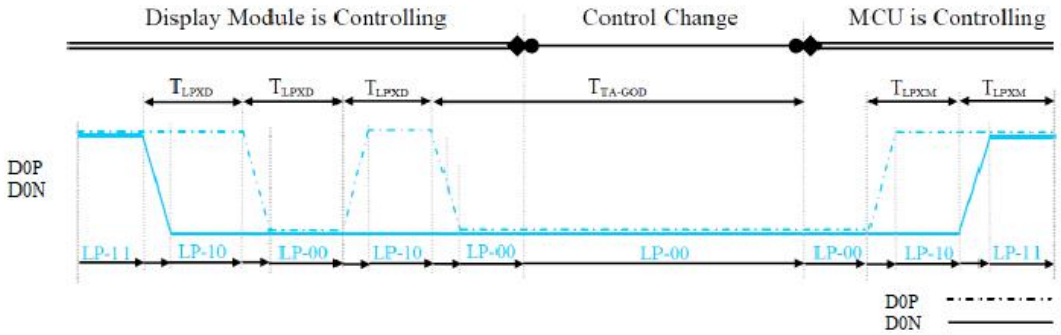


Figure 122: BTA from the Display Module to the MCU

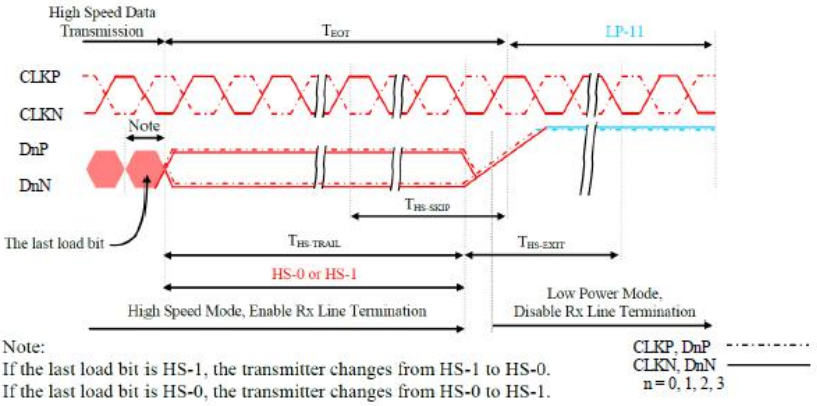
Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

Data Lanes from Low Power Mode to High Speed Mode

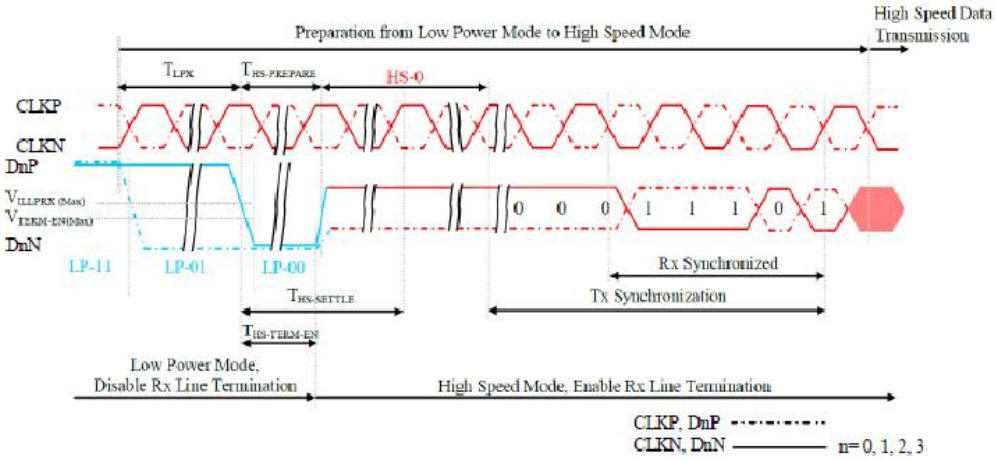


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

DSI Clock Burst – High Speed Mode to/from Low Power Mode

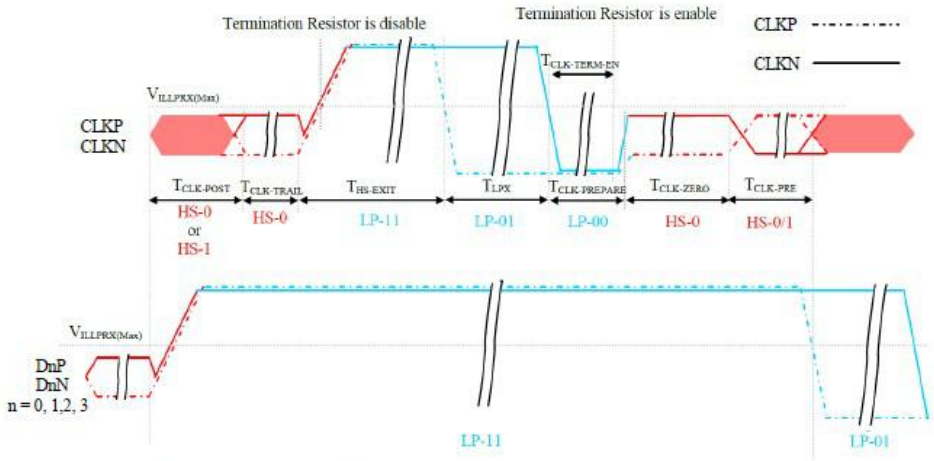
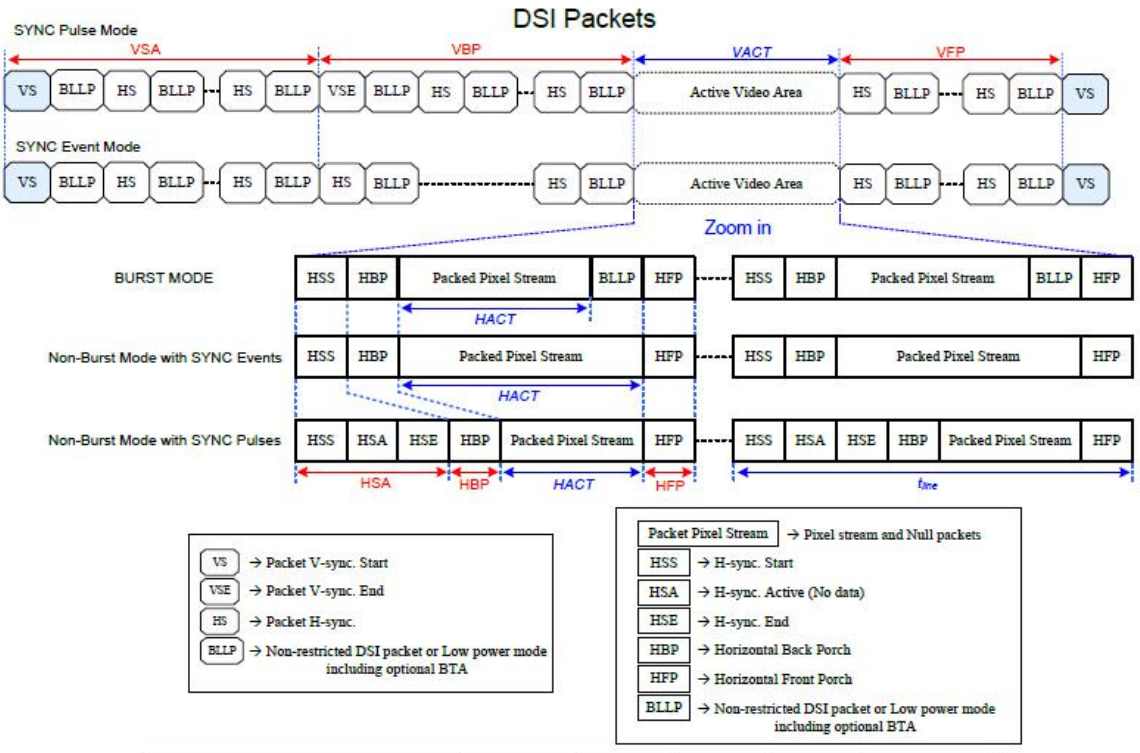


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

5.2 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	4	-	Line
Vertical Back Porch	VBP	14 (Note 6)	20	-	Line
Vertical Front Porch	VFP	8 (Note 6)	8	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	24	-	Pixel
Horizontal Back Porch	HBP	1.6	100	-	Pixel
Horizontal Front Porch	HFP	1.6	50	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	200	-	-	bps/lane
Bit rate	BR_{bps}	200	-	Note 5	Line

5.3 Reset Timing

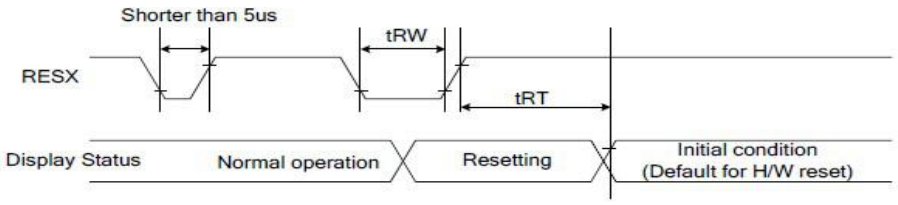


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

6 Optical Characteristics

6.1 Driving the backlight condition

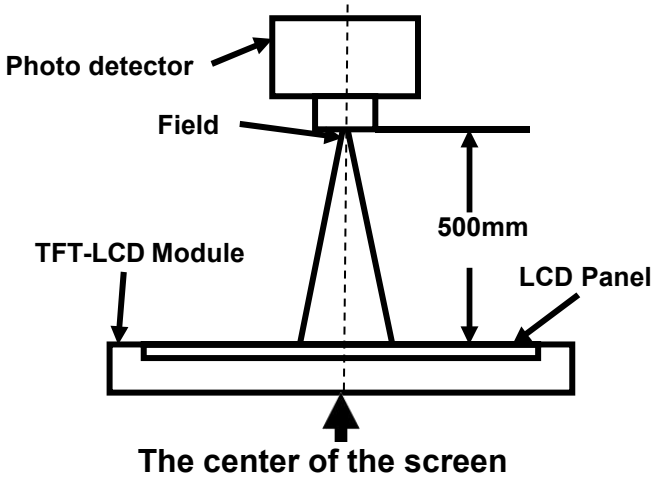
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	70	80	--	Degree	Note2
		θB		70	80	--		
		θL		70	80	--		
		θR		70	80	--		
Contrast Ratio		CR	θ=0°	600	800	--		Note 3
Response Time		T_{ON}	25℃	--	25	35	ms	Note 4
		T_{OFF}						
Chromaticity	**White**	x	Backlight is on	0.263	0.313	0.363		Note 1,5
		y		0.279	0.329	0.379		
	Red	x		--	TBD	--		Note 1,5
		y		--	TBD	--		
	Green	x		--	TBD	--		Note 1,5
		y		--	TBD	--		
	Blue	x		--	TBD	--		Note 1,5
		y		--	TBD	--		
Uniformity		U		75	80	--	%	Note 6
NTSC				65	70	--	%	Note 5
Luminance		L		280	350	--	cd/m^2	Note 7

Test Conditions:

1. I_F= 20 mA(one LED), and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

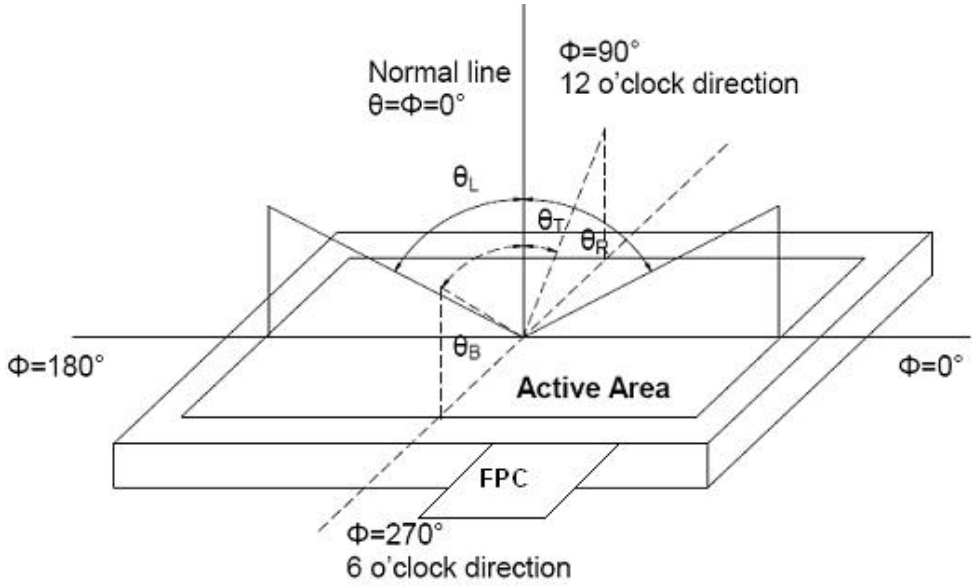
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

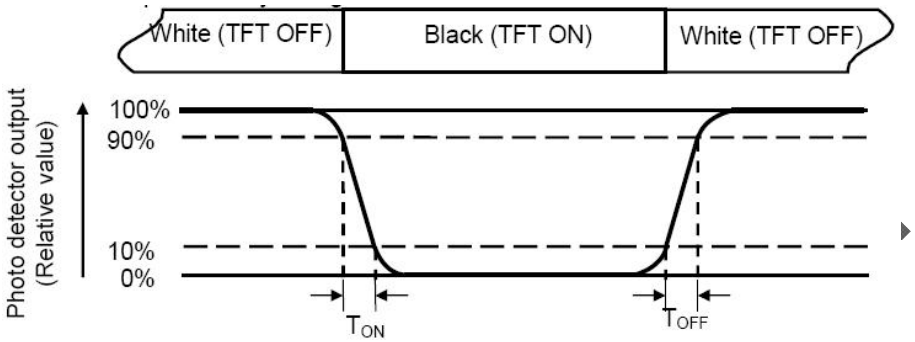
"White state ": The state is that the LCD should drive by Vwhite.

“Black state”: The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

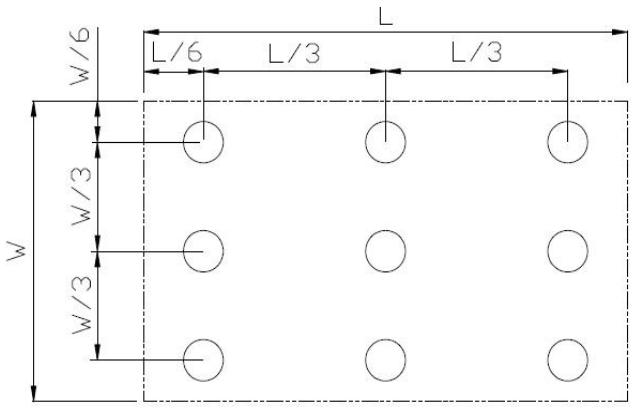
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts=+70℃, 120hrs Restore 2H at 25℃ Power off	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	Ta=-20℃, 120hrs Restore 2H at 25℃ Power off	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta=+80℃, 120hrs Restore 2H at 25℃ Power off	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	Ta=-30℃, 120hrs Restore 2H at 25℃ Power off	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	Ta=+60℃, 90% RH, 120 hours Restore 2H at 25℃ Power off	IEC60068-2-78 :2001 GB/T2423.3—2006
7	ESD Sensitivity test	C=150pF, R=330Ω,5points/panel Air:± 8KV, 5times, Contact:± 4KV, 5 times, （Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa）	IEC61000-4-2:2001 GB/T17626.2-2006

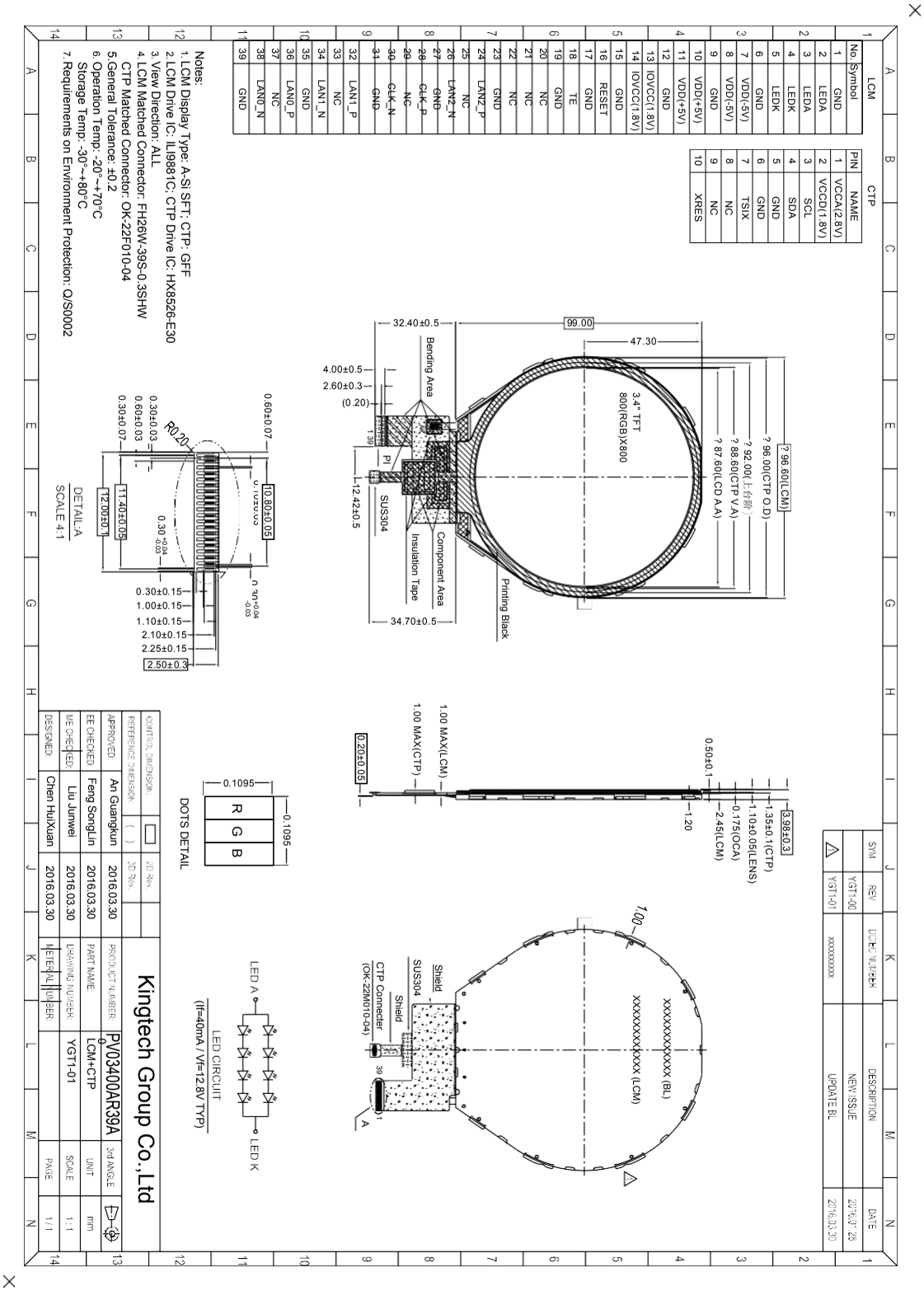
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

8 Mechanical Drawing



9 Packing Drawing

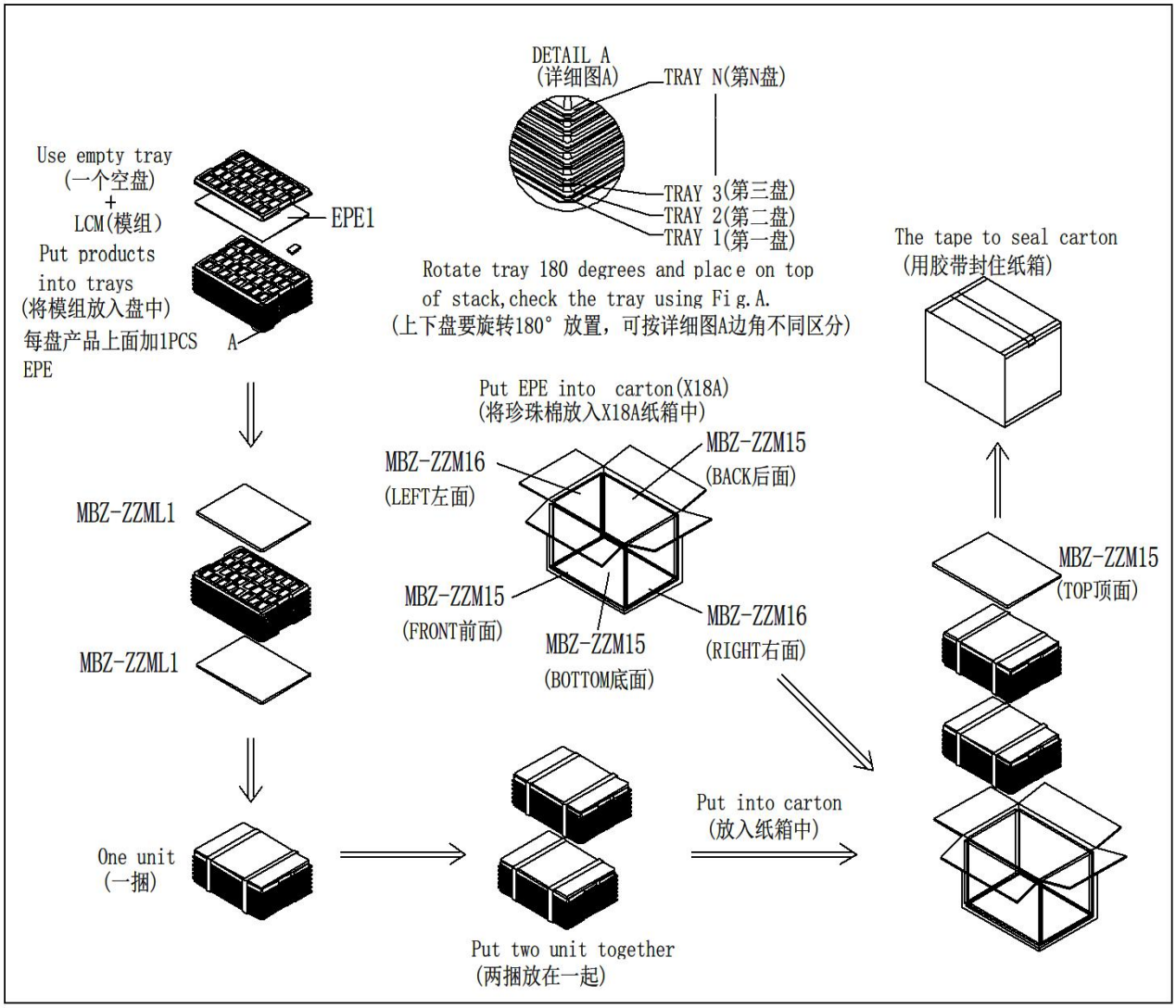
9.1 Per Carton

No.	Item	Model (Materiel)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM module	PV03400AR39A	96.6×99.0×3.98mm	TBD	96	
2	Tray	PV03400AR39A YBZ1-00	356x256x13.50	TBD	26	
3	EPE（珍珠棉1）	PV03400AR39A YPF1-00	312.67×216×1mm	TBD	24	
4	EPE（珍珠棉2）	MBZ-ZZML1	336×246×6mm	TBD	4	
5	EPE（珍珠棉3）	MBZ-ZZM15	375×275×10mm	TBD	4	
6	EPE（珍珠棉4）	MBZ-ZZM16	250×280×12mm	TBD	2	
7	Carton（纸箱）	X18A	395×290×315mm	TBD	1	
8	Total weight	TBD				

9.2 Packaging Specification and Quantity

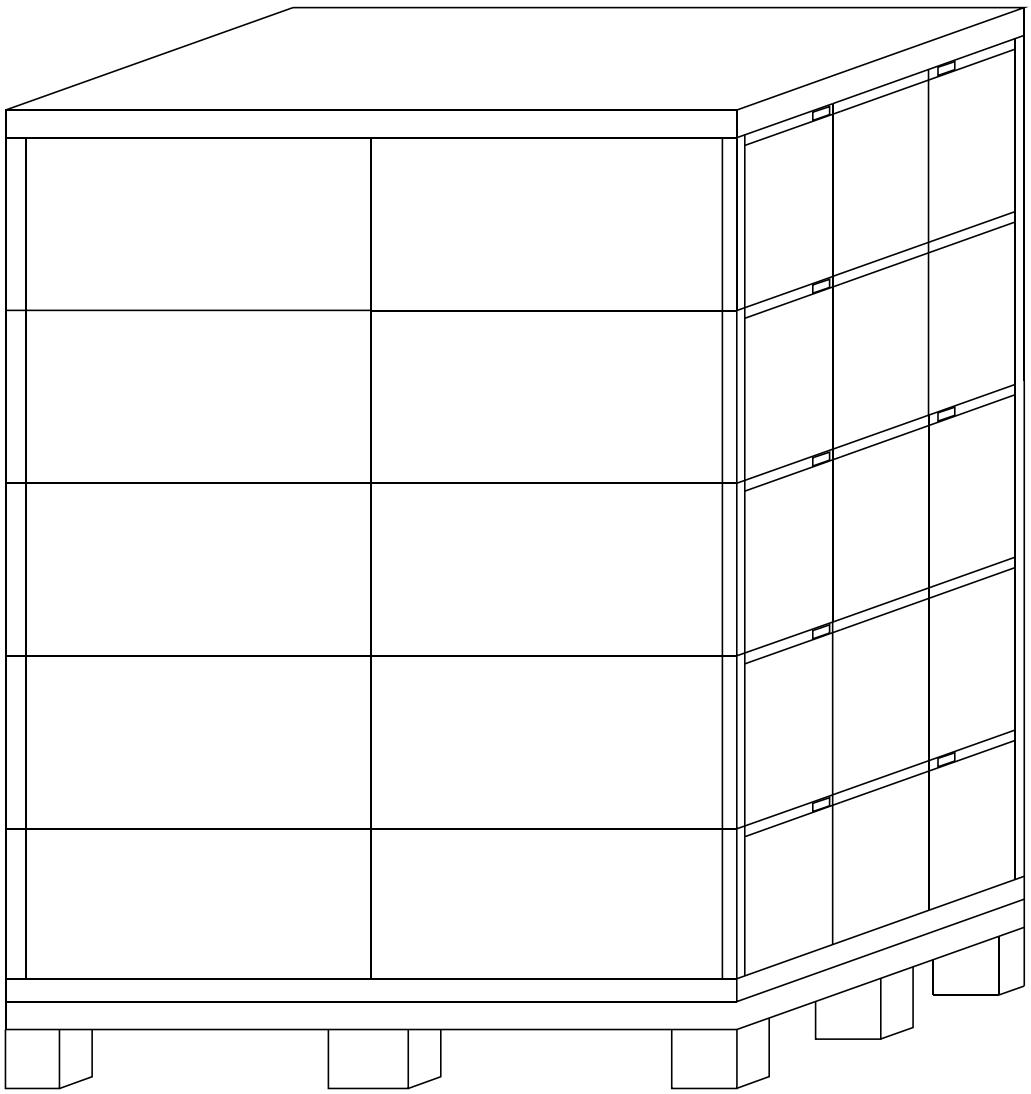
(1) LCM quantity per tray（每盘模组数量）:4 pcs
(2) Total LCM quantity per group（每组模组总数量）：48 pcs（12Tray盘+1 Enpty tray空盘）
(3) Total LCM quantity per Carton（每箱模组总数量）：quantity per group（每组模组总数量）48 pcs×group quantity per Carton（每箱组数量）2= 96 pcs

9.3 Packing Form



9.4 Shipping Package of Palletizing Sequence

纸箱堆叠数按 2×3/每层×共 5 层



10 Precautions for Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

10.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.