DisplayModule

DM-TFTR34-359

3.4“ 800x800 Round Screen Display Panel with Capacitive Touch -MIPI

Contents

1 Revision History

Date	Changes
2018-06-21	First release

2 Main Features

Item	Specification	Unit
Resolution	800(RGB) x 800	pixel
Module Dimension	99.00 x 96.60 x 3.98	mm
TFT Controller IC	ILI9881C	-
CTP Controller IC	HX8526-E30	
Interface	MIPI 3lane	-
Dot Pitch	0.109 x 0.109	mm
Display Color	16.7M	
View Direction	FREE	
Display mode	Super-fine TFT	
Weight	TBD	g

3 Pin Description

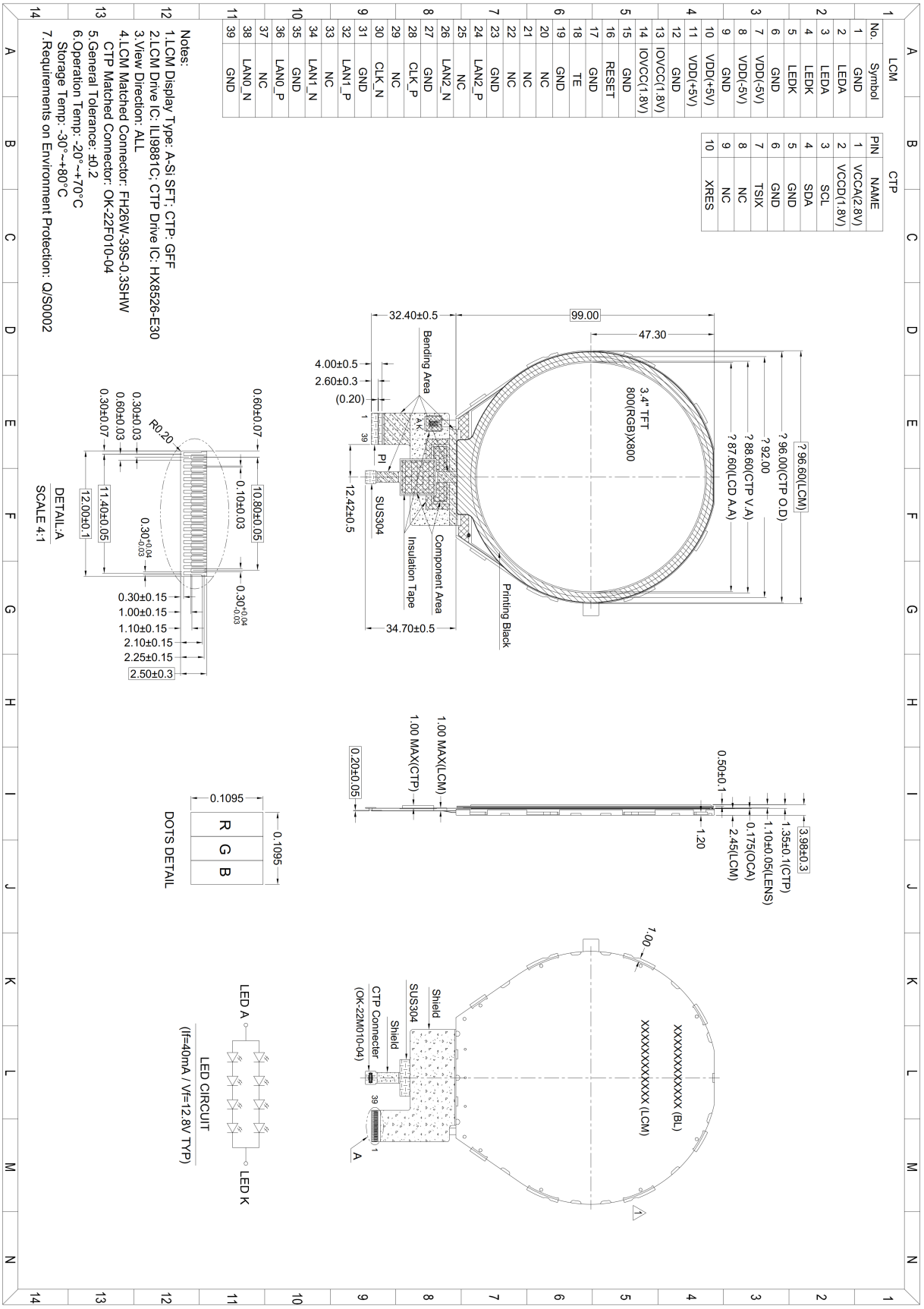
3.1 TFT

No.	Symbol	Description
1	GND	Ground
2	LEDA	LED Anode
3	LEDA	LED Anode
4	LEDK	LED Cathode
5	LEDK	LED Cathode
6	GND	Ground
7	VDD(-5V)	-5V input
8	VDD(-5V)	-5V input
9	GND	Ground
10	VDD(+5V)	+5V input
11	VDD(+5V)	+5V input
12	GND	Ground
13	IOVCC	Power supply 1.8V
14	IOVCC	Power supply 1.8V
15	GND	Ground
16	RESET	Global Reset Pin
17	GND	Ground
18	TE	Tearing effect Output
19	GND	Ground
20	NC	No connect
21	NC	No connect
22	NC	No connect
23	GND	Ground
24	LAN2_P	MIPI lane 2+
25	NC	No connect
26	LAN2_N	MIPI lane 2-
27	GND	Ground
28	CLK_P	MIPI clock +
29	NC	No connect
30	CLK_N	MIPI clock -
31	GND	Ground
32	LAN1_P	MIPI lane 1+
33	NC	No connect
34	LAN1_N	MIPI lane 1-
35	GND	Ground
36	LAN0_P	MIPI lane 0+
37	NC	No connect
38	LAN0_N	MIPI lane 0-
39	GND	Ground

3.2 CTP

No.	Symbol	Description
1	VCCA(2.8V)	Supply voltage
2	VCCD(1.8V)	I/O power supply voltage
3	SCL	I2C clock input
4	SDA	I2C data input and output
5	GND	Ground
6	GND	Ground
7	TSIX	
8	NC	No connect
9	NC	No connect
10	XRES	

4 Mechanical Drawing



5 Electrical Characteristics

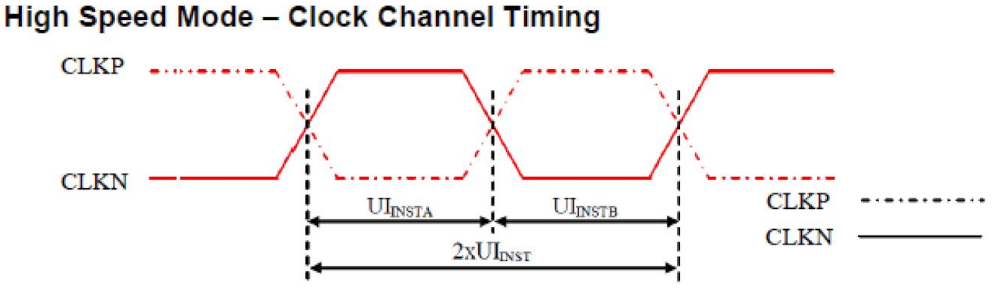
Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	IOVCC		1.75	1.8	3.3	V
Power Supply Voltage	VDD(+5V)		4.5	5.0	6	V
Power Supply Voltage	VDD(-5V)		-6	-5.0	-4.5	
Low Level Input Voltage	V_{IL}		GND		0.3*IOVCC	V
High Level Input Voltage	V_{IH}		0.7*IOVCC		IOVCC	V
Operating Temperature	TOP	Absolute Max	-20		+70	℃
Storage Temperature	TST	Absolute Max	-30		+80	℃

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	AV	70	80		deg
View Angles Bottom	AV	70	80		deg
View Angles Right	AH	70	80		deg
View Angles Left	AH	70	80		deg
Response Time	Tr +Tf		25	35	ms
LED Forward Current	If	18	20	22	mA
LED Forward Voltage	Vf		12.8		V
Contrast Ratio	CR	600	800		--
LCM Luminance	Lv	280	350		cd/m^2

7 Timing Characteristics

7.1 Mipi Data to clock Timing Definition-High Speed Mode



Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

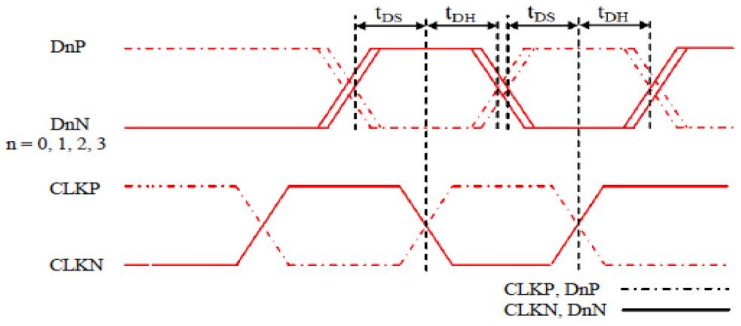
DSI Clock Channel Timing

Notes:

1. UI=UIINSTA=UIINSTB
2. Define the minimum value of 24 UI per Pixel, see Table below

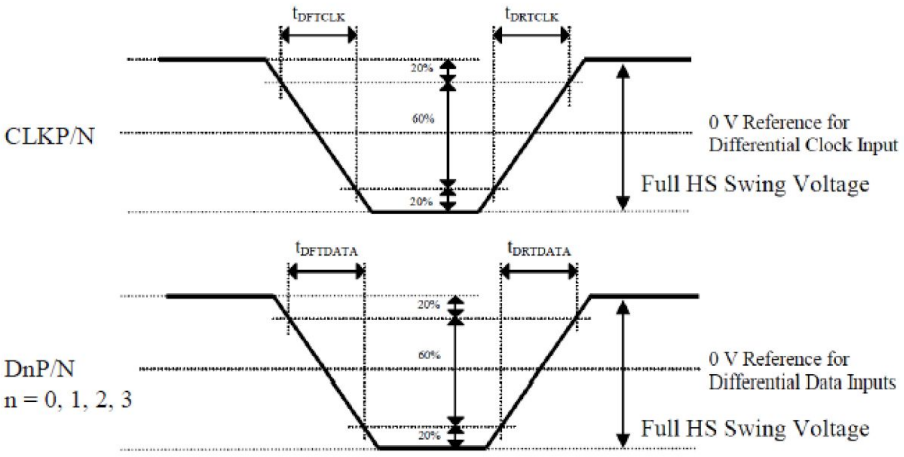
Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

Limited Clock Channel Speed



Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rising and Falling Timings



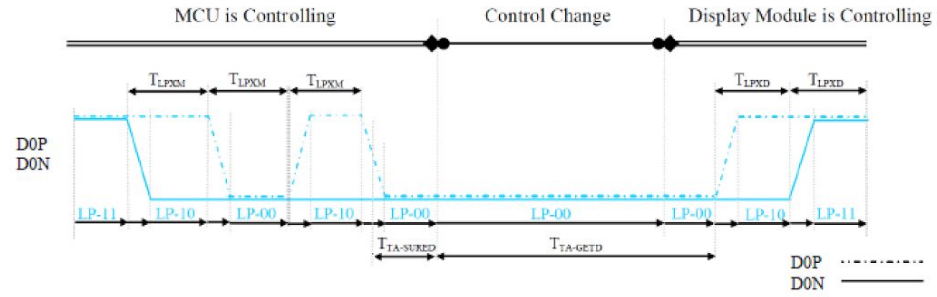
Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

7.2 Mipi Data to clock Timing Definition-Low Speed Mode

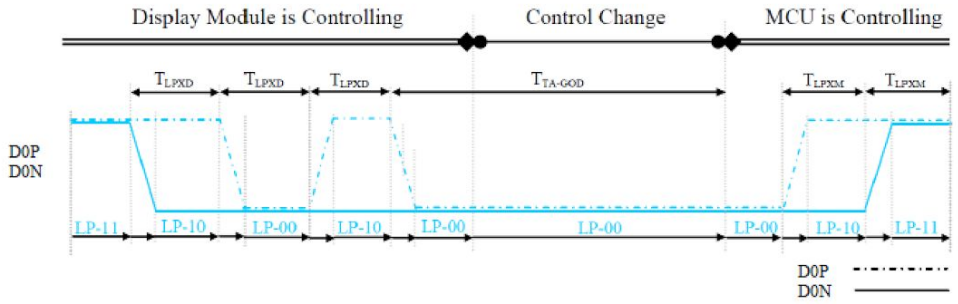
Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.



BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.



BTA from the Display Module to the MCU

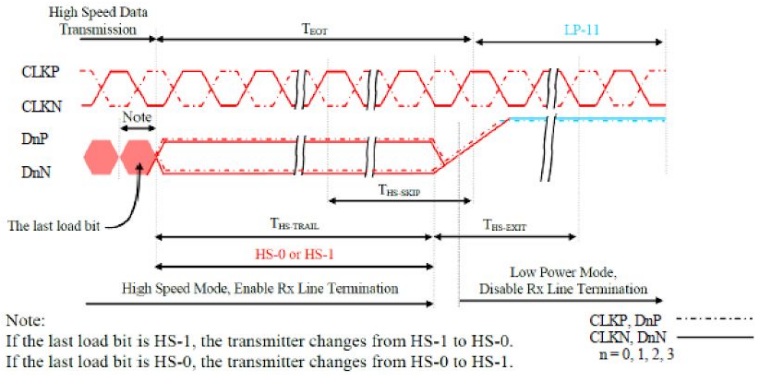
Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

Data Lanes from High Speed Mode to Low Power Mode



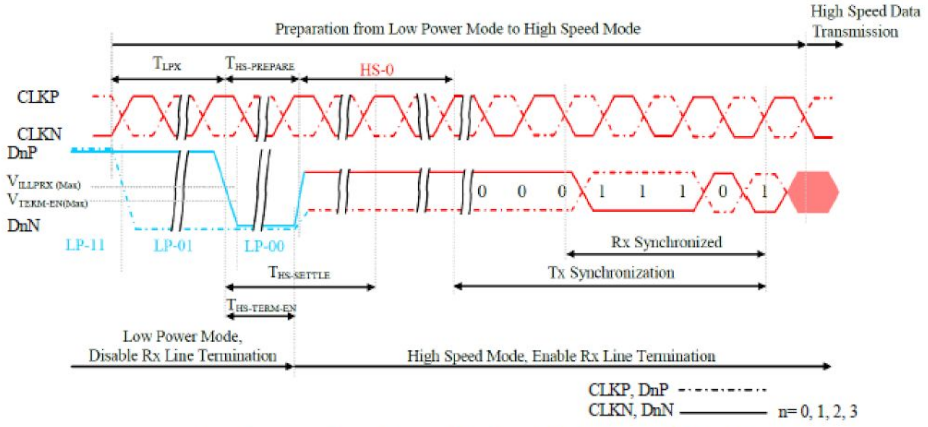
Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Data Lanes - High Speed Mode to Low Power Mode Timings

Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

Data Lanes from Low Power Mode to High Speed Mode

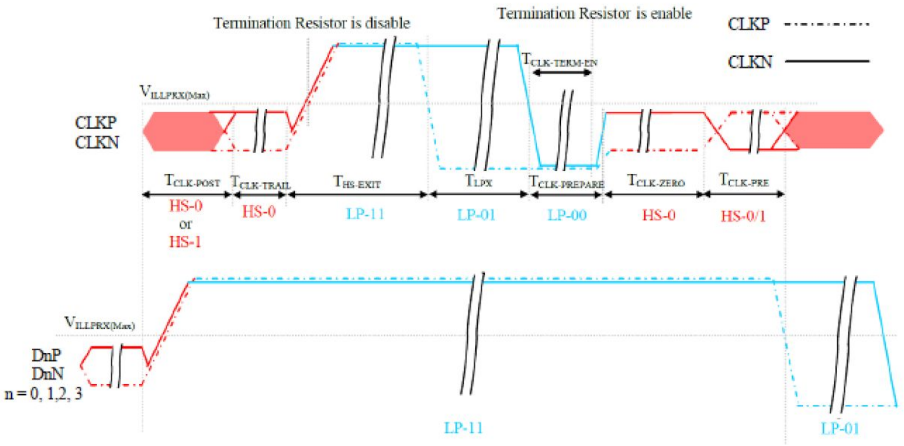


Data Lanes - Low Power Mode to High Speed Mode Timings

Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

DSI Clock Burst – High Speed Mode to/from Low Power Mode

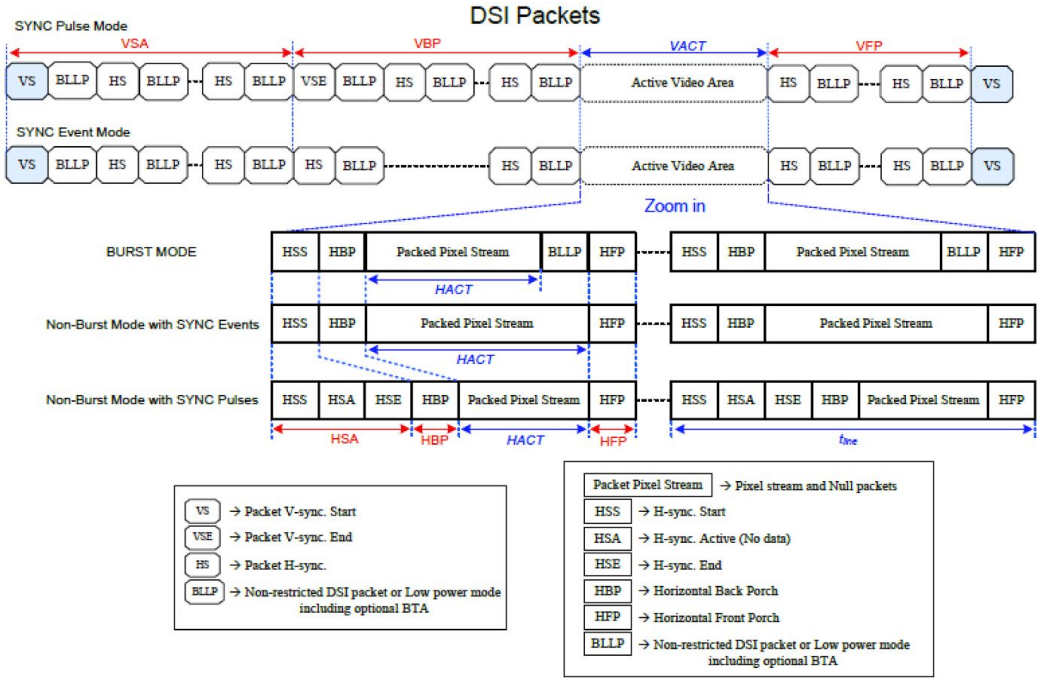


Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Clock Lanes - High Speed Mode to/from Low Power Mode Timings

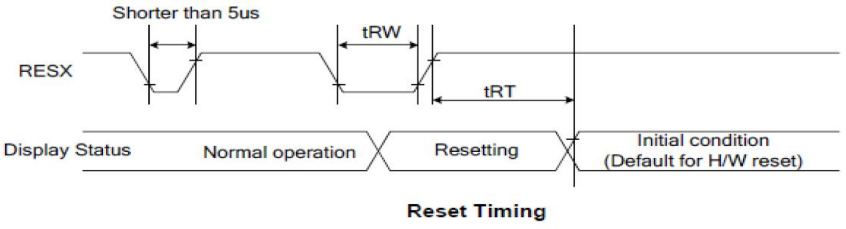
Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

7.3 Timing For DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR_{bps}	200		Note 5	Line

7.4 Reset Timing



Reset Timing

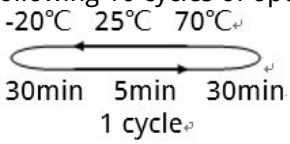
Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

8 CTP Specification

8.1 Elective Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCI		2.8		3.3	V
I/O Digital Voltage	VDDIO		1.8		3.3	V
Input Current	IDD					mA
Low Level Input Voltage	V_{IL}		-0.3		$0.25V_{DDIO}$	V
High Level Input Voltage	V_{IH}		$0.75V_{DDIO}$		V_{DDIO}+0.3	V
Low Level Output Voltage	V_{OL}		-		$0.15V_{DDIO}$	V
High Level Output Voltage	V_{OH}		$0.85V_{DDIO}$		-	V
Operating Temperature	TOP	Absolute Max	-20		+70	℃
Storage Temperature	TST	Absolute Max	-30		+80	℃

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.
Note3: Test performed on product itself, not inside a container

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq