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CUSTOMER APPROVAL SHEET

Company Name

MODEL H120BLN02.0

CUSTOMER Title :

APPROVED Name :

- APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)
- APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)
- APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)
- CUSTOMER REMARK :

1 Li-Hsin Rd. 2. Science-Based Industrial Park
Hsinchu 300, Taiwan, R.O.C.
Tel: +886-3-500-8899
Fax: +886-3-577-2730

Product Specification

1.20" AMOLED

MODEL NAME: H120BLN02.0

AUO Product P/N: 95.01H79.000

< >Preliminary Specification

< ◆ >Final Specification

Note: The content of this specification is subject to change.

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Record of Revision

Version	Revise Date	Page	Content
1	2017/5/10	1-22	First edition

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A. General Specification

1. Physical Specifications

	Item	Description	Remark
1	Screen Size (inch)	1.20"	
2	Display Mode	AMOLED	
3	Display Resolution	390x390	
4	Active Area (mm*mm)	30.42 (H)×30.42(V)	
5	Frame rate (normal mode)	45 (Hz)	
6	Pixel Configuration	Hyper R.G.B	
7	Display Color (M)	16.7	
8	Brightness (nits)	350	
9	Interface	MIPI	CMD Mode
10	Driver IC	W022	
11	Outline Dimension (mm*mm*mm)	33.22 (H) × 33.75 (V) × 0.656(T)	cell+foam

2. FPC Pin Assignment

Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interfac

FPCA recommended connector: AXG220144

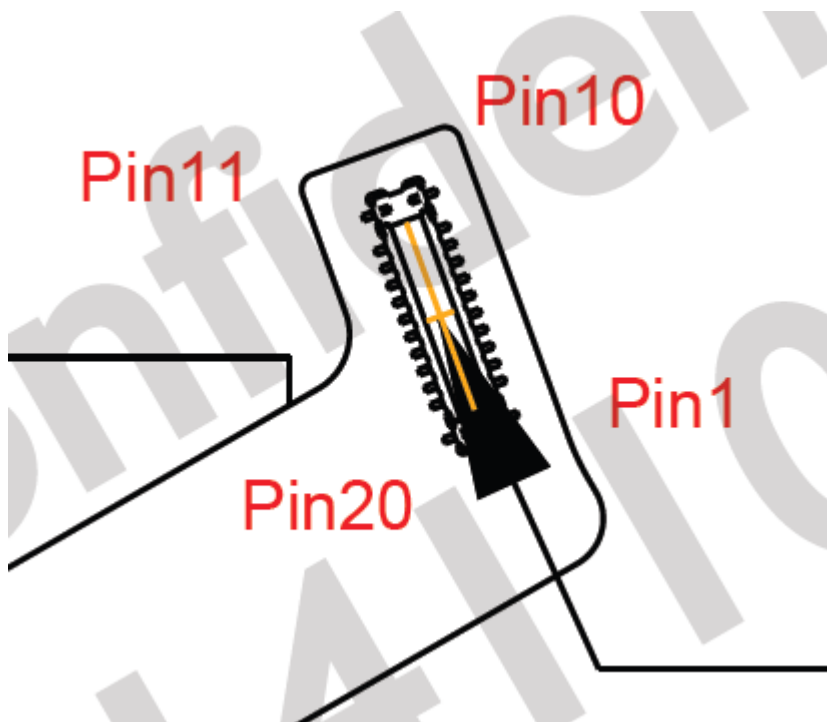
Main board recommended connector: AXG120144

FPC	Pin_name	I/O	Description
1	ELVSS	P	AMOLED negative power supply (Power IC needs to follow AUO's suggestion)
2	ELVSS	P	AMOLED negative power supply (Power IC needs to follow AUO's suggestion)
3	ELVSS	P	AMOLED negative power supply (Power IC needs to follow AUO's suggestion)
4	VCI	P	Driver analog power supply
5	VDDIO	P	Power supply for Interface system excep MIPI interface
6	GND	P	Ground
7	TE	O	Tearing effect output pin to synchronize MCU to frame writing.
8	NC	-	No Connection
9	RESX	I	Device reset signal (0 : Enable ; 1: Disable)
10	SWIRE	O	SWIRE signal for PWR IC control
11	GND	P	Ground
12	DSI_CLKP	I	MIPI positive clock signal
13	DSI_CLKN	I	MIPI negative clock signal
14	GND	P	Ground
15	DSI_D0P	I/O	MIPI positive data signal
16	DSI_D0N	I/O	MIPI negative data signal

17	GND	P	Ground
18	ELVDD	P	AMOLED positive power supply (Power IC needs to follow AUO's suggestion)
19	ELVDD	P	AMOLED positive power supply (Power IC needs to follow AUO's suggestion)
20	ELVDD	P	AMOLED positive power supply (Power IC needs to follow AUO's suggestion)

Note1: I = input ; O = output ; P = Power ; I/O = input / Output; NC= No Connection

Note2: Pin assignment may be adjust according to Layout condition



3. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
Digital Power Supply	VDDIO	-0.3	5.5	V	
Analog Power Supply	VCI	-0.3	5.5	V	
ELVDD power Supply	ELVDD	-	5.0	V	
ELVSS power Supply	ELVSS	-5.0	-	V	

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently.

B. DC Characteristics

1. Display DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark	
Digital Power Supply	VDDIO	1.65	1.8	1.95	V	Note1	
Battery power Voltage	VCI	3.27	3.3	3.33	V	Note1	
ELVDD power Supply	ELVDD	3.27	3.3	3.33	V	Note1	
ELVSS power Supply	ELVSS	-3.27	-3.3	-3.33	V	Note1	
Input Signal Voltage	H Level	V_{IH}	0.8* VDDIO	-	VDDIO	V	Note1
	L Level	V_{IL}	0	-	0.2* VDDIO	V	
Output Signal Voltage	H Level	V_{OH}	0.8* VDDIO	-	VDDIO	V	Note1
	L Level	V_{OL}	0	-	0.2* VDDIO	V	Note1

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

2. Display Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	
Panel Power	P_{OLED}	ELVDD:3.3V	--	--	117	mW	Note1	
	I_{OLED}	ELVSS:-3.3V	--	--	17.5	mA	Note1	
IC	Normal	P_{VCI}	--	--	5.7	6.9	mW	Note2
		I_{VCI}	--	--	1.7	2.1	mA	Note2
		P_{VDDIO}	--	--	2.2	2.7	mW	Note2
		I_{VDDIO}	--	--	1.2	1.5	mA	Note2
	Idle	P_{VCI}	--	--	3.8	4.6	mW	Note3
		I_{VCI}	--	--	1.2	1.4	mA	Note3
		P_{VDDIO}	--	--	1.2	1.4	mW	Note3
		I_{VDDIO}	--	--	0.7	0.8	mA	Note3
	Sleep	P_{VCI}	VCI : 3.3V	--	--	0.17	mW	
		I_{VCI}	VCI : 3.3V	--	--	0.05	mA	
		P_{VDDIO}	VDDIO :1.8V	--	--	0.33	mW	
		I_{VDDIO}	VDDIO :1.8V	--	--	0.18	mA	

	Deep Standby	P_{VCI}	VCI : 3.3V	--	--	0.14	mW	Note4
		I_{VCI}		--	--	0.05	mA	Note4
		P_{VDDIO}	VDDIO :1.8V	--	--	0.09	mW	Note4
		I_{VDDIO}		--	--	0.05	mA	Note4

Note 1: Based on L255 (350nits) full white pattern

Note 2: Based on black pattern. MIPI-DSI frame rate 45Hz command mode.

Note 3: Based on black pattern. MIPI-DSI frame rate 15Hz command mode.

Note 4: MIPI has to enter ULP mode when IC enter deep standby mode.

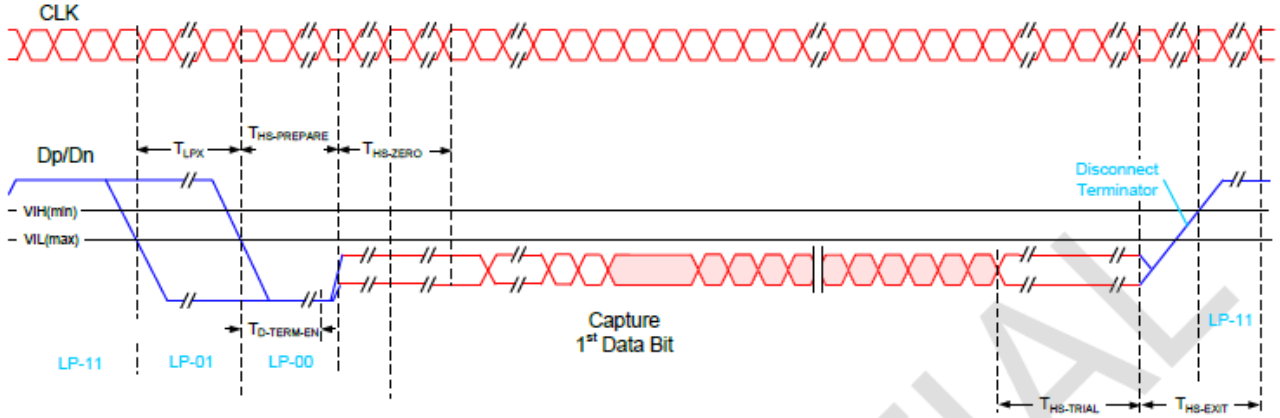
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C. AC Characteristics

1. MIPI Interface Characteristics

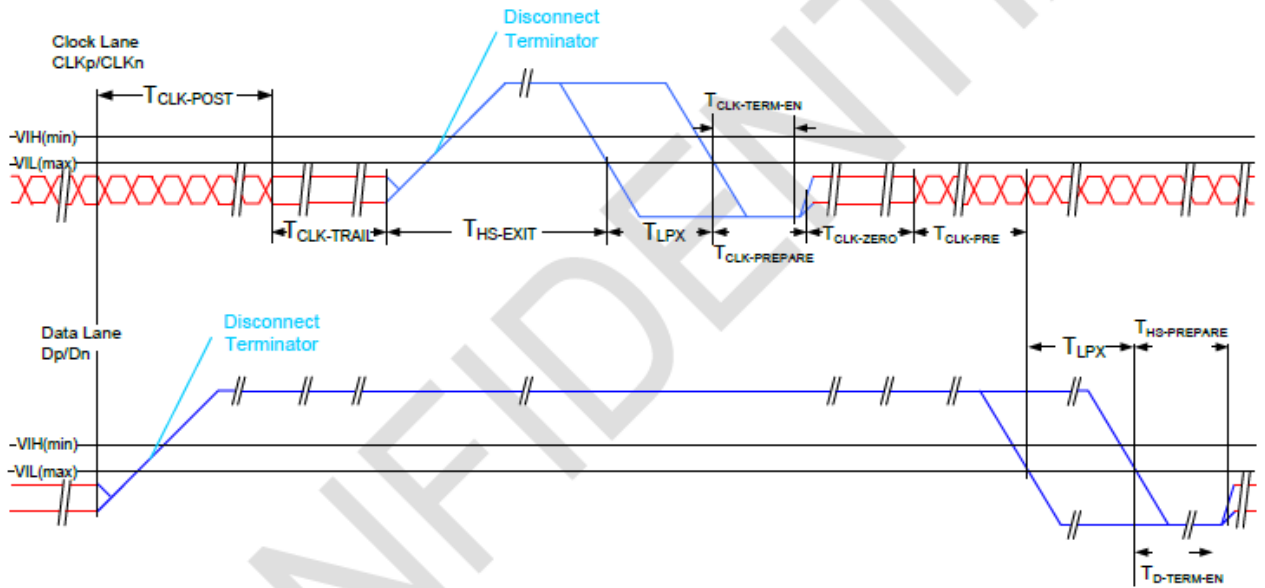
HS Data Transmission Burst

HS Data Transmission Burst



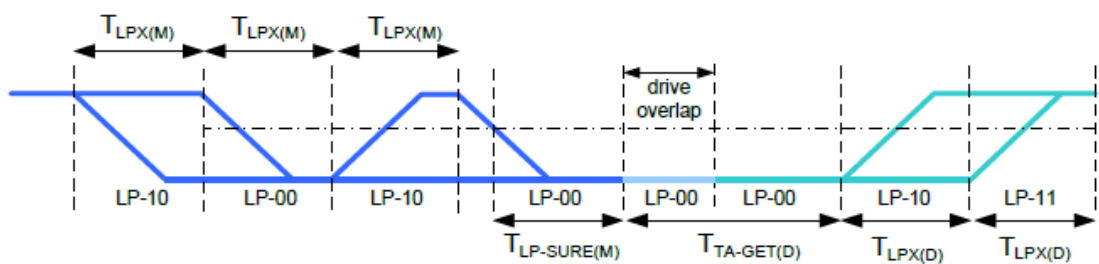
HS clock transmission

HS clock transmission



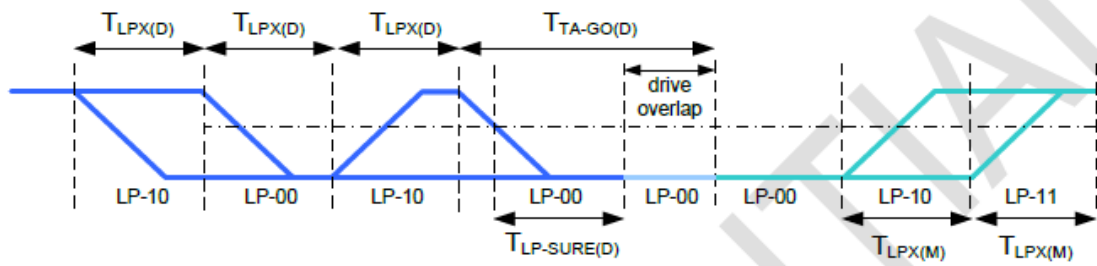
Turnaround Procedure

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing

Bus turnaround (BAT) from MPU to display module timing



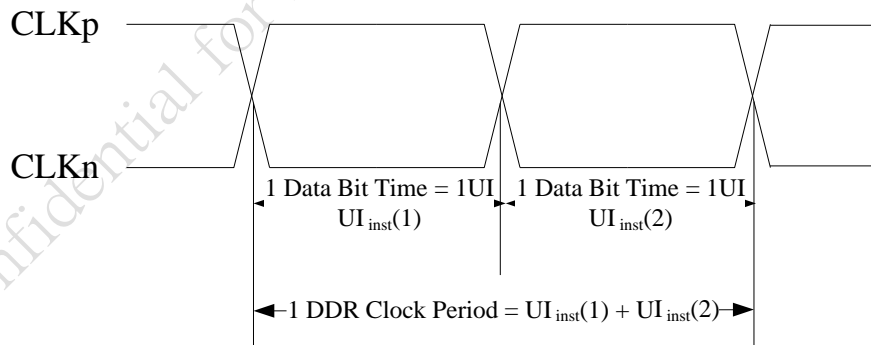
Bus turnaround (BAT) from display module to MPU timing

Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	$60ns + 52*UI$			Ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			Ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			Ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	Ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	Ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			Ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns + $4*UI$	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40ns + 4*UI$		$85 ns + 6*UI$	ns

$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145ns + 10*UI$			Ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$60ns + 4*UI$			Ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	Ns
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	Ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	Ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		Ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		Ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	Ns

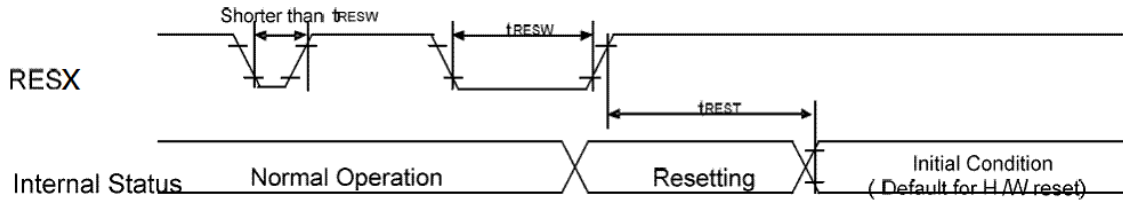
DDR Clock Definition



Clock Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI _{inst}	2		12.5	Ns

2. Display RESET Timing Characteristics

Reset input timing



Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

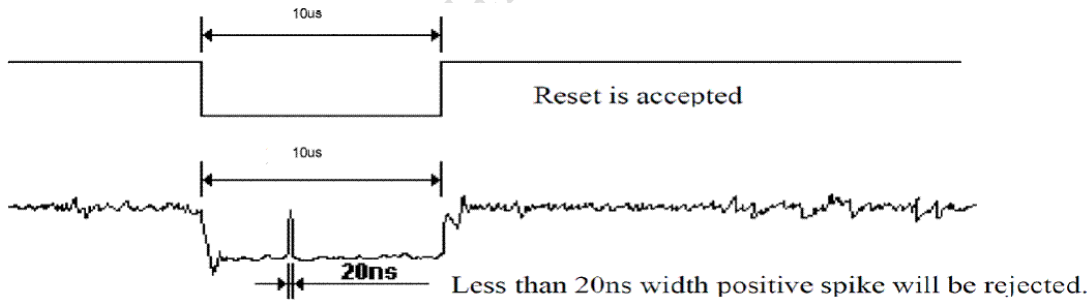
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than $5\mu s$	Invalid Reset
Longer than $10\mu s$	Valid Reset
Between $5\mu s$ and $10\mu s$	Reset Initialigation Precedure

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

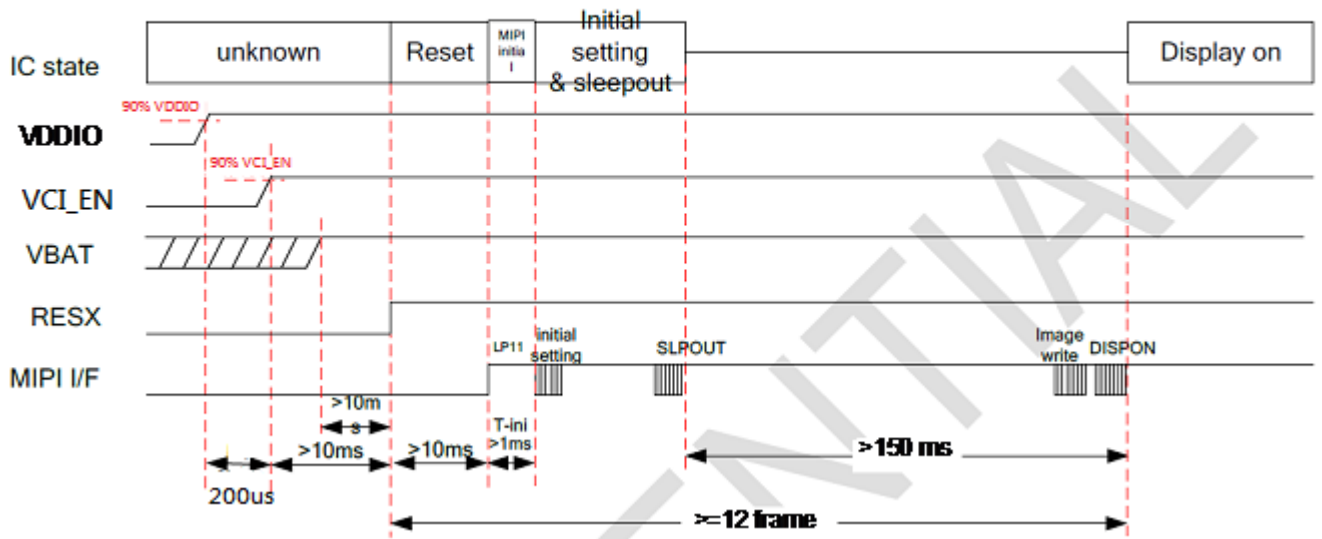


Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Operating Sequence

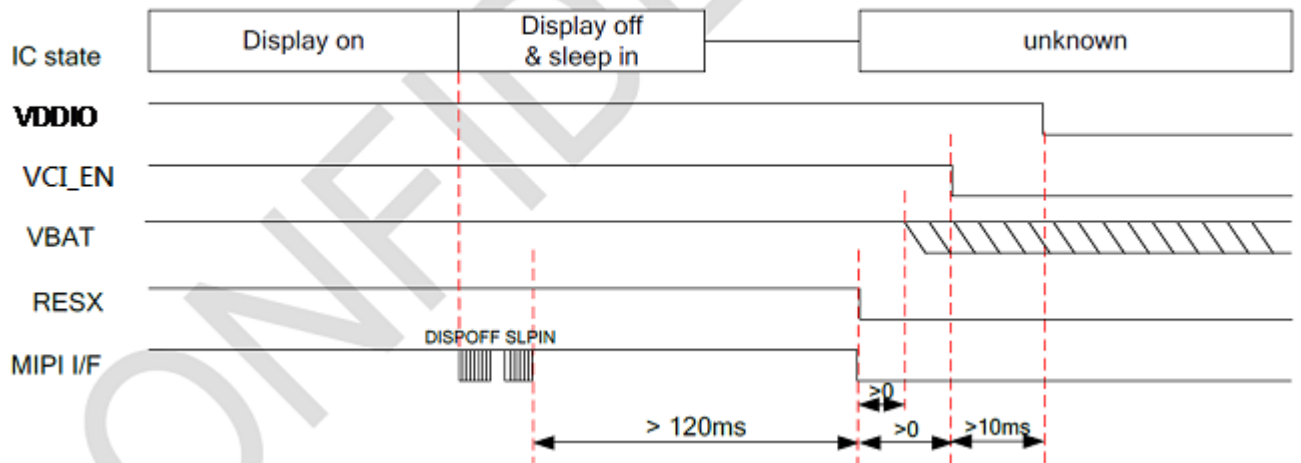
Power on sequence

Power On sequence

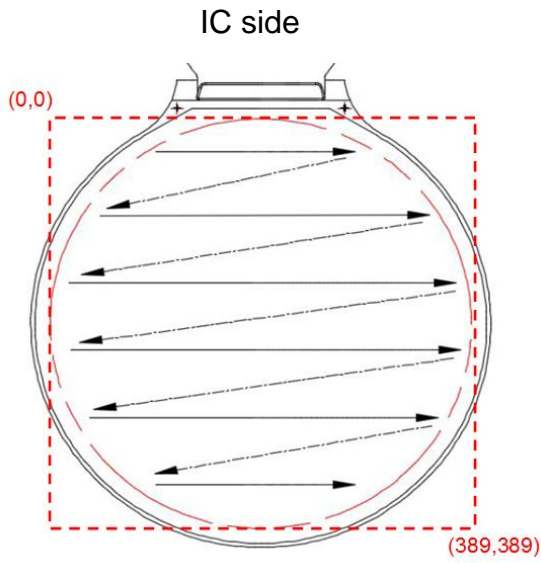


Power off sequence

Power Off sequence



D. Display Scan Direction & Coordinate



Panel Start Point = $(0, 0)$

Panel End Point = $(389, 389)$

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E. Optical Specifications

Item	Abbr.	Min.	Typ.	Max.	Unit	Remark	
Optical Characteristic	Brightness	315	350	--	nits	Note 3	
Contrast ratio	@25deg	10000	--	--		Note 4	
Brightness Uniformity	350nits	85	--	--		Note 5	
Viewing angle CR>1600	Top	80°	--	--	deg	Note 6	
	Bottom	80°	--	--	deg		
	Left	80°	--	--	deg		
	Right	80°	--	--	deg		
Color	White	CIE1931 x	0.28	0.30	0.32	Note 7	
	White	CIE1931 y	0.29	0.31	0.33		
	Red	CIE1931 x	0.640	0.670	0.700		
	Red	CIE1931 y	0.300	0.330	0.360		
	Green	CIE1931 x	0.186	0.236	0.286		
	Green	CIE1931 y	0.661	0.711	0.761		
	Blue	CIE1931 x	0.090	0.130	0.170		
	Blue	CIE1931 y	0.025	0.065	0.105		
NTSC	CIE x , y	82	100	--	%		
Life time	LT95	25°C	150	--	hrs	Note 8	
Crosstalk	L128△CT	Vertical	--	--	110	%	Note 9
Flicker			--	--	-30	db	Note 10
Gamma	γ	1.9	2.2	2.5		Note 11	

Note 1: Ambient temperature =25 °C±2 °C, measured by CA-310

Note 2: To be measured in the dark room.

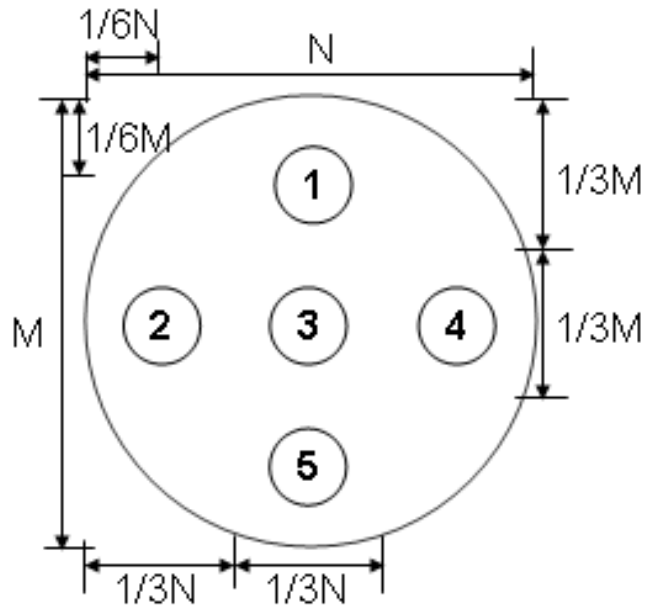
Note 3: The brightness measurement shall be done at the center of the display with a full white image.

Note 4: Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at "White" state}}{\text{Photo detector output when OLED is at "Black"}}$$

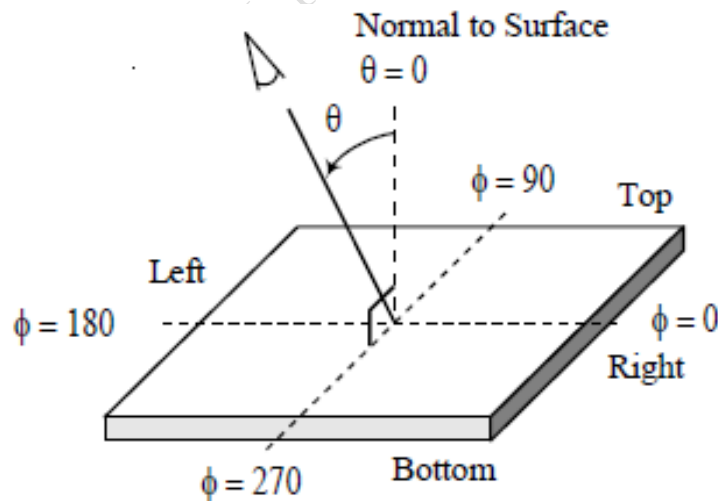
Note 5: Uniformity. Refer to figure as below



- $\Delta B_p = B_p (\text{Min.}) / B_p (\text{Max.}) \times 100 (\%)$
- $B_p (\text{Max.}) =$ Maximum brightness in 5 measured spots
- $B_p (\text{Min.}) =$ Minimum brightness in 5 measured spots.

Note 6: Definition of viewing angle :

The optical performance is specified as the driver IC located at $\approx 270^\circ$



Note 7: The color chromaticity should be based on sample performance because new OLED material should be verified later.

Note 8: Time to 95% Luminance

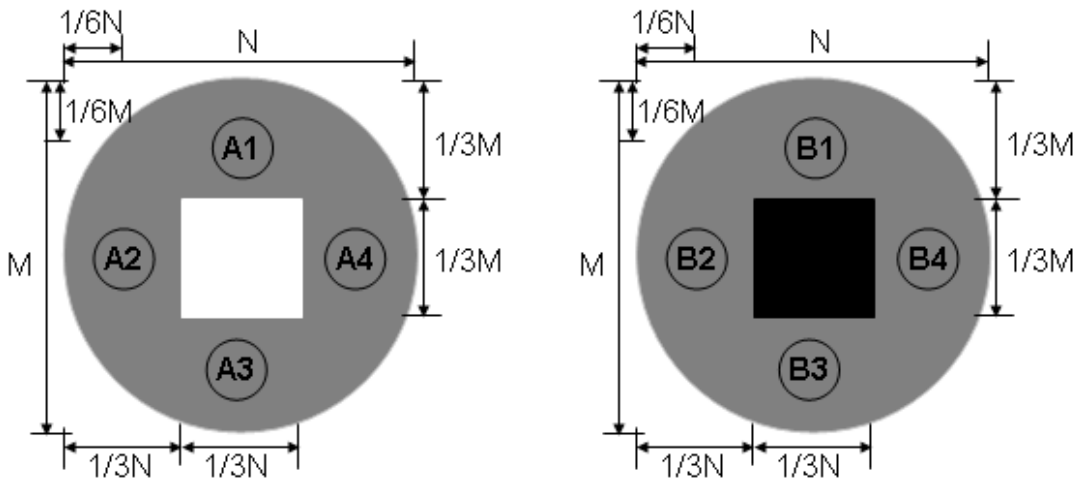
To measure the burn-in effect, a test pattern with white background applied to the AMOLED display at 100% loading

Note 9: Cross-talk

- There should be no visible cross-talk in normal direction of the display when the two "Cross-talk Test Patterns " below are loaded.
- Measurement equipment: DMS-803 or similar equipments
- The point should be marked is, the background of Cross-talk Test Pattern-"gray " are defined as middle gray scale . For example, RGB 24bit "gray" defined as below:

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

- $\Delta B_{pn} = B_{pn}(\text{gray}) / B_{pn}(\text{white})$
Which n means the dot No. In the Cross-talk Test Pattern ;
B_{pn} (gray) means the brightness of the No.n spots in Cross-talk Test Pattern A and B;
B_{pn} (white) means the brightness of the No.n spots in Full white Test Pattern;
- $\Delta B_p(\text{Max.}) = \text{Maximum value in A1~A4 and B1~B4.}$
- $\Delta B_p(\text{Min.}) = \text{Minimum value in A1~A4 and pB1~B4.}$
- $\Delta CT = \Delta B_p(\text{Max.}) / \Delta B_p(\text{Min.}).$
- ΔCT must be less than 1.10



Note 10: Flicker

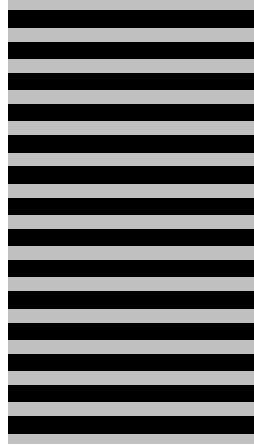
The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flicker = 20 \log_{10} \left(2 \frac{f_{FFTC}(n)}{f_{FFTC}(0)} \right) + FS(Hz) \quad (\text{dB})$$

where f_{FFTC}(n) is the nth FFT coefficient, and f_{FFTC}(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

The flicker level shall be measured with the test pattern in below.

The gray levels of test pattern is 128.



Note 11 : Gamma spec. is based on Gray level 255, 250, 244, 240, 232, 224, 206, 192, 160, 128, 95, 63, 47 & 31.

F. Reliability Test Items

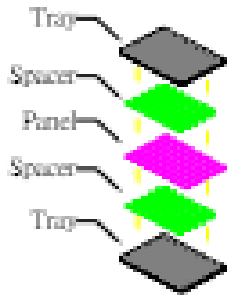
Category	No.	Test items	Conditions	Amount	Remark
Reliability (Environment)	1	High Temp. Operation	Ta= 60°C 168 hrs	5 pcs	
	2	High Temp. Storage	Ta= 70 °C 168 hrs	5 pcs	Non-operation
	3	Low Temp. Operation	Ta= -20 °C 168 hrs	5 pcs	
	4	Low Temp. Storage	Ta= -30 °C 168 hrs	5 pcs	Non-operation
	5	High Temp./Humi. Operation	Ta= 60 °C. 90% RH 168 hrs	5 pcs	
	6	Thermal Shock	-40 °C ~70 °C, Dwell for 30 min. 100 cycles.	5 pcs	Non-operation
	7	ESD	Contact mode	± 4KV; discharge time:10; Interval:1sec; Criteria: B	5 pcs
	Air mode		± 8KV; discharge time:10;Interval:Discharge; Criteria: B	5 pcs	

Judge Criteria: No functional defect.

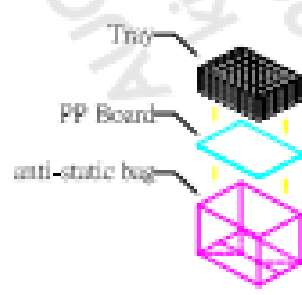
Drop test

Test items	Conditions	Remark
Drop Test	Drop the packing from 76cm height, 6 surfaces, 3 edges and 1 corner.	Box

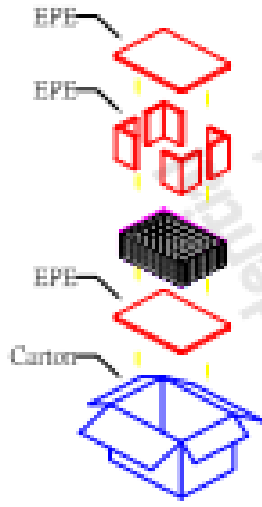
G. Packing



1 tray for 30 pcs Panels

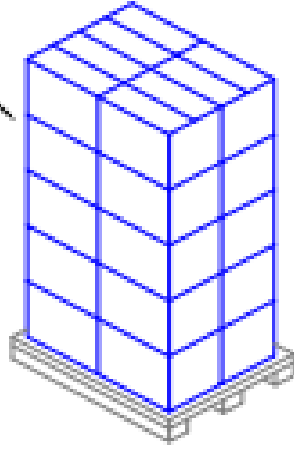


1 set for 20+1 pcs trays
=600 pcs panels

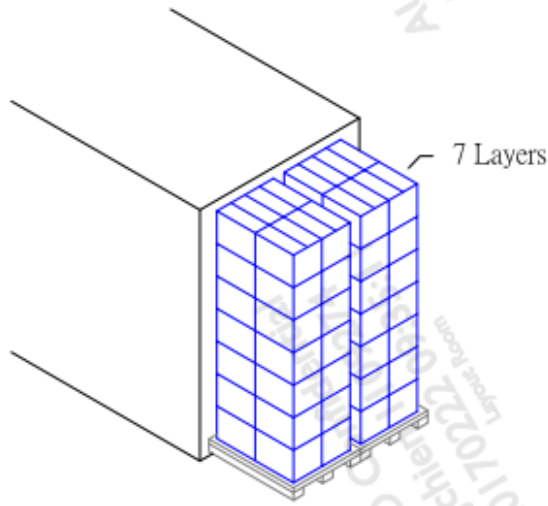


5 layers for ASRS
=30 Cartons
=12000 pcs TP

Carton DIM :
540*400*265 mm

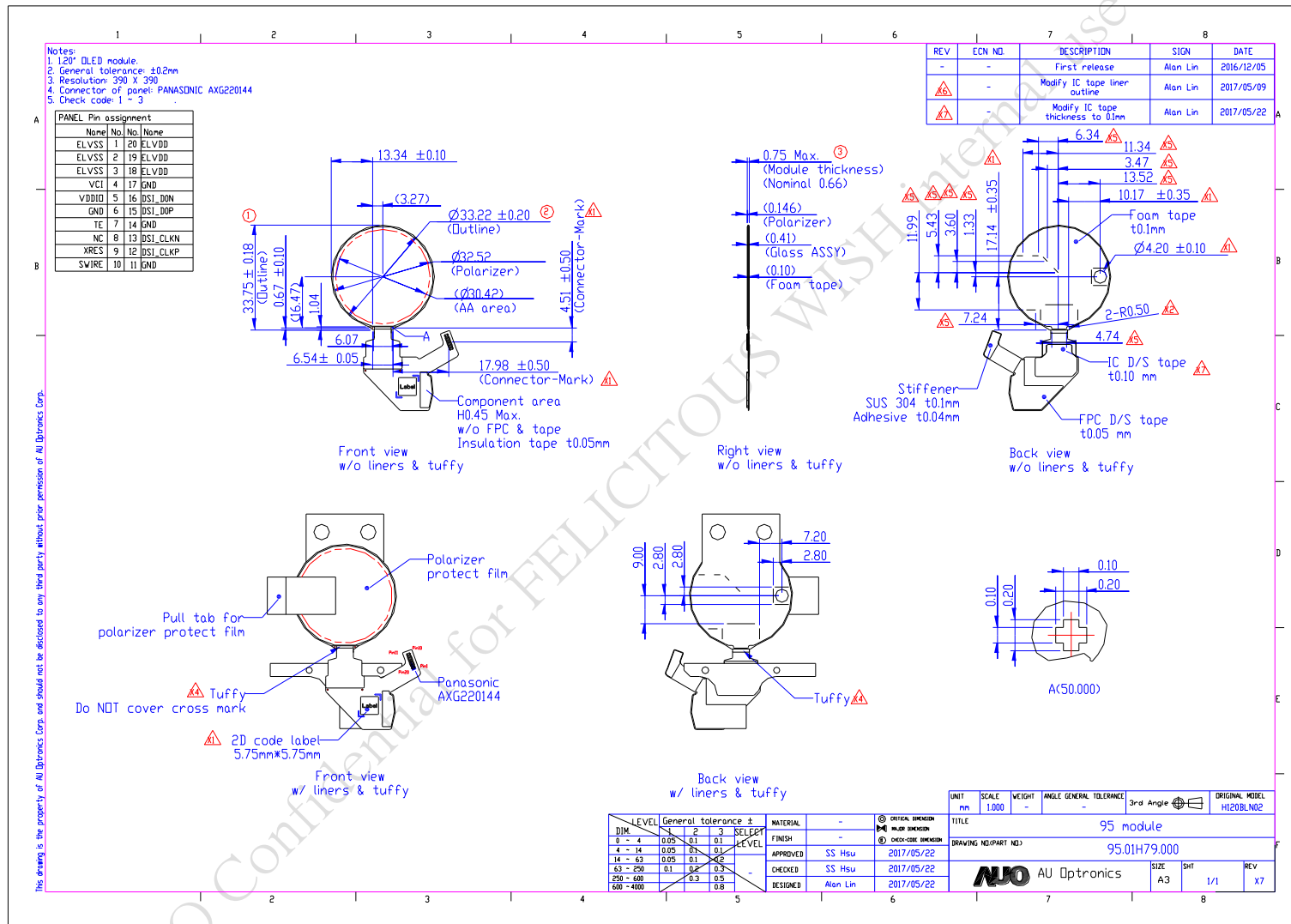


Pallet DIM :
1150*840*132 mm



For 20' Container : 12 Pallets=336 cartons=201600 pcs Panels
For 40' Container : 28 Pallets=784 cartons=470400 pcs Panels

H. Outline Demension



I. Precaution

Please pay attention to the following items when you use the OLED Modules(Panel):

1. Do not twist or bend the module(panel) and prevent the unsuitable external force for display during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module(panel) within the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module(panel).
5. Less EMI: it will be more safety and less noise.
6. Please operate module(panel) in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Please be sure to turn-off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dew drop may lead to destruction. Please wipe off any moisture before using module(panel).
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module(panel) to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with AMOLED display module(panel).
15. Static electricity will damage the module(panel), please do not touch the module(panel) without any grounded device.
16. Please avoid any static electricity damage (ESD) during producing and operating.
17. Do not disassemble and reassemble the module(panel) by self.
18. Be careful do not touch the rear side directly.
19. No strong vibration or shock. It will cause module(panel) broken.
20. Storage the modules(panel) in suitable environment with regular packing.
21. Be careful of injury from a broken display module(panel).
22. Please avoid the pressure adding to the surface (front or rear side) of modules(panel), because it will cause the display non-uniformity or other function issue.
23. Please check there is no mechanical interference between AMOLED display module (panel) and customer's mechanical.
24. UV light would damage OLED material. To avoid damage, UV light must shine directly onto the front side of the OLED panel, any light to the side/back of the panel must be avoided, and black tray must be used to avoid any UV reflection via tray to the side/back of the OLED panel.