

DisplayModule



DM-TFT55-419

5.5" 1440 × 2560 HIGH RESOLUTION
TFT LCD –MIPI

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1 Revision History

Date	Changes
2020-06-24	First release

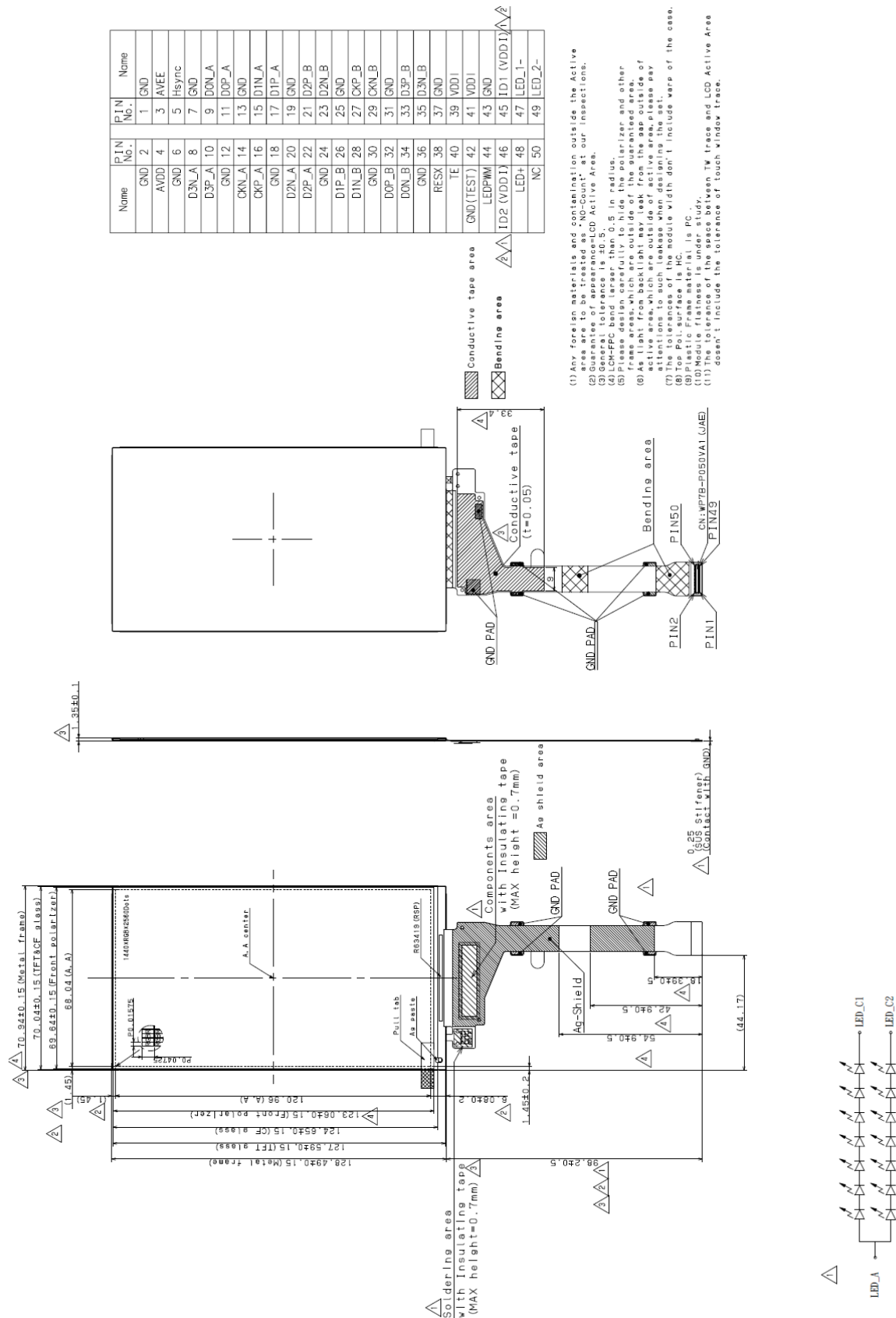
2 Main Features

Item	Specification	Unit
Diagonal Size	5.5	inch
Pixel arrangement	RGB vertical stripe	-
Display mode	Normally Black	-
Display Colors	16.7M	Colors
Resolution	1440 x 2560	pixel
LCD Interface	MIPI	-
Active Area	68.04 x 120.96	mm
Panel Dimension	70.94 x 128.49 x 1.35	mm
Pixel Pitch	0.01575 x 0.04725	mm
Liquid Crystal Mode	New Mode2	
Weight	TBD	g

3 Pin Description

Pin No.	Symbol	Function Description
1	GND	Ground
2	GND	Ground
3	VSN	Power supply for analog(-5.75V)
4	VSP	Power supply for analog(+5.75V)
5	HSYNC	Horizontal Synchronizing signal
6	GND	Ground
7	GND	Ground
8	DSI_A_D3-	IPI DSI(-) of Port A
9	DSI_A_D0-	IPI DSI(-) of Port A
10	DSI_A_D3+	IPI DSI(+) of Port A
11	DSI_A_D0+	IPI DSI(+) of Port A
12	GND	Ground
13	GND	Ground
14	DSI_A_CLK-	MIPI DSI Clock (-) of PortA
15	DSI_A_D1-	MIPI DSI (-) of PortA
16	DSI_A_CLK+	MIPI DSI Clock (+) of PortA
17	DSI_A_D1+	MIPI DSI (+) of PortA
18	GND	Ground
19	GND	Ground
20	DSI_A_D2-	MIPI DSI (-) of PortA
21	DSI_B_D2+	MIPI DSI (+) of PortB
22	DSI_A_D2+	MIPI DSI (+) of PortA
23	DSI_B_D2-	MIPI DSI (-) of PortB
24	GND	Ground
25	GND	Ground
26	DSI_B_D1+	MIPI DSI (+) of PortB
27	DSI_B_CLK+	MIPI DSI Clock (+) of PortB
28	DSI_B_D1-	MIPI DSI (-) of PortB
29	DSI_B_CLK-	MIPI DSI Clock (-) of PortB
30	GND	Ground
31	GND	Ground
32	DSI_B_D0+	MIPI DSI (+) of PortB
33	DSI_B_D3+	MIPI DSI (+) of PortB
34	DSI_B_D0-	MIPI DSI (-) of PortB
35	DSI_B_D3-	MIPI DSI (-) of PortB
36	GND	Ground
37	GND	Ground
38	RESX	Device reset signal
39	IOVCC	Power supply for I/O
40	TE	Tearing signal output from driver IC
41	IOVCC	Power supply for I/O
42	GND	Ground
43	GND	Ground
44	LED_PWM	Control signal for brightness of LED backlight
45	ID1	ID1(connect to VDDI in FPC)
46	ID2	ID2(connect to VDDI in FPC)
47	LED1-	LED back light power negative1 (group1)
48	LED+	LED back light power positive
49	LED2-	LED back light power negative1 (group2)
50	NC	No connect

4 Mechanical Drawing



UNIT : mm

5 Optics & Electrical Characteristics

5.1 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles		70	80	-	°	
Response time	Rising	T _R +T _F	-	35	-	msec
	Falling					
Contrast Ratio	CO	900	1300	-	-	

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	VSP	-0.3	6.5	V	
Supply Voltage	VSN	-6.5	+0.3	V	
Digital interface Supply Voltage	Iovcc	-0.3	4.6	V	
Operating Temperature	T _{OP}	-20	60	°C	-
Storage Temperature	T _{STG}	-30	70	°C	-

Note:

5.3 DC Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Remark
Supply Voltage	VSP	5.6	5.75	5.9	V	-
Supply Voltage	VSN	-5.9	-5.75	-5.6	V	
Digital interface supply Voltage	Iovcc	1.7	1.8	1.9	V	-
Differential Input High Threshold Voltage	VIDTH	-	0	70	mV	
Differential Input Low Threshold Voltage	VIDTL	-70	0	-	mV	

Note :

5.4 LED Backlight Characteristics

The back-light system is edge-lighting type with 16 chips White LED

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Forward voltage	V _F	-	3.0	-	V	
Forward current	I _{led}		20	-	mA	Note1
Uniformity	AV _g	70	-	-	%	

Note1: per one piece of LED

6 MIPI DC/AC Characteristics

6.1 DC Characteristics

	Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVDD=1.65V~3.30V	-	-	70	2
	Differential input low threshold	VIDTL	mV	IOVDD=1.65V~3.30V	-70	-	-	2
	Single-ended input low voltage	VILHS	mV	IOVDD=1.65V~3.30V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVDD=1.65V~3.30V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVDD=1.65V~3.30V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVDD=1.65V~3.30V	-	100	-	
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVDD=1.65V~3.30V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVDD=1.65V~3.30V	880	-	1350	
	I/O leakage current	ILEAK	μA	V _{in} = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVDD=1.65V~3.30V	-50	-	50	
	Thevenin output high level	VOH	V	IOVDD=1.65V~3.30V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVDD=1.80V	110	-	-	
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVDD=1.65V~3.30V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVDD=1.65V~3.30V	450	-	-	

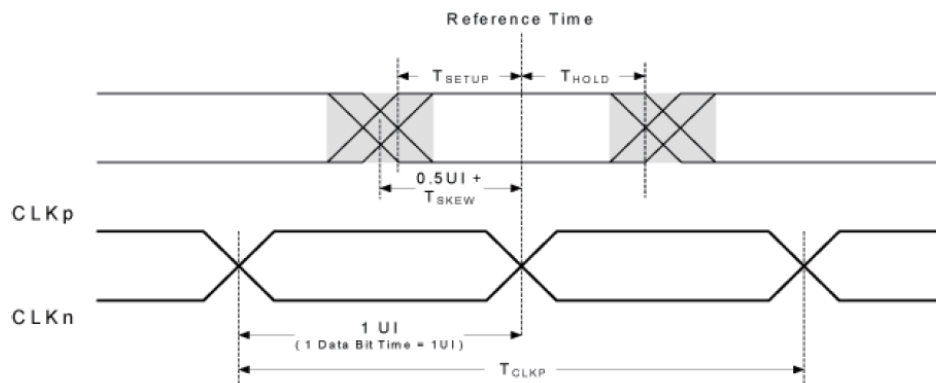
Notes: 1. $V_{CMRX}(DC) = (V_P + V_{DN})/2$

2. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

6.2 AC Characteristics

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~3.30V DPHYVCC=1.65V~3.30V	100	-	500	1
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~3.30V DPHYVCC=1.65V~3.30V	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~3.30V DPHYVCC=1.65V~3.30V DSI 2 lanes, 3 lanes,4lane	200	-	1000	1
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~3.30V DPHYVCC=1.65V~3.30V	0.15	-	-	3
		ns	IOVCC=1.65V~3.30V DPHYVCC=1.65V~3.30V	0.15	-	-	2,3
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~3.30V DPHYVCC=1.65V~3.30V	0.15	-	-	3
		ns	IOVCC=1.65V~3.30V DPHYVCC=1.65V~3.30V	0.15	-	-	2,3

- Notes:
1. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
 2. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
 3. tSETUP/tHOLD Time are measured without HS-TX Jitter.



6.3 MIPI Video Setting

Condition

- DSI 4Lane, 2port
- 850Mbps/Lane

Vertical Display Timing

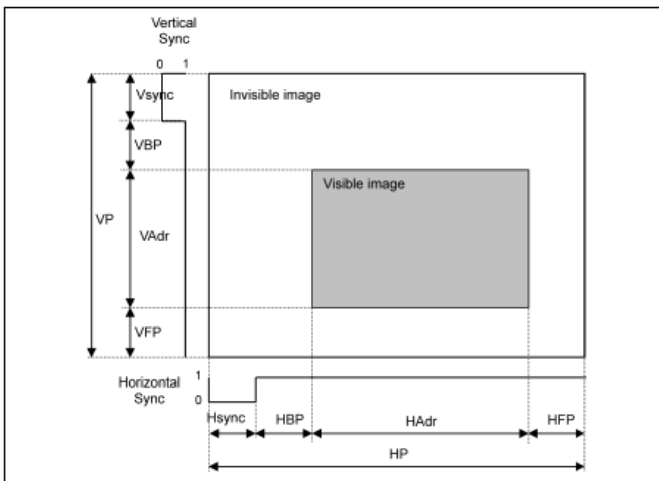
Item	Symbol	Condition	Unit	Value
Vertical cycle	VP		Line	2568
Vertical low pulse width	VS		Line	1
Vertical front porch	VFP		Line	4
Vertical back porch	VBP		Line	3
Vertical data start point	-	BP	Line	4
vertical blanking period	VBL	VFP+BP	Line	8
Vertical active area	Vadr		Line	2560

Horizontal Display Timing

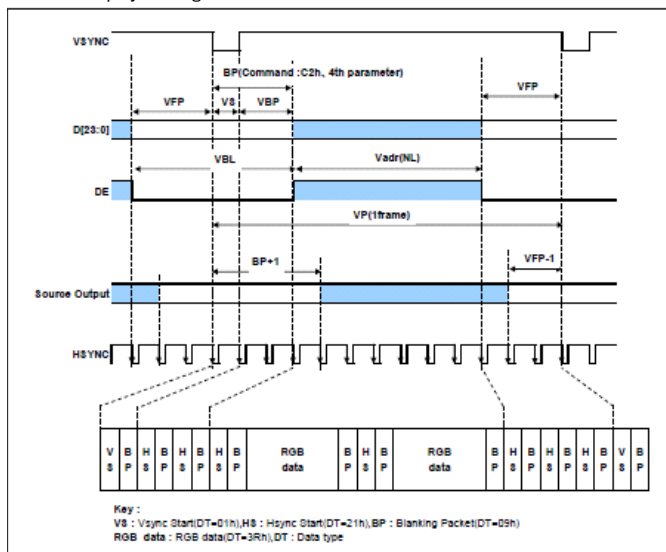
Item	Symbol	Condition	Unit	Value
Horizontal front porch	HFP		ByteClock	100
Horizontal data start point	-	HS+HBP	ByteClock	46
Horizontal active area	Hadr		Pixel	1440

Frame Frequency:60.3Hz

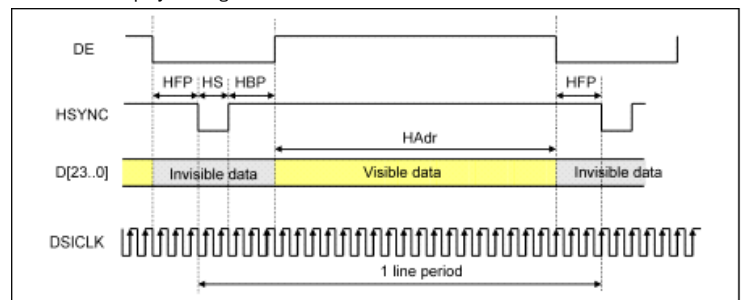
Display Timing



Vertical Display Timing



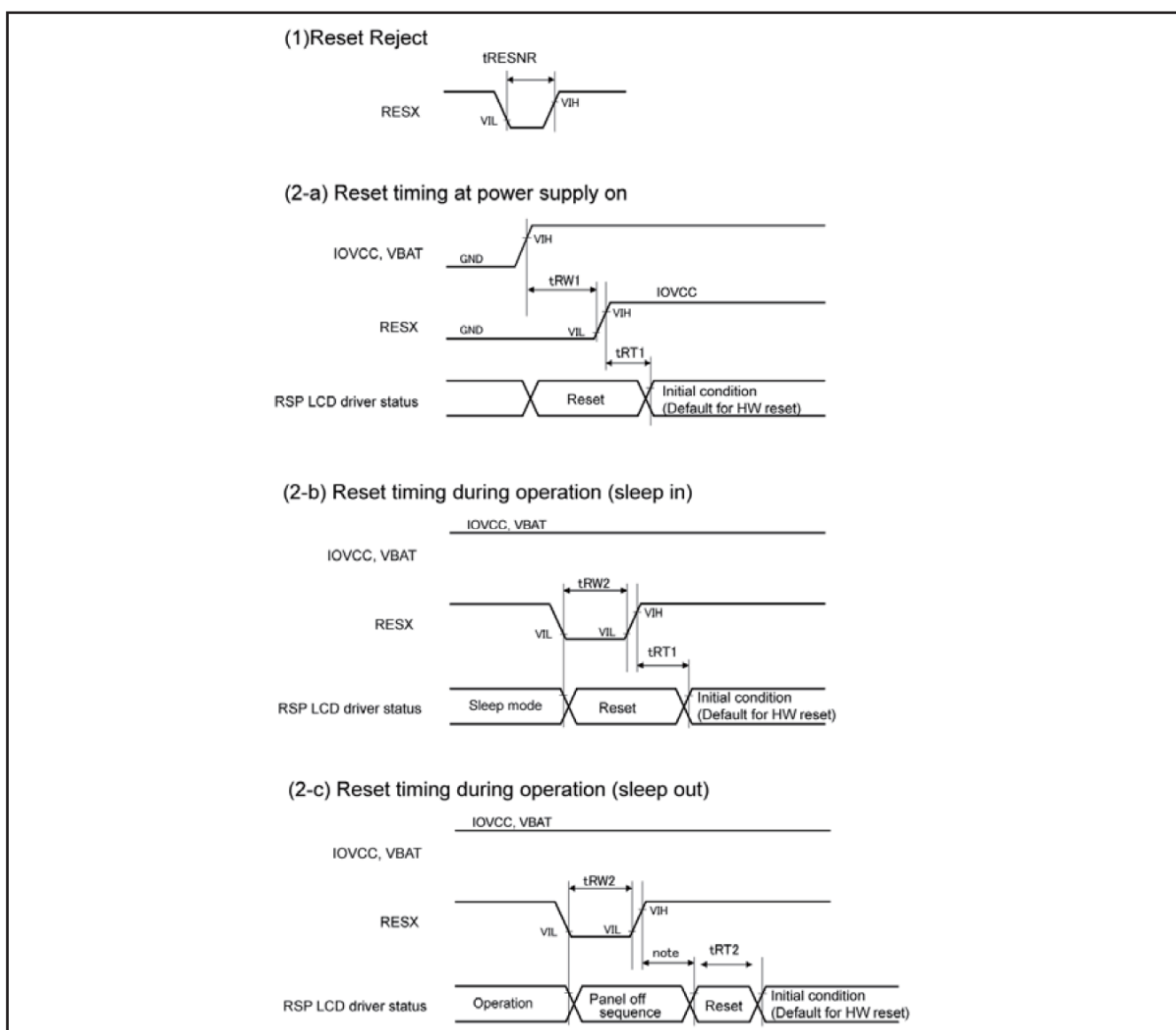
Horizontal Display Timing



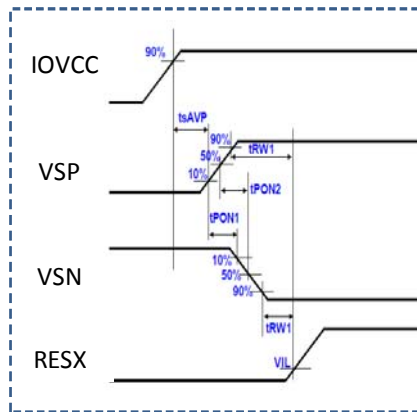
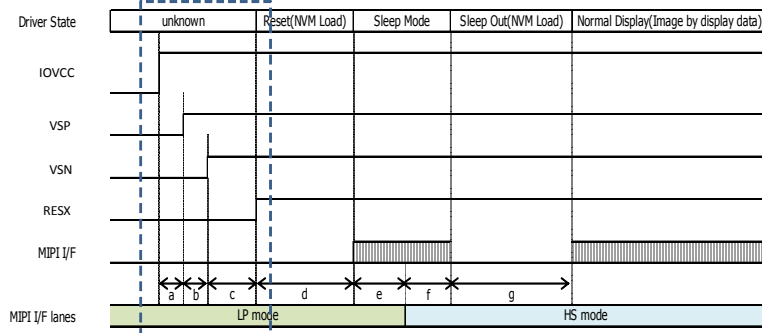
7 Initial Sequence

7.1 Reset Timing Characteristics

Item	Symbol	Unit	Test condition	Min.	Max.
Reset low-level width1	tRW1	us	Power supply on	1000	—
Reset low-level width2	tRW2	us	Operation	1000	—
Reset time (Sleep IN)	tRT1	ms	—	—	3
Reset time (Sleep OUT)	tRT2	ms	—	—	3
Noise reject width	tRESNR	us	—	—	1



7.2 Power on Sequence(Command mode)

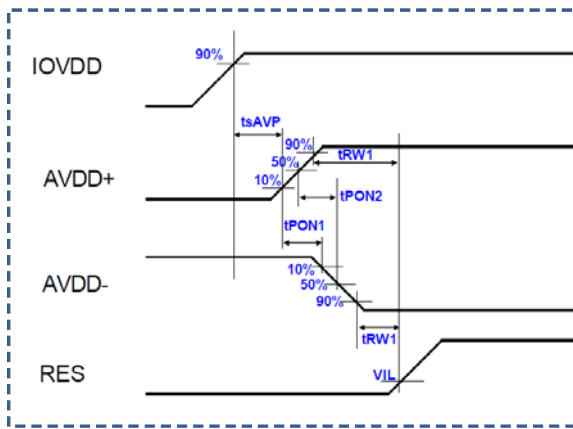
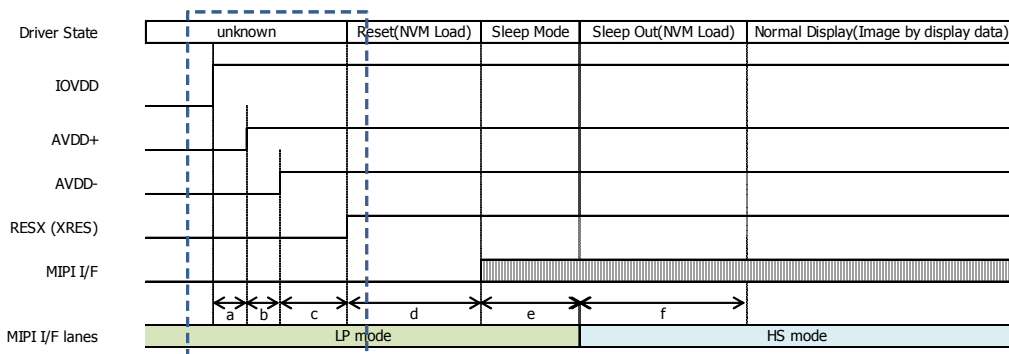


Item	Symbol	min
VSP to VSN delay time (10% to 10%)	tPON1	0ms
VSP to VSN delay time (50% to 50%)	tPON2	0ms
System power on to vsp ON time	tsAVP	1ms
Reset low-level width	tRW1	1ms

<Command mode>

Recommended Power On Sequence							tem	
Step	Address	Parameter	Data	DSI data type	Delay	Command		
1	Initial condition						RESX = L	
2	Power Supply IOVCC (Typ1.8V)						IOVCC ON	
3	Wait						tsAVP	a.
4	Power Supply VSP (Typ5.75V)						VSP ON	
5	Wait						tPON1/tPON2	b.
6	Power Supply VSN (Typ-5.75V)						VSN ON	
7	Wait						tRW1	c.
8	RESET High						RESX = H	
9	Wait						Min.10 ms	d.
10							[Automatic] Sleep Mode On	
11	0xB0	P1	00h	Generic	29h	The command to unlock manufacturing command write (CABC, CE etc.)	e.	
	0xD6	P1	01h	Generic	29h	The command to remove NVM reload after sleep out.		
	0xB3	P1	08h	Generic	29h	MIPI Command mode=08h		
	0x51	P1	FFh	DCS	39h	Display Brightness = 100%		
	0x53	P1	0Ch	DCS	39h	LED PWM output enable / Dimming function ON		
	0x35	P1	00h	DCS	39h	TE enable		
	0x2A	P1	00h	DCS	39h	start Column address : 000h		
	P2	00h			end Column address : 59Fh (1439)			
	P3	05h						
	P4	9Fh						
If customer need, please add initial command in here.								
	0xB0	P1	03h	Generic	29h	The command to lock manufacturing command write		
12	Display data transfer						Image Write	
13	0x29	-	-	DCS	39h	Display On	f.	
14	0x11	-	-	DCS	39h	Sleep Out		
15	Wait						Min.6 frame	
16							[Automatic] Sleep Mode Off/Display On	g.

7.3 Power on Sequence(Video mode)

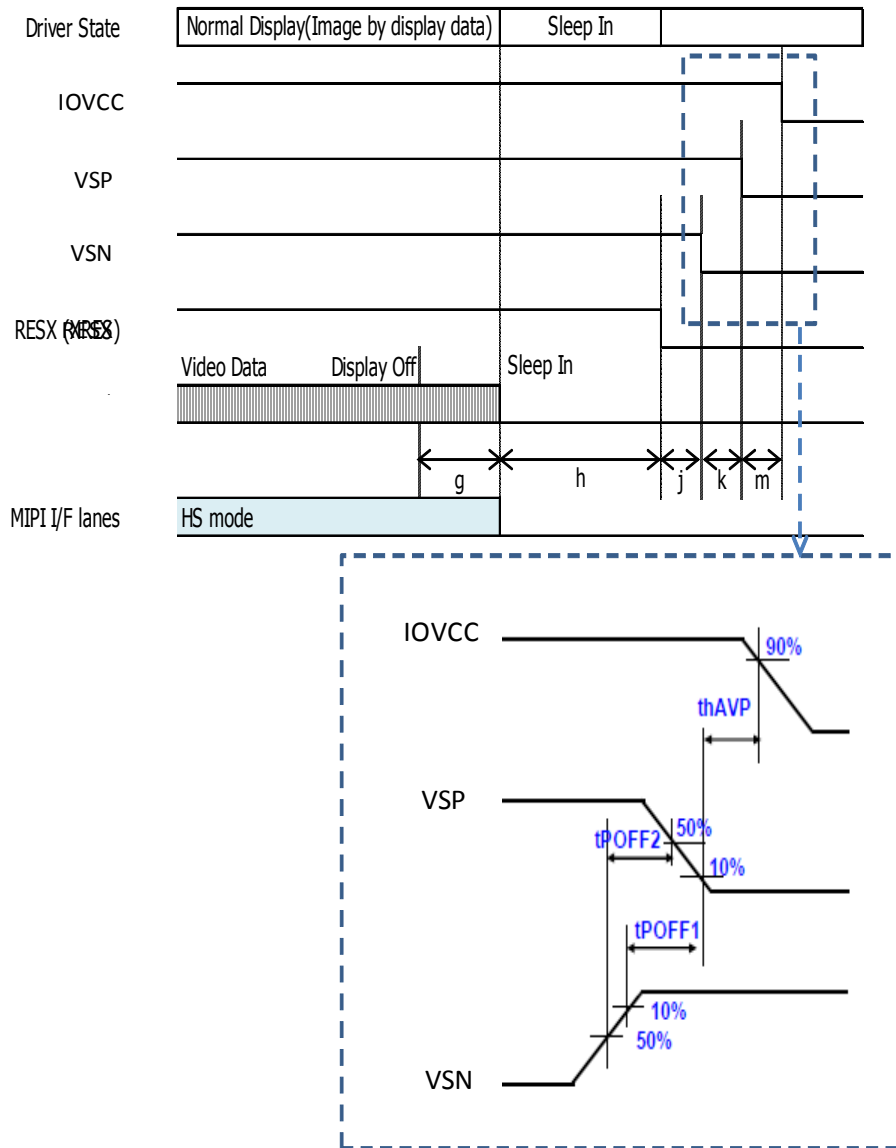


Item	Symbol	min
AVDD+ to AVDD- delay time (10% to 10%)	tPON1	0ms
AVDD+ to AVDD- delay time (50% to 50%)	tPON2	0ms
System power on to AVDD+ ON time	tsAVP	1ms
Reset low-level width	tRW1	1ms

<Video mode>

Recommended Power On Sequence							term
Step	Address	Parameter	Data	DSI data type	Delay	Command	
1	Initial condition					XRES = L	
2	Power Supply IOVDD (Typ1.8V)					IOVDD ON	
3	Wait				tsAVP	Wait until power stable	a.
4	Power Supply AVDD+ (Typ5.75V)					AVDD+ ON	
5	Wait				tPON1/tPON2		b.
6	Power Supply AVDD- (Typ-5.75V)					AVDD- ON	
7	Wait				tRW1		c.
8	RESX High					XRES = H	
9	Wait				Min.10 ms	[Automatic] NVM Auto load	d.
10						[Automatic] Sleep Mode On	
11	0xB0	P1	00h	Generic	29h	The command to unlock manufacturing command write (CABC, CE etc.)	e.
	0xD6	P1	01h	Generic	29h	The command to remove NVM reload after sleep out.	
	0xB3	P1	18h	Generic	29h	MIPI Video through mode=18h	
	0x51	P1	FFh	DCS	39h	Display Brightness = 100%	
	0x53	P1	0Ch	DCS	39h	LED PWM output enable / Dimming function ON	
	0x35	P1	00h	DCS	39h	TE enable	
If customer need, please add initial command in here.							
	0xB0	P1	03h	Generic	29h	The command to lock manufacturing command write	
12	0x29	-	-	DCS	39h	Display On	
13	0x11	-	-	DCS	39h	Sleep Out	
14	Host Display Data transfer					Image Write(Send Video Stream Packet)	
15	Wait				Min.6 frame		f.
16						[Automatic] Sleep Mode Off/Display On	

7.4 Power off Sequence Command Mode

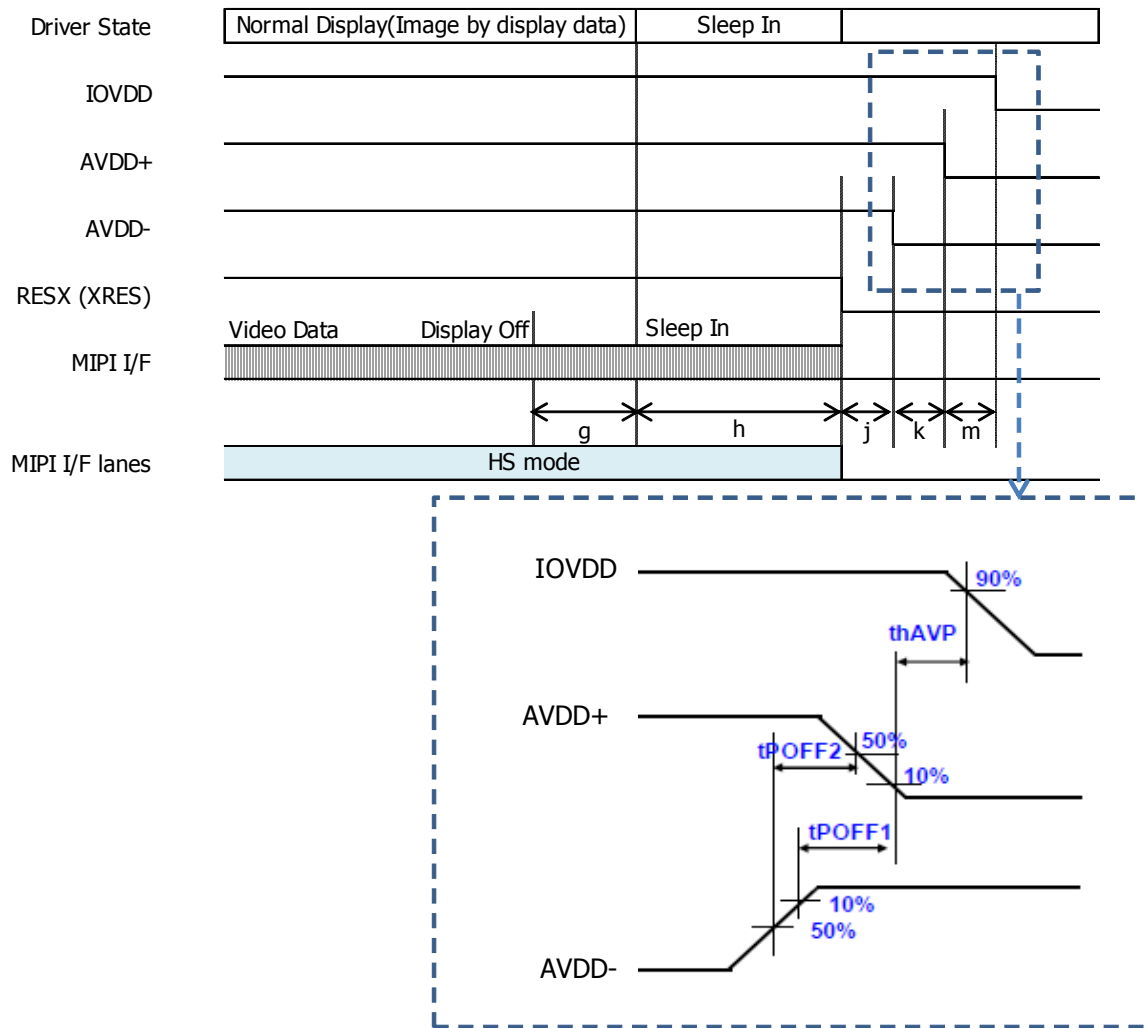


Item	Symbol	Min
VSN to VSP delay time (10% to 10%)	tPOFF1	0ms
VSN to VSP delay time (50% to 50%)	tPOFF2	0ms
VSP off to system power off time	thAVP	100ms

<Command mode>

Recommended Power Off Sequence								
Step	Address	Parameter	Data	DSI data type		Delay	Command	term
1	28h	-	-	DCS	39h		Display Off	
2	Wait					Min.1 frame		g
3	10h	-	-	DCS	39h		Sleep In	
4	Wait					Min. 4frame		h
5	RESET Low						RESX = L	
6	Wait					Min.0ms		j
7	VSN(Typ-5.75V) OFF							
8						tPOFF1/tPOFF2	Wait	k
9	VSP(Typ+5.75V) OFF							
10						thAVP	Wait	m
11	IOVCC OFF(Typ1.8V) OFF							

7.5 Power off Sequence (Video Mode)



Item	Symbol	Min
AVDD- to AVDD+ delay time (10% to 10%)	tPOFF1	0ms
AVDD- to AVDD+ delay time (50% to 50%)	tPOFF2	0ms
AVDD+ off to system power off time	thAVP	100ms

<Video mode>

Recommended Power Off Sequence							
Step	Address	Parameter	Data	DSI data type	Delay	Command	term
1	28h	-	-	DCS	39h	Display Off	g
2	Wait				Min.1 frame		
3	10h	-	-	DCS	39h	Sleep In	h
4	Wait				Min. 4frame	Hsync/Vsync signals should be send after Sleep In command	
5						Mipi data transfer Stop	
6	RESX Low					XRES = L	
7	Wait				Min.0ms		j
8	AVDD-(Typ-5.75V) OFF						
9					tPOFF1/tPOFF2	Wait	k
10	AVDD+(Typ+5.75V) OFF						
11					thAVP	Wait	m
12	IOVDD OFF(Typ1.8V) OFF						

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	70°C 96hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30°C 96hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	60°C 96hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 96hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-30°C/70°C 20 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

<http://www.displaymodule.com/pages/faq> HYPERLINK

"http://www.displaymodule.com/pages/faq"