DisplayModule

DM-TFT55-370

5.5" IPS 720x1280 DISPLAY PANEL WITH CAPACITIVE TOUCH –MIPI

Contents

1 Revision History

Date	Changes
2018-08-30	First release

2 Main Features

Item	Specification	Unit
Size	5.5	Inch
Resolution	720(RGB) x 1280	pixel
Module Dimension	86.04 x 144.96 x 4.75	mm
Display area	68.04 x 120.96	mm
Pixel pitch	0.0945 x 0.0945	mm
TFT Controller IC	ILI9881C	-
CTP Driver IC	GT911	
Interface	4 Lane MIPI	-
Display Color	65K/262K/16.7M	colors
View Direction	All	
Touch mode	Five points and Gestures	
Backlight Type	LED Normally black	-
Weight	TBD	g

3 Pin Description

3.1 TFT

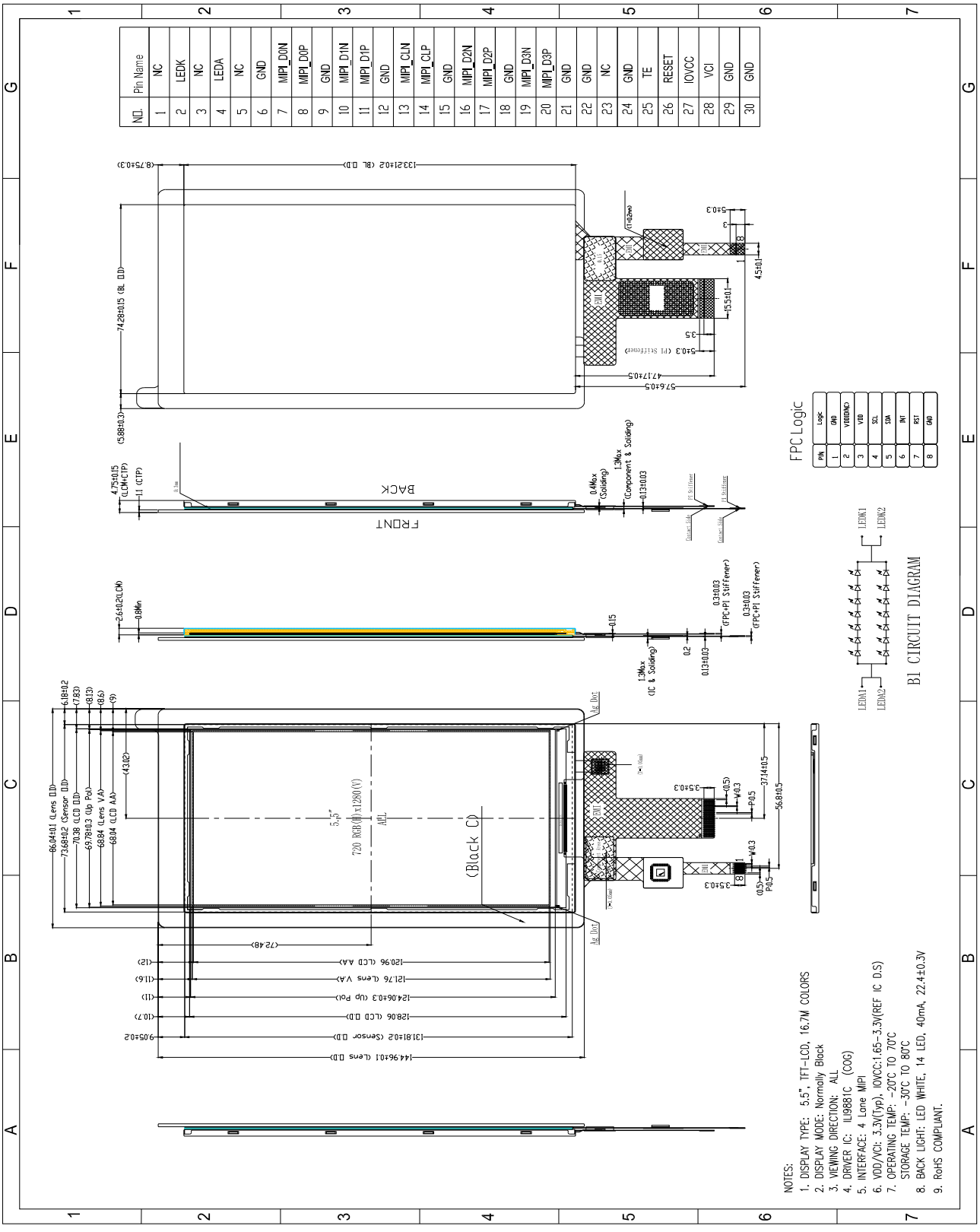
No.	Symbol	Description
1	NC	
2	LEDK	Cathode pin of backlight
3	NC	
4	LEDA	Anode pin of backlight
5	NC	
6	GND	Ground
7	MIPI_D0N	MIPI DSI differential data pair.(Data lane 0)
8	MIPI_D0P	Leave it open or fix to GND level when not in use
9	GND	Ground
10	MIPI_D1N	MIPI DSI differential data pair.(Data lane 1)
11	MIPI_D1P	Leave it open or fix to GND level when not in use
12	GND	Ground
13	MIPI_CLN	MIPI DSI differential clock pair
14	MIPI_CLP	Leave it open or fix to GND level when not in use
15	GND	Ground
16	MIPI_D2N	MIPI DSI differential data pair.(Data lane 2)
17	MIPI_D2P	Leave it open or fix to GND level when not in use
18	GND	Ground
19	MIPI_D3N	MIPI DSI differential data pair.(Data lane 3)
20	MIPI_D3P	Leave it open or fix to GND level when not in use
21	GND	Ground
22	GND	Ground
23	NC	
24	GND	Ground
25	TE	Tearing effect output pin Leave it open or fix to GND level when not in use

26	RESET	The external reset pin Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power. Fix to IOVCC level when not in use
27	IOVCC	Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 3.3V
28	VCI	Power supply for analog circuits. Connect to an external power supply of 2.5V to 3.3V
29	GND	Ground
30	GND	Ground

3.2 CTP

No.	Symbol	Description
1	GND	Ground
2	NC	No connection
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground

4 Mechanical Drawing



5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VCI		2.5	3.3	6.0	V
I/O Digital Voltage	IOVCC		1.65	2.8	3.3	V
Normal mode Current	IDD			31		mA
Low Level Input Voltage	V_{IL}		GND		0.3 IOVCC	V
High Level Input Voltage	V_{IH}		0.7 IOVCC		IOVCC	V
Low Level Output Voltage	V_{OL}		GND		0.2 IOVCC	V
High Level Output Voltage	V_{OH}		0.8 IOVCC		IOVCC	V
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃
LED Forward Current	If		30	160	-	mA
LED Forward Voltage	Vf		-	22.4	-	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	AV	-	80	-	deg
View Angles Bottom	AV	-	80	-	deg
View Angles Right	AH	-	80	-	deg
View Angles Left	AH	-	80	-	deg
Response Time	Tr +Tf		35	40	ms
Contrast Ratio	CR	720	900	-	--
LCM Luminance	Lv	310	360	-	cd/m^2

7 MIPI Interface Characteristics

7.1 High Speed Mode-Clock Channel Timing

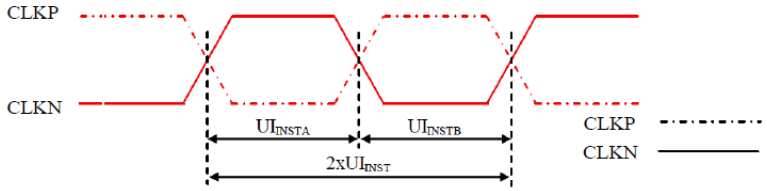


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

7.2 High Speed Mode – Data Clock Channel Timing

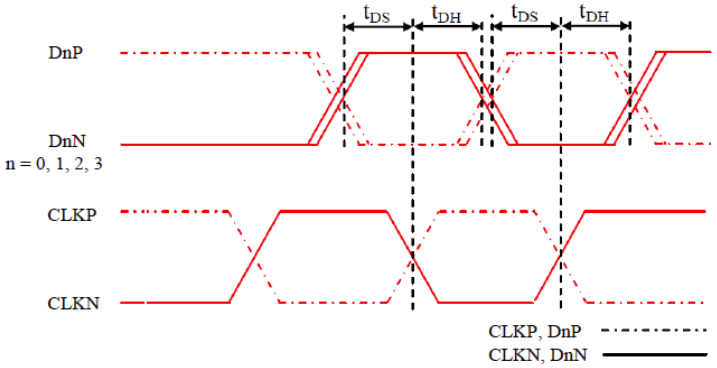


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

7.3 High Speed Mode – Rising and Fall Timings

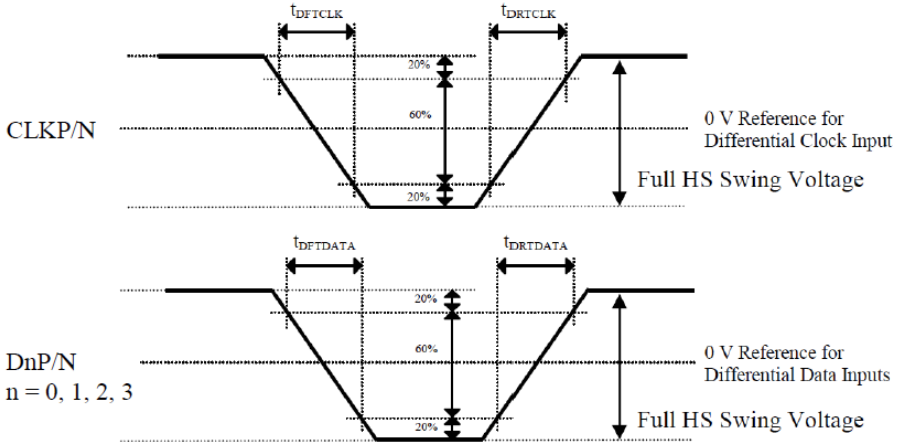


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

7.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

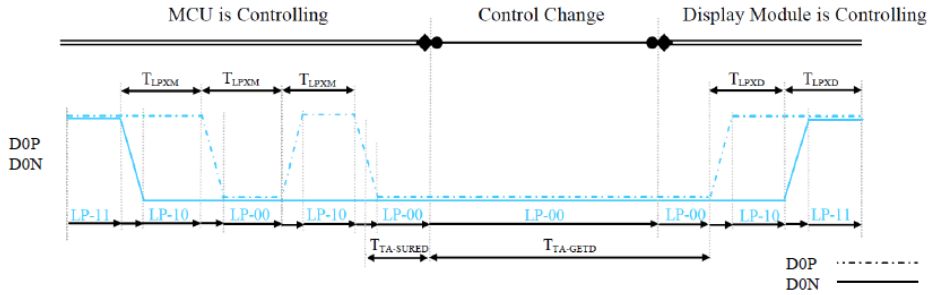


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

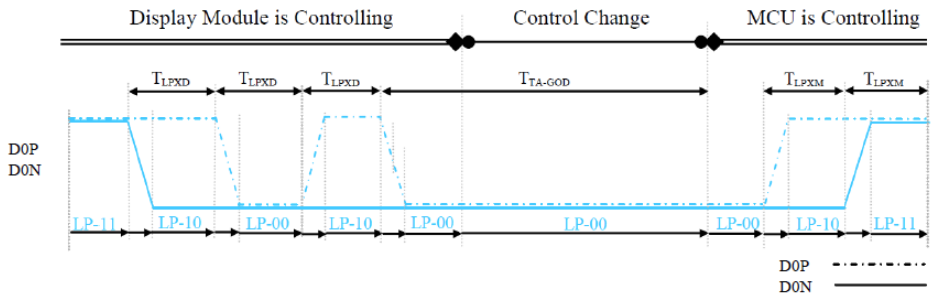


Figure 122: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

7.5 Data Lanes from Low Power Mode to High Speed Mode

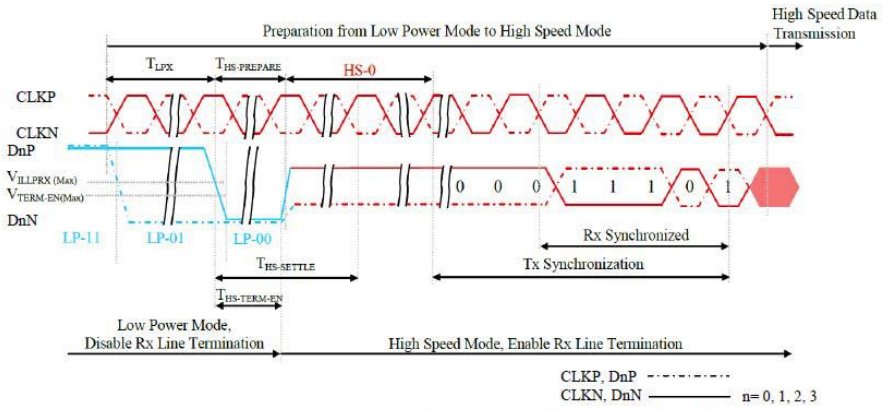
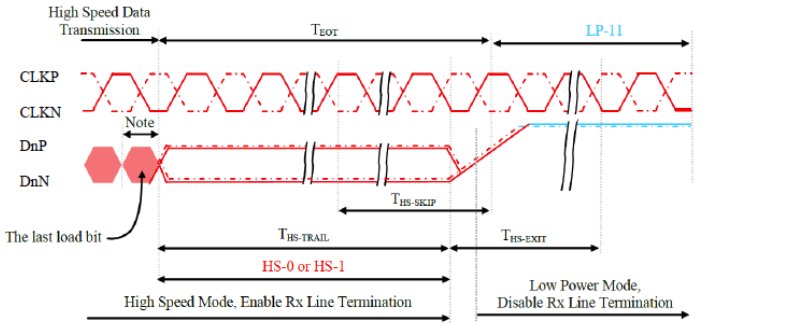


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

7.6 Data Lanes from High Power Mode to High Speed Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

7.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

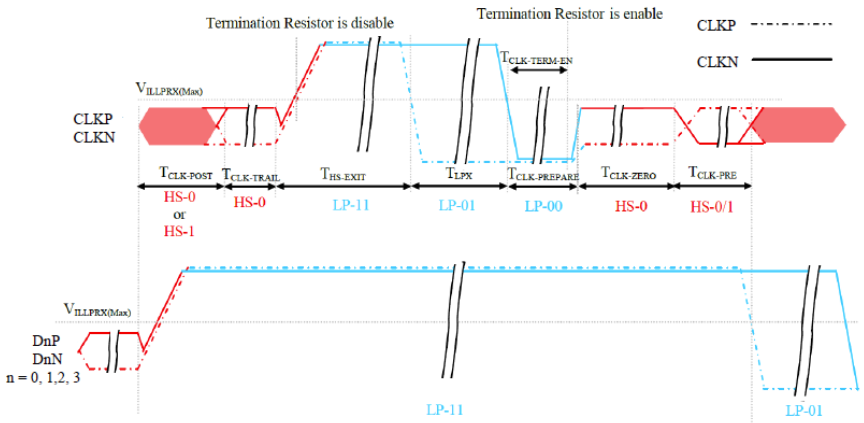
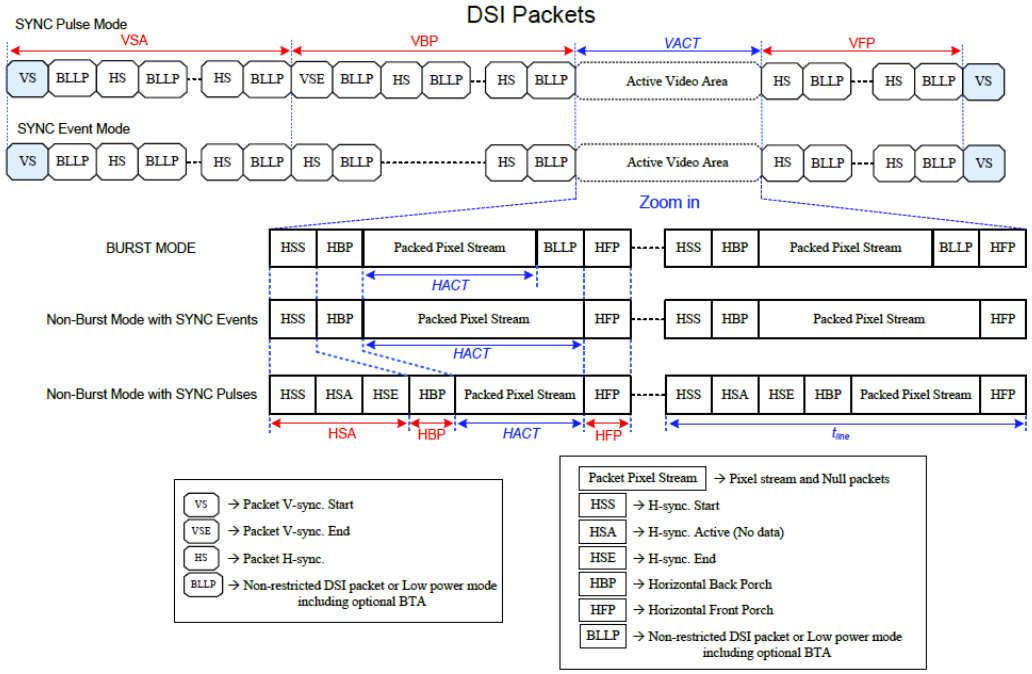


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

7.8 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR_{bps}	200		Note 5	Line

1 UI=1/Bit rate

HAS(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”

7.9 Reset input timing

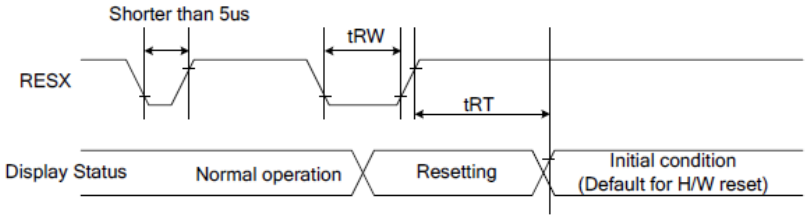


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

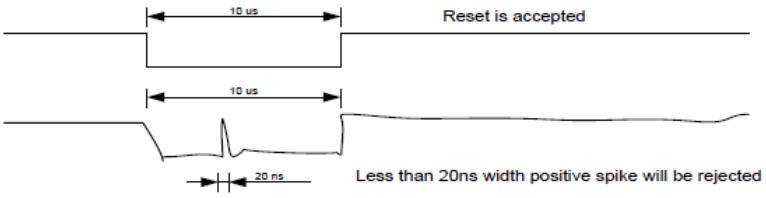


Figure 127: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 CTP Specification

8.1 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	VDD		2.66	-	3.47	V
Normal mode Current			-	8	14.5	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃

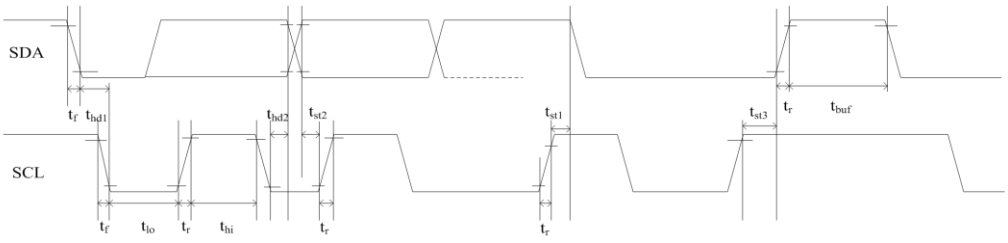
8.2 AC Characteristics

Item	Condition	Min	Typ	Max	Unit
OSC clock	AVDD=2.8V;VDDIO=1.8V	59	60	61	MHz

AC characteristics of Oscillators

I2C interface:

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



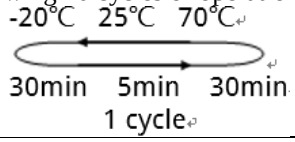
Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq