DisplayModule

DM-TFT50-415

5.0" IPS 480× 854 TFT LCD Display Panel with Capacitive Touch - RGB

Contents

1 Revision History

Date	Changes
2020-4-16	First release

2 Main Features

Item	Specification	Unit
Diagonal Size	5.0	inch
Driver element	TFT active matrix	-
TFT Pixel arrangement	RGB vertical stripe	-
Display mode	Transmissive/Normally Black	-
Viewing angle	ALL	o'clock
Display Colors	65K/262K/16.7M	Colors
Resolution	480 x 854	pixel
Controller IC	ILI9806E	-
CTP Driver IC	GT911	-
Interface	3-SPI+16/18/24-bits RGB	-
Active Area	61.63 x 109.65	mm
Panel Dimension	78.56 x 135.65 x 4.40	mm
Pixel Pitch	0.128 x 0.128	mm
Touch mode	5-point and Gestures	-
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

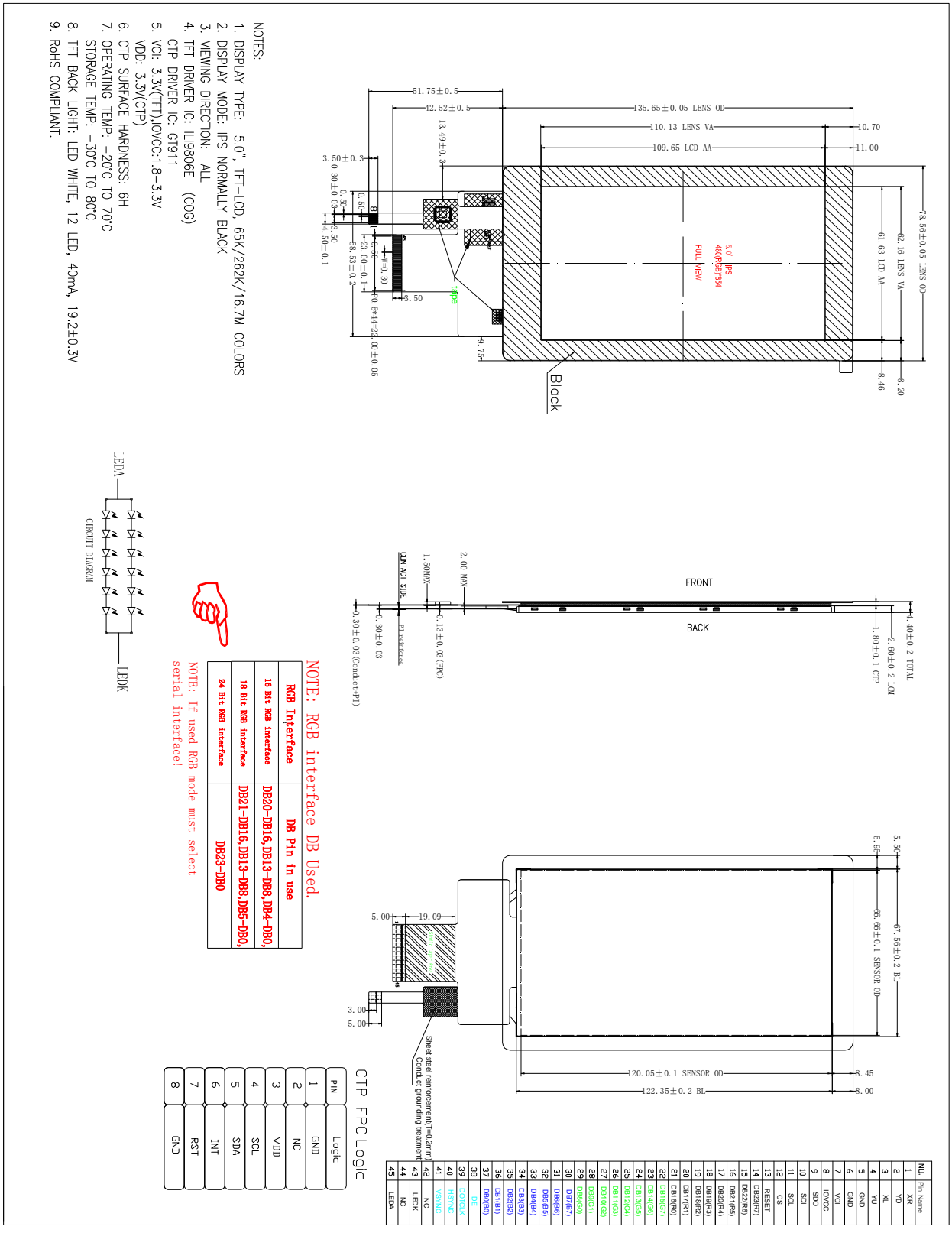
Pin No.	Symbol	Function Description
1	XR(NC)	Touch panel Right Glass Terminal
2	YD(NC)	Touch panel Bottom Film Terminal
3	XL(NC)	Touch panel LIFT Glass Terminal
4	YU(NC)	Touch panel Top Film Terminal
5	GND	Ground.
6	GND	Ground.
7	VCI	Supply voltage (3.3V).
8	IOVCC	I/O power supply voltage.
9	SDO	SPI interface output pin.-The data is output on the falling edge of the SCL signal.-If not used, let this pin open.
10	SDI	Data lane in 1 data lane serial interface. The data is latched on the rising edge of the SCL signal.
11	SCL	This pin is used to select “Data or Command” in the parallel interface. When D/CX = ’1’, data is selected. When D/CX = ’0’, command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4- wire 8-bit serial data interface. fix this pin at VCI or GND when not in use.
12	CS	Chip select input pin (“Low” enable). fix this pin at VCI or GND when not in use.
13	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
14-37	DB23-DB0	24-bit parallel bi-directional data bus for MCU system and RGB interface mode .Fix to GND level when not in use
38	DE	Data enable signal for RGB interface peration. fix this pin at VCI or GND when not in use.
39	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.
40	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.
41	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.
42	NC	
43	LEDK	Cathode pin of backlight.
44	NC	
45	LEDA	Anode pin of backlight.

3.2 CTP Pin Description

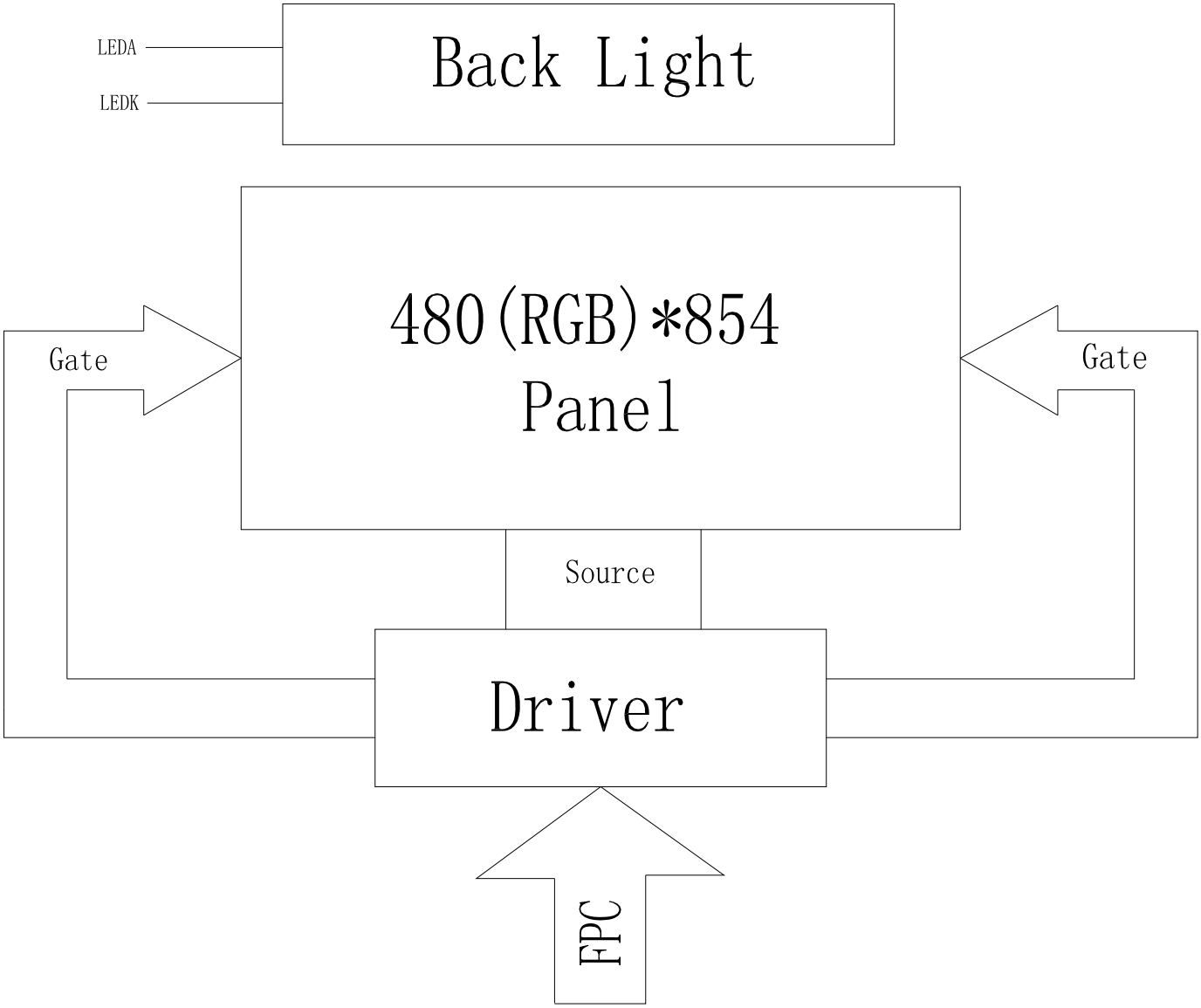
Pin No.	Symbol	Function Description
1	GND	Ground.
2	NC	
3	VDD	Supply voltage.
4	SCL	I2C clock input.
5	SDA	I2C data input and output
6	INT	External interrupt to the host.
7	RST	External Reset, Low is active.
8	GND	Ground.

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



5 Function Block Diagram



6 Optics & Electrical Characteristics

6.1 Optical Characteristics

Item		Symbol	Min	Typ	Max	Unit	Remark
View Angles			-	80	-	°	CR>10
C.I.E. (White)		(x) (y)	-	0.305 0.340	-	-	Θ=0 Normal viewing angle
C.I.E(Red)		(x) (y)	-	-	-	-	
C.I.E(Green)		(x) (y)	-	-	-	-	
C.I.E(Blue)		(x) (y)	-	-	-	-	
Contrast Ratio		CR	640	800	-	-	-
Response time	Rising	T_R	-	16	21	Msec	-
	Falling	T_F	-	19	24	Msec	-
Color gamut		S(%)	-	70	-	%	C-light
Option View Direction		Free					-

Note:

- Measuring surrounding：dark room
- Ambient temperature：25±2℃
- 15min. warm-up time.

6.2 Absolute Maximum Ratings (Ta=25 VSS=0V)

Parameter	Symbol	Min	Max	Unit	Remark
Digital Supply Voltage	V_{DD}	-0.3	4.6	V	-
Digital interface supple Voltage	I_{OVCC}	-0.3	4.6	V	-
Operating Temperature	T_{OP}	-20	70	℃	-
Storage Temperature	T_{STG}	-30	80	℃	-

Note : If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.SSS

6.3 DC Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Digital Supply Voltage	VDD	2.5	2.8/3.3	.6	V	V
Digital interface supple Voltage	IOVCC	1.65	1.8	3.6	V	V
Normal mode Current consumption	IDD	-	30	-	mA	V
Low Level Input Voltage	VIL	-	-0.3	-	0.3 * V_{DDIO}	V
High Level Input Voltage	VIH	-	0.7 * V_{DDIO}	-	V_{DDIO}	V
Low Level Output Voltage	VOL	-	GND	-	0.2 * V_{DDIO}	V
High Level Output Voltage	VOH	-	0.8 * V_{DDIO}	-	V_{DDIO}	V

Note : The VCC input must be kept in a stable value; ripple and noise are not allowed.

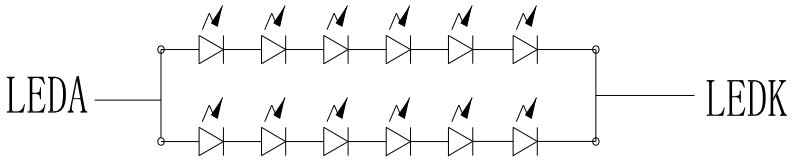
6.4 LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips White LED

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Forward voltage	V_F	-	19.2	-	V	-
Forward current	I_F	30	40	-	mA	-
LCM Luminance	L_V	430	-	-	cd/m^2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

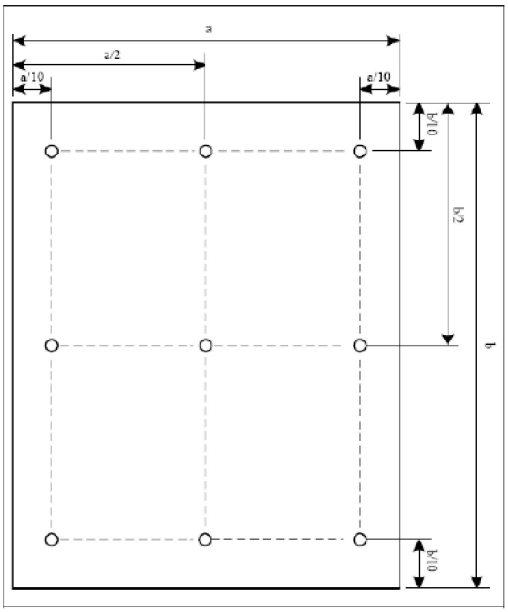
Note 1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2:The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

NOTE 3：Luminance Uniformity of these 9 points is defined as below:

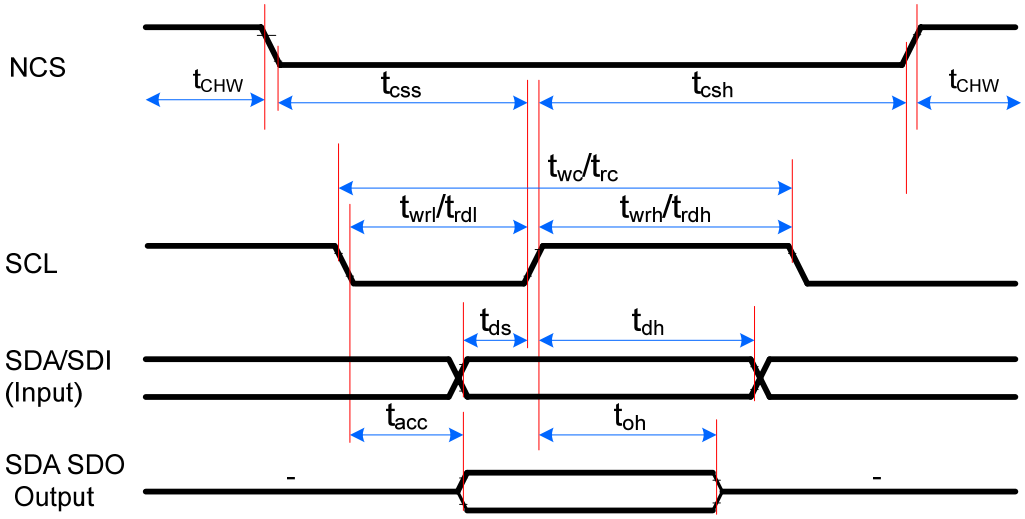


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points}(1-9)}{\text{maximum luminance in 9 points}(1-9)}$$

$$\text{Lumiance} = \frac{\text{Total lumincace of 9 points}}{9}$$

6.5 AC Characteristics

6.5.1 Serial Interface Characteristics (3-line serial):



IOVCC=1.8V,VCI=2.8V,Ta=25℃

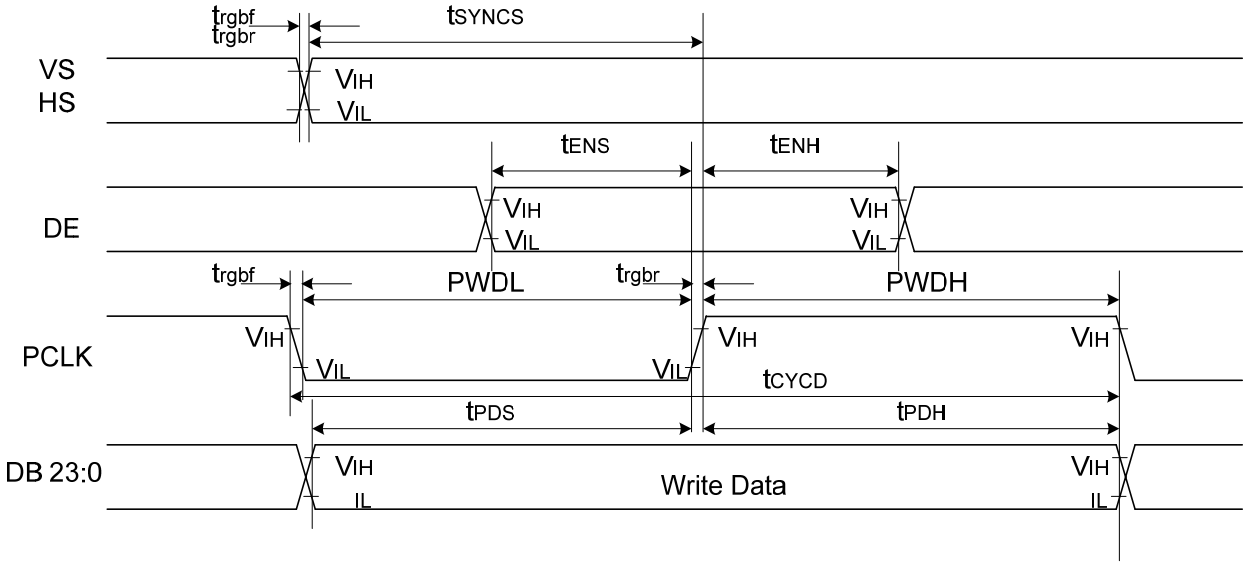
Signal	Symbol	Description	Min	Max	Unit	Remark
CSX	T_{CSS}	Chip select time (Write)	15	-	ns	
	T_{CSH}	Chip select hold time (Read)	15	-	ns	
	T_{CHW}	CS “H” pulse width	40	-	ns	
SCL	T_{WC}	Serial clock cycle (Write)	30	-	ns	
	T_{WRH}	SCL “H” pulse width (Write)	10	-	ns	
	T_{WRL}	SCL “L” pulse width (Write)	10	-	ns	
	T_{RC}	Serial clock cycle (Read)	150	-	ns	
	T_{RDH}	SCL “H” pulse width (Read)	60	-	ns	
	T_{RDL}	SCL “L” pulse width (Read)	60	-	ns	
SDA/SDO (Output)	T_{ACC}	Access time (Read)	10	100	ns	For maximum CL=30pF
	T_{OH}	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA (DIN)	T_{DS}	Data setup time (Write)	10	-	ns	
	T_{DH}	Data hold time (Write)	10	-	ns	

Note:

1. Ta = -30 to 70 ℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.

2. Does not include signal rise and fall times.

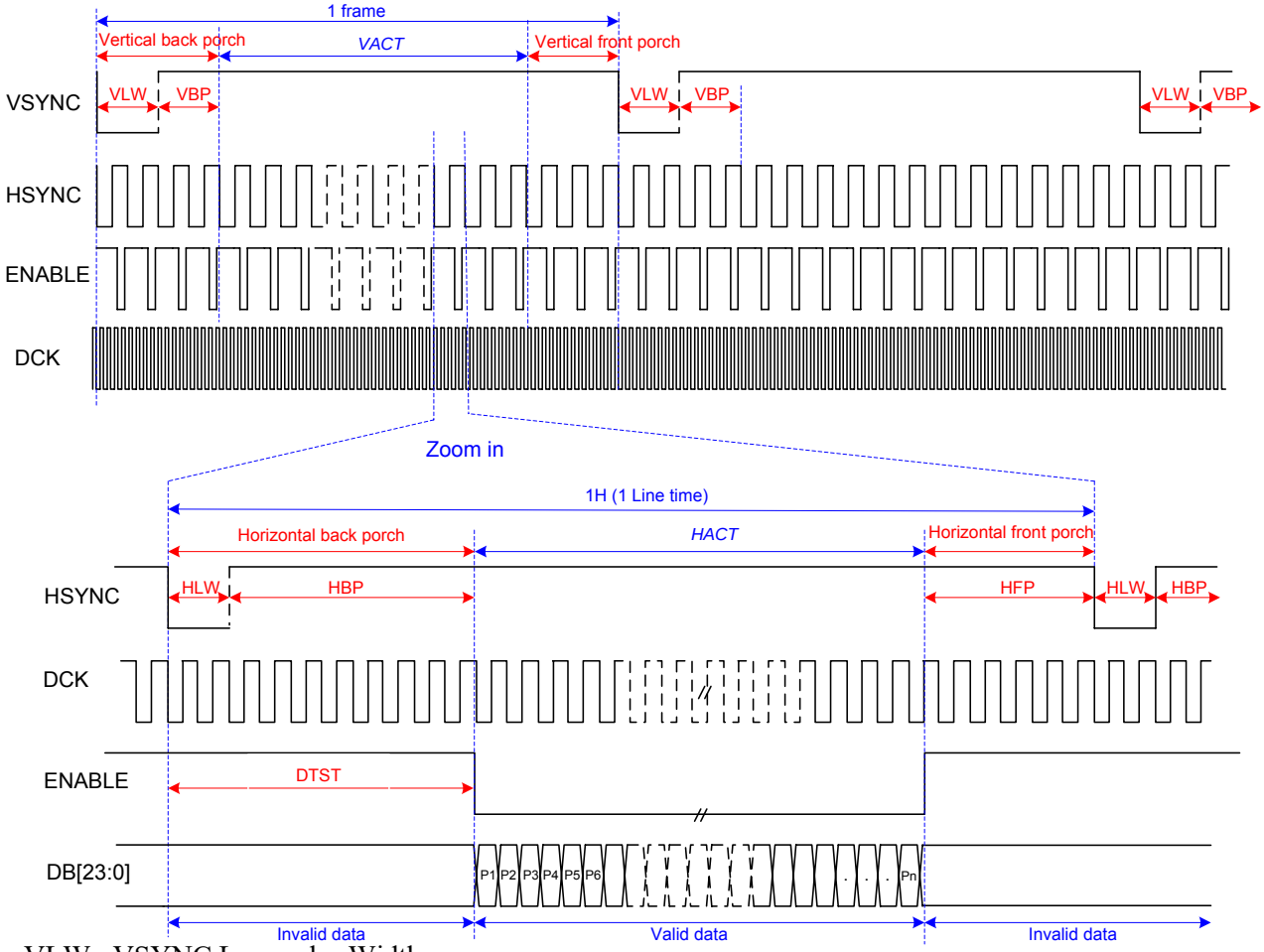
6.5.2 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Ta = -30 to 70℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V

Signal	Symbol	Description	Min	Max	Unit	Remark
VS/HS	T_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	T_{SYNCH}	VS/HS hold time	5	-	ns	
DE	T_{ENS}	DE setup time	5	-	ns	
	T_{ENH}	DE hold time	5	-	ns	
DB[23:0]	T_{POS}	Data setup time	5	-	ns	
	T_{PDH}	Data hold time	5	-	ns	
PCLK	P_{WDH}	PCLK high-level period	13	-	ns	
	P_{WDL}	PCLK low-level period	13	-	ns	
	T_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} ,t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

6.5.3 DPI Interface Timing



VLW : VSYNC Low pulse Width

HLW : HSYNC Low pulse Width

DTST : Data Transfer Startup Time

Pn : pixel 1, pixel 2…, pixel n.

The timing chart of 24-/18-/16-bit DPI (RGB) interface mode

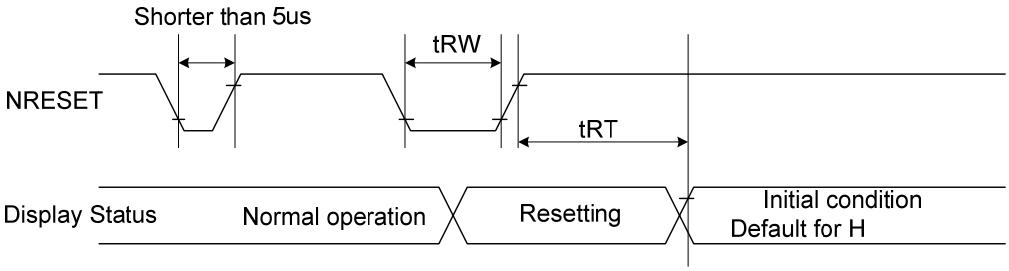
Symbol	Description	Min	Typ.	Max	Unit
FR	Frame Rate	54		66	fps
HLW	Horizontal Low Pulse width	1		-	DOTCLK
HBP	Horizontal Back Porch	2		126	DOTCLK
HACT	Horizontal Address		480		DOTCLK
HFP	Horizontal Front Porch	2		-	DOTCLK
VLW	Vertical Low Pulse width	1		126	Line
VBP	Vertical Back Porch	1		126	Line
VACT	Vertical Address			864	Line
VFP	Vertical Front Porch	1		255	Line
DCLK	Data Clock	16.6		41.7	MHz

Note 1: HLW+HBP+HFP >= 2us.

Note 2: VSPL=’0’, HSPL=’0’, DPL=’0’ and EPL=’0’ of “(Interface Mode Control 21h of the Page 1)” command.

6.5.4 Display RESET Timing Characteristics

Reset input timing



Timing Parameters

Siganl	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	µs
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

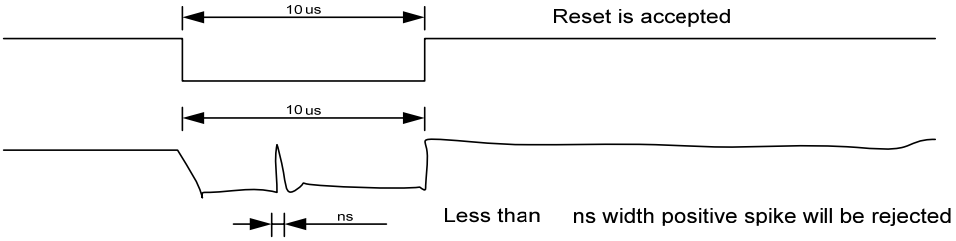
Note 1:The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: 2.Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset starts

Note 3: 3.During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7 CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min	Max	Unit	Note
Digital Supply Voltage	VDD	2.66	3.47	V	
Operating Temperature	T_{OP}	-30	+85	℃	
Storage Temperature	T_{ST}	-30	+85	℃	
ESD protection voltage (HB Model)	-	-	±2	KV	

7.1.2 DC Electrical Characteristics(Ta=25 ℃)

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V or VDDIO=VDD)

Item	Min	Type	Max	Unit	Note
Normal mode operating current	-	8	14.5	mA	
Green mode operating current	-	3.3	-	mA	
Sleep mode operating current	70	-	120	uA	
Doze mode operating current	-	0.78	-	mA	
Digital Input low voltage/VIL	-0.3	-	0.25*VDD	V	
Digital Input high voltage/VIH	0.75*VDD	-	VDD+0.3	V	
Digital Output low voltage/VOL	-	-	0.15*VDD	V	
Digital Output high voltage/VOH	0.85*VDD	-	-	V	

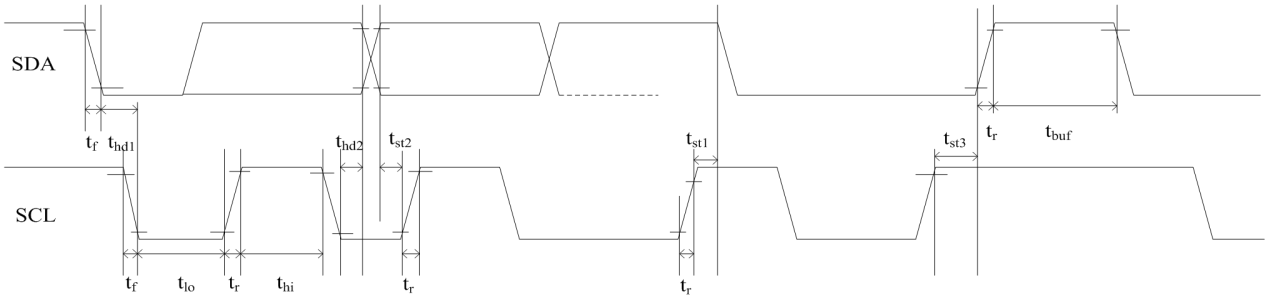
7.1.3 AC Characteristics

(Ambient temperature:25℃, VDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit	Note
OSC oscillation frequency	59	60	61	MHz	
I/O output rise time,low to high	-	14	-	ns	
I/O output rfall time,high to low	-	14	-	ns	

7.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

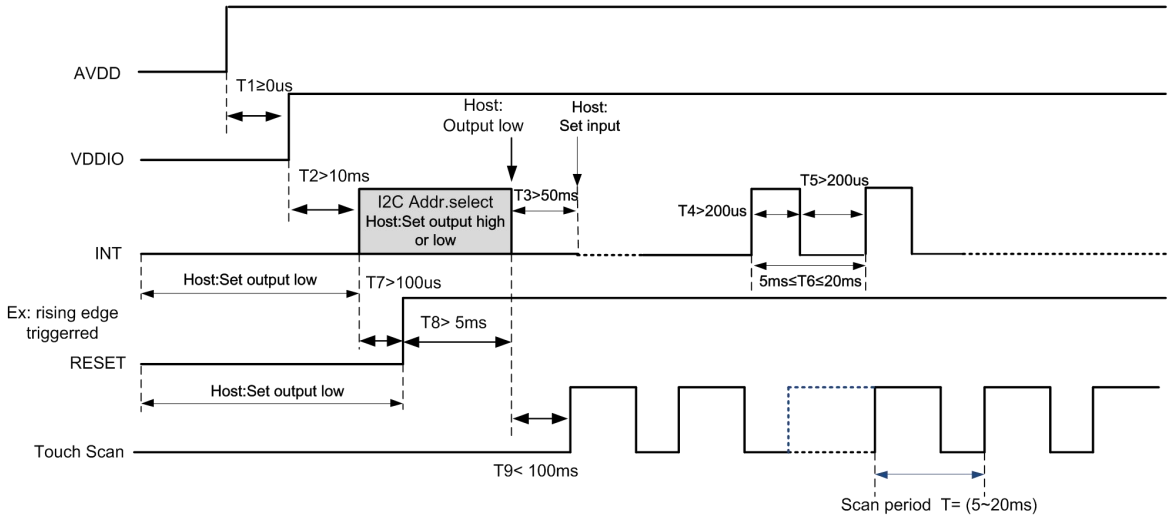
Item	Symbol	Min	Max	Unit
SCL low period	t_{lo}	1.3	-	μs
SCL high period	t_{hi}	0.6	-	μs
SCL setup time for Start condition	t_{st1}	0.6	-	μs
SCL setup time for Stop condition	t_{st3}	0.6	-	μs
SCL hold time for Start condition	t_{hd1}	0.6	-	μs
SDA setup time	t_{st2}	0.1	-	μs
SDA hold time	t_{hd2}	0	-	μs

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

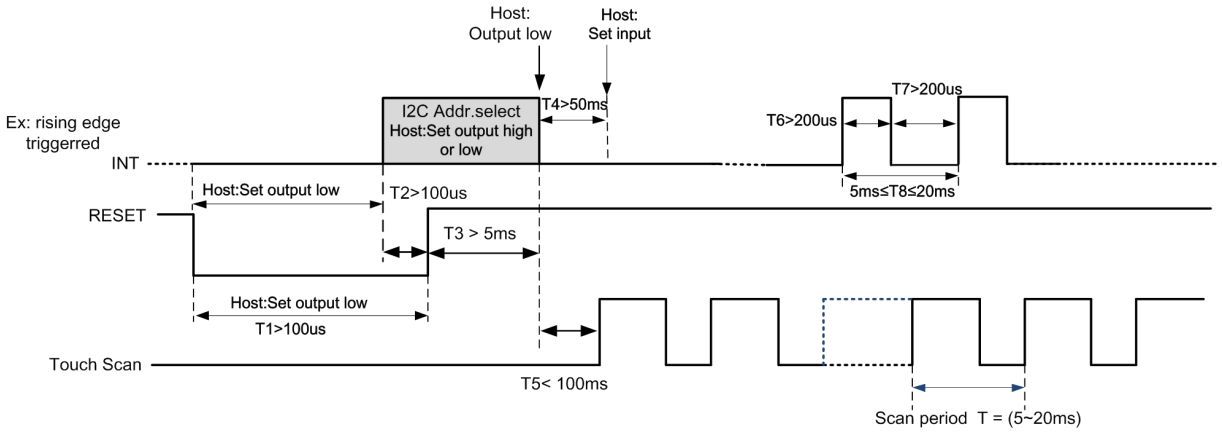
Item	Symbol	Min	Max	Unit
SCL low period	t_{lo}	1.3	-	μs
SCL high period	t_{hi}	0.6	-	μs
SCL setup time for Start condition	t_{st1}	0.6	-	μs
SCL setup time for Stop condition	t_{st3}	0.6	-	μs
SCL hold time for Start condition	t_{hd1}	0.6	-	μs
SDA setup time	t_{st2}	0.1	-	μs
SDA hold time	t_{hd2}	0	-	μs

GT911 supports two I²C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

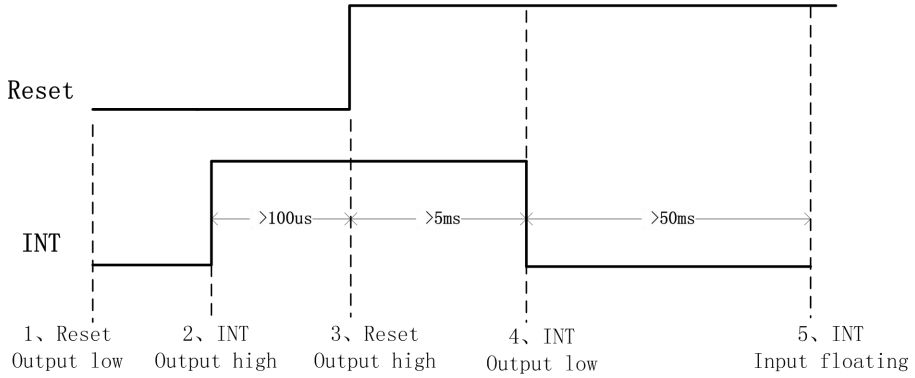
Power-on Timing:



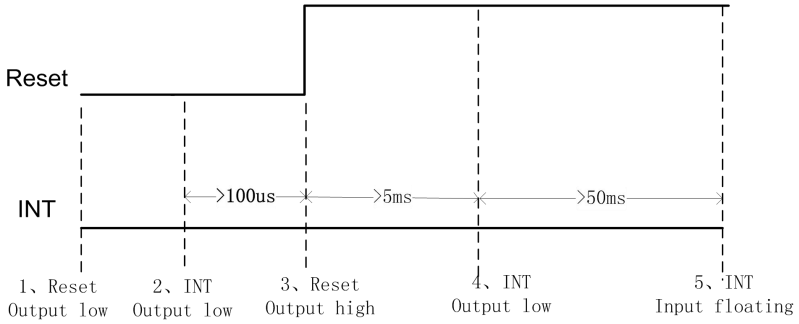
Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



a) Data Transmission

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

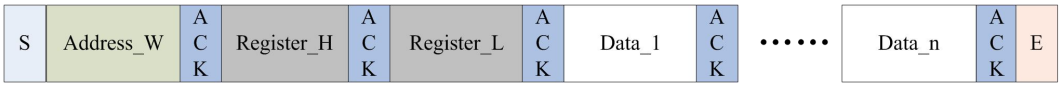
All slave devices connected to I 2 C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

b) Writing Data to GT911

(For example：device address is 0xBA/0xBB)



Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

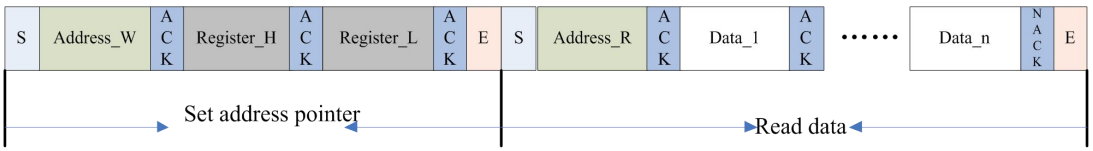
After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation.

Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT911

(For example：device address is 0xBA/0xBB)



Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8 Reliability

Test Item	Content of Test	Test Condition	Note
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 96hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 96hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20 ℃ 96hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	70℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation	-20℃/70℃ 20 cycles	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"