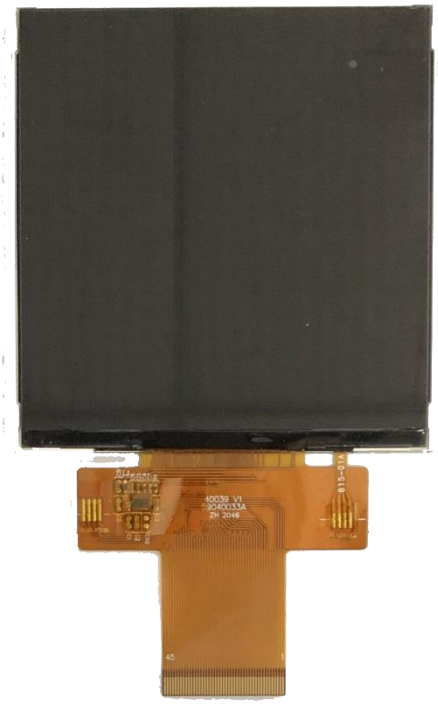
DisplayModule



DM-TFT40-445

4.0" IPS 720 X 720 TFT LCD Transmissive DISPLAY PANEL - SPI, RGB

Contents

1 Revision History

Date	Changes
2022-06-29	First release

2 Main Features

Item	Specification	Unit
Resolution	720(RGB)*720	pixel
Display area(AA)	71.928(H)*71.928(V) (4.0 inch)	mm
Module Dimension	77(H) x 80(V) x 2.6(D)	mm
TFT Controller IC	NV3052C	-
Interface	3SPI+16/18/24 bit RGB	-
Dot Pitch	0.0999(H)*0.0999(V)	mm
Display Color	16.7M	colors
View Direction	ALL	o'clock
Display mode	Transmissive /Normally Black	
Operating temperature	-30～+80	℃
Storage temperature	-30～+85	℃
Weight	30	g

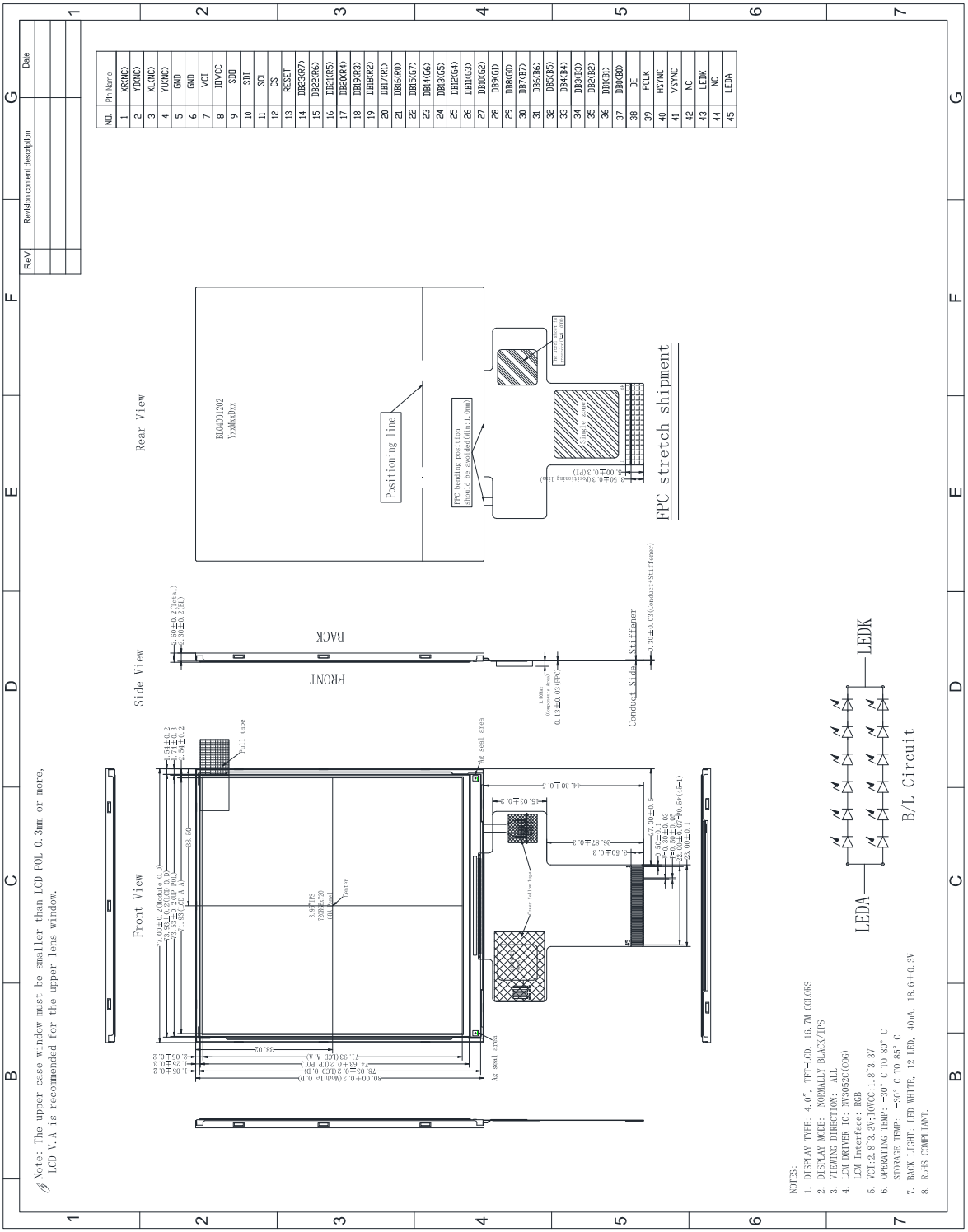
3 Pin Description

3.1 TFT

No.	Symbol	Description
1	XR(NC)	
2	YD(NC)	
3	XL(NC)	
4	YU(NC)	
5	GND	Ground
6	GND	Ground
7	VCI	Supply voltage (3.3V)
8	IOVCC	Supply voltage (Logic)(1.8~3.3V).
9	SDO	Serial data output pin used for the SPI Interface. Leave the pin to open when not in use.
10	SDI	SDI: Serial data input/output bidirectional pin for SPI Interface.
11	SCL	Serial clock input for SPI Interface.
12	CS	- A chip select signal Low: the chip is selected and accessible

		High: the chip is not selected and not accessible
13	RESET	- The external reset input - Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
14-37	DB23-DB0	24-bit parallel data bus for RGB Interface. Fix to IOVCC or GND level when not in use.
38	DE	Data enable signal for RGB interface operation Low: access enabled High: access inhibited Fix to IOVCC or GND level when not in use.
39	PCLK	Dot clock signal for RGB interface operation.
40	HSYNC	Line synchronizing signal for RGB interface operation.
41	VSYNC	Frame synchronizing signal for RGB interface operation.
42	NC	--
43	LEDK	Cathode pin of backlight.
44	NC	--
45	LEDA	Anode pin of backlight.

4 Mechanical Drawing



NO.	Pin Name
1	XR(NC)
2	YD(NC)
3	XL(NC)
4	YU(NC)
5	GND
6	GND
7	VCI
8	IOVCC
9	SDO
10	SDI
11	SCL
12	CS
13	RESET
14	DB23(R7)
15	DB22(R6)
16	DB21(R5)
17	DB20(R4)
18	DB19(R3)
19	DB18(R2)
20	DB17(R1)
21	DB16(R0)
22	DB15(G7)
23	DB14(G6)
24	DB13(G5)
25	DB12(G4)
26	DB11(G3)
27	DB10(G2)
28	DB9(G1)
29	DB8(G0)
30	DB7(B7)
31	DB6(B6)
32	DB5(B5)
33	DB4(B4)
34	DB3(B3)
35	DB2(B2)
36	DB1(B1)
37	DB0(B0)
38	DE
39	PCLK
40	HSYNC
41	VSYNC
42	NC
43	LEDK
44	NC
45	LEDA

ReV.	Revision content description	Date

5 Electrical Characteristics

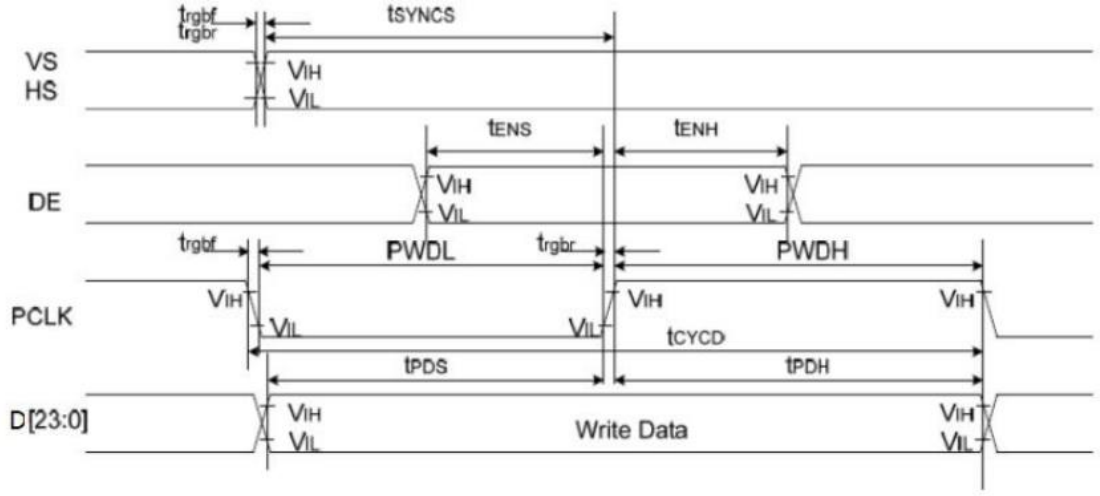
Item		Symbol	Min	Typ.	Max	Unit
Digital Supply Voltage	Absolute Maximum Rating	VCI	-0.3		6.6	V
Digital interface supple Voltage	Absolute Maximum Rating	IOVCC	-0.3		4.5	V
Operating Temperature	Absolute Maximum Rating	TOP	-30		+80	℃
Storage Temperature	Absolute Maximum Rating	TST	-30		+85	℃
Digital Supply Voltage		VCI	2.5	3.3	3.6	V
Digital interface supple Voltage		IOVCC	1.65	1.8	3.6	V
Normal mode Current		IDD	--	28	56	mA
Level input voltage		V_{IH}	0.7*IOVCC	--	IOVCC	V
		V_{IL}	GND	--	0.3*IOVCC	V
Level output voltage		V_{OH}	0.8*IOVCC	--	IOVCC	V
		V_{OL}	GND	--	0.2*IOVCC	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
Forward Current	I_F	--	40	-	mA
Forward Voltage	V_F	--	18.6	-	V
LCM Luminance	LV	650	700	-	cd/m2
LED life time	H_r	--	50000	-	Hour
Uniformity	Avg	80	--	-	%

7 AC Characteristics

7.1 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
D[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr},t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

7.2 Serial interface characteristics

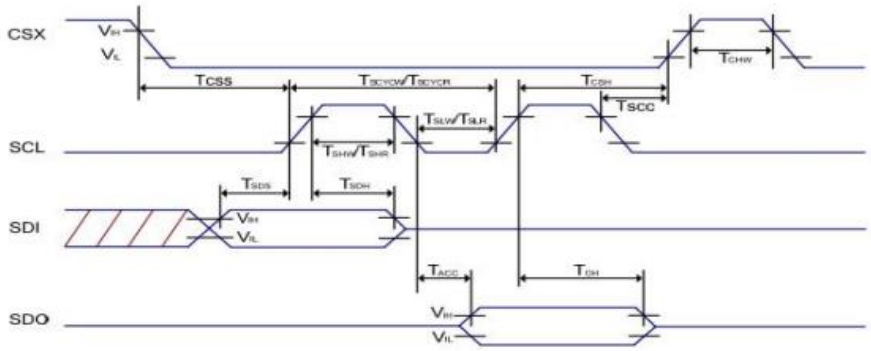


Figure: 3-pin Serial Interface Characteristics

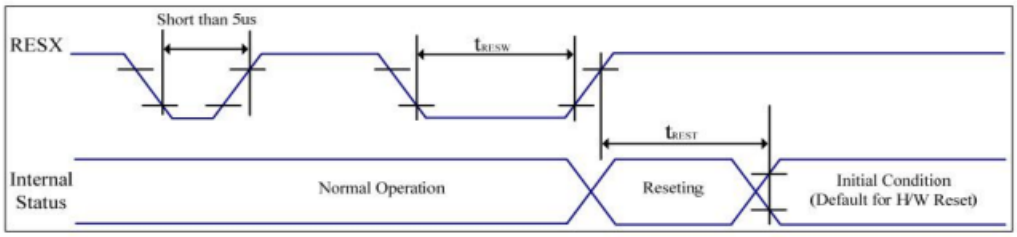
Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	Tcss	Chip select setup time	15	-	ns	-
	Tcsh	Chip select hold time	15	-	ns	
	Tscc	Chip select setup time	20	-	ns	
	Tchw	Chip "H" pulse width	40	-	ns	
SCL	Tscycw	Serial clock cycle (Write)	66	-	ns	-
	Tshw	SCL "H" pulse width (Write)	10	-	ns	
	Tslw	SCL "L" pulse width (Write)	10	-	ns	
	Tscycr	Serial clock cycle (Read)	150	-	ns	-
	Tshr	SCL"H" pulse width (Read)	60	-	ns	
	Tslr	SCL"L" pulse width (Read)	60	-	ns	
SDI	TSDS	Data setup time	10	-	ns	-
	Tsdh	Data hold time	10	-	ns	
	Tacc	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	Toh	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSA=VSS=0V

Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.3 Reset Timing



Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

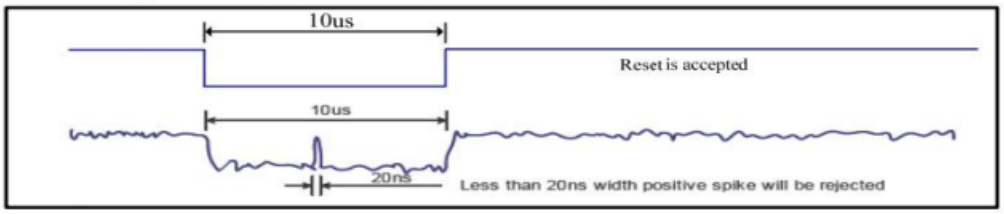
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms..The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

8 RGB Interface Selection

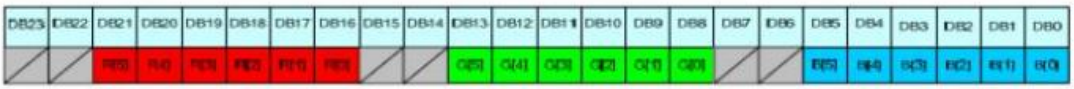
The RGB interface is operated with VS, HS, DE, PCLK, D[23:0] lines.It supports several pixel formats that can be selected by dpi [2:0] bits in "Interface Pixel Format (R3Ah)" of Page 0 command. The selection of a given interface is defined by dpi [2:0] as show in the below table

RGB Interface Selection

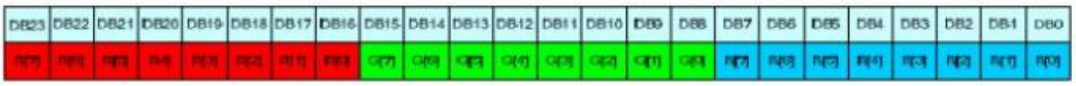
dpi[2:0]			RGB Interface Mode	Used Pins
1	0	1	16-bit RGB interface	VS,HS,DE,PCLK,D[20:16],D[13:8],D[4:0]
1	1	0	18-bit RGB interface	VS,HS,DE,PCLK,D[21:16],D[13:8],D[5:0]
1	1	1	24-bit RGB interface	VS,HS,DE,PCLK,D[23:0]
Others			Setting prohibited	

16-bit DPI interface connection:set pixel format DPI[2:0]=3'h5

18-bit DPI interface connection:set pixel format DPI[2:0]=3'h6



24-bit DPI interface connection:set pixel format DPI[2:0]=3'h7



RGB Interface 16/18/24-bit pixel format selection

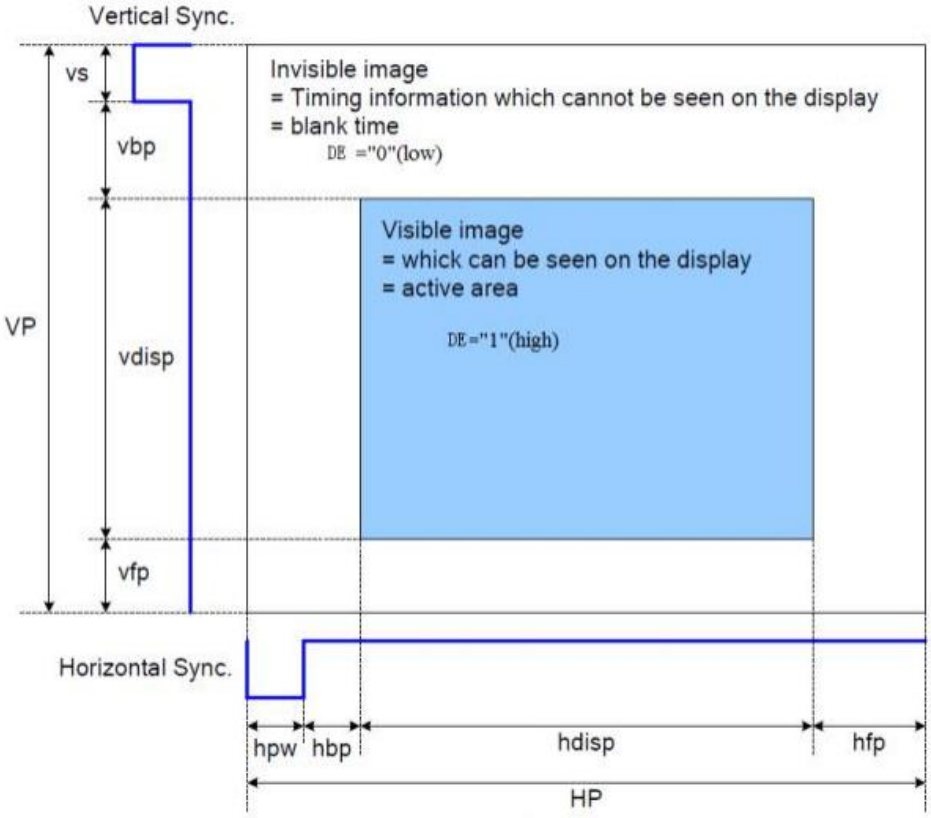
The Pixel clock (PCLK) is running all the time without stopping, it is used for entering VS, HS, DE and D[23:0] states when there is a rising edge of the PCLK. The PCLK can not be used as the internal clock for other functions of the display module.

Vertical sync hronization (VS) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchroni zation (HS) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal .

DE (Data Enable) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal.

D[23:0] are used to tell what is the information of the image that is transferred on the display(When DE= '0' (low) and there is a rising edge of PCLK). D[23:0] can be '0' (low) or '1'(high). These lines are read by a rising edge of the PCLK signal.



DRAM Access Area by RGB Interface

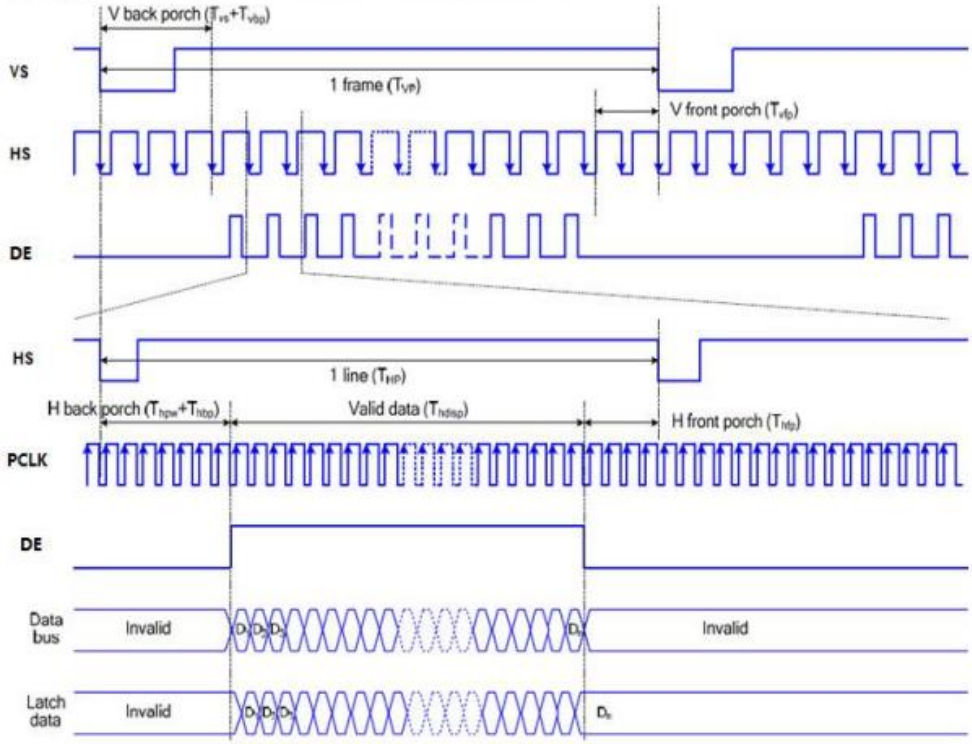
8.1 RGB Interface Mode Selection

NV3052CGRB supports two kinds of RGB interface, DE mode and SYNC mode.The table shown below uses command 23h to select RGB interface mode.

sync_mode[1:0]	RGB Mode
00	SYNC+DE mode
01	SYNC mode
10	DE mode
11	SYNC+DE mode

8.2 RGB Interface Timing

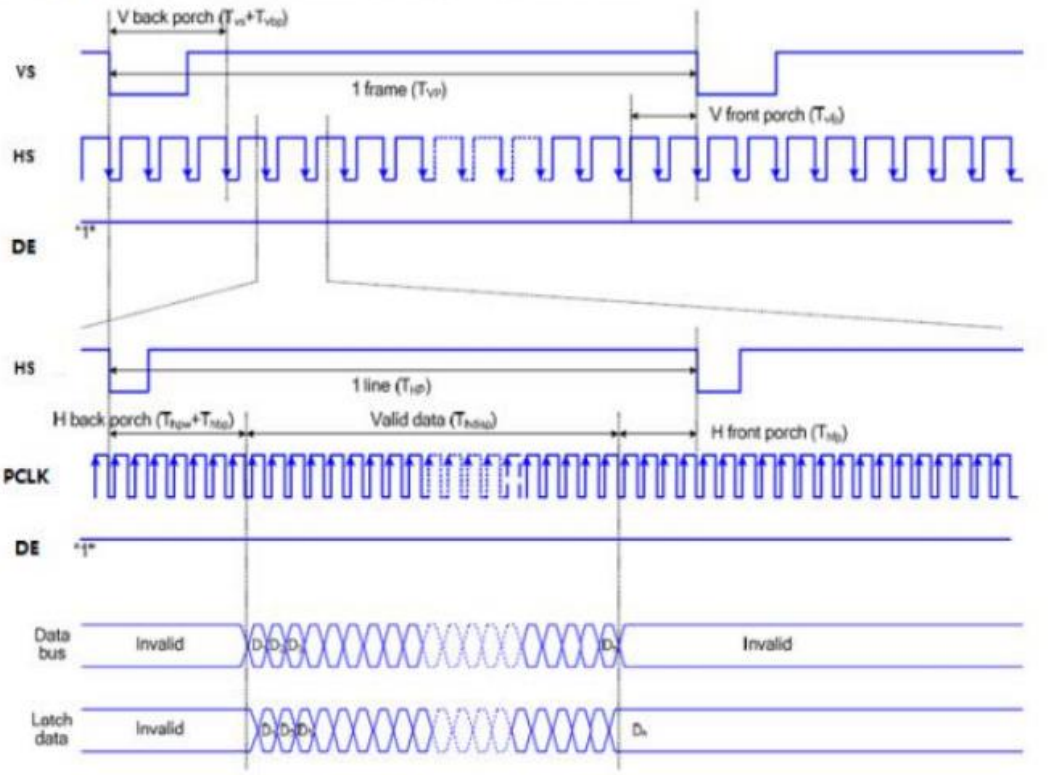
The timing chart of RGB interface DE mode is shown as follows.



Timing Chart of Signals in RGB Interface DE Mode

Note: The setting of front porch and back porch in host must match that in IC as this mode.

The timing chart of RGB interface SYNC mode is shown as follows.



Timing chart of RGB interface SYNC mode

Please refer to the following table for the setting limitation of RGB interface signals.

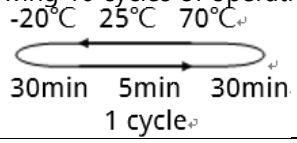
Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	37	--	MHz
Horizontal Sync. Width	hpw	1	4	255	Clock
Horizontal Sync. Back Porch	hbp	1	40	255	Clock
Horizontal Sync. Front Porch	hfp	1	44	--	Clock
Vertical Sync. Width	vs	1	4	254	Line
Vertical Sync. Back Porch	vbp	1	22	254	Line
Vertical Sync. Front Porch	vfp	1	16	--	Line

Note:

1. Typical value are related to the setting frame rate is 60Hz..

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-

Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation.  	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

10 Warranty and Conditions

http://www.displaymodule.com/pages/faqhttp://www.displaymodule.com/pages/faq