DisplayModule

DM-TFT40-388

4.0" IPS 480x480 HIGH BRIGHTNESS TFT DISPLAY PANEL –RGB

Contents

1 Revision History

Date	Changes
2019-05-17	First release
2019-07-16	Second release

2 Main Features

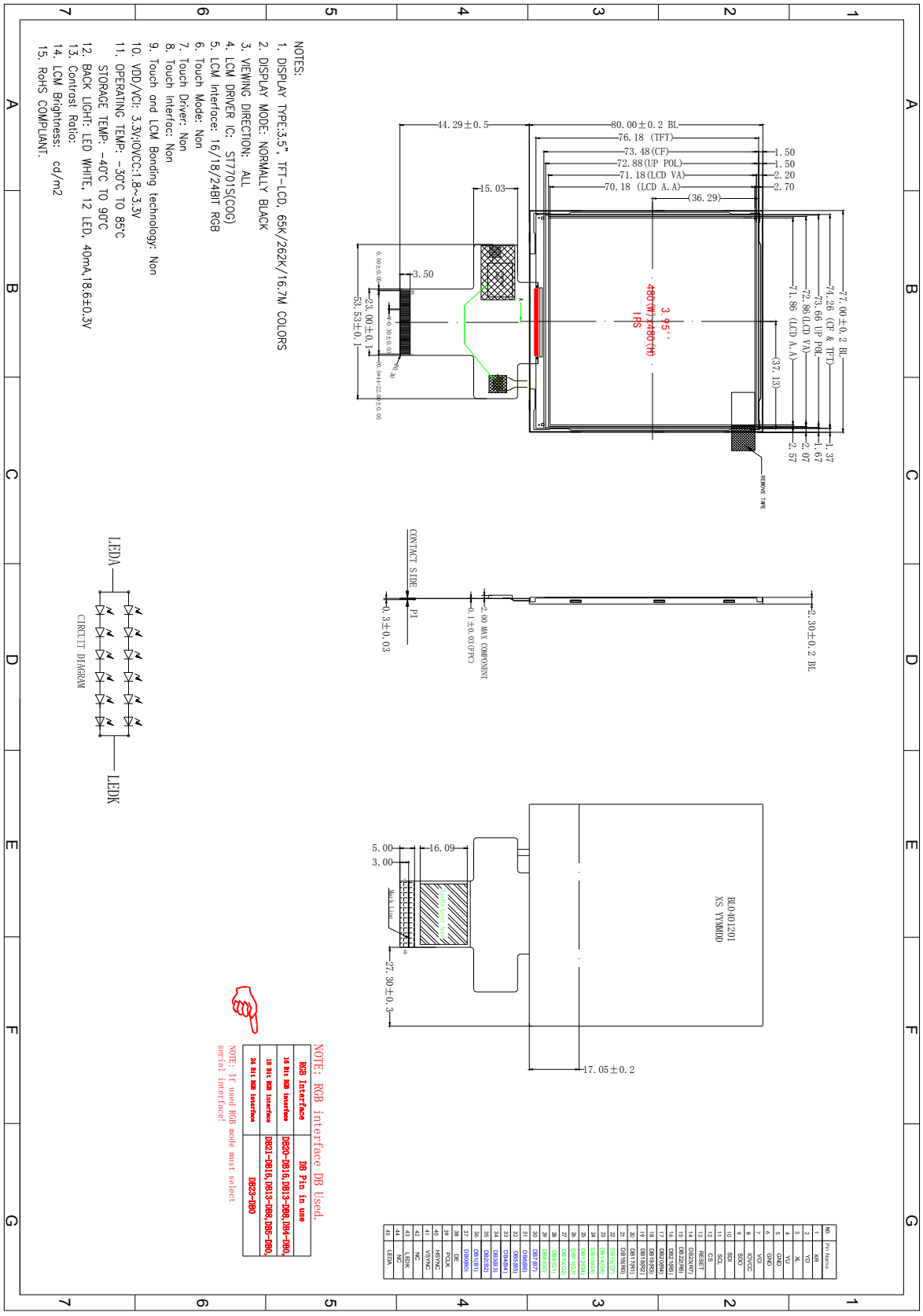
Item	Specification	Unit
Size	4.0	Inch
Resolution	480(RGB) x 480	pixel
Module Dimension	77.0 x 80.0 x 2.3	mm
Display area	71.86 x 70.18	mm
Pixel pitch	0.1497 x 0.1462	mm
TFT Controller IC	ST7701S	-
CTP Driver IC	None	-
Interface	16/18/24bit RGB	-
Display Color	65K/262K/16.7M	colors
Pixel arrangement	RGB vertical stripe	
View Direction	ALL	O'clock
Display mode	Transmissive /Normally Black	-
Weight	30	g

3 Pin Description

3.1 TFT

No.	Symbol	Description
1	XR	Touch panel Right Glass Terminal
2	YD	Touch panel Bottom Film Terminal
3	XL	Touch panel LIFT Glass Terminal
4	YU	Touch panel Top Film Terminal
5	GND	Ground.
6	GND	Ground.
7	VCI	Supply voltage (3.3V).
8	IOVCC	Supply Voltage (Logic)(1.8~3.3V).
9	SDO	Serial data output pin used for the SPI Interface. Leave the pin open when not in use.
10	SDI	SDI: Serial data input/output bidirectional pin for SPI Interface. Fix to GND level when not in use.
11	SCL	SCL: Serial clock input for SPI interface. Fix to IOVCC or GND level when not in use.
12	CS	- A chip select signal Low: the chip is selected and accessible High: the chip is not selected and not accessible Fix to IOVCC or GND level when not in use.
13	RESET	- The external reset input - Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
14-37	DB23-DB0	24-bit parallel data bus for RGB Interface. Fix to IOVCC or GND level when not in use.
38	DE	Data enable signal for RGB interface operation Low: access enabled High: access inhibited Fix to IOVCC or GND level when not in use.
39	PCLK	Dot clock signal for RGB interface operation Fix to IOVCC or GND level when not in use.
40	HSYNC	Line synchronizing signal for RGB interface operation Fix to IOVCC or GND level when not in use.
41	VSYNC	Frame synchronizing signal for RGB interface operation Fix to IOVCC or GND level when not in use.
42	NC	
43	LEDK	Cathode pin of backlight.
44	NC	
45	LEDA	Anode pin of backlight.

4 Mechanical Drawing



5 Optics & Electrical Characteristics

5.1 Optics Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
View Angles TOP	ΘU	70	80	-	deg	CR ≥ 10
View Angles Bottom	ΘD	70	80	-	deg	
View Angles Right	ΘR	70	80	-	deg	
View Angles Left	ΘL	70	80	-	deg	
C.I.E(Red)	(x) (y)	0.571 0.323	0.611 0.363	0.651 0.403	-	Θ=0 Normal viewing angle
C.I.E(Green)	(x) (y)	0.277 0.530	0.317 0.570	0.357 0.610	-	
C.I.E(Blue)	(x) (y)	0.110 0.060	0.150 0.100	0.190 0.140	-	
C.I.E(White)	(x) (y)	0.269 0.310	0.309 0.350	0.349 0.390	-	
Uniformity	S(%)	55	60	-	%	C-light
Response Time	$T_R + T_F$	-	25	35	ms	-
Contrast Ratio	CR	640	800	-	--	-

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

5.2 Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Digital Supply Voltage	VCI	-0.3	-	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	-	4.6	V
Operating Temperature	T_{OP}	-30	-	+85	℃
Storage Temperature	T_{ST}	-40	-	+90	℃
LED Forward Current	I_F	35	40	-	mA
LED Forward Voltage	V_F	-	18.6	-	V

Note 1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.3 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Digital Supply Voltage	VCI	2.5	3.3	3.6	V
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3	V
Normal mode Current	ICC	--	30	--	mA
Low Level Input Voltage	V_{IL}	GND	-	0.3 x IOVCC	V
High Level Input Voltage	V_{IH}	0.7 x IOVCC	-	IOVCC	V
Low Level Output Voltage	V_{OL}	GND	-	0.2 x IOVCC	V
High Level Output Voltage	V_{OH}	0.8 x IOVCC	-	IOVCC	V

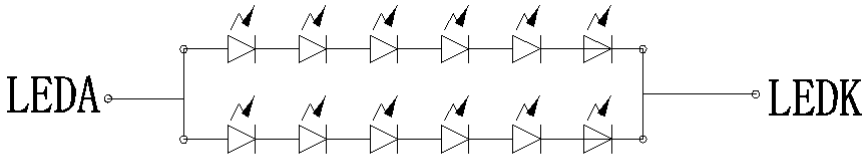
5.4 LED Backlight Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	IF	35	40	-	mA	
Forward Voltage	VF	-	18.6	-	V	
LCM Luminance (IF =20mA)	LV	950	1000	-	cd/m^2	Note3
LED life time	Hr	-	50000	-	Hour	Note1,2
Uniformity	Avg	80	-	-	%	Note3

The back-light system is edge-lighting type with 12 chips LED.

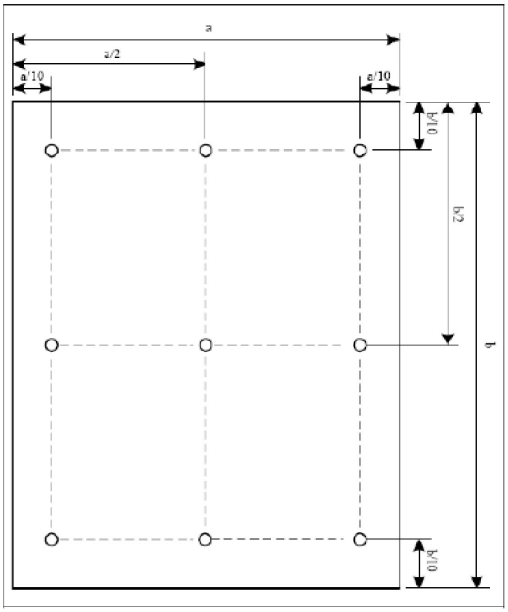
Note1:LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note2:The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

Note3:Luminance Uniformity of these 9 points is defined as below:

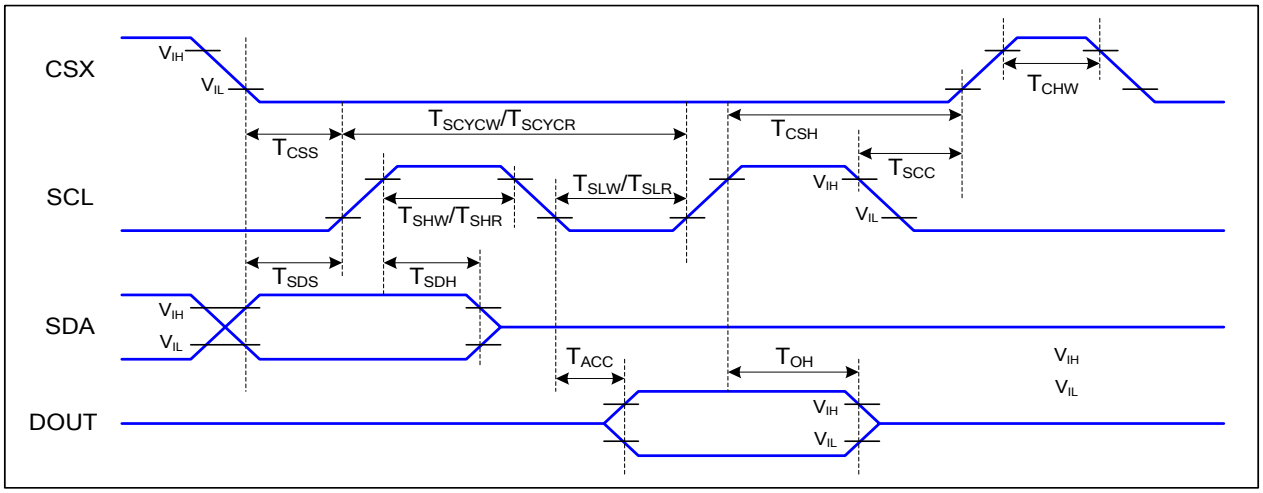


$$\text{Uniformity} = \frac{\text{minimun luminance in 9 point(1 - 9)}}{\text{maximun luminance in 9 point(1 - 9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

5.5 AC Characteristics

5.5.1 Serial Interface Characteristics (3-line serial):



3-line serial Interface Timing Characteristics

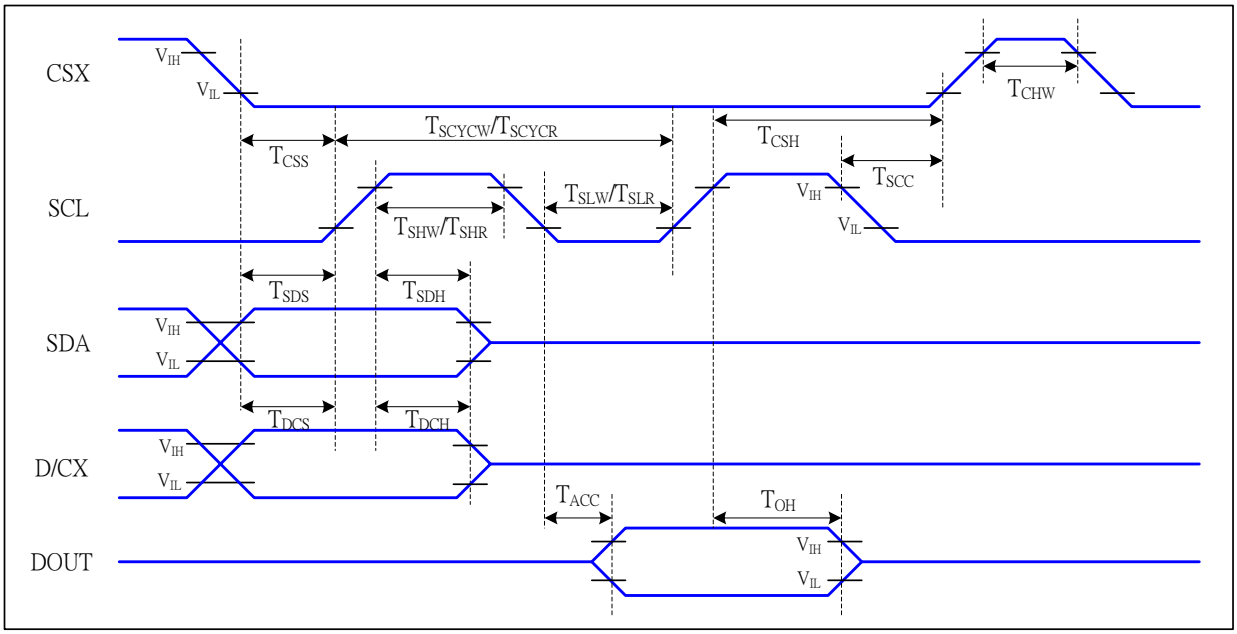
IOVCC=1.8V,VCI=2.8V,Ta=25℃

Signal	Symbol	Description	Min	Max	Unit	Remark
CSX	T_{CSS}	Chip Select Setup Time (Write)	15	-	ns	
	T_{CSH}	Chip Select Hold Time (Write)	15	-	ns	
	T_{CSS}	Chip Select Setup Time (Read)	60	-	ns	
	T_{SCC}	Chip Select Hold Time (Read)	60	-	ns	
	T_{CHW}	Chip Select “H” Pulse Width	40	-	ns	
SCL	T_{SCYCW}	Serial Clock Cycle (Write)	66	-	ns	
	T_{SHW}	SCL “H” Pulse Width (Write)	15	-	ns	
	T_{SLW}	SCL “L” Pulse Width (Write)	15	-	ns	
	T_{SCYCR}	Serial Clock Cycle (Read)	150	-	ns	
	T_{SHR}	SCL “H” Pulse Width (Read)	60	-	ns	
	T_{SLR}	SCL “L” Pulse Width (Read)	60	-	ns	
SDA (DIN)	T_{SDS}	Data Setup Time	10	-	ns	
	T_{SDH}	Data Hold Time	10	-	ns	

3-line serial Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

5.5.2 Serial Interface Characteristics (4-line serial):



4-line serial Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

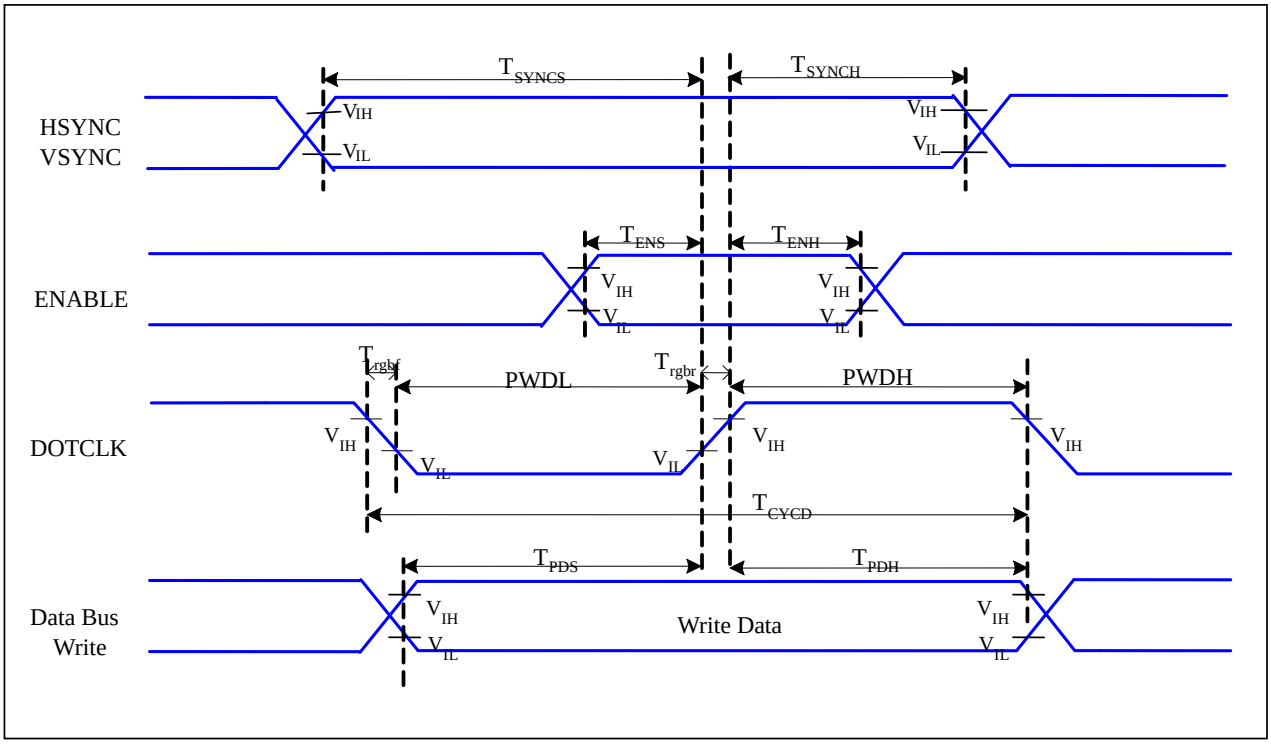
Signal	Symbol	Description	Min	Max	Unit	Remark
CSX	T_{CSS}	Chip Select Setup Time (Write)	15	-	ns	
	T_{CSH}	Chip Select Hold Time (Write)	15	-	ns	
	T_{CSS}	Chip Select Setup Time (Read)	60	-	ns	
	T_{SCC}	Chip Select Hold Time (Read)	65	-	ns	
	T_{CHW}	Chip Select “H” Pulse Width	40	-	ns	
SCL	T_{SCYCW}	Serial Clock Cycle (Write)	66	-	ns	-Write Command & Data Ram
	T_{SHW}	SCL “H” Pulse Width (Write)	15	-	ns	
	T_{SLW}	SCL “L” Pulse Width (Write)	15	-	ns	
	T_{SCYCR}	Serial Clock Cycle (Read)	150	-	ns	-Read Command & Data Ram
	T_{SHR}	SCL “H” Pulse Width (Read)	60	-	ns	
	T_{SLR}	SCL “L” Pulse Width (Read)	60	-	ns	
D/CX	T_{DCS}	D/CX Setup Time	10	-	ns	
	T_{DCH}	D/CX Hold Time	10	-	ns	
SDA (DIN)	T_{SDS}	Data Setup Time	10	-	ns	
	T_{SDH}	Data Hold Time	10	-	ns	

4-line serial Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

5.5.3 RGB Interface Characteristics :

IOVCC=1.8V,VCI=2.8V,Ta=25℃

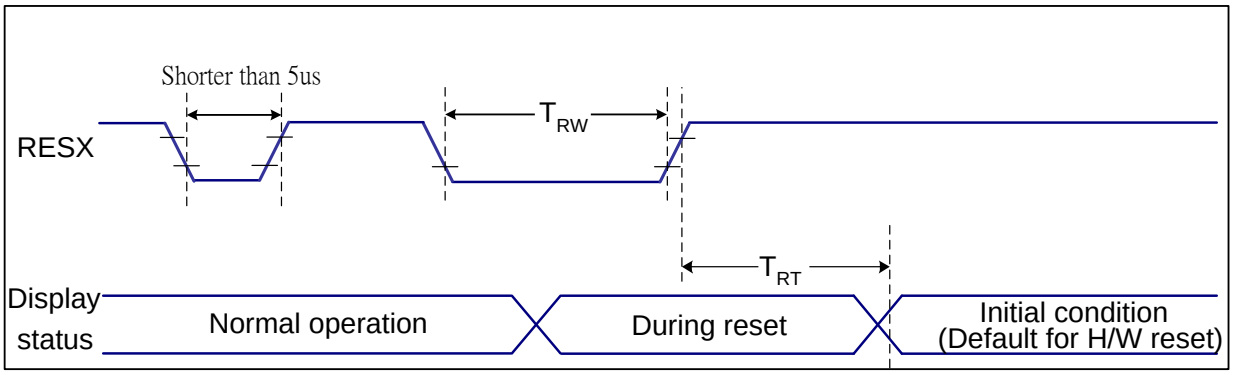


RGB Interface Timing Characteristics

Signal	Symbol	Description	Min	Max	Unit	Remark
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

18/16 Bits RGB Interface Timing Characteristics

5.5.4 Reset input timing:



VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

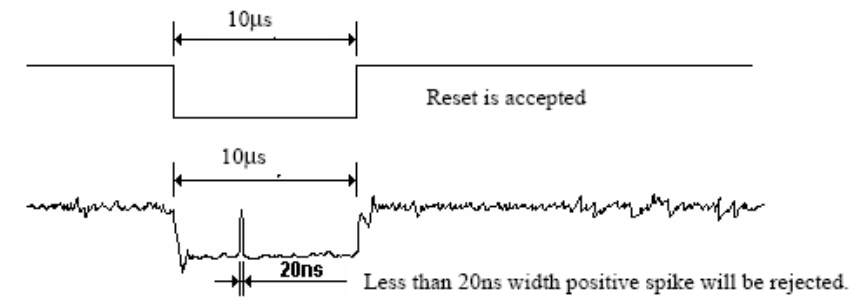
Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset Pulse Duration	10	-	µs
	TRT	Reset Cancel	-	5(Note 1,5)	ms
			-	120(Note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset Starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6 RGB Interface

The ST7701 support RGB interface Mode 1 and Mode 2. The interface signals as shown in ST7701S datasheet table 7.3.1.The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note.In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state.The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to ST7701.In RGB Mode 2, back porch of Vsync is defined by VBP[5:0] of RGBPRCTR command. And back porch of Hsync is defined by HBP[5:0] of RGBPRCTR command. Front porch of Vsync is defined by VFP[5:0] of RGBPRCTR command. And front porch of Hsync is defined by HFP[5:0] of RGBPRCTR command.

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HS	Horizontal sync	Horizontal synchronization timing signal
VS	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
DB[23:0]	Pixel data	Pixel data in 16-bit,18-bit and 24-bit format

The interface signals of RGB interface

6.1 RGB Color Format

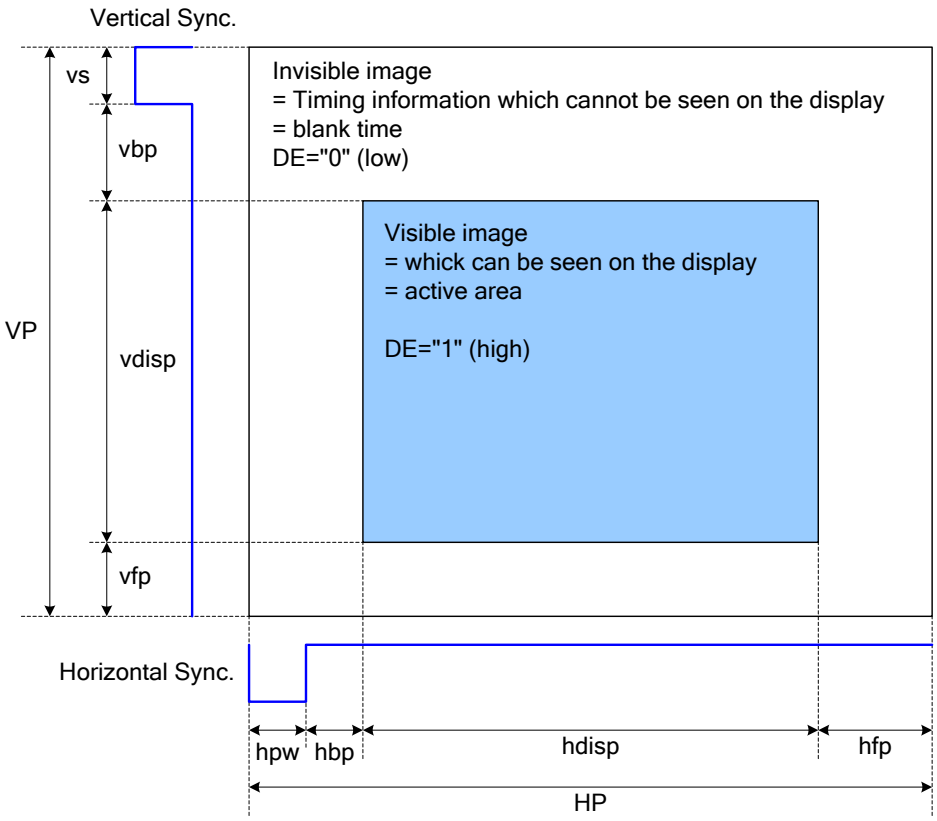
ST7701 supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24 bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[17:0] pins can be used;when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[17:0] pins can be used. When using RGB interface, only serial interface can be selected.

Pad name	24 bits configuration VIPF[3:0]=0111	18 bits configuration VIPF[3:0]=0110		16 bits configuration VIPF[3:0]=0101
		MDT=0	MDT=1	
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	R0	R0	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	B7	Not used	G1	Not used
DB[06]	B6	Not used	G0	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	B3	B3	B3	B3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	B0	B0	B0	B0

The interface color mapping of RGB interface

6.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	-	(17)	-	MHz
Horizontal Sync. Width	hpw	1	(8)	255	Clock
Horizontal Sync. Back Porch	hbp	1	(50)	255	Clock
Horizontal Sync. Front Porch	hfp	1	(10)	-	Clock
Vertical Sync. Width	vs	1	(8)	254	Line
Vertical Sync. Back Porch	vbp	1	(20)	254	Line
Vertical Sync. Front Porch	vfp	1	(10)	-	Line

Note:
Typical value are related to the setting frame rate is 60Hz..s

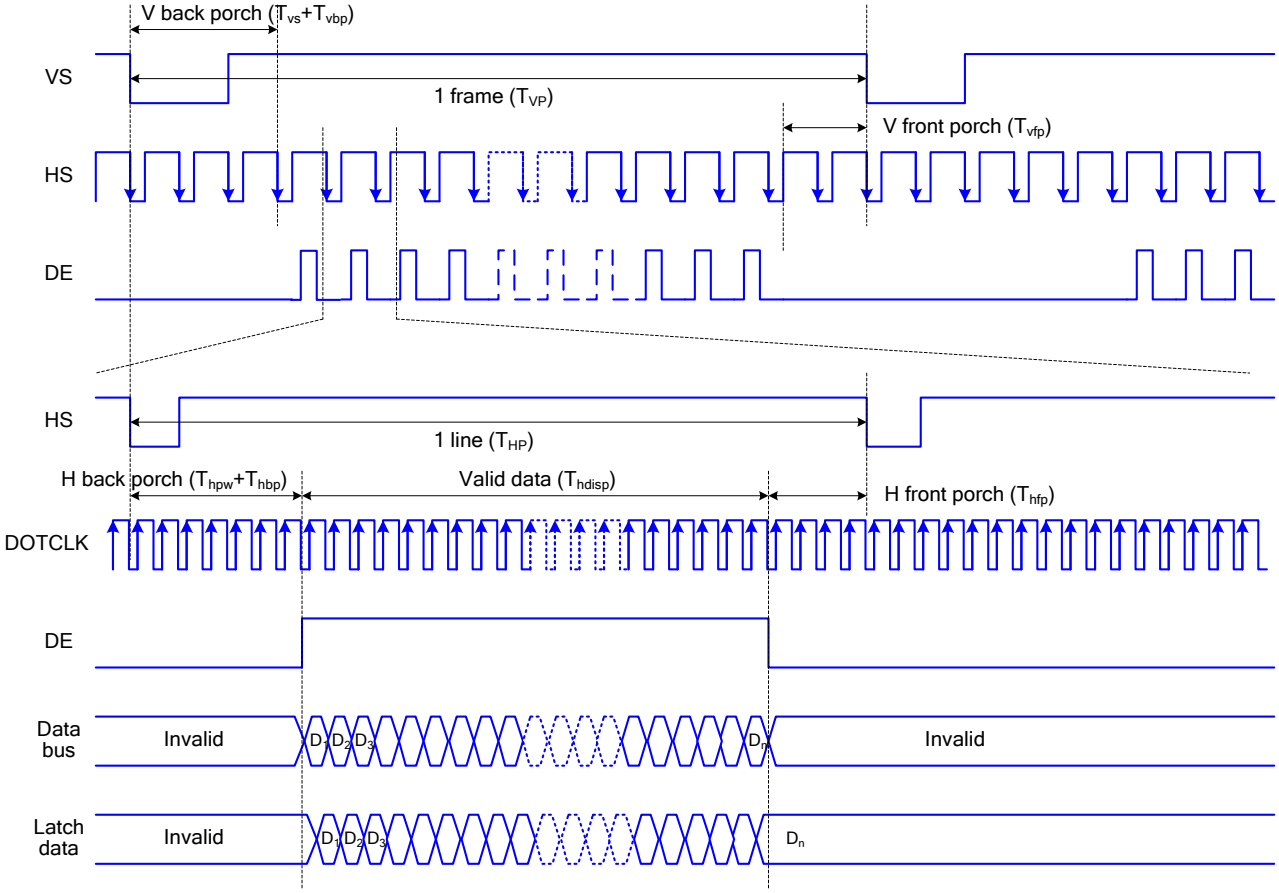
6.3 RGB Interface Mode Selection

ST7701 supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/Sync	RGB Mode
0	DE mode
1	HV mode

6.4 RGB Interface Timing

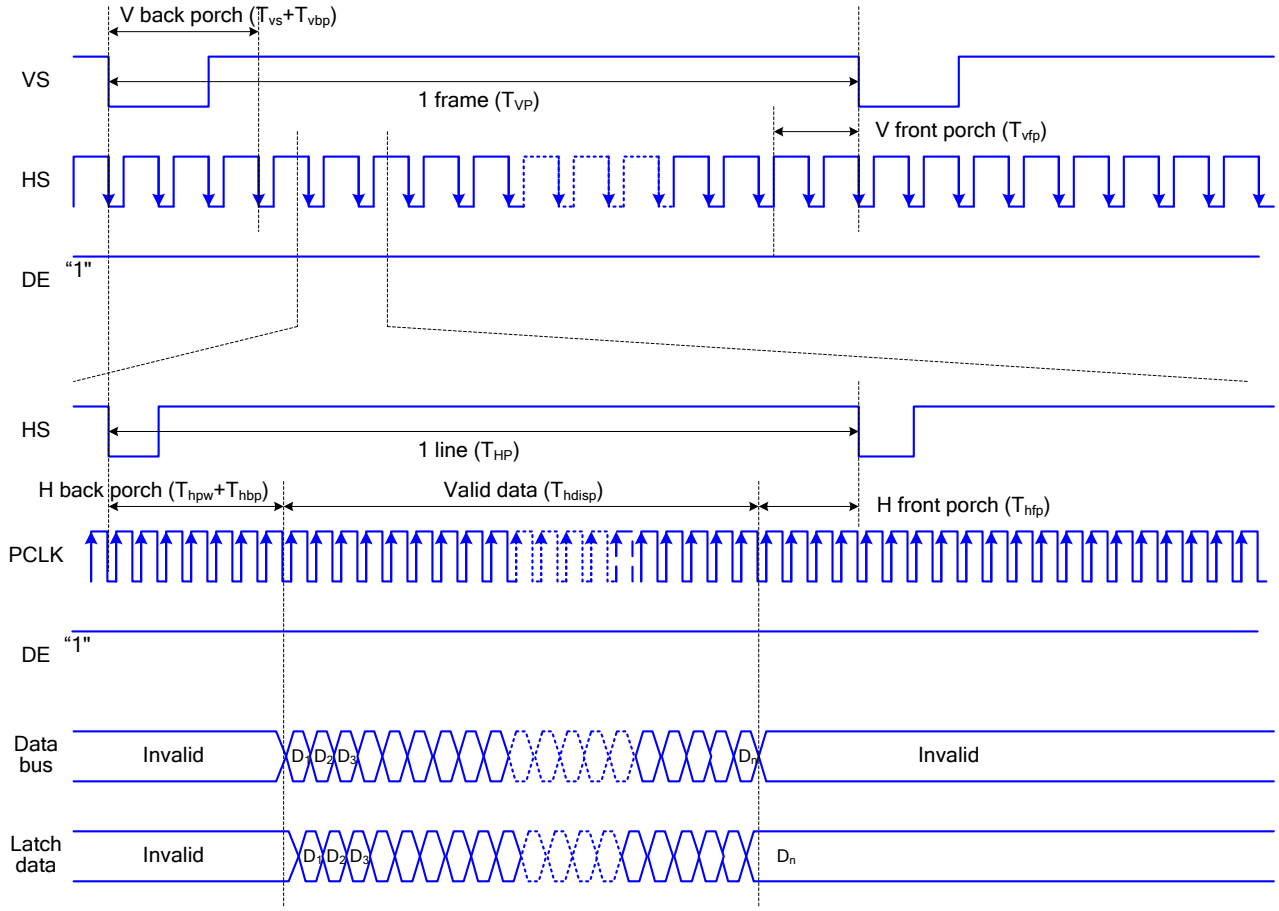
The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



Timing Chart of RGB Interface HV Mode

7 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	90°C 96hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 96hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85°C 96hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30°C 96hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation.	-30°C/85°C 20 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55 Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	C=150pF, R=330,5points /panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

8 Warranty and Conditions

http://www.displaymodule.com/pages/faq