DisplayModule

DM-TFT40-380

4.0" 320x480 DISPLAY PANEL WITH CAPACITIVE TOUCH – SPI ,MCU, RGB

Contents

1 Revision History

Date	Changes
2018-11-13	First release

2 Main Features

Item	Specification	Unit
Size	4.0	Inch
Resolution	320(RGB) x 480	pixel
Module Dimension	62.0 x 95.0 x 4.08	mm
Display area	55.68 x 83.52	mm
Pixel pitch	0.174 x 0.174	mm
TFT Controller IC	ILI9488	-
CTP Driver IC	GT911	-
Interface	8/9/16/18 Bit MCU 3/4SPI+16/18bit RGB 3-line/4-line Serial	-
Display Color	262K	colors
View Direction	12	O'clock
Touch mode	Five points and Gestures	-
Display mode	Transmissive /LED Normally white	-
Weight	TBD	g

3 Pin Description

3.1 TFT

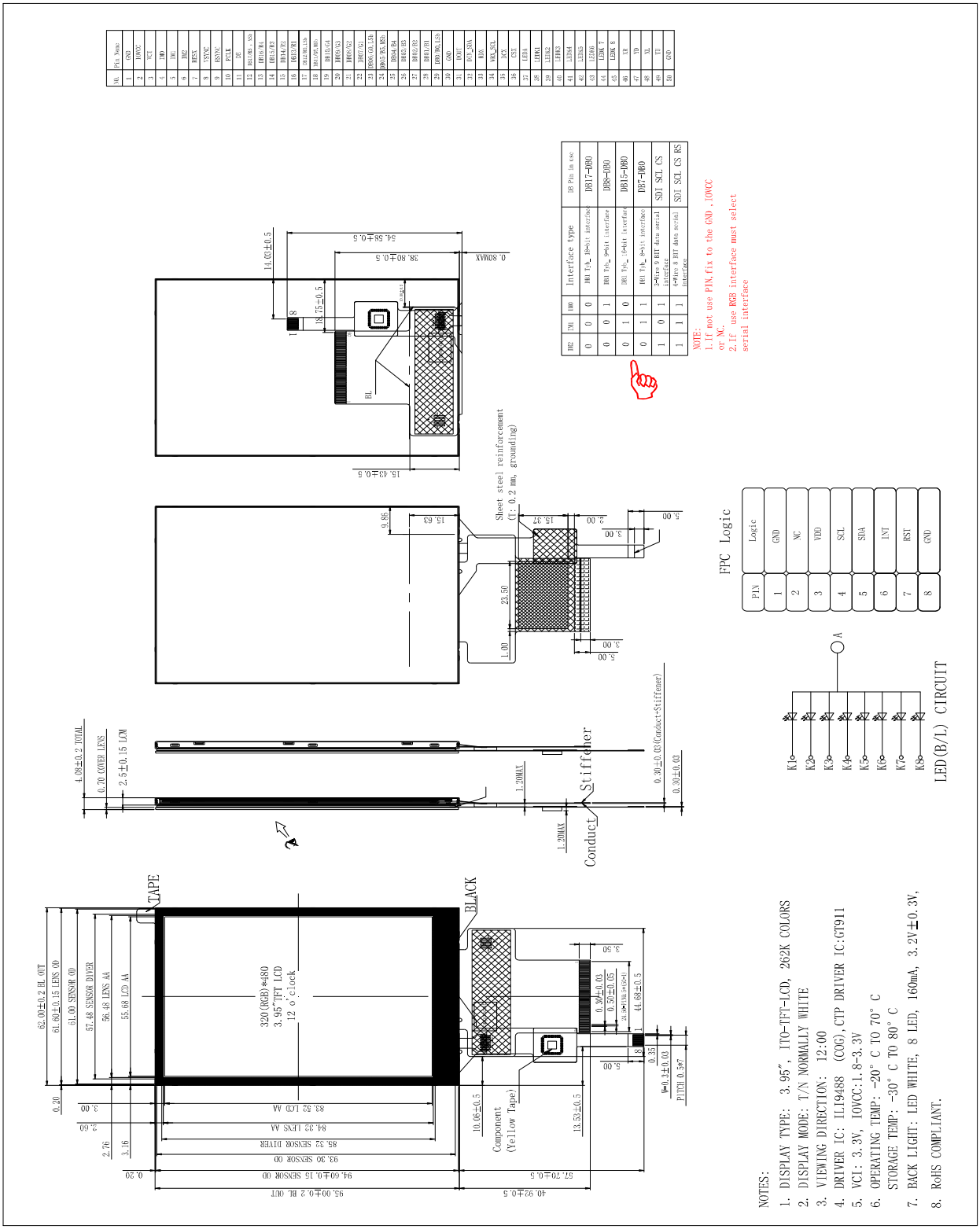
No.	Symbol	Description
1	GND	Ground.
2	IOVCC	Supply voltage(1.8-3.3V)
3	VCI	Supply voltage(3.3V).
4	IM0	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at VCI and GND.
5	IM1	
6	IM2	
7	RESX	This signal will reset the device and must be applied to properly initialize the chip.
8	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.
9	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use
10	PCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.
11	DE	Data enable signal for RGB interface operation. Fix this pin at VCI or GND when not in use.
12-29	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use
30	GND	Ground.
31	DOUT	Serial data output pin in serial bus system interface. If not used, please open this pin.
32	DIN_SDA	Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VCI or GND.
33	RDX	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.
34	WRX_SCL	DBI Type B: WRX pin, serves as a write signal DBI Type C: SCL pin as Serial Clock when operates in the serial interface
35	DCX	Display data/ command selection pin
36	CSX	Chip select input pin (“Low” enable). fix this pin at VCI or GND when not

		in use.
37	LEDA	Anode pin of backlight
38-45	LEDK1-K7	Cathode pin OF backlight
46	XR	Touch panel Right Glass Terminal
47	YD	Touch panel Bottom Film Terminal
48	XL	Touch panel Left Glass Terminal
49	YU	Touch panel Top Film Terminal
50	GND	Ground.

3.2 CTP

No.	Symbol	Description
1	GND	Ground
2	NC	NC
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground

4 Mechanical Drawing



5 Electrical Characteristics

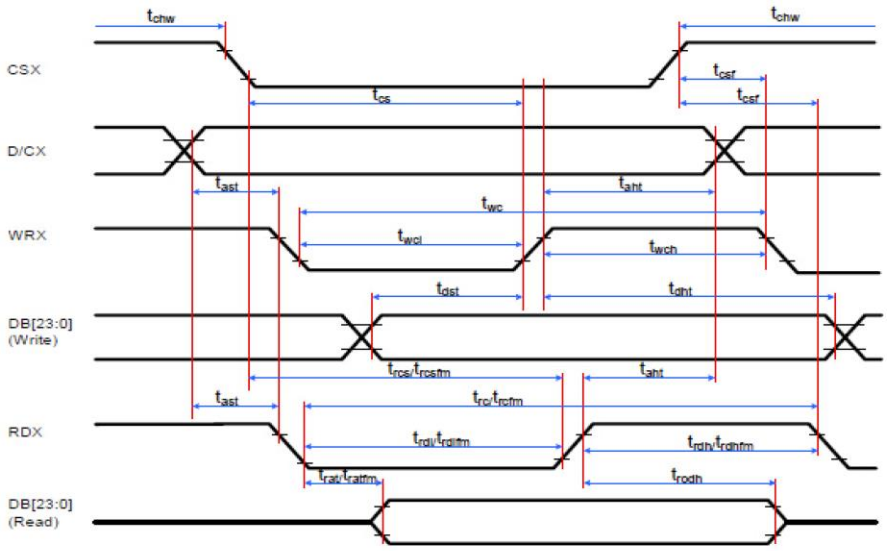
Item	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VCI		2.5	2.8	3.3	V
Normal mode Current	IDD		-	7	-	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃
LED Forward Current	If		120	160	-	mA
LED Forward Voltage	Vf		-	3.2	-	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	ΘU	-	70	-	deg
View Angles Bottom	ΘD	-	60	-	deg
View Angles Right	ΘR	-	70	-	deg
View Angles Left	ΘL	-	70	-	deg
Response Time	Tr +Tf		30	40	ms
Contrast Ratio	CR	-	500	-	--
LCM Luminance	Lv	-	400	-	cd/m^2

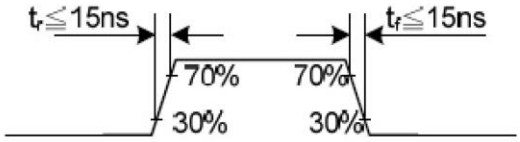
7 AC Characteristics

7.1 DBI Type B Timing Characteristics

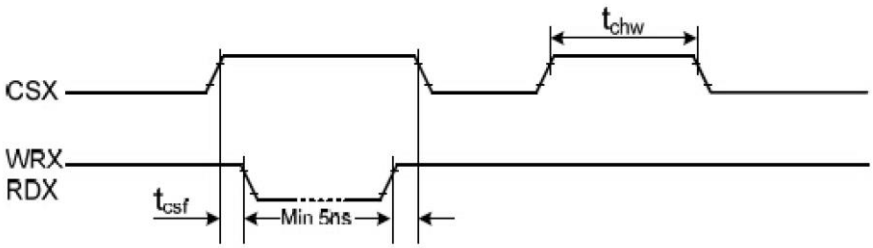


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	that	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	40	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

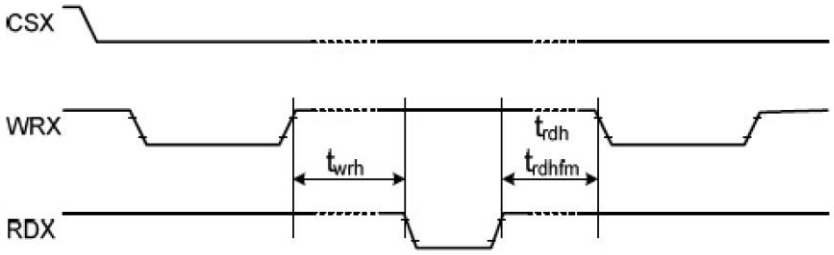
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V
2. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.
3. Input signal rising time and falling time:



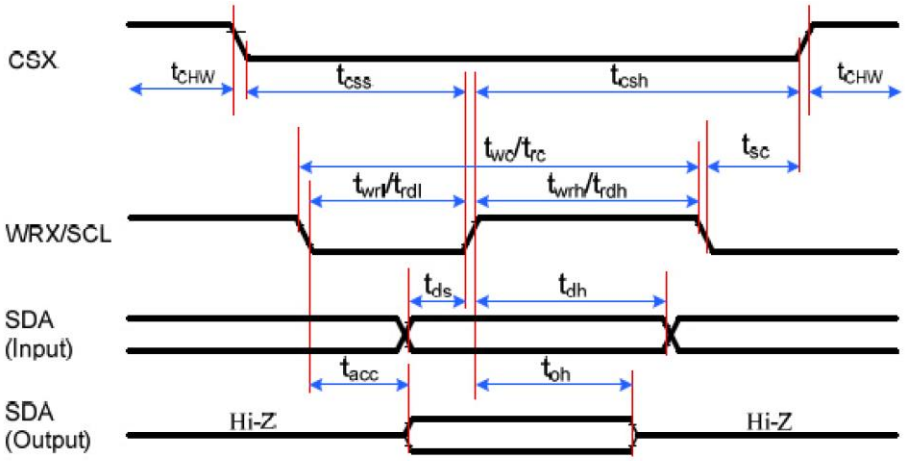
4. The CSX timing:



5. The Write to Read or the Read to Write timing:

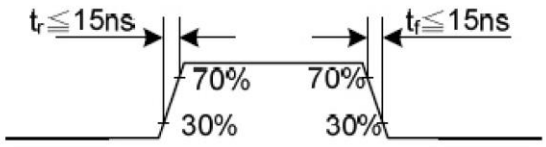


7.2 DBI Type C Option 1 (3-line SPI system) Timing Characteristics

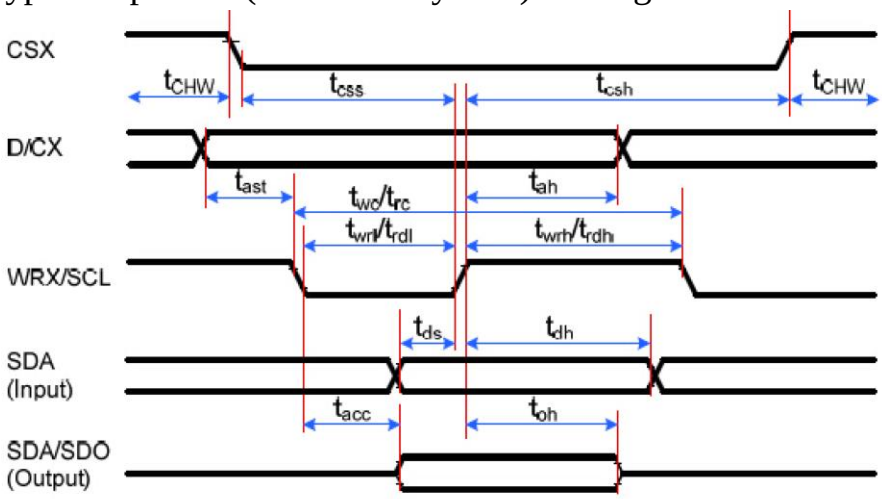


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H Pulse Width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial Clock Cycle (Write)	66	-	ns	
	twrh	SCL H Pulse Width (Write)	15	-	ns	
	twrl	SCL L Pulse Width (Write)	15	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL H Pulse Width (Read)	60	-	ns	
	trdl	SCL L Pulse Width (Read)	60	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.6V, VCI = 2.5V to 3.6V, AGND = DGND = 0V, T = 10+/-0.5ns



7.3 DBI Type C Option 3 (4-line SPI system) Timing Characteristics

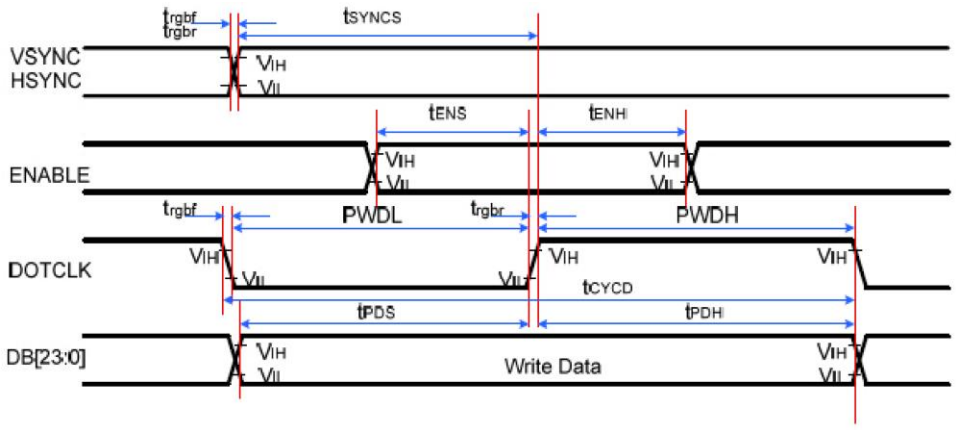


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS H pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	50	-	ns	
	twrh	SCL H pulse width (Write)	10	-	ns	
	twrl	SCL L pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	tod	Output disable time (Read)	15	50	ns	

Notes:

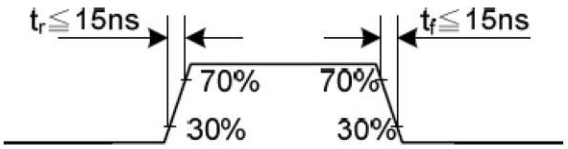
1. Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V, T = 10+/-0.5ns.
2. Does not include signal rising and falling times.

7.4 DBI (Display Parallel 16/18/24 bit interface) Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	16-/18-/24-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB [23:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	20	-	ns	
	PWDL	DOTCLK low-level period	20	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC = 1.65V to 3.3V, VCI = 2.5V to 3.3V, AGND = DGND = 0V



7.5 Reset Timing Characteristics

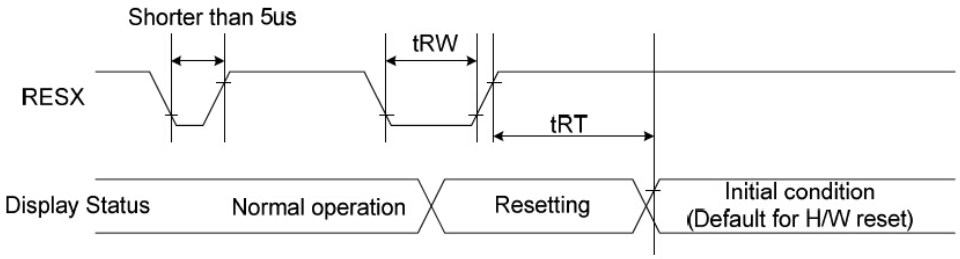


Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

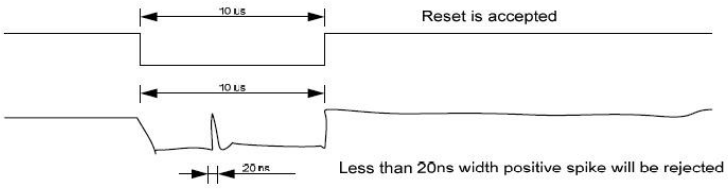
Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:



5. When Reset is applied during the Sleep In Mode.
6. When Reset is applied during the Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. The Sleep Out command also cannot be sent in 120msec.

8 CTP Specification

8.1 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	VDD		2.66	3.3	3.47	V
Normal mode Current			-	8	14.5	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃

NOTES:

If used beyond the absolute maximum ratings, FT6336G may be permanently damaged. It is strongly recommanded that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device

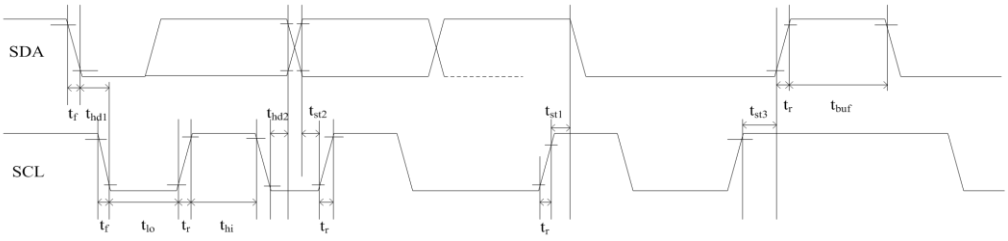
8.2 AC Characteristics

Item	Condition	Min	Typ	Max	Unit
OSC clock	AVDD=2.8V;Ta=25° C	59	60	61	MHz

AC characteristics of Oscillators

I2C Timing.

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



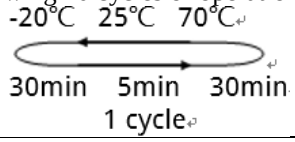
Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq