DisplayModule

DM-TFT40-336

4.0" IPS 480 X 800 TFT LCD DISPLAY PANEL WITH CAPACITIVE TOUCH - SPI, RGB

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1 Revision History

Date	Changes
2016-06-15	First release

2 Main Features

Item	Specification	Unit
Resolution	480(RGB) x 800	pixel
Module Dimension	66.84 x 111.50 x 4.13	mm
TFT Controller IC	ILI9806E	-
CTP Controller IC	GT911	
Interface	3SPI+16/18/24 bit RGB	-
Dot Pitch	0.108 x 0.108	mm
Display Color	65K/262K/16.7M	
View Direction	ALL	
Display mode	Transmissive	
Touch Points	5	-
Weight	TBD	g

3 Pin Description

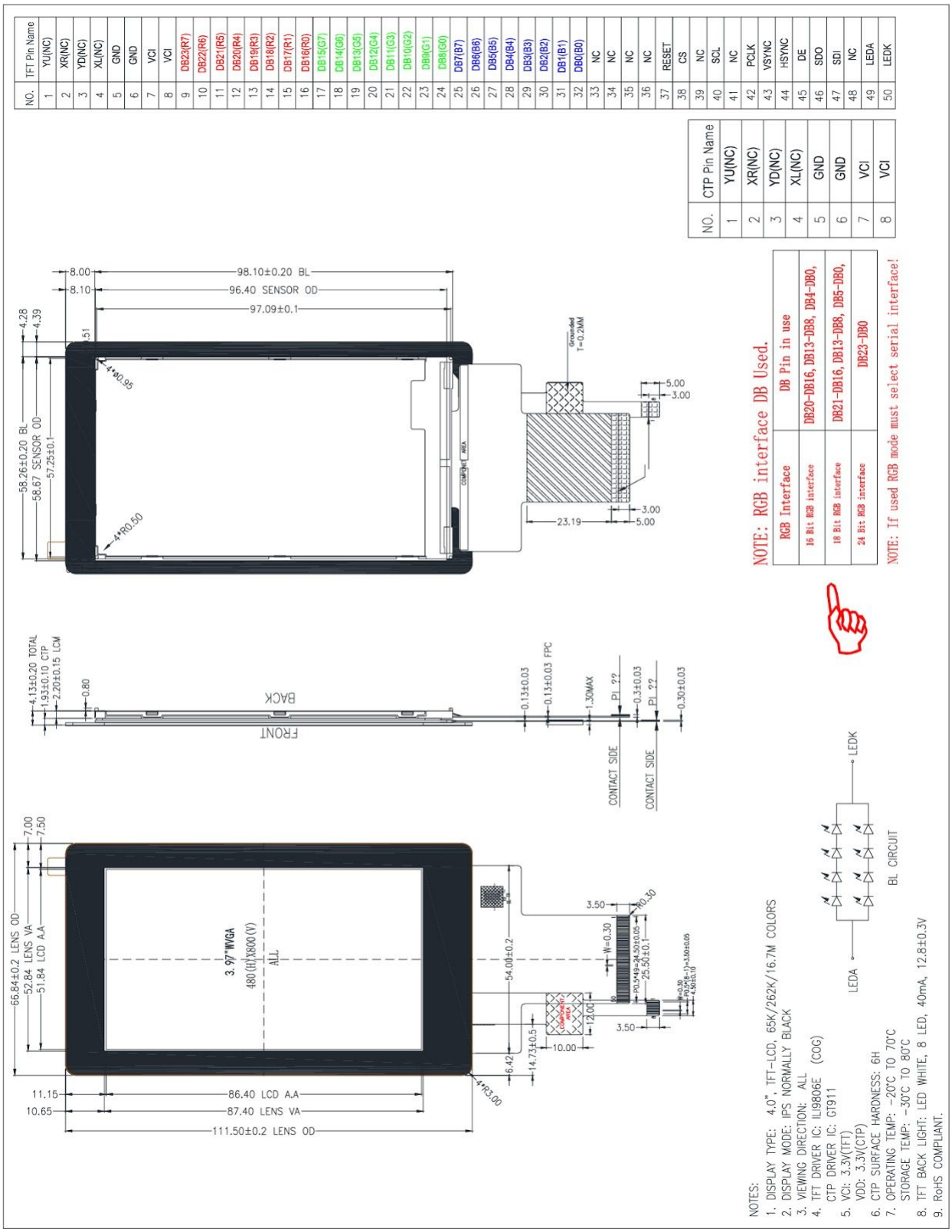
3.1 TFT

No.	Symbol	Description
1	YU(NC)	
2	XR(NC)	
3	YD(NC)	
4	XL(NC)	
5	GND	Ground
6	GND	Ground
7	VCI	Supply voltage (3.3V)
8	VCI	Supply voltage (3.3V)
9-32	DB23-DB0	Data bus PINS. -RGB data bus used. 24-bitbus: use DB23-DB0 18-bit bus: use DB21-DB16,DB13-DB8,DB5-DB0. 16-bit bus: use DB20-DB16,DB13-DB8,DB4-DB0 If not used PINS, please must connect to GND.
33-36	NC	
37	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
38	CS	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.
39	NC	
40	SCL	Serial clock input.
41	NC	
42	PCLK	Dot clock signal.
43	VSYNC	Frame synchronizing signal.
44	HSYNC	Line synchronizing signal.
45	DE	Data enable signal
46	SDO	Serial data output pin used for the SPI Interface. Leave the pin to open when not in use.
47	SDI	Serial data input pin used for the SPI Interface.
48	NC	
49	LEDA	Anode pin of backlight.
50	LEDK	Cathode pin of backlight.

3.2 CTP

No.	Symbol	Description
1	GND	Ground
2	VDDIO	I/O power supply voltage
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground

4 Mechanical Drawing



5 Electrical Characteristics

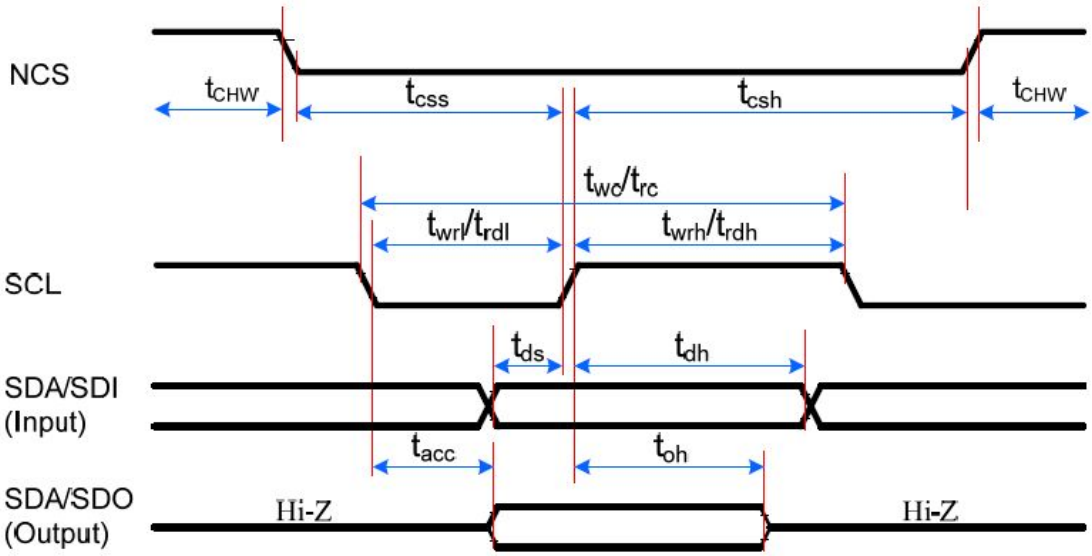
Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCI		3.0	3.3	4.2	V
I/O Digital Voltage	VDDIO		1.65	3.3	4.2	V
Input Current	IDD			30		mA
Low Level Input Voltage	V_{IL}		GND		$0.3V_{DDIO}$	V
High Level Input Voltage	V_{IH}		$0.7V_{DDIO}$		V_{DDIO}	V
Low Level Output Voltage	V_{OL}		GND		GND+0.4	V
High Level Output Voltage	V_{OH}		V_{DDIO}-0.4			V
Operating Temperature	TOP	Absolute Max	-20		+70	℃
Storage Temperature	TST	Absolute Max	-30		+80	℃

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	AV	80	85		deg
View Angles Bottom	AV	80	85		deg
View Angles Right	AH	80	85		deg
View Angles Left	AH	80	85		deg
Response Time	Tr +Tf		35		ms
Contrast Ratio	CR	550	800		--
LED Forward Current	If	30	40		mA
LED Forward Voltage	Vf		12.8		V
LCM Luminance	Lv	400			cd/m^2

7 Timing Characteristics

7.1 3-Line SPI Serial Interface Timing Characteristics

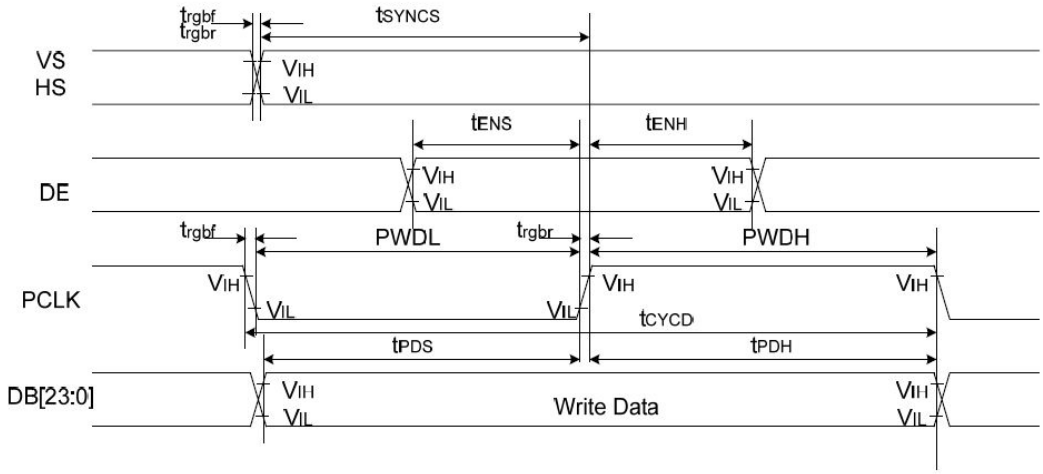


Item	Symbol	Min	Typ	Max	Unit
Chip select setup time (Write)	TCSS	15			ns
Chip select hold time (Read)	TCSH	15			ns
CS "H" pulse width	TCHW	40			ns
Serial clock cycle (Write)	TWC	30			ns
SCL "H" pulse width (Write)	TWRH	10			ns
SCL "L" pulse width (Write)	TWRL	10			ns
Serial clock cycle (Read)	TRC	150			ns
SCL "H" pulse width (Read)	TRDH	60			ns
SCL "L" pulse width (Read)	TRDL	60			ns
Access time (Read)	TACC	10		100	ns
Output disable time (Read)	TOH	15		100	ns
Data setup time (Write)	TDS	10			ns
Data hold time (Write)	TDH	10			ns

Note: 1. Ta=-30 to 70 ℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.

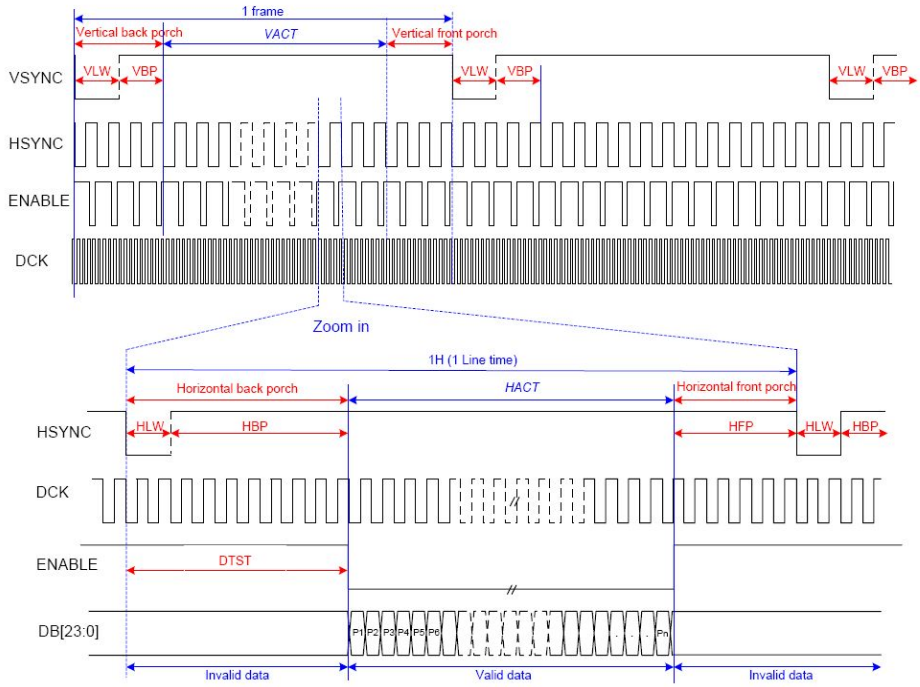
2. Does not include signal rise and fall times.

7.2 Parallel 24/18/16-bit RGB Interface Timing Characteristics



Item	Symbol	Min	Typ	Max	Unit
VS/HS setup time	tSYNCS	5			ns
VS/HS hold time	tSYNCH	5			ns
DE setup time	tENS	5			ns
DE hold time	tENH	5			ns
Data setup time	tPOS	5			ns
Data hold time	tPOH	5			ns
PCLK high-level period	PWDH	13			ns
PCLK low-level period	PWDL	13			ns
PCLK cycle time	tCYCD	28			ns
PCLK, HS, VS rise/fall time	Trgbr, trgbf			15	ns

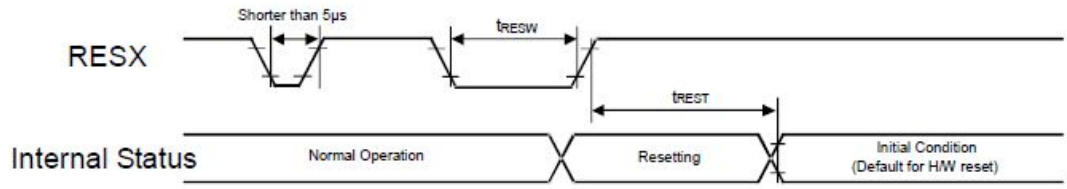
Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2···, pixel n.

Item	Symbol	Min	Typ	Max	Unit
Frame Rate	FR	54		66	fps
Horizontal Low Pulse width	HLW	1			DOTCLK
Horizontal Back Porch	HBP	2		126	DOTCLK
Horizontal Address	HACT		480		DOTCLK
Horizontal Front Porch	HFP	2			DOTCLK
Vertical Low Pulse width	VLW	1		126	Line
Vertical Back Porch	VBP	1		126	Line
Vertical Address	VACT			864	Line
Vertical Front Porch	VFP	1		255	Line
Data Clock	DCLK	16.6		41.7	MHz

7.3 Reset Input Timing



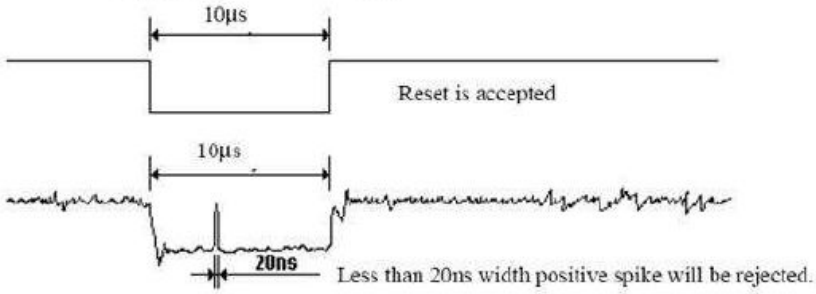
Reset Input Timing

Item	Symbol	Min	Typ	Max	Note	Unit
Reset low pulse width	tRESW	10				us
Reset complete time	tREST			5	When reset is applied during Sleep In mode	ms
				120	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µ	Reset Rejected
Longer than 10 µs	Reset
Between 5µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In -mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

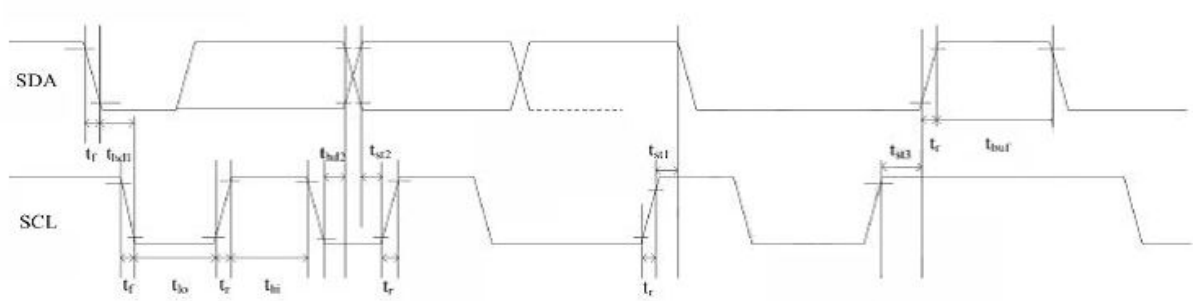
8 CTP Specification

8.1 Elective Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCI		2.8		3.3	V
I/O Digital Voltage	VDDIO		1.8		3.3	V
Input Current	IDD					mA
Low Level Input Voltage	V_{IL}		-0.3		$0.25V_{DDIO}$	V
High Level Input Voltage	V_{IH}		$0.75V_{DDIO}$		V_{DDIO}+0.3	V
Low Level Output Voltage	V_{OL}		-		$0.15V_{DDIO}$	V
High Level Output Voltage	V_{OH}		$0.85V_{DDIO}$		-	V
Operating Temperature	TOP	Absolute Max	-20		+70	℃
Storage Temperature	TST	Absolute Max	-30		+80	℃

8.2 I2C Interface

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Item	Symbol	Min	Typ	Max	Unit
SCL low period	t_{lo}	1.3			us
SCL high period	t_{hi}	0.6			us
SCL setup time for Start condition	t_{st1}	0.6			us
SCL setup time for Stop condition	t_{st3}	0.6			us
SCL hold time for Start condition	t_{hd1}	0.6			us
SDA setup time	t_{st2}	0.1			us
SDA hold time	t_{hd2}	0			us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

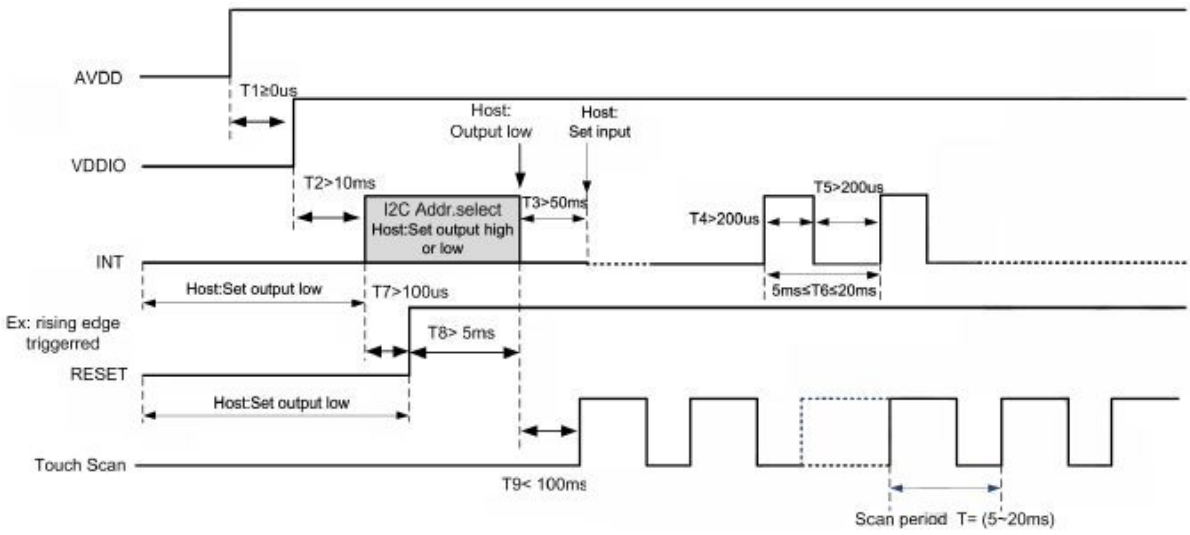
Item	Symbol	Min	Typ	Max	Unit
SCL low period	t_{lo}	1.3			us
SCL high period	t_{hi}	0.6			us
SCL setup time for Start condition	t_{st1}	0.6			us
SCL setup time for Stop condition	t_{st3}	0.6			us
SCL hold time for Start condition	t_{hd1}	0.6			us
SDA setup time	t_{st2}	0.1			us
SDA hold time	t_{hd2}	0			us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the

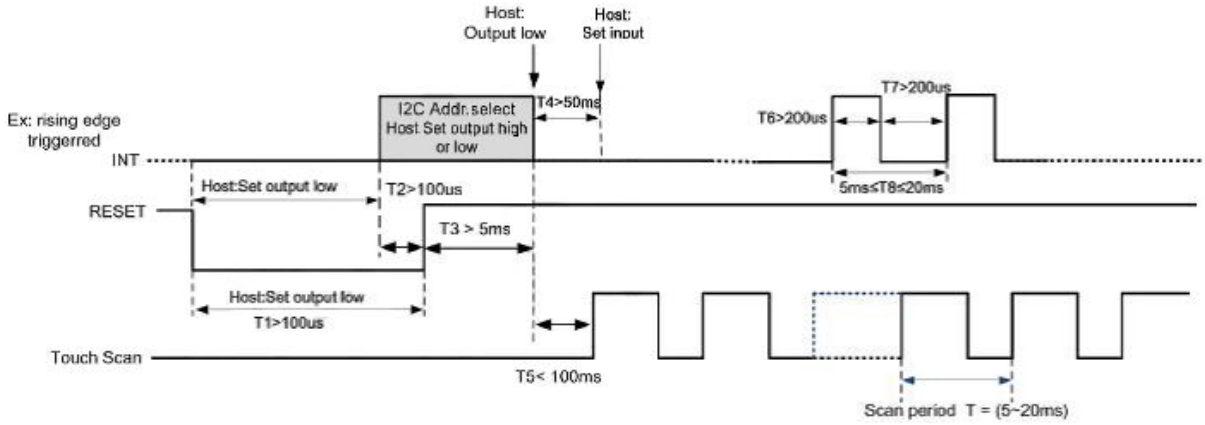
address by changing the status of Reset and INT pins during the power-on initialization phase. See the

diagram below for configuration methods and timings:

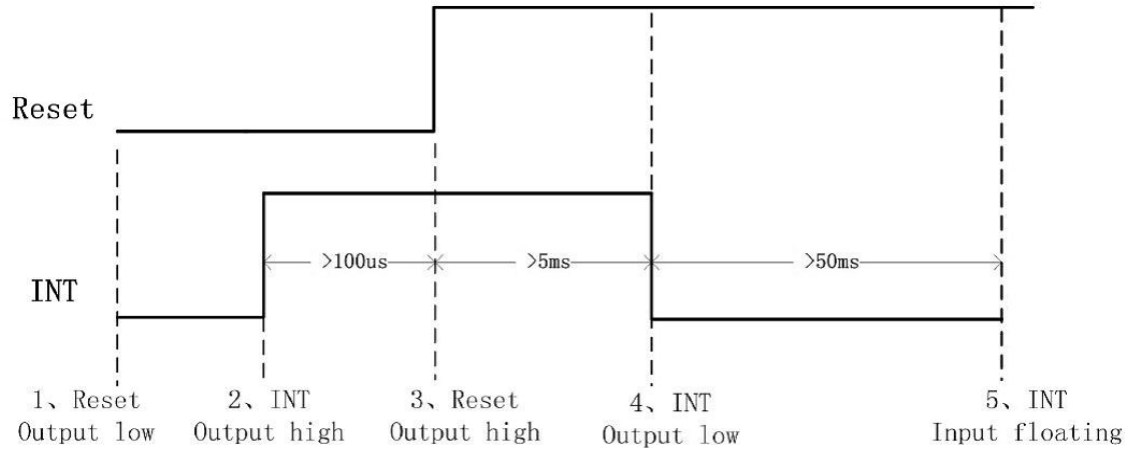
Power-On Timing:



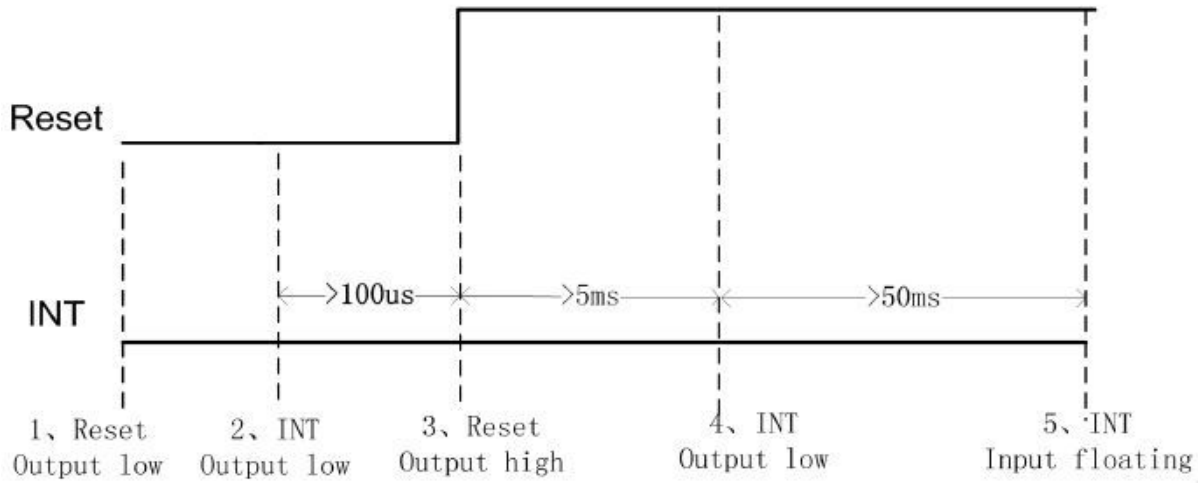
Timing for host resetting GT911:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



Data Transmission

(For example: device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL is “high”. Data flow or address is transmitted after the Start condition.

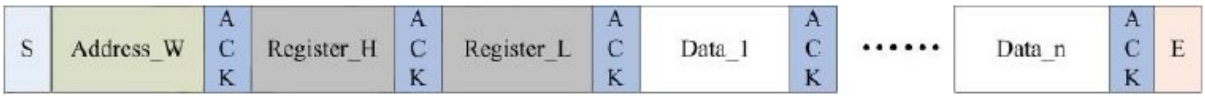
All slave devices connected to I2C bus should detect the 8-bit address issused after Start condition and send the correct ACK. After receiving matching address, GT911 achnowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

Writing Data to GT911

(For example: device address is 0xBA/0xBB)



Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends OXBA(address bits and R/W bit; R/W bit as 0 indicate Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes(to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

Reading Data from GT911

(For example: device address is 0xBA/0xBB)

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA(address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

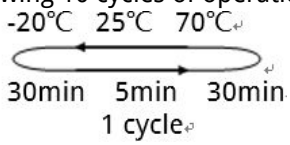
Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After rceiving ACK, the host starts to read data,

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

9 Driver/Controller Information

Built-in ILI9806E IC:
https://drive.google.com/file/d/0B5lkVYnewKTGUmVkSG4yMDl0SGs/view?usp=sharing
CTP GT911 Driver IC:
https://drive.google.com/file/d/0BxCL-uXywP6wcTljd2pDUVVuOEU/view?usp=sharing

10 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.
Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.
Note3: Test performed on product itself, not inside a container

11 Warranty and Conditions

http://www.displaymodule.com/pages/faq