DisplayModule

DM-TFT35-431

3.5" IPS 320x480 DISPLAY PANEL
SPI, MCU ,RGB

Contents

1 Revision History

Date	Changes
2022-05-19	First release

2 Main Features

Item	Specification	Unit
Size	3.5	Inch
Resolution	320(RGB) x 480	pixel
Display area	48.96(H)*73.44(V)	mm
Module Dimension	54.58 x 83.57 x 2.18	mm
TFT Controller IC	ST7796S	-
Interface	8/9/16/18Bit MCU Interface 3/4 line SPI 3/4SPI+16/18Bit RGB Interface	-
Display Color	65K/262K	colors
View Direction	All	
Backlight Type	Transmissive/Normally black	-
Weight	20	g
Operating temperature	-20~+70	℃
Storage temperature	-30~+80	℃

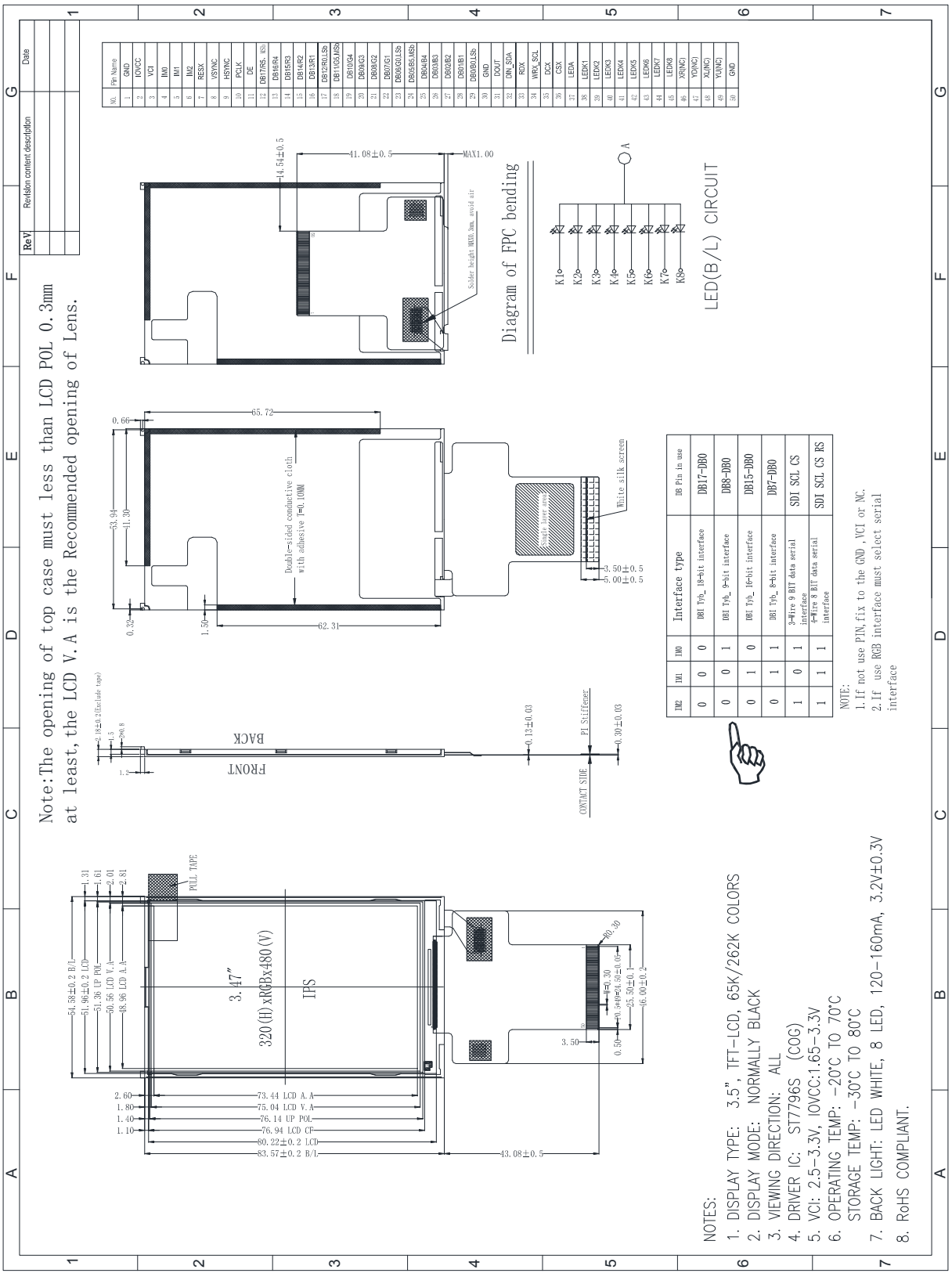
3 Pin Description

3.1 TFT

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>GND</td><td>Ground</td></tr>
<tr><td>2</td><td>IOVCC</td><td>Supply Voltage for IO (1.65-3.3V)</td></tr>
<tr><td>3</td><td>VCI</td><td>Supply Voltage(3.3V)</td></tr>
<tr><td>4
5
6</td><td>IM0
IM1
IM2</td><td>
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_9-bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_16-bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_8-bit interface</td><td>DB7-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-Wire 9bit data serial interface</td><td>SDA SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-Wire 8bit data serial interface</td><td>SDA SCL CS RS</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>RESX</td><td>This signal will reset the device and must be applied to properly initialize the chip</td></tr>
<tr><td>8</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation.
Fix this pin at IOVCC or GND when not in use.</td></tr>
<tr><td>9</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation.
Fix this pin at IOVCC or GND when not in use.</td></tr>
<tr><td>10</td><td>PCLK</td><td>Dot clock signal for RGB interface operation.
Fix this pin at IOVCC or GND when not in use.</td></tr>
<tr><td>11</td><td>DE</td><td>Data enable signal for RGB interface operation.
fix this pin at IOVCC or GND when not in use</td></tr>
<tr><td>12-29</td><td>DB17-DB0</td><td>18-bit parallel bi-directional data bus for MCU system and RGB interface mode.
Fix to GND level when not in use</td></tr>
<tr><td>30</td><td>GND</td><td>Ground</td></tr>
<tr><td>31</td><td>DOUT</td><td>Serial data output pin in serial bus system interface.
If not used, please open this pin</td></tr>
<tr><td>32</td><td>DIN_SDA</td><td>Serial input signal. The data is applied on the rising edge of the SCL signal.
If not used, fix this pin at IOVCC or GND</td></tr>
<tr><td>33</td><td>RDX</td><td>Serves as a read signal and MCU read data at the rising edge.</td></tr>
</table>

		fix this pin at IOVCC or GND when not in use
34	WR(SPI-SCL)	DBI Type B: WRX pin, serves as a write signal DBI Type C: SCL pin as Serial Clock when operates in the serial interface
35	DCX(RS)	Display data/ command selection pin
36	CSX	Chip select input pin (“Low” enable). fix this pin at IOVCC or GND when not in use
37	LEDA	Anode pin of backlight
38	LEDK1	Cathode pin OF backlight
39	LEDK2	Cathode pin OF backlight
40	LEDK3	Cathode pin OF backlight
41	LEDK4	Cathode pin OF backlight
42	LEDK5	Cathode pin OF backlight
43	LEDK6	Cathode pin OF backlight
44	LEDK7	Cathode pin OF backlight
45	LEDK8	Cathode pin OF backlight
46	XR(NC)	Touch panel Right Glass Terminal
47	YD(NC)	Touch panel Bottom Film Terminal
48	XL(NC)	Touch panel LIFT Glass Terminal
49	YU(NC)	Touch panel Top Film Terminal
50	GND	Ground

4 Mechanical Drawing



5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VCI		2.5	2.8	3.3	V
I/O Digital Voltage	IOVCC		1.65	1.8	3.3	V
Normal mode Current	IDD			14	28	mA
Low Level Input Voltage	V_{IL}		GND		0.3 IOVCC	V
High Level Input Voltage	V_{IH}		0.7 IOVCC		IOVCC	V
Low Level Output Voltage	V_{OL}		GND		0.2 IOVCC	V
High Level Output Voltage	V_{OH}		0.8 IOVCC		IOVCC	V
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃
LED Forward Current	If		120	160	-	mA
LED Forward Voltage	Vf		-	3.2	-	V

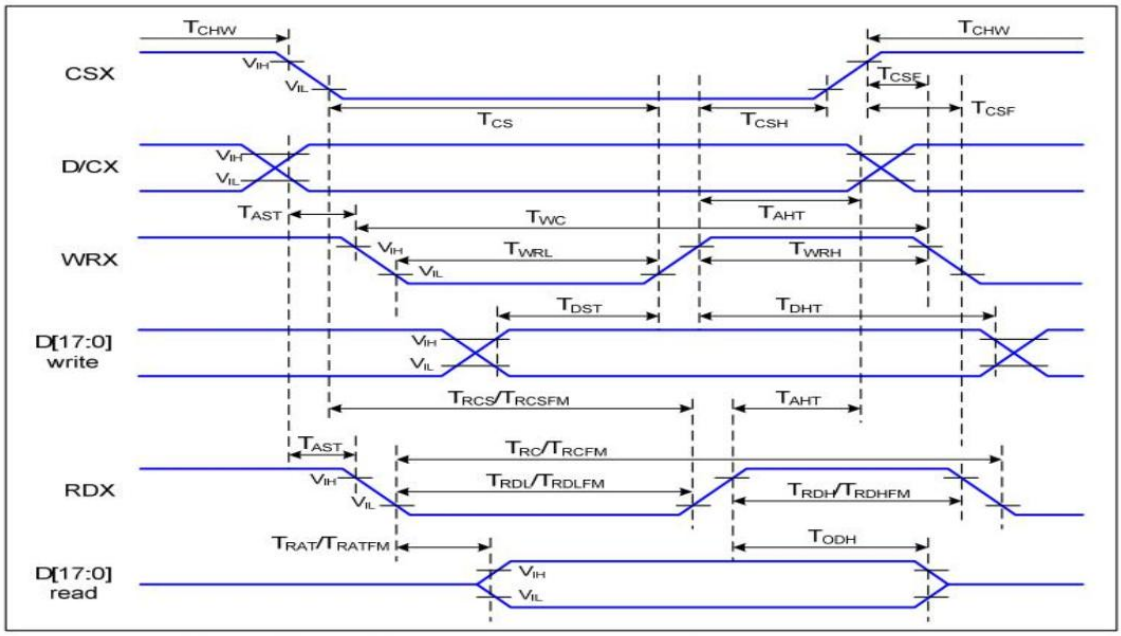
The back-light system is edge-lighting type with 8 chips White LED

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	AV	70	80	-	deg
View Angles Bottom	AV	70	80	-	deg
View Angles Right	AH	70	80	-	deg
View Angles Left	AH	70	80	-	deg
Response Time	Tr +Tf		30	40	ms
Contrast Ratio	CR	800	1000	-	--
LCM Luminance	Lv	550	600	-	cd/m^2

7 Timing Characteristics

7.1 8080 Series MCU Parallel Interface Characteristics:18/16/9/8-bit Bus



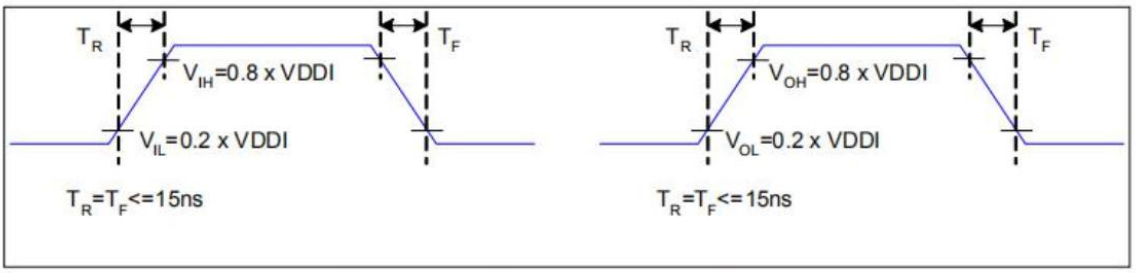
Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	

	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)	-	40	ns	
	T_{RATFM}	Read access time (FM)	-	340	ns	
	T_{ODH}	Output disable time	20	80	ns	

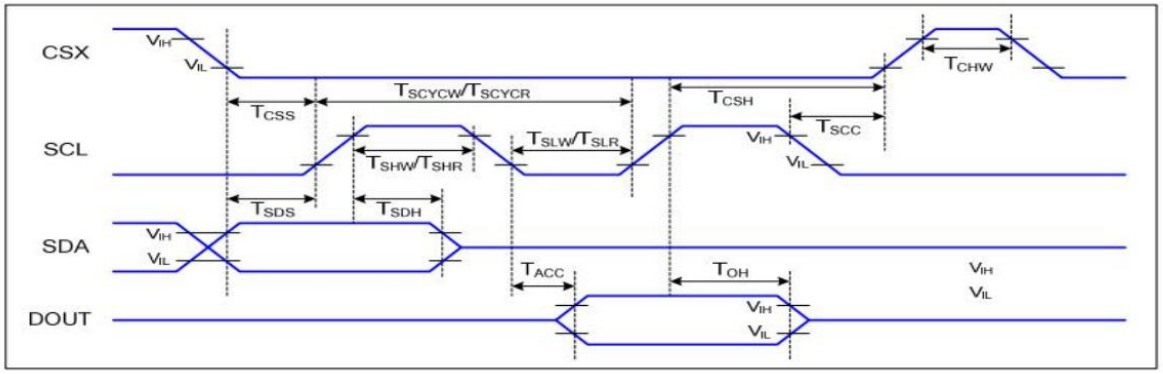
8080 Parallel Interface Characteristics



Rising and Falling Timing for I/O Signal

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

7.2 3-SPI Serial Data Transfer Interface Characteristics:



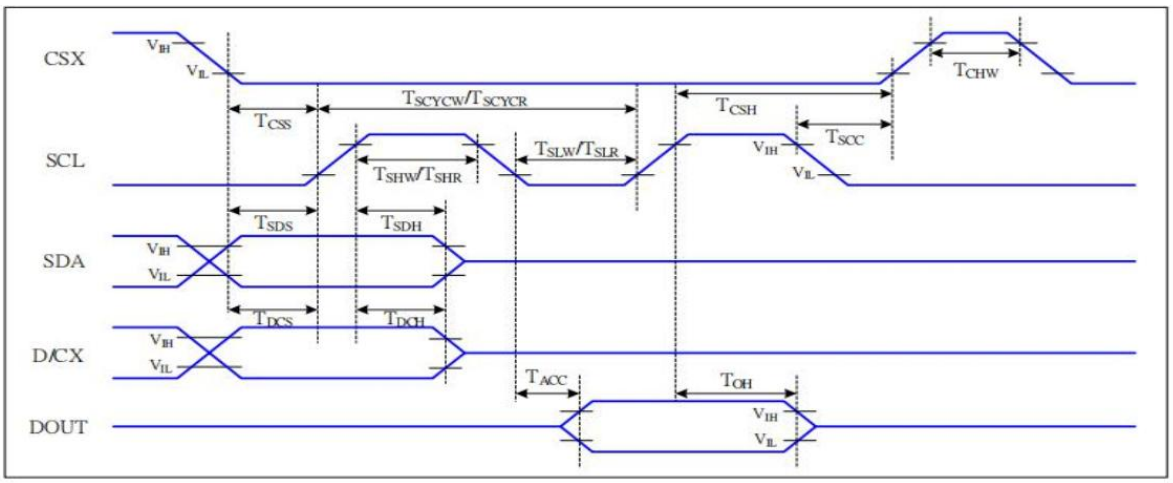
3-SPI Interface Timing Characteristics

VDDI=1.8V, VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

7.3 4-SPI Serial Data Transfer Characteristics:

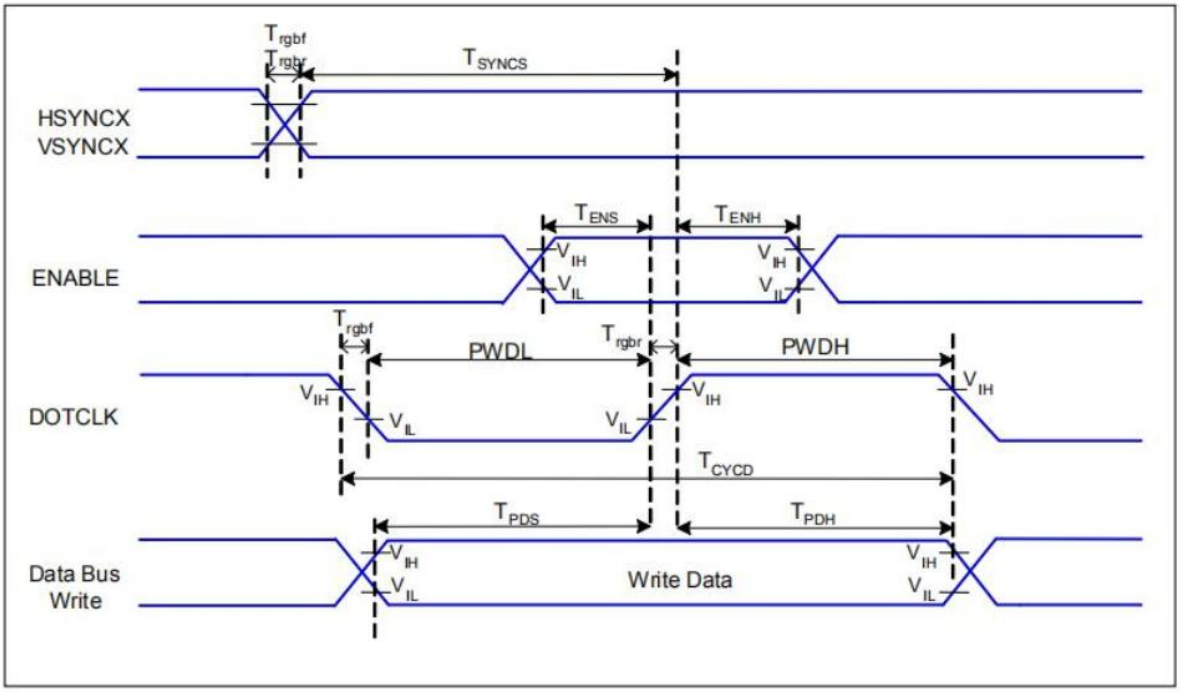


4-SPI Interface Timing Characteristics

VDDI=1.8V, VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

7.4 RGB Interface Characteristics:



VDDI=1.8V, VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics

7.5 Reset Timing

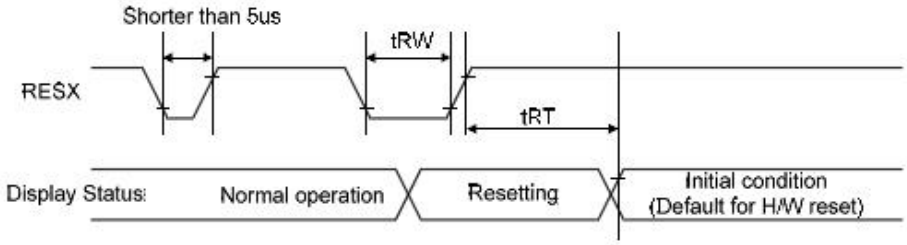


Table 39: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes the required time for loading ID bytes, VCOM setting and other settings from the EEPROM to registers. After a rising edge of RESX, this loading is done within 5 ms after the H/W reset cancel (tRT).
2. According to the Table 40, a spike due to an electrostatic discharge on the RESX line does not cause irregular system reset.

Table 40: Reset Description

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Reset period, the display will be blanked (When Reset starts in the Sleep Out mode, the display will enter the blanking sequence in at least 120 ms. The display remains the blank state in the Sleep In mode.) and then return to the default condition for the Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

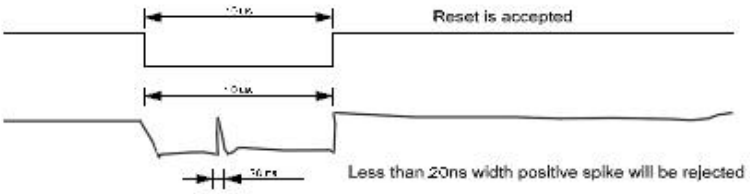
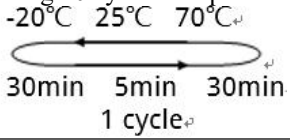


Figure 137: Positive Noise Pulse during Reset Low

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq