DisplayModule

DM-TFT35-385

3.5" 480x640 TRANSFLECTIVE DISPLAY PANEL –RGB

Contents

1 Revision History

Date	Changes
2019-04-30	First release

2 Main Features

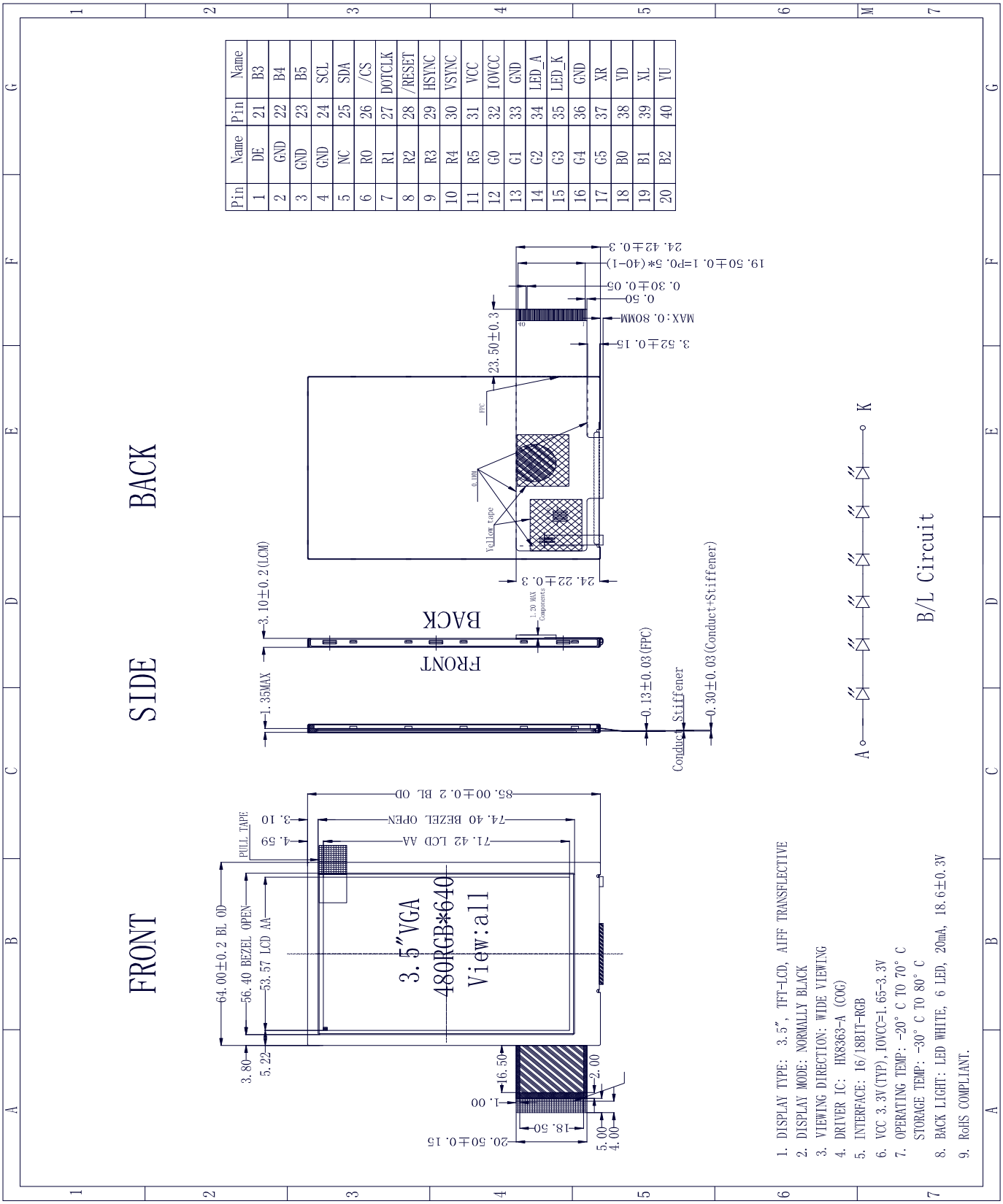
Item	Specification	Unit
Size	3.5	Inch
Resolution	480(RGB) x640	pixel
Module Dimension	64.0 x 85.0 x 3.1	mm
Display area	53.57 x 71.42	mm
Pixel pitch	0.1116 x 0. 1116	mm
TFT Controller IC	HX8363	-
CTP Driver IC	None	-
Interface	3SPI+16/18bit RGB	-
Display Color	65K/262K	colors
View Direction	Wide angle	O'clock
Display mode	Transflective / Normally Black	-
Weight	34	g

3 Pin Description

No.	Symbol	Description
1	DE	A data ENABLE signal in RGB I/F mode. Has to be fixed to GND level in MPU interface mode.
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	NC	-
6-11	R0-R5	Red Data BUS
12-17	G0-G5	Green Data BUS
18-23	B0-B5	Blue Data BUS
24	SCL	Serves as a write signal and writes data at the rising edge. When operate in serial interface, it serves as SCL (Serial Clock) If not used, let it open or connected to VCC
25	SDA	Serial data input pin in serial interface operation
26	CS	Chip select input pin (“Low” enable). fix this pin at VCI or GND when not in use.
27	DOTCLK	Dot clock signal. Must be connected to GND or VCC if not used.
28	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to GND or VCC). (Latch type)
29	HSYNC	Line synchronizing signal. Must be connected to GND or VCC if not used.
30	VSYNC	Frame synchronizing signal. Must be connected to GND or VCC if not used.
31	VCC	Supply voltage(3.3V).
32	IOVCC	A power supply for the I/O circuit. (1.65-3.3V)
33	GND	Ground

34	LED_A	Anode pin of backlight
35	LED_K	Cathode pin OF backlight
36	GND	Ground
37	XR	Touch panel Right Glass Terminal
38	YD	Touch panel Bottom Film Terminal
39	XL	Touch panel Left Glass Terminal
40	YU	Touch panel Top Film Terminal

4 Mechanical Drawing



Pin	Name	Pin	Name
1	DE	21	B3
2	GND	22	B4
3	GND	23	B5
4	GND	24	SCL
5	NC	25	SDA
6	R0	26	/CS
7	R1	27	DOTCLK
8	R2	28	/RESET
9	R3	29	HSYNC
10	R4	30	VSYNC
11	R5	31	VCC
12	G0	32	IOVCC
13	G1	33	GND
14	G2	34	LED_A
15	G3	35	LED_K
16	G4	36	GND
17	G5	37	XR
18	B0	38	YD
19	B1	39	XL
20	B2	40	YU

5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VCC		2.5	3.3	3.6	V
Supply Voltage Logic	IOVCC		1.65	1.8	3.3	V
Normal mode Current	IDD		-	20	40	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃
LED Forward Current	If		15	20	-	mA
LED Forward Voltage	Vf		-	18.6	-	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	ΘU	60	80	-	deg
View Angles Bottom	ΘD	60	80	-	deg
View Angles Right	ΘR	60	80	-	deg
View Angles Left	ΘL	60	80	-	deg
Response Time	Tr +Tf		30	50	ms
Contrast Ratio	CR	200	300	-	--
LCM Luminance	Lv	65	115	-	cd/m^2

7 AC Characteristics

7.1 Serial Interface Characteristics (3-Pin Serial)

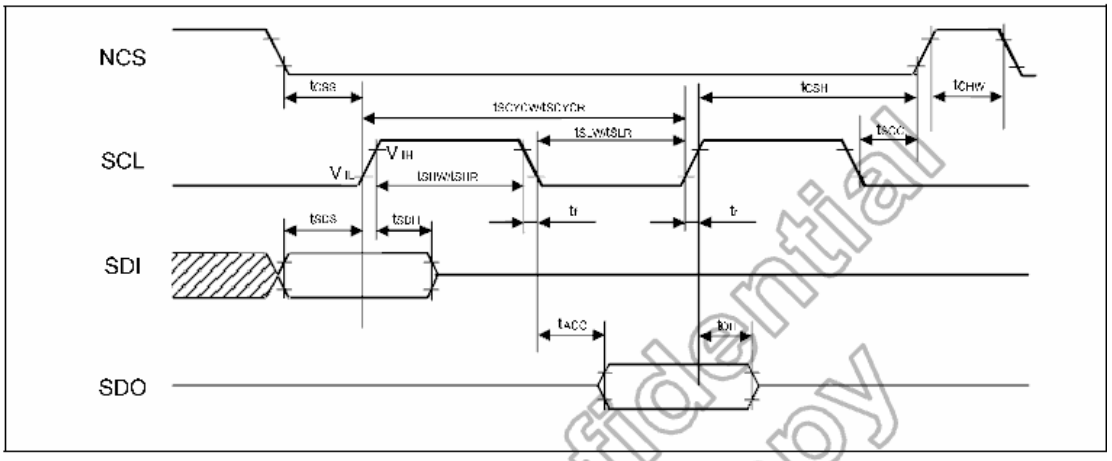


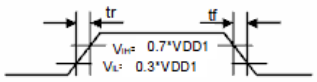
Figure 8.1: 3-pin Serial Interface Characteristics

(VSSA=VSSD=0V, VDD1=1.65V to 1.95V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

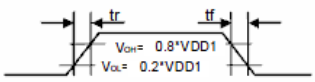
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write) SCL "H" pulse width (Write) SCL "L" pulse width (Write)	tSCYCW tSHW tSLW	SCL	80 30 30	- - -	- - -	ns
Data setup time (Write) Data hold time (Write)	tSDS tSDH	SDI	10 10	- -	- -	ns
Serial clock cycle (Read) SCL "H" pulse width (Read) SCL "L" pulse width (Read)	tSCYCR tSHR tSLR	SCL	150 60 60	- - -	- - -	ns
Access rime	tACC	SDO For maximum CL=30pF For maximum CL=8pF	10	-	60	ns
Output disable time	tOH	SDO For maximum CL=30pF For maximum CL=8pF	15	-	100	ns
SCL to Chip select	tSCC	NCS	30	-	-	ns
NCS "H" pulse width	tCHW	NCS	60	-	-	ns
NCS-SCL time (write) NCS-SCL time (write	tCSS tCSH	NCS	30 30	- -	-	ns
NCS-SCL time (Read) NCS-SCL time (Read)	tCSS tCSH	NCS	60 65	- -	-	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Input Signal Slope



Output Signal Slope

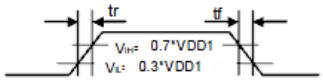


(VSSA=VSSD=0V, VDD1=1.95V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

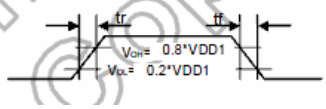
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write)	t_{SCYCW}	SCL	80	-	-	ns
SCL "H" pulse width (Write)	t_{SHW}		30	-	-	
SCL "L" pulse width (Write)	t_{SLW}		30	-	-	
Data setup time (Write)	t_{SDS}	SDI	10	-	-	ns
Data hold time (Write)	t_{SDH}		10	-	-	
Serial clock cycle (Read)	t_{SCYCR}	SCL	150	-	-	ns
SCL "H" pulse width (Read)	t_{SHR}		60	-	-	
SCL "L" pulse width (Read)	t_{SLR}		60	-	-	
Access rime	t_{ACC}	SDO For maximum C_L=30pF For maximum C_L=8pF	5	-	60	ns
Output disable time	t_{OH}	SDO For maximum C_L=30pF For maximum C_L=8pF	8	-	100	ns
SCL to Chip select	t_{SCC}	NCS	30	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	60	-	-	ns
NCS-SCL time (write)	t_{CSS}	NCS	30	-	-	ns
NCS-SCL time (write	t_{CSH}		30	-		
NCS-SCL time (Read)	t_{CSS}	NCS	60	-	-	ns
NCS-SCL time (Read)	t_{CSH}		65	-		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Input Signal Slope



Output Signal Slope



Vertical Timings for RGB I/F

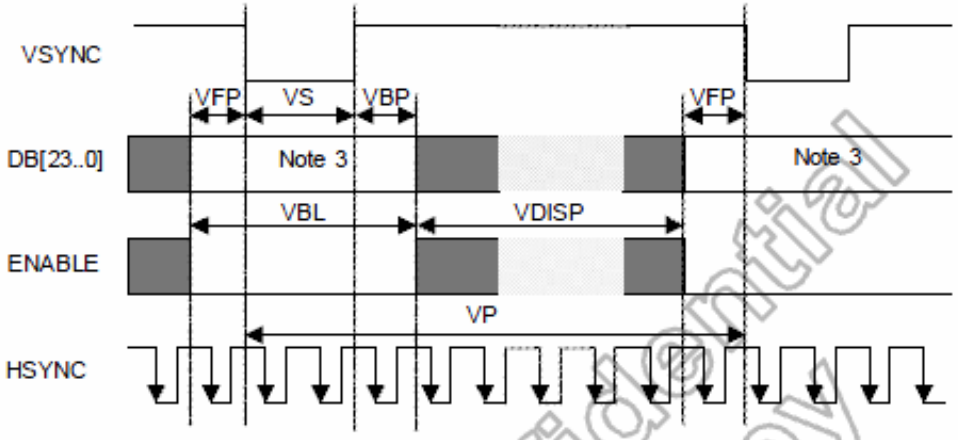


Figure 8.2: Vertical Timings for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	860	-	864	Line
Vertical low pulse width	VS	-	2	-	4	Line
Vertical front porch	VFP	-	2	-	4	Line
Vertical back porch	VBP	-	2	-	4	Line
Vertical data start point	-	VS+VBP	4	-	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	10	Line
Vertical active area	-	VDISP	-	854	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(4) VRR must keep from 50Hz to 70Hz when adjust other items

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	806	-	810	Line
Vertical low pulse width	VS	-	2	-	4	Line
Vertical front porch	VFP	-	2	-	4	Line
Vertical back porch	VBP	-	2	-	4	Line
Vertical data start point	-	VS+VBP	4	-	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	10	Line
Vertical active area	-	VDISP	-	800	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(4) VRR must keep from 50Hz to 70Hz when adjust other items

Table 8.5: Vertical Timings for RGB I/F

Horizontal Timings for RGB I/F

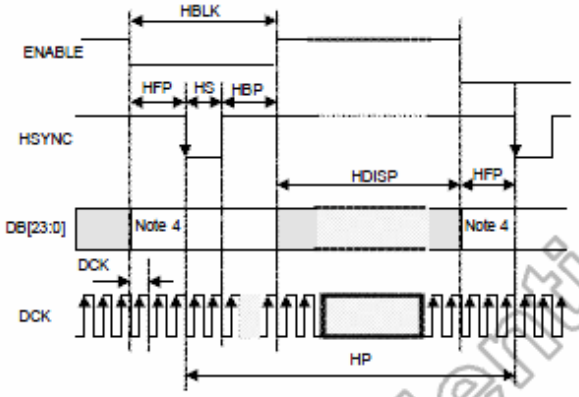


Figure 8.3: Horizontal Timing for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note(3)	504	-	568	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	19	-	83	DCK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK
Pixel clock frequency When RGB I/F is running	DCK	VRR = Min. 50Hz	21.6	-	34.3	MHz
		- Max. 70Hz	29.1	-	46.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) HP is multiples of eight DCK.
(4)Data lines can be set to "High" or "Low" during blanking time – Don't care.
(5) VRR must keep from 50Hz to 70Hz when adjust other items.

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note(3)	504	-	568	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	19	-	83	DCK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK
Pixel clock frequency When RGB I/F is running	DCK	VRR = Min. 50Hz	20.3	-	32.2	MHz
		- Max. 70Hz	31	-	49.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) HP is multiples of eight DCK.
(4)Data lines can be set to "High" or "Low" during blanking time – Don't care.
(5) VRR must keep from 50Hz to 70Hz when adjust other items.

Table 8.6: Horizontal Timings for RGB I/F

General Timings for RGB I/F

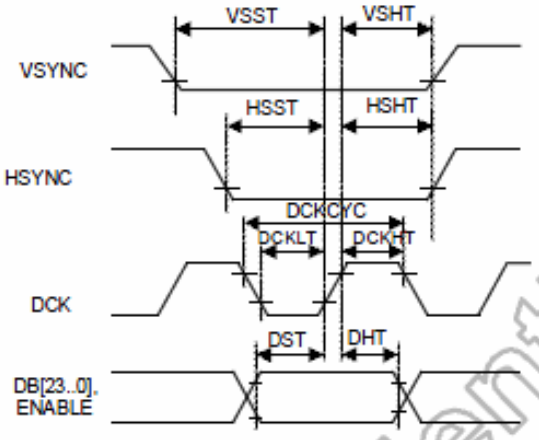


Figure 8.4: General Timings for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Setup time	VSST	-	5	-	-	ns
Vertical sync. Hold time	VSHT	-	5	-	-	ns
Horizontal sync. Setup time	HSST	-	5	-	-	ns
Horizontal sync. Hold time	HSHT	-	5	-	-	ns
Pixel clock cycle When RGB I/F is running	DCKCYC	VRR = Min . 50 Hz Max. 70 Hz	29.1(3)	-	46.2(4)	ns
Pixel clock low time	DCKLT	-	5	-	-	ns
Pixel clock high time	DCKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data Hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) 34.3 MHz
(4) 21.6 MHz

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Setup time	VSST	-	5	-	-	ns
Vertical sync. Hold time	VSHT	-	5	-	-	ns
Horizontal sync. Setup time	HSST	-	5	-	-	ns
Horizontal sync. Hold time	HSHT	-	5	-	-	ns
Pixel clock cycle When RGB I/F is running	DCKCYC	VRR = Min . 50 Hz Max. 70 Hz	31(3)	-	49.2(4)	ns
Pixel clock low time	DCKLT	-	5	-	-	ns
Pixel clock high time	DCKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data Hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) 32.2MHz
(4) 20.3MHz

Table 8.7: General Timings for RGB I/F

7.2 Reset Timing

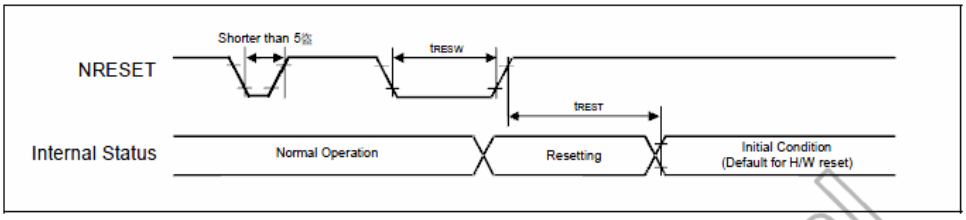


Figure 8.10: Reset Input Timing

Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	μs
tREST	Reset complete time(2)	-	-	-	5	When reset is applied during Sleep In mode	ms
		-		-	120	When reset is applied during Sleep Out mode	ms

Table 8.18: Reset Timing

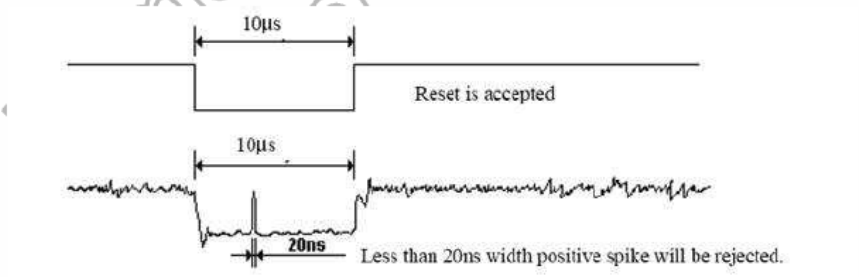
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown below:

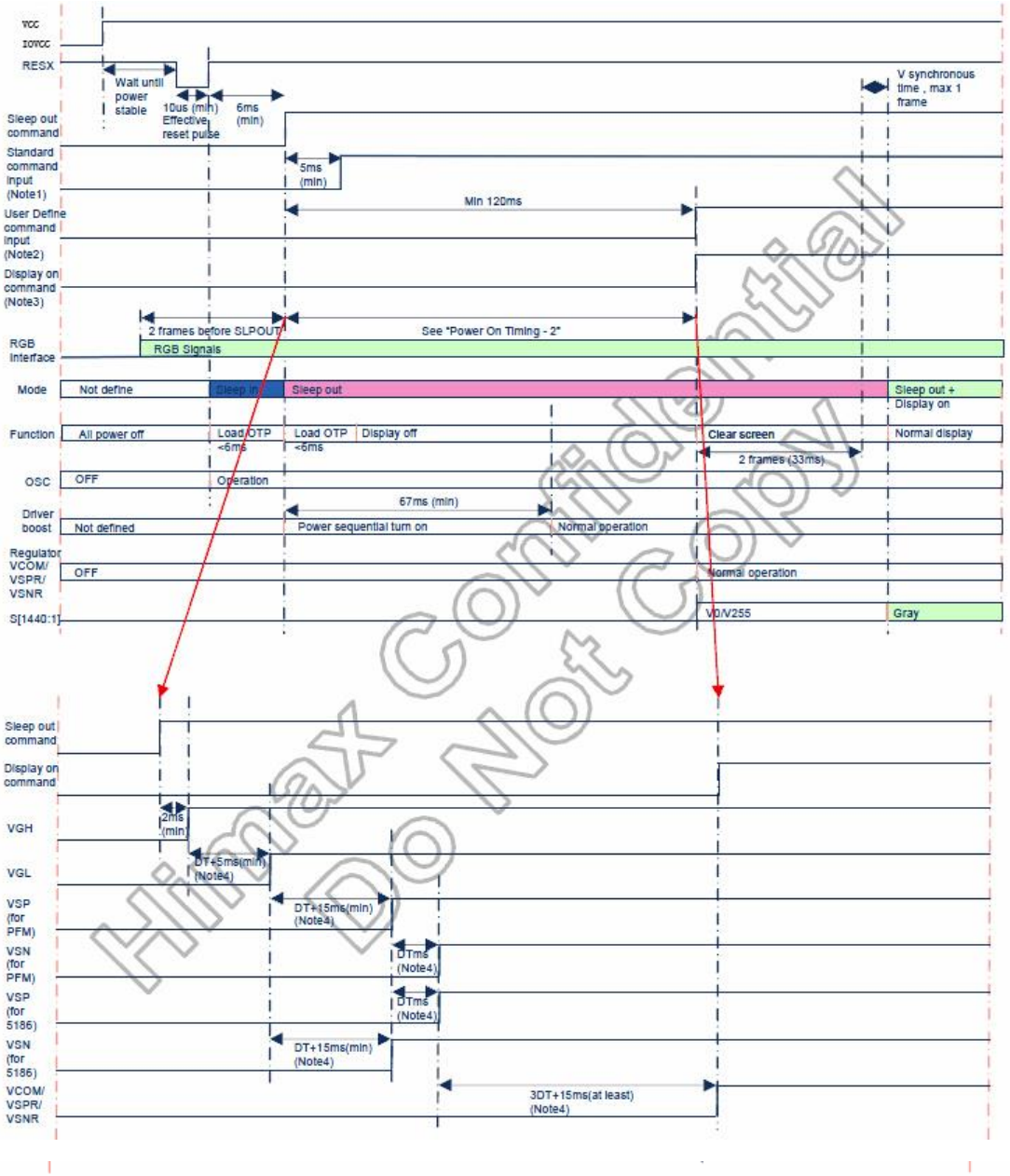


(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.3 Power ON/OFF Timing



Note1:
"Standard" command except "01h" & "10h" command must wait 5ms after "Sleep out" command then can be sent. "01h" & "10h" command must wait 100ms after "Sleep out" command then can be sent.

Note2:
"User Define" command must wait 100ms after "Sleep out" command then can be sent. "B9h" command must be sent first then other command can be sent after "B9h" command.

Note3:
"Display on" command must send after "User Define" command or at the same time.

Note4:

DT[1:0]: Delay time of power on and power off sequence

DT1	DT0	Delay time of power on and power off sequence on
0	0	5ms
0	1	10ms
1	0	1ms
1	1	0ms

Default DT=5ms

Figure 8.11: Power On Timing

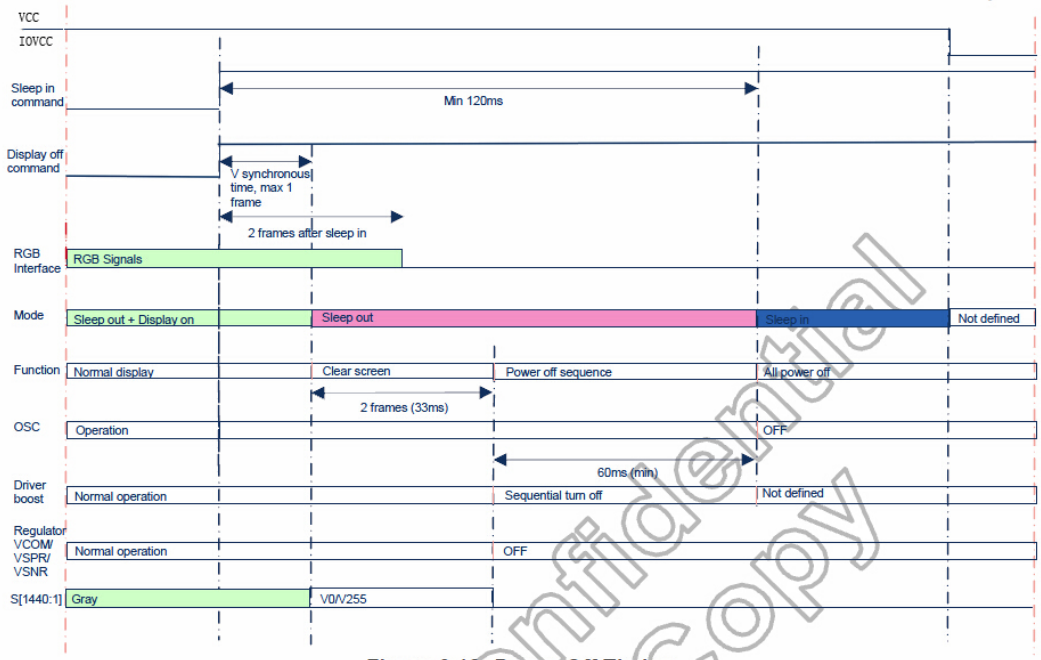
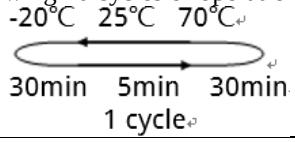


Figure 8.12: Power Off Timing

8 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-30℃/80℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

9 Warranty and Conditions

http://www.displaymodule.com/pages/faq