DisplayModule

DM-TFT30-418

3.0" IPS 240x400 DISPLAY PANEL WITH TOUCH –SPI,MCU,RGB

Contents

1 Revision History

Date	Changes
2018-10-09	First release

2 Main Features

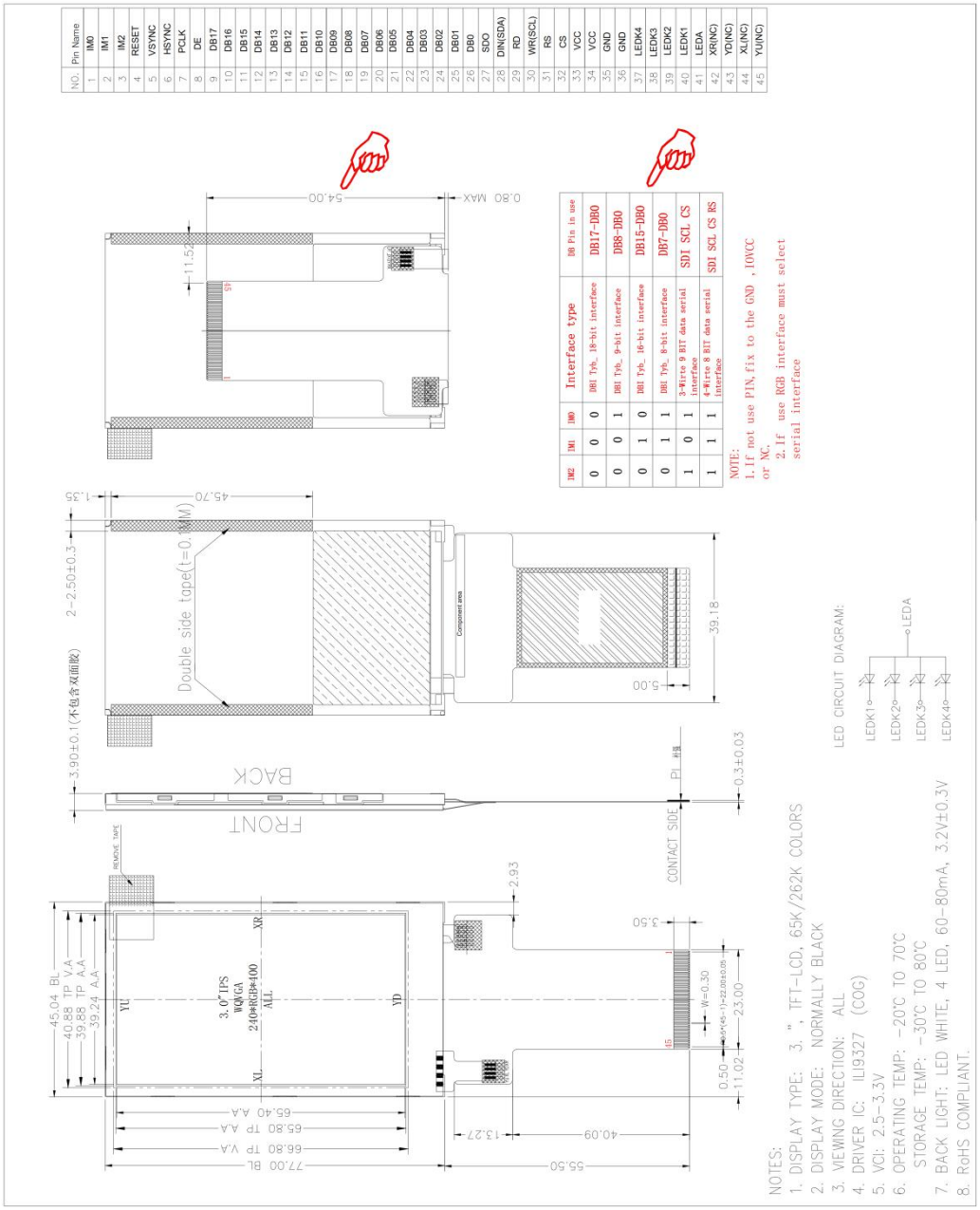
Item	Specification	Unit
Size	3.0	Inch
Resolution	240(RGB) x 400	pixel
Module Dimension	45.04 x 77.0 x 3.9	mm
Display area	39.24 x 65.4	mm
Pixel pitch	0.1635 x 0.1635	mm
TFT Controller IC	ILI9327	-
Interface	8/9/16/18 MCU 3/4 SPI+16/18bit RGB	-
Display Color	65K/262K	colors
View Direction	All	
Touch mode	Resistive touch	-
Display mode	Transmissive / Normally black	-
Weight	TBD	g

3 Pin Description

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>IM0</td><td rowspan="3">
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_9-bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_16-bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_8-bit interface</td><td>DB7-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-Wire 9 bit data serial interface</td><td>SDI SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-Wire 8 bit data serial interface</td><td>SDI SCL CS RS</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>IM1</td></tr>
<tr><td>3</td><td>IM2</td></tr>
<tr><td>4</td><td>RESET</td><td>This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active</td></tr>
<tr><td>5</td><td>VSYNC</td><td>Vertical sync. Signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_CS) In MDDI mode, this is an output pin, If it’s not used; please let this pin as open. In other mode, this is an input pin, If it’s not used; please fix this pin as GND.</td></tr>
<tr><td>6</td><td>HSYNC</td><td>Horizontal sync. signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_RS) In MDDI mode, this is an output pin, If it’s not used; please let this pin as open. In other mode, this is an input pin, If it’s not used; please fix this pin as GND.</td></tr>
<tr><td>7</td><td>PCLK</td><td>Pixel clock signal in DPI interface mode.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>8</td><td>DE</td><td>Data enable signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_WR) In MDDI mode, this is an output pin, If it’s not used; please let this pin as open. In other mode, this is an input pin, If it’s not used; please fix this pin as GND.</td></tr>
<tr><td>9-26</td><td>DB17-DB0</td><td>These pins are data bus. In MDDI operation, DB[17:9]/S_DB[8:0] can be assigned for the sub-display interface output. In MDDI mode, these pins are output, If they are not used; please let these pins as open. In other mode, these pins are input, If they are not used; please fix these pins as GND.</td></tr>
<tr><td>27</td><td>SDO</td><td>Serial data output pin and used for the DBI type C mode.</td></tr>
<tr><td>28</td><td>DIN</td><td>Serial data input pin and used for the DBI type C mode. If not used, please connect this pin to ground.</td></tr>
<tr><td>29</td><td>RD</td><td>Read control pin for the DBI interface. If not used, please connect this pin to VCC.</td></tr>
<tr><td>30</td><td>WR(SCL)</td><td>Write control pin for the DBI interface. When the DBI type C is selected, this pin is used as serial clock pin. If not used, please connect this pin to VCC.</td></tr>
<tr><td>31</td><td>RS</td><td>Display data / Command selection pin</td></tr>
</table>

		D/CX='1': Display data. D/CX='0': Command data. If not used, please fix this pin at GND level.
32	CS	Chip select input pin (“Low” enable). When it is not used, please fix this pin at VCC.
33-34	VCC	Power supply voltage(VCI=2.5V-3.3V)
35-36	GND	Ground
37-40	LEDK4-1	LED Cathode 4 – Cathode 1
41	LEDA	LED Anode
42	XR	Touch panel Right Glass Terminal.
43	YD	Touch panel Bottom Film Terminal.
44	XL	Touch panel LIFT Glass Terminal.
45	YU	Touch panel Top Film Terminal.

4 Mechanical Drawing



5 Electrical Characteristics

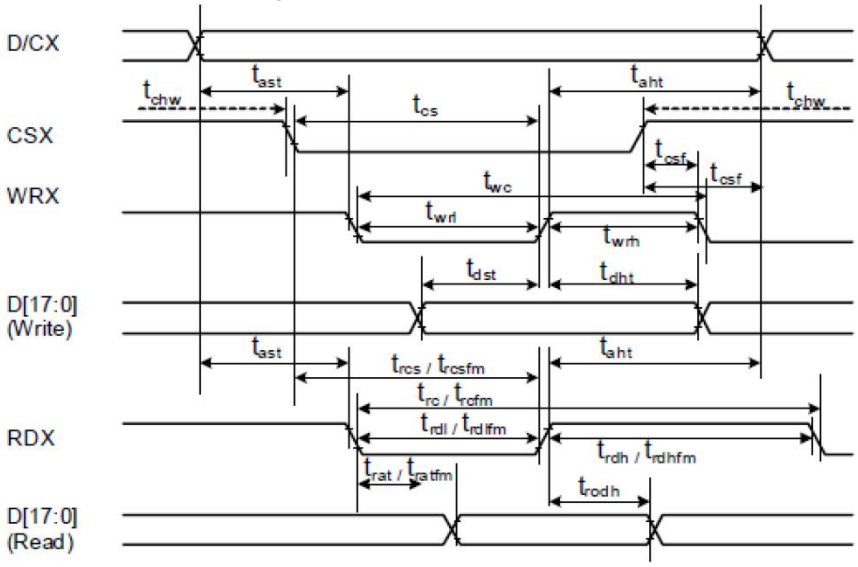
Item	Symbol	Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VDD		2.4	3.3	4.2	V
Normal mode Current	IDD		-	8	-	mA
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃
LED Forward Current	If		60	80	-	mA
LED Forward Voltage	Vf		-	3.2	-	V

6 Optical Characteristics

Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	θ U	-	80	-	deg
View Angles Bottom	Θ D	-	80	-	deg
View Angles Right	Θ R	-	80	-	deg
View Angles Left	Θ L	-	80	-	deg
Response Time	Tr +Tf		35	50	ms
Contrast Ratio	CR	400	500	-	--
LCM Luminance	Lv	-	380	-	cd/m^2

7 AC Characteristics

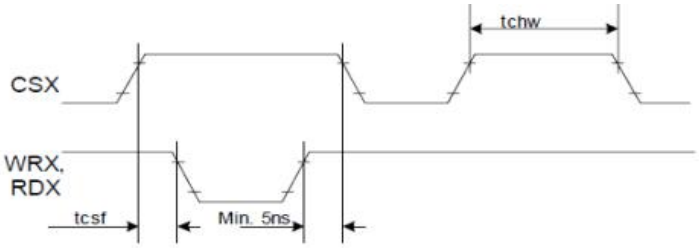
7.1 Parallel Interface Timing Characteristics:



Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" Pulse Width	0	-	ns	
	tcs	Chip Select setup time (Write)	20	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	80	-	ns	
	twrh	Write Control pulse H duration	25	-	ns	
	twrl	Write Control pulse L duration	25	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration (ID)	90	-	ns	
	trdl	Read Control pulse L duration (ID)	45	-	ns	
RDX (FM)	trcfm	Read cycle (FM)	450	-	ns	
	trdhfm	Read Control pulse H duration (FM)	90	-	ns	
	trdlfm	Read Control pulse L duration (FM)	355	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	tdst	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Data hold time	10	-	ns	
	trat	Read access time (ID)	-	40	ns	
	tratfm	Read access time (FM)	-	340	ns	
	todh	Output disable time	20	-	ns	

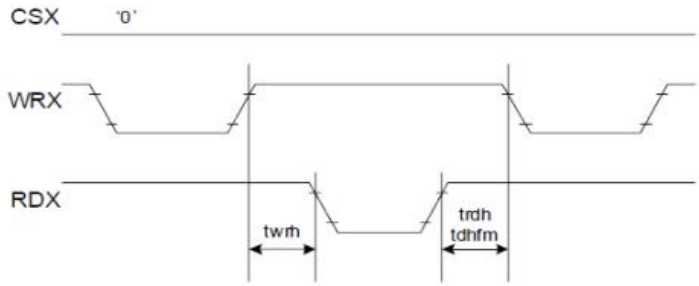
Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, DGND=0V

CSX timings:



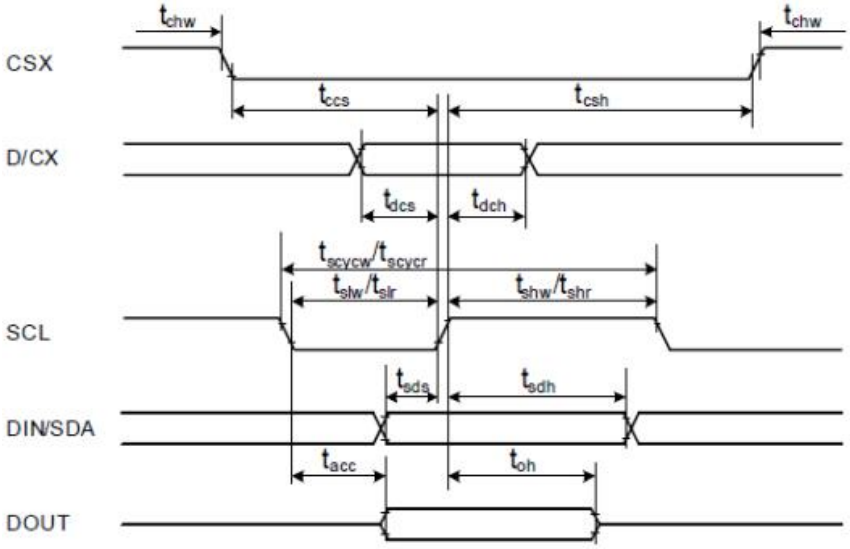
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

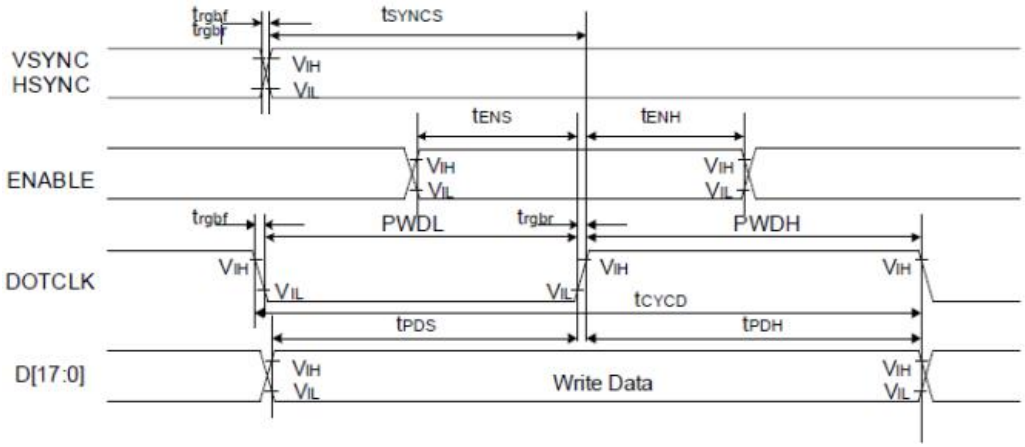
7.2 DBI Type C(SPI) Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	CSX-SCL time (Write)	15	-	ns	
	tcsh	CSX-SCL time (Write)	15	-	ns	
	tcss	CSX-SCL time (Read)	60	-	ns	
	tcsh	CSX-SCL time (Read)	60	-	ns	
	tchw	CSX "H" pulse time	40	-	ns	
SCL	tscycw	Serial clock cycle (Write)	60	-	ns	
	tshw	SCL "H" pulse width (Write)	15	-	ns	
	tslw	SCL "L" pulse width (Write)	15	-	ns	
	tscycr	Serial clock cycle (Read GRAM)	300	-	ns	
	tshr	SCL "H" pulse width (Read GRAM)	110	-	ns	
	tslr	SCL "L" pulse width (Read GRAM)	110	-	ns	
	tscycr	Serial clock cycle (Read ID)	150	-	ns	
	tshr	SCL "H" pulse width (Read GRAM)	54	-	ns	
	tslr	SCL "L" pulse width (Read GRAM)	54	-	ns	
D/CX	tdcs	D/CX setup time	7	-	ns	
	tdch	D/CX hold time	7	-	ns	
SDA (Input) (Output)	tacc	Access time	10	50	ns	For maximum CL=30pF
	toh	Output disable time	15	50	ns	For minimum CL=8pF
	tsds	Data setup time	7	-		
	tsdh	Data hold time	7	-		

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, AGND=DGND=0V

7.3 DBI Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, AGND=DGND=0V

7.4 Reset Timing Characteristics

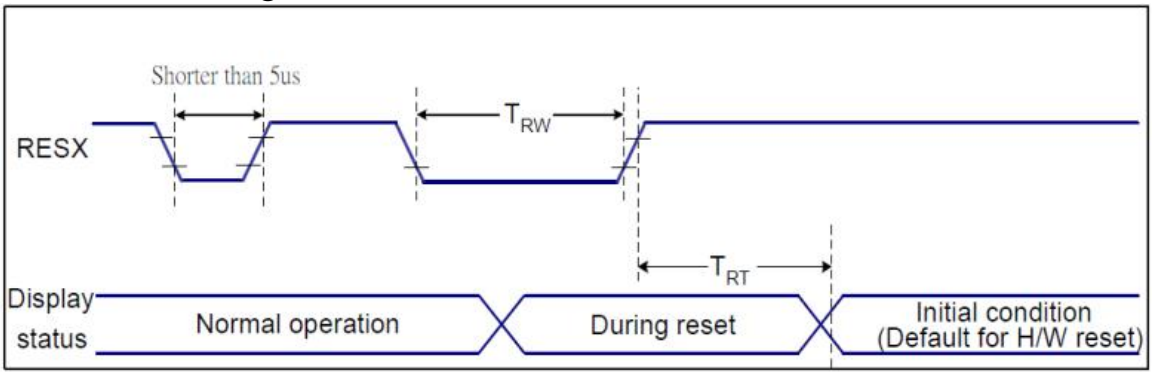
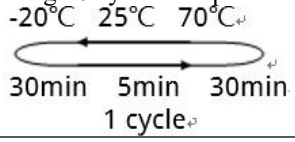


Figure 7 Reset Timing

8 TP Specification

Item	Symbol	Condition	Min	Typ	Max	Unit
Maximum Voltage			-	-	5	V
Resistance between terminals	X	Film side	200	-	600	Ω
	Y	Glass side	300	-	900	Ω
Chattering			<10	-	-	msec
Total light transmittance			80%	-	-	

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq