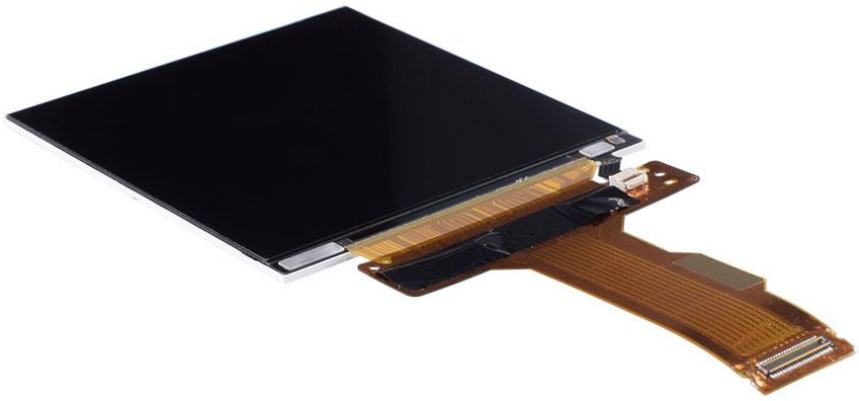
DisplayModule



DM-TFT29-392

2.89" 1440x1440 Sharp High Resolution TFT Display Panel –MIPI

Contents

1 Revision History

Date	Changes
2019-06-11	First release

2 Main Features

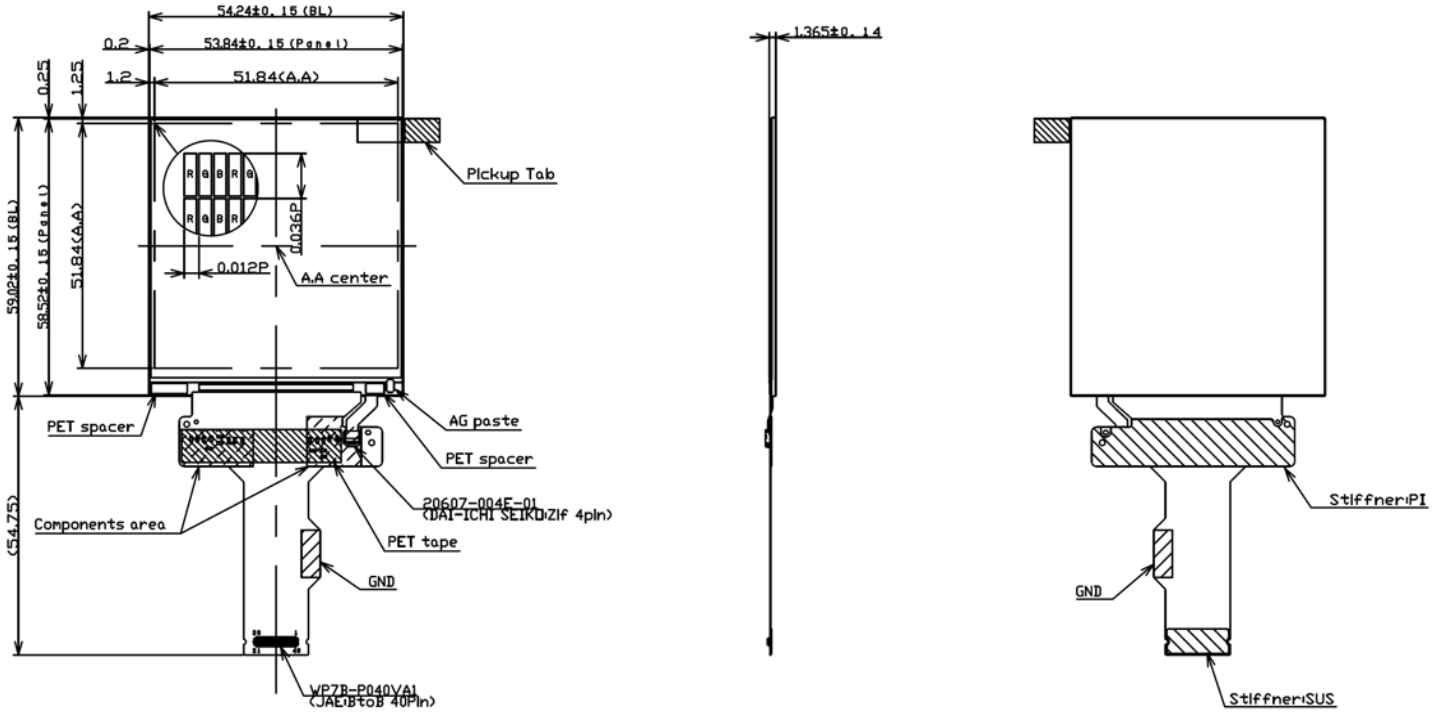
Item	Specification	Unit
Size	2.89	Inch
Resolution	1440(RGB) x 1440	pixel
Module Dimension	54.24 x 59.02 x 1.365	mm
Display area	51.84 x 51.84	mm
Pixel pitch	0.012 x 0.036	mm
Pixel configuration	R,G,B vertical stripes	-
TFT Controller IC	R63423	-
CTP Driver IC	None	-
Interface	4 lane MIPI	-
Display Color	16.7M (24 bits)	colors
View Direction	ALL	O'clock
Display mode	Normally Black	-
Weight	7	g

3 Pin Description

No.	Symbol	Description
1	DSIA_D3_N	MIPI data3 negative signal of MIPI Port A
2	DSIA_D3_P	MIPI data3 positive signal of MIPI Port A
3	DSIA_D0_N	MIPI data0 negative signal of MIPI Port A
4	DSIA_D0_P	MIPI data0 positive signal of MIPI Port A
5	DSIA_CLK_N	MIPI clock negative signal of MIPI Port A
6	DSIA_CLK_P	MIPI clock positive signal of MIPI Port A
7	DSIA_D1_N	MIPI data1 negative signal of MIPI Port A
8	DSIA_D1_P	MIPI data1 positive signal of MIPI Port A
9	DSIA_D2_N	MIPI data2 negative signal of MIPI Port A
10	DSIA_D2_P	MIPI data2 positive signal of MIPI Port A
11	DSIB_D2_P	MIPI data2 positive signal of MIPI Port B
12	DSIB_D2_N	MIPI data2 negative signal of MIPI Port B
13	DSIB_D1_P	MIPI data1 positive signal of MIPI Port B
14	DSIB_D1_N	MIPI data1 negative signal of MIPI Port B
15	DSIB_CLK_P	MIPI clock positive signal of MIPI Port B
16	DSIB_CLK_N	MIPI clock negative signal of MIPI Port B
17	DSIB_D0_P	MIPI data0 positive signal of MIPI Port B
18	DSIB_D0_N	MIPI data0 negative signal of MIPI Port B
19	DSIB_D3_P	MIPI data3 positive signal of MIPI Port B
20	DSIB_D3_N	MIPI data3 negative signal of MIPI Port B
21	EN1PORT	EN1PORT is used for enable or disable MIPI dual port.(“H” single port)
22	AVDD	Power supply for analog
23	VDDI	Power supply for I/O
24	VDDI	Power supply for I/O
25	EXCK	External Clock (not used).(GND)
26	GND	Ground
27	GND	Ground
28	GND	Ground
29	RESX	Device reset signal.(“L” Active)
30	FTE	Frame head pulse signal (not used).(Open)
31	Sync	Synchronizing signal (not used).(Open)
32	LEDPWM	Backlight LED driver PWM (if not used, “floating”)
33	AGND	Ground
34	AGND	Ground
35	AGND	Ground
36	AVEE	Power supply for analog
37	LED_CA1	LED back light power negative1
38	LED_CA2	LED back light power negative2
39	LED_AN1	LED back light power positive1
40	LED_AN2	LED back light power positive2

Connector: JAE WP7B-S040VA1(Board to Board Receptacle)

4 Mechanical Drawing



5 Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Condition
Digital Supply Voltage	VDDI	1.70	1.80	1.9	V	Note5-1
Positive Analog Supply Voltage	AVDD	5.3	5.5	6.0	V	Note5-1
Negative Analog Supply Voltage	AVEE	-6.0	-5.5	-5.3	V	Note5-1
Low Level Input Voltage	V_{IL}	0	-	0.3VDDI	V	Note5-2
High Level Input Voltage	V_{IH}	0.7VDDI	-	VDDI	V	Note5-2
Low Level Input Current	I_{IL}	-10	-	-	μA	
High Level Input Current	I_{IH}	-	-	10	μA	
Low Level Output Voltage	V_{OL}	0	-	0.2VDDI	V	I_{OL}=+0.1mA
High Level Output Voltage	V_{OH}	0.8VDDI	-	VDDI	V	I_{OH}=-0.1mA
Current consumption Video mode without RAM 2port(SDC)	I_{VDDIO}	-	$33_{(*1)}$	$65_{(*3)}$	mA	Note5-3
	I_{VSP}	-	$20_{(*1)}$	$40_{(*2)}$	mA	
	I_{VSN}	$-30_{(*3)}$	$-12_{(*1)}$	-	mA	
LED Forward Current	I_{LED}	-	11	20	mA	
LED Forward Voltage	V_{LED}	-	2.9	3.2	V	per unit

Note5-1) Include Ripple Noise

Note5-2) Applied overshoot

Note5-3) 120Hz / (*1) Gradation shift pattern, (*2) 1dot checker pattern, (*3) Random dot pattern

6 Absolute Maximum Ratings

Item	Symbol	Condition	Rated value	Unit	Remarks
Digital Supply Voltage	VDDI	Ta=+25℃	-0.3 to +5.5	V	Note6-1
Positive Analog Supply Voltage	AVDD	Ta=+25℃	-0.3 to +6.5	V	Note6-1
Negative Analog Supply Voltage	AVEE	Ta=+25℃	+0.3 to -6.5	V	Note6-1
Operating Temperature	T_{OP}	-	-20 to +60	℃	Note6-2
Storage Temperature	T_{STG}	-	-30 to +70	℃	Note6-2
ED Input Electric Current	I_{LED}	Ta=+25℃	25	mA	Note6-3

Note6-1) Voltage applied to GND pins. GND pin conditions are based on all the same voltage (0V).

Always connect all GND externally and use at the same voltage.

Note6-2)Humidity: 95%RHMax.(at Ta≤40°C). Maximum wet-bulb temperature is less than 39℃ (at Ta>40℃).

Condensation of dew must be avoided.

Note6-3) Ambient temperature and the maximum input are fulfilling the following operating conditions.

7 Optical Characteristic

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angles TOP	Θ U	CR>10	80	-	-	degree
View Angles Bottom	Θ D	CR>10	80	-	-	degree
View Angles Right	Θ R	CR>10	80	-	-	degree
View Angles Left	Θ L	CR>10	80	-	-	degree
Response Time	T_R+T_F	θ=0°	-	10	-	ms
Contrast Ratio	CR	θ=0°	770	1100	-	--
LCM Luminance	L	θ=0°	210	300	-	cd/m^2
Uniformity	U	θ=0°	70		-	%
NTSC Ratio	S	θ=0°	-	75	-	%
Gamma	γ	θ=0°	1.8	2.2	2.6	-
Flicker	F	θ=0°	-	-	30	%
Crosstalk	CT	θ=0°	-	-	5	%

8 Timing characteristics

8.1 Power on sequence

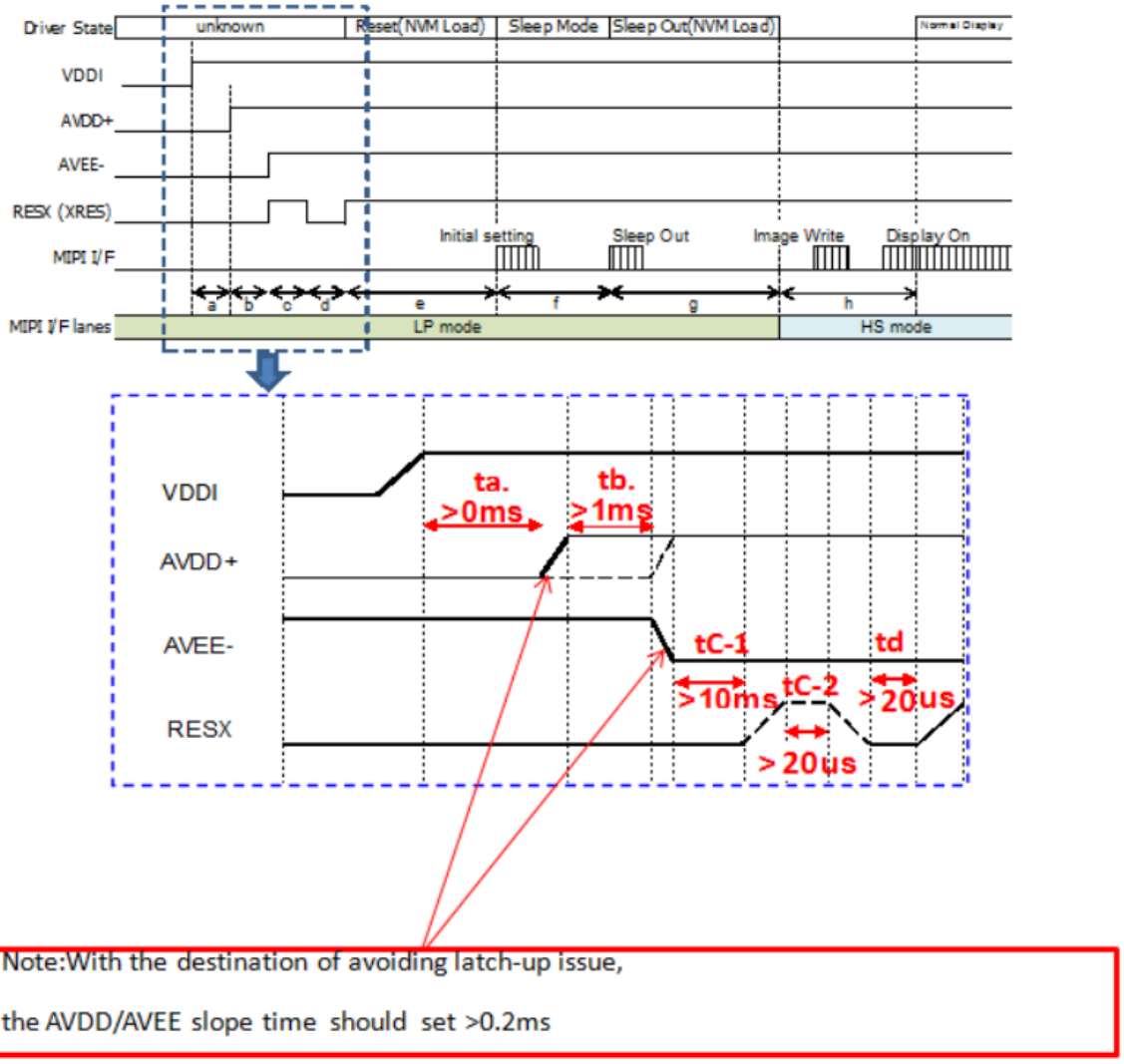
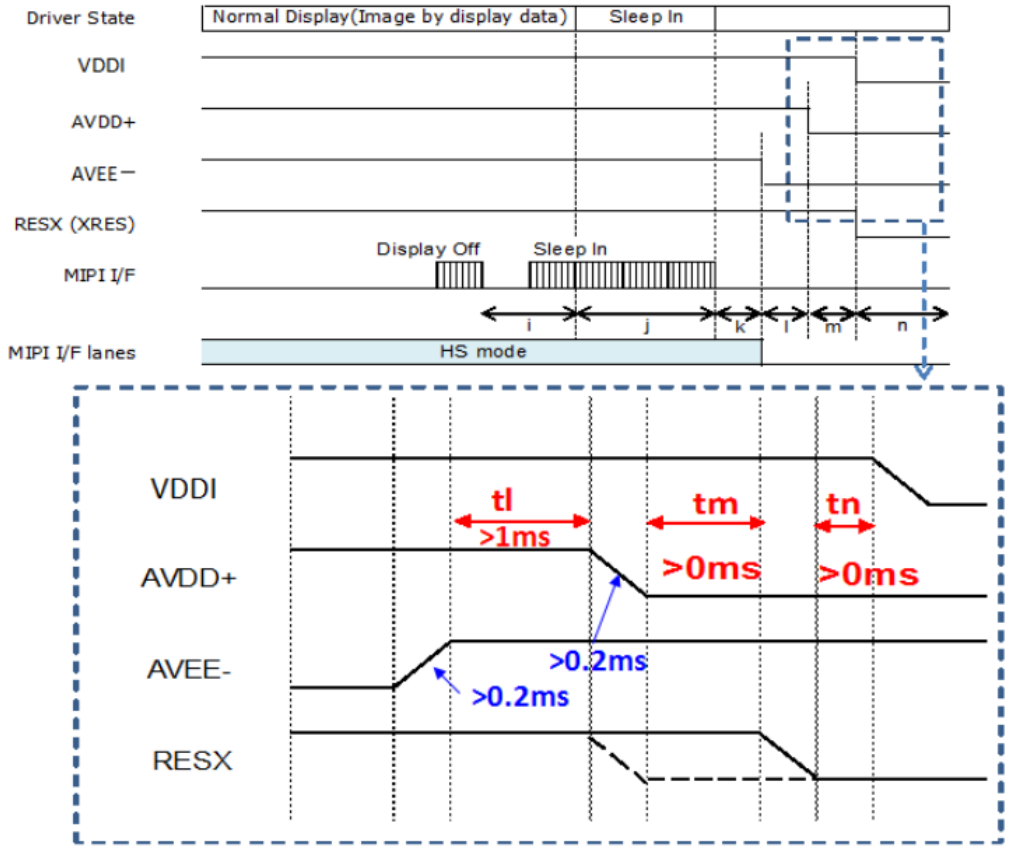


Table 8-1：Recommended Power On Sequence

No.	Address	Parameter	Data	DSI data type	Delay	Command
1	Initial condition					XRES = L
2	Power Supply V DDI (Typ. 1.8V)					V DDI ON
3	Wait				Min.>0ms	(a.) Wait until VDDI power stable
4	Power Supply AV DD+ (Typ. +5.5V)					AV DD+ ON
5	Wait				Min.>1ms	(b.) After wait until AVDD+ power stable (rising slope > 0.2ms)
6	Power Supply AV DD- (Typ. -5.5V)					AV DD- ON
7	Wait				Min. 10ms	(c.) After Wait until AVDD- power stable (rising slope > 0.2ms)
8	RESX High					XRES = H
9	Wait				Min. 20us	
10	RESX go Low					XRES = L
11	Wait				Min. 20us	
12	RESX go High					XRES = H
13	Wait				Min. 10ms	[Automatic] NVM Auto load
14						[Automatic] Sleep Mode On
15	11h	-	-	DCS	05h	Sleep Out
16	Wait				Min. 100ms	
17	29h	-	-	DCS	05h	[Automatic] Sleep Mode Off
18	Display data transfer					Image Write
19						
20	Wait				Min. 40ms	
21						[Automatic] Display On
22	Backlight on					

8.2 Power off sequence



Recommended Power Off Sequence

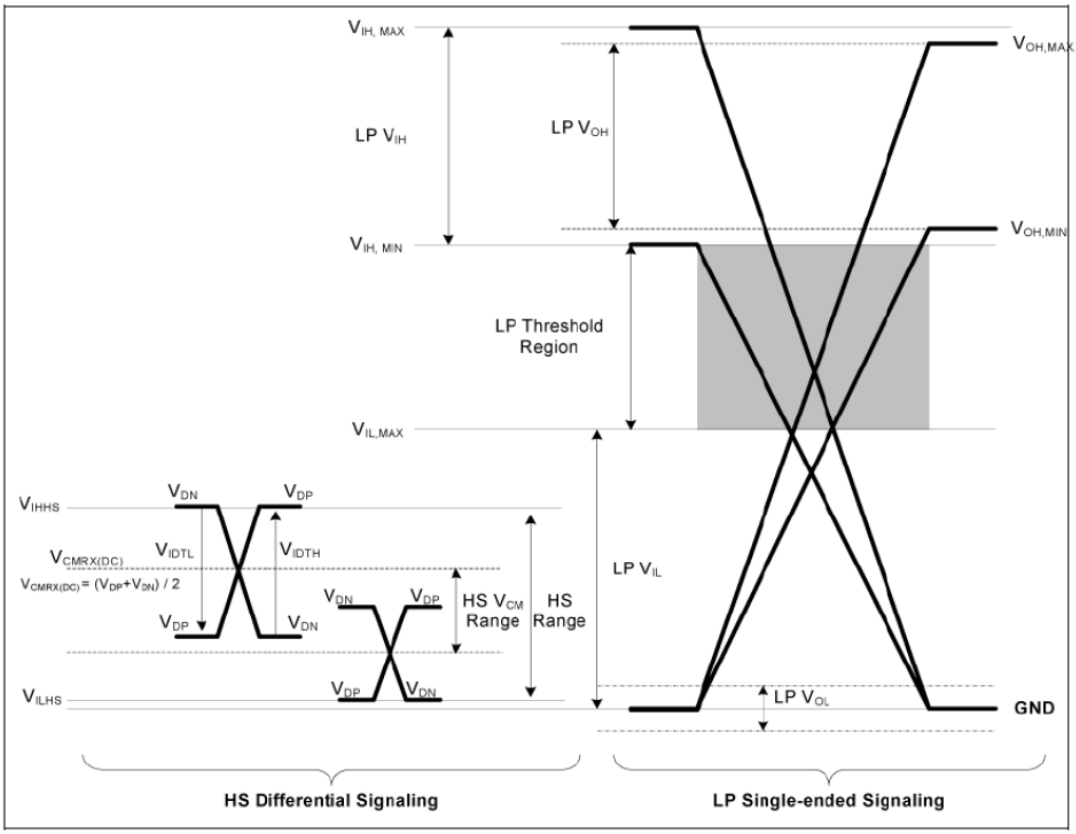
No.	Address	Parameter	Data	DSI data type	Delay	Command
1	28h	-	-	DCS 39h		Display Off
2	Wait				Min.1 frame	
3	10h	-	-	DCS 39h		Sleep In
4	Wait				Min.4 frame	Hsync/Vsync signals should be send after Sleep In command
5						Mipi data transfer Stop
6	AVEE-(Typ -5.5V) OFF					
7					tPOFF1/tPOFF2	Wait
8	AVDD+(Typ +5.5V) OFF					
9					thAVP	Wait
10	RESX Low					XRES = L
11	Wait				Min. 0ms	
12	VDDI OFF (Typ.1.8V) OFF					

8.3 MIPI DC Characteristics

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	70	
	Differential input low threshold	VIDTL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-70	-	-	
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65V~ 1.95V	880	-	1350	
	I/O leakage current	ILEAK	μA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=DPHYVCC= 1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	450	-	-	

Notes: 1. VCMRX (DC) = (VP+VDN)/2

2. Excluding COG resistance (contact resistance and ITO wiring resistance).

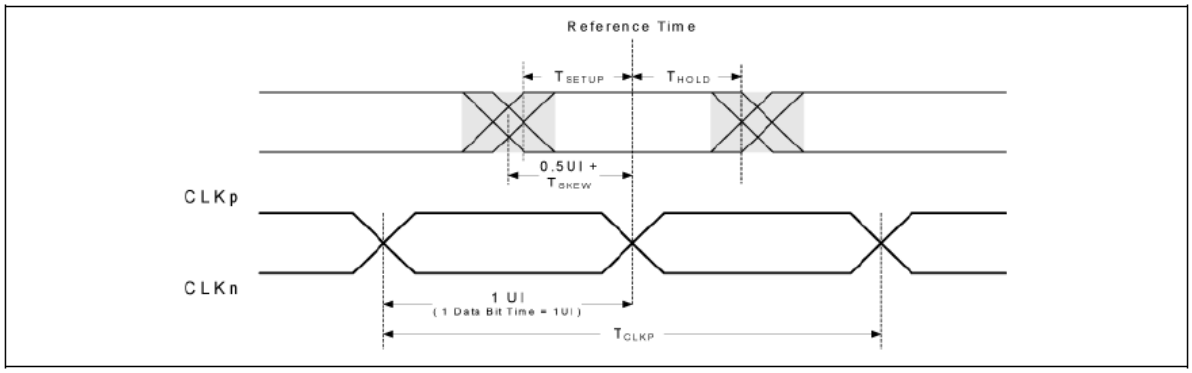

VIH, MAX
LP VIH
VIH, MIN
LP VOH
VOH,MAX
VOH,MIN
LP Threshold Region
VIL,MAX
LP VIL
VIHHS
VDN
VDP
VIDTL
VIDTH
VCMRX(DC)
VCMRX(DC) = (VDP+VDN) / 2
HS VCM Range
HS Range
VILHS
LP VOL
GND
HS Differential Signaling
LP Single-ended Signaling

8.4 MIPI AC Characteristics

A MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	100	-	500	4
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	2	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1,95V	0.15	-	-	6
		ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	6
		ns	IOVCC=1.65V~ 1.95V DPHYVCC=1.65V~ 1.95V	0.15	-	-	5,6

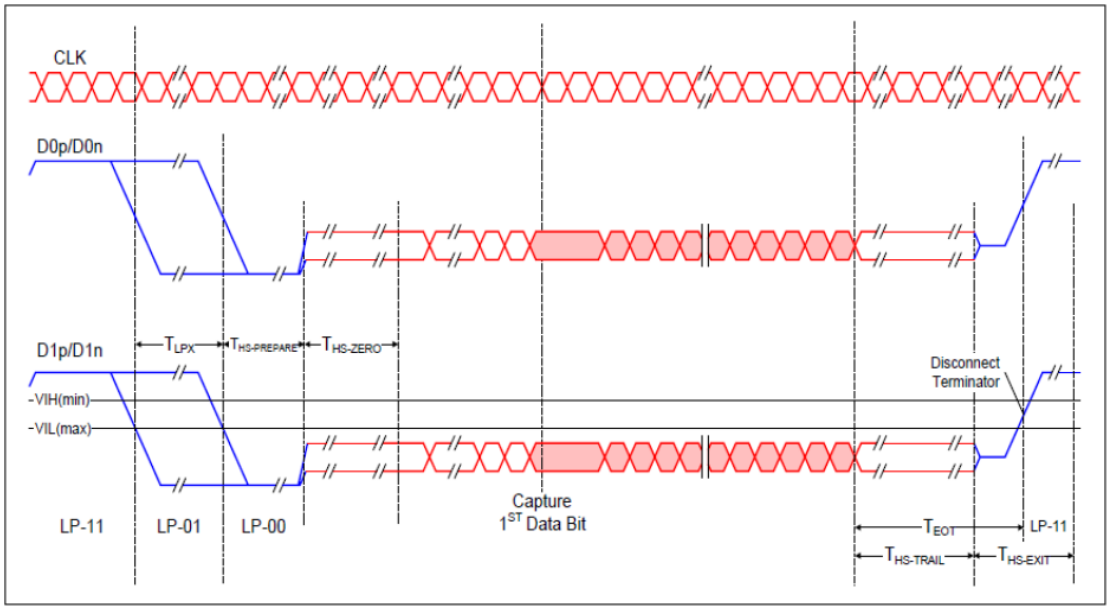
Notes:
4. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
6. tSETUP/tHOLD Time is measured without HS-TX Jitter.

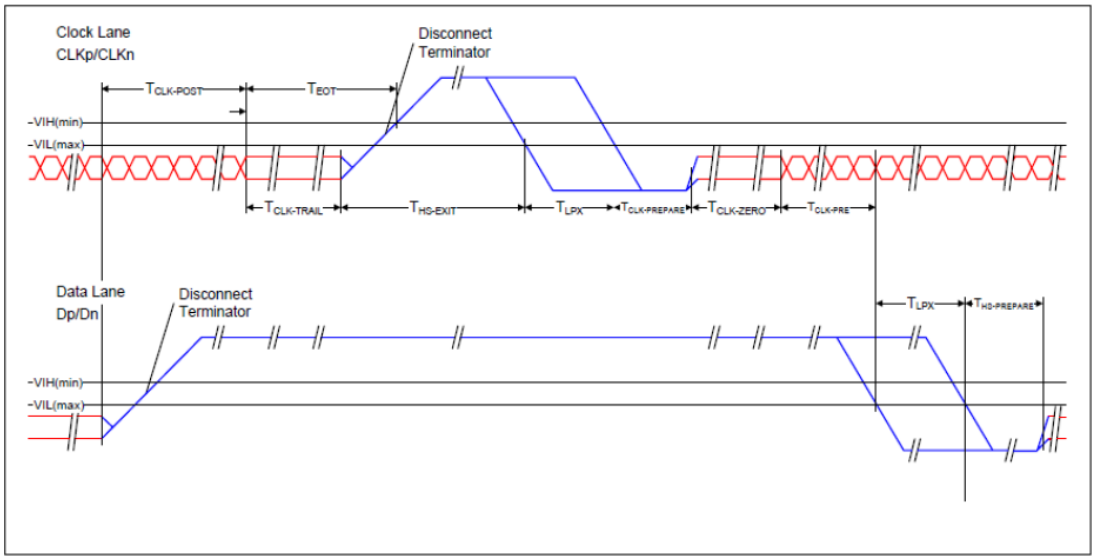


B MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

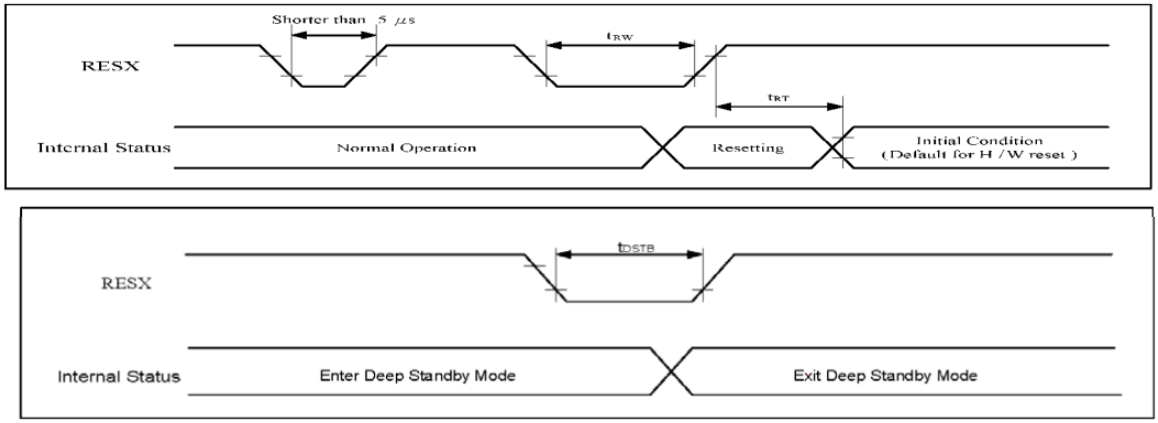
Item	Symbol	Unit	Test condition	Min	Typ	Max	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	40 ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	145ns + 10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	**$T_{HS-TRAIL}$**		IOVCC=DPHYVCC =1.65 ~ 1.95V	max (n*8*UI, 60 ns + n*4*UI)	-	-	1,2
Time to drive LP-11after HS burst	$T_{HS-EXIT}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		IOVCC=DPHYVCC =1.65 ~ 1.95V	$4*T_{LPTX}$			
Time-out before new TX side starts driving	$T_{TA-SURE}$		IOVCC=DPHYVCC =1.65 ~ 1.95V	$1*T_{LPTX}$	-	$2*T_{LPTX}$	
Time to drive LP-00 by new TX	T_{TA-GET}		IOVCC=DPHYVCC =1.65 ~ 1.95V	$5*T_{LPTX}$			
Length of any Low-Power state period	T_{LPX}	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	50	-	-	
Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		IOVCC=DPHYVCC =1.65 ~ 1.95V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	**$T_{CLK-POST}$**		IOVCC=DPHYVCC =1.65 ~ 1.95V	60 ns + 52UI	-	-	3
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC=DPHYVCC =1.65 ~ 1.95V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		IOVCC=DPHYVCC =1.65 ~ 1.95V	-	-	105 ns + n*12*UI	2
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI	IOVCC=DPHYVCC =1.65 ~ 1.95V	-	32	-	4
Length of Low-Power TX period in case of using internal OSC clock	T_{LPTX2}	ns	IOVCC=DPHYVCC =1.65 ~ 1.95V	-	1/(fosc/4)	-	

Notes:
1. If a > b then max(a, b) = a, otherwise max(a, b) = b
2. Where n = 1 for Forward-direction HS mode.
3. The R63423 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63423 can work without the remained process if tCLK-POST is more than 512 UI.
4. The R63423 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled.


CLK
D0p/D0n
D1p/D1n
TLPX
THS-PREPARE
THS-ZERO
VIH(min)
VIL(max)
Disconnect Terminator
LP-11
LP-01
LP-00
Capture 1ST Data Bit
TEOT
LP-11
THS-TRAIL
THS-EXIT


Clock Lane
CLKp/CLKn
Disconnect Terminator
TCLK-POST
TEOT
VIH(min)
VIL(max)
TCLK-TRAIL
THS-EXIT
TLPX
TCLK-PREPARE
TCLK-ZERO
TCLK-PRE
Data Lane
Dp/Dn
Disconnect Terminator
TLPX
THS-PREPARE
VIH(min)
VIL(max)

8.5 Reset timing



Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	t_{RW}	Reset pulse duration	10(Note)	-	us
	t_{RT}	Reset cancel	-	10(Note)	ms
			-	120(Note)	ms
	t_{DSTB}	Reset pulse duration	3	-	ms

Note :

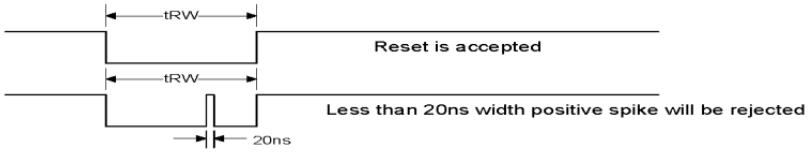
-The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 10 ms after a rising edge of RESX.

-Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below :

RESX	Pulse Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

-During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.

-Spike Rejection also applies during a valid reset pulse as shown below :

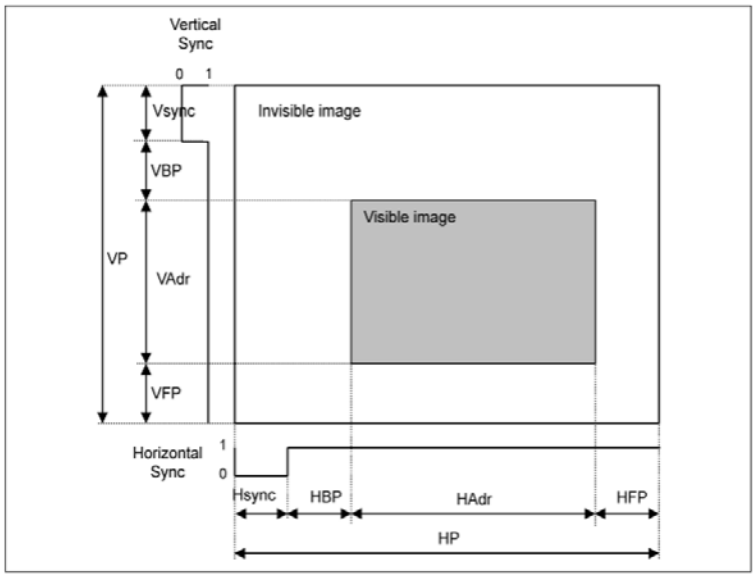


-When Reset applied during Sleep-In Mode.

-When Reset applied during Sleep-Out Mode.

-It is necessary to wait 10ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.

8.6 Display Timing



< Interface Display timing (60Hz, no compression) >

I/F:MIPI DSI 4lane, Dots Size:1440xRGBx1440

Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		24		Pixel
Horizontal active area (HAdr)		1440		Pixel
Horizontal front porch(HFP)		24		Pixel
Vertical low pulse width(VS)		1		H
Vertical front porch(VFP)		8		H
Vertical back porch(VBP)		7		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(58.2)	60	(61.8)	Hz
1H Time	(11.103)	11.446	(11.790)	us
DSI DATA rate	(756.6)	(780.0)	(803.4)	Mbps/Lane

<Interface Display timing (90Hz, with 1/2 compression) *>

I/F:MIPI DSI 4lane, Dots Size:1440xRGBx1440

Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		20		Pixel
Horizontal active area (HAdr)		720		Pixel
Horizontal front porch(HFP)		38		Pixel
Vertical low pulse width(VS)		2		H
Vertical front porch(VFP)		8		H
Vertical back porch(VBP)		6		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(87.3)	90	(92.7)	Hz
1H Time	(7.092)	7.31	(7.552)	us
DSI DATA rate	(593.6)	(612.0)	(630.4)	Mbps/Lane

<Interface Display timing (120Hz, with 1/2 compression) *>

I/F:MIPI DSI 4lane, Dots Size:1440xRGBx1440

Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		20		Pixel
Horizontal active area (HAdr)		720		Pixel
Horizontal front porch(HFP)		38		Pixel
Vertical low pulse width(VS)		2		H
Vertical front porch(VFP)		8		H
Vertical back porch(VBP)		6		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(118.8)	120	(121.2)	Hz
1H Time	(5.663)	5.721	(5.778)	us
DSI DATA rate	(807.8)	(816.0)	(824.1)	Mbps/Lane

Additional Command for 90Hz and 120Hz

Address	Value	Data Type	Comment
EB	82	Genelic long WRITE , 2parameter	1/2 Compression Support
	00		

<Interface Display timing (120Hz, with 1/2 compression) *>

I/F:MIPI DSI 4lane, Dots Size:1440xRGBx1440

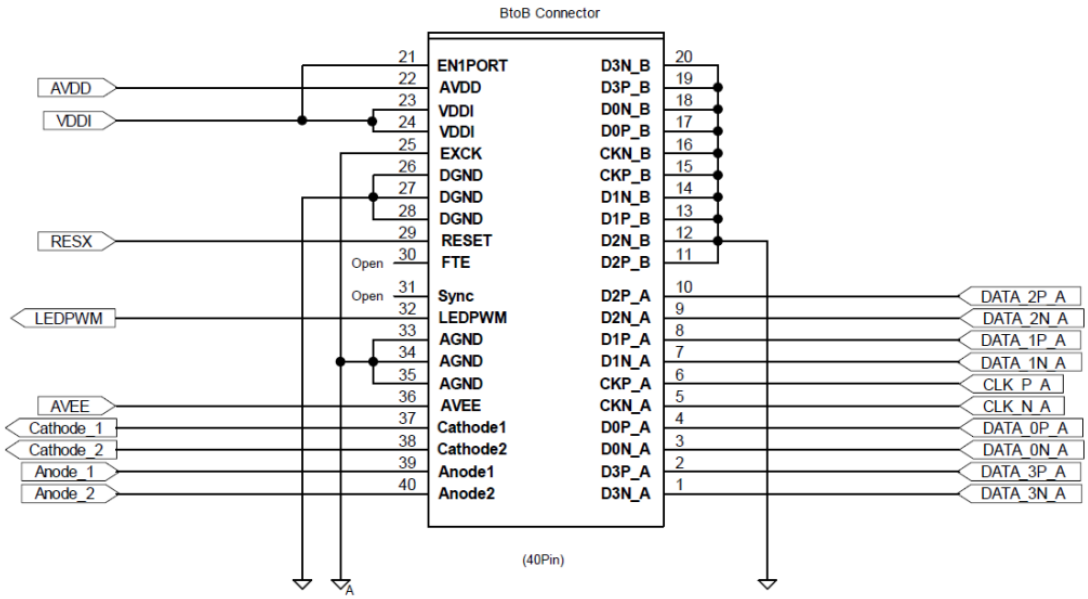
Item	Min	Typ	Max	Unit
Horizontal data start point(HS+HBP)		20		Pixel
Horizontal active area (HAdr)		720		Pixel
Horizontal front porch(HFP)		38		Pixel
Vertical low pulse width(VS)		2		H
Vertical front porch(VFP)		8		H
Vertical back porch(VBP)		6		H
Vertical active area (VAdr)		1440		H
Frame Frequency	(118.8)	120	(121.2)	Hz
1H Time	(5.663)	5.721	(5.778)	us
DSI DATA rate	(807.8)	(816.0)	(824.1)	Mbps/Lane

Additional Command for 90Hz and 120Hz

Address	Value	Data Type	Comment
EB	82	Genelic long WRITE , 2parameter	1/2 Compression Support
	00		

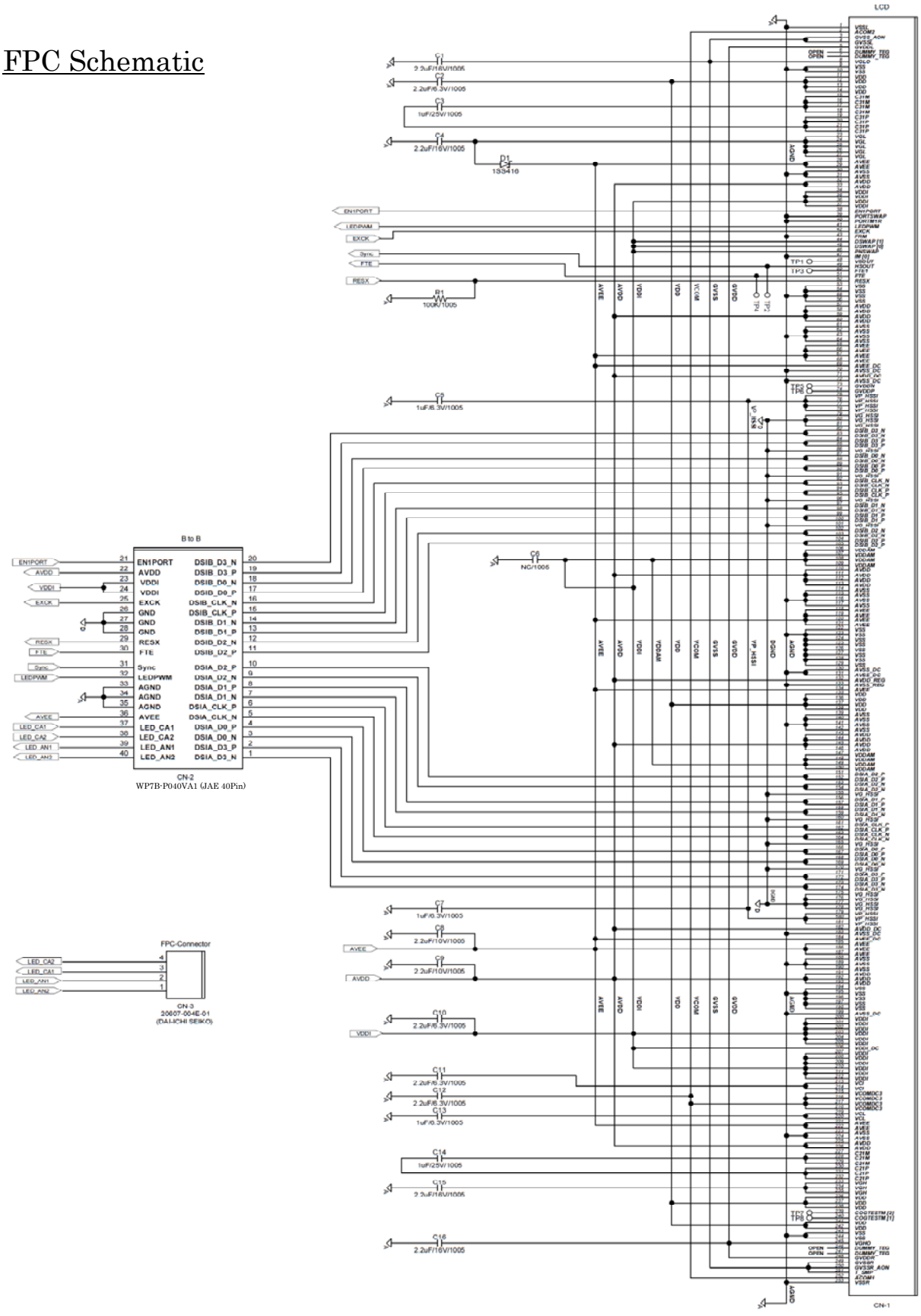
9 Recommended outside circuit

<MIPI DSI (Single Port)>



10 FPC Schematic

FPC Schematic



11 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 120hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 120hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	50℃,90%RH 120hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation.	-30℃/85℃ 20 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Frequency: 5 to 50Hz (Round trip 3 minutes) Acceleration: 1G All Amplitude: 20 to 0.2mm Direction: Up/Down(60min), Left/Right(15min), Front/Back(15min) (3 Direction)	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	±200V, 200pF(0Ω) to Terminals(Contact) (1 time for each terminals) None Operation	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

12 Warranty and Conditions

http://www.displaymodule.com/pages/faq