DisplayModule

DM-TFT28-367

2.8" IPS 240x320 TFT LCD DISPLAY PANEL WITH CAPACITIVE TOUCH - SPI, MCU, RGB

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1 Revision History

Date	Changes
2018-08-15	First release

2 Main Features

Item	Specification	Unit
LCD Type	TFT/TRANSMISSIVE	
Resolution	240(RGB) x 320	pixel
Module Dimension	56.10 x 77.29 x 4.38	mm
TFT Controller IC	ST7789V	-
CTP Driver IC	FT6236	
Interface	8/9/16/18Bit MCU Interface 3/4SPI+16/18Bit RGB Interface 3-line/4-line Serial Interface	-
Display Color	65K/262K	colors
View Direction	All	
Touch mode	Single point and Gestures	
Backlight Type	LED Normally black	-
Weight	TBD	g

3 Pin Description

3.1 TFT

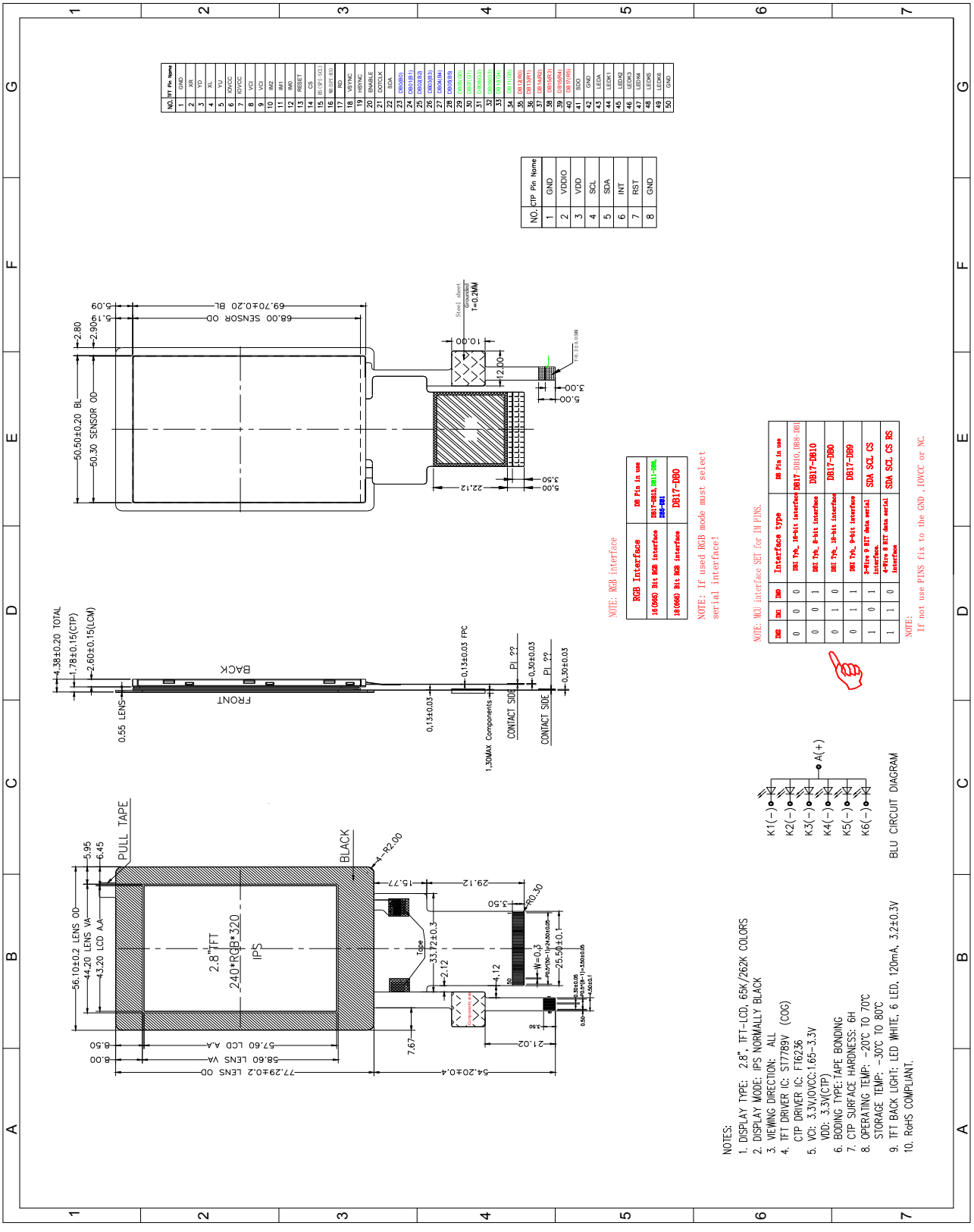
No.	Symbol	Description
1	GND	Ground
2	XR(NC)	Touch panel Right Glass Terminal
3	YD(NC)	Touch panel Bottom Film Terminal
4	XL(NC)	Touch panel LIFT Glass Terminal
5	YU(NC)	Touch panel Top Film Terminal
6	IOVCC	Supply Voltage for IO (1.65-3.3V)
7	IOVCC	Supply Voltage for IO (1.65-3.3V)
8	VCI	Supply voltage(3.3V)
9	VCI	Supply voltage(3.3V)
10	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface. Fix this pin at IOVCC and GND.
11	IM1	
12	IM0	
13	RESET	This signal will reset the device and must be applied to properly initialize the chip.
14	CS	Chip select input pin (“Low” enable). Fix this pin at IOVCC or GND when not in use.
15	RS(SPI-SCL)	This pin is used to select “Data or Command” in the parallel interface. When D/CX = ’1’, data is selected. When D/CX = ’0’, command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. Fix this pin at IOVCC or GND when not in use.
16	WR(SPI-RS)	The data is applied on the rising edge of the SCL signal. If not used, Fix this pin at IOVCC or GND when not in use.
17	RD	Serves as a read signal and MCU read data at the rising edge. Fix this pin at IOVCC or GND when not in use.
18	VSYNC	Frame synchronizing signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
19	HSYNC	Line synchronizing signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
20	ENABLE	Data enable signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
21	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at IOVCC or GND when not in use.
22	SDA	Serial input signal. The data is latched on the rising edge of the SCL signal. Fix this pin at IOVCC or GND when not in use.
23-40	DB0-DB17	Data bus Fix to GND level when not in use
41	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.
42	GND	Ground
43	LEDA	Anode pin of backlight
44	LEDK1	Cathode pin OF backlight

45	LEDK2	Cathode pin OF backlight
46	LEDK3	Cathode pin OF backlight
47	LEDK4	Cathode pin OF backlight
48	LEDK5	Cathode pin OF backlight
49	LEDK6	Cathode pin OF backlight
50	GND	Ground

3.2 CTP

No.	Symbol	Description
1	GND	Ground
2	VDDIO	I/O power supply voltage
3	VDD	Supply voltage
4	SCL	I2C clock input
5	SDA	I2C data input and output
6	INT	External interrupt to the host
7	RST	External Reset, Low is active
8	GND	Ground

4 Mechanical Drawing



5 Electrical Characteristics

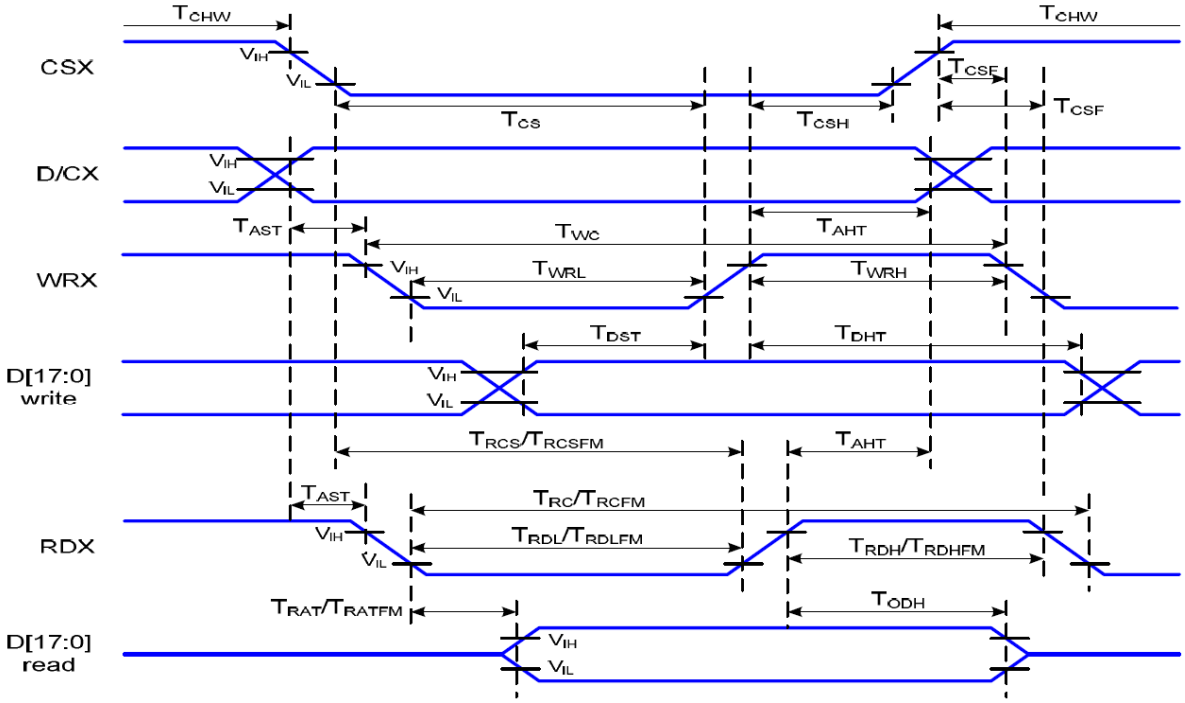
Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCI		2.4	2.8	3.3	V
I/O Digital Voltage	IOVCC		1.65	1.8	3.3	V
Input Current	IDD			6.8		mA
Low Level Input Voltage	V_{IL}		GND		$0.3V_{DDIO}$	V
High Level Input Voltage	V_{IH}		$0.7V_{DDIO}$		VDDIO	V
Low Level Output Voltage	V_{OL}		GND		$0.2V_{DDIO}$	V
High Level Output Voltage	V_{OH}		$0.8V_{DDIO}$		VDDIO	V
Operating Temperature	TOP	Absolute Max	-20	-	+70	℃
Storage Temperature	TST	Absolute Max	-30	-	+80	℃

6 Optical Characteristics

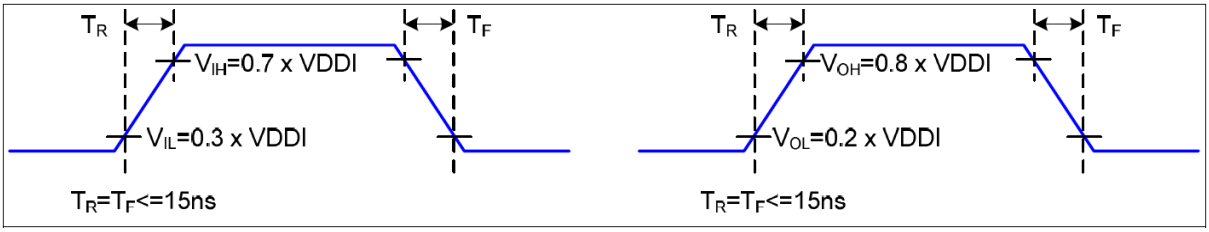
Item	Symbol	Min	Typ	Max	Unit
View Angles TOP	AV	-	80	-	deg
View Angles Bottom	AV	-	80	-	deg
View Angles Right	AH	-	80	-	deg
View Angles Left	AH	-	80	-	deg
Response Time	Tr +Tf		30	40	ms
Contrast Ratio	CR	600	800	-	--
LED Forward Current	If	60	80		mA
LED Forward Voltage	Vf		3.2		V
LCM Luminance	Lv	580	630	-	cd/m^2

7 Timing Characteristics

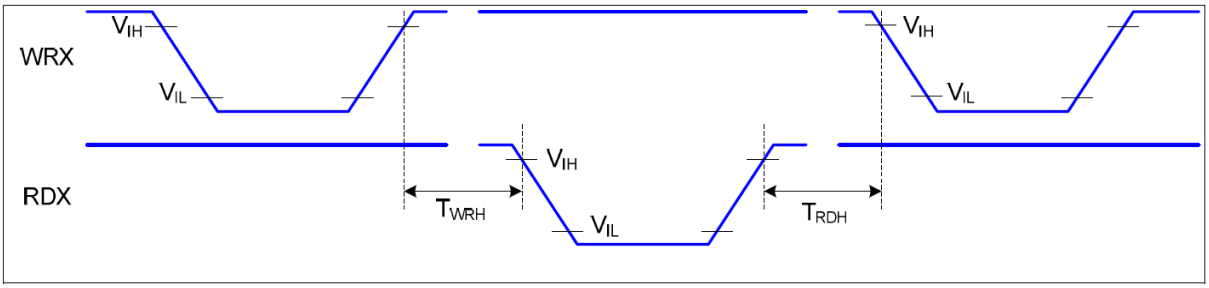
7.1 18/16/9/8-bit Bus MCU Parallel Interface Timing Characteristics



Item	Symbol	Min	Typ	Max	Unit
Address setup time	TAST	0			ns
Address hold time (Write/Read)	TAHT	10			ns
Chip select “H” pulse width	TCHW	0			ns
Chip select setup time (Write)	TCS	15			ns
Chip select setup time (Read ID)	TRCS	45			ns
Chip select setup time (Read FM)	TRCSFM	355			ns
Chip select wait time (Write/Read)	TCSF	10			ns
Chip select hold time	TCSH	10			ns
Write cycle	TWC	66			ns
Control pulse “H” duration	TWRH	15			ns
Control pulse “L” duration	TWRL	15			ns
Read cycle (ID)	TRC	160			ns
Control pulse “H” duration (ID)	TRDH	90			ns
Control pulse “L” duration (ID)	TRDL	45			ns
Read cycle (FM)	TRCFM	450			ns
Control pulse “H” duration (FM)	TRDHFM	90			ns
Control pulse “L” duration (FM)	TRDLFM	355			ns
Data setup time	TDST	10			ns
Data hold time	TDHT	10			ns
Read access time (ID)	TRAT			40	ns
Read access time (FM)	TRATFM			340	ns
Output disable time	TODH	20		80	ns



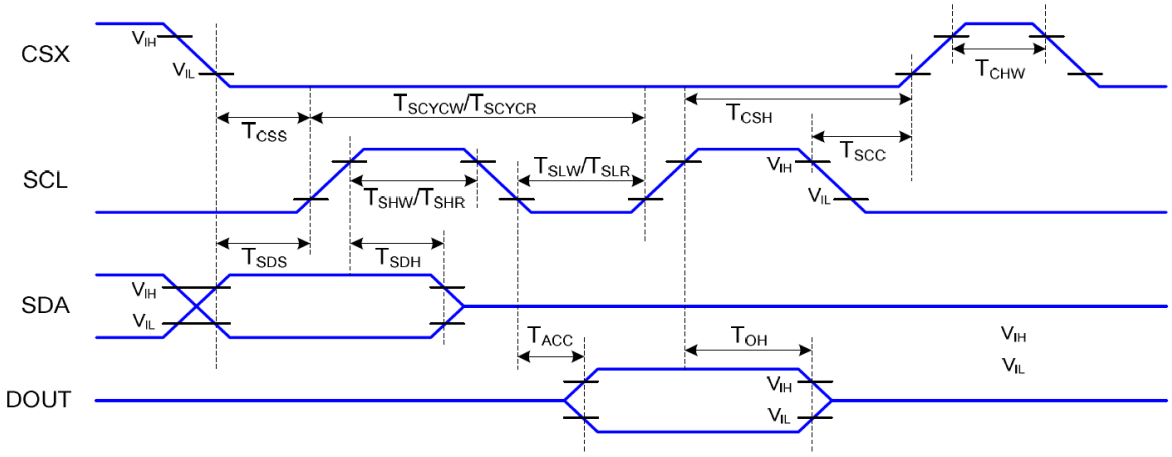
Rising and Falling Timing for I/O Signal



Write-to-Read and Read-to-Write Timing

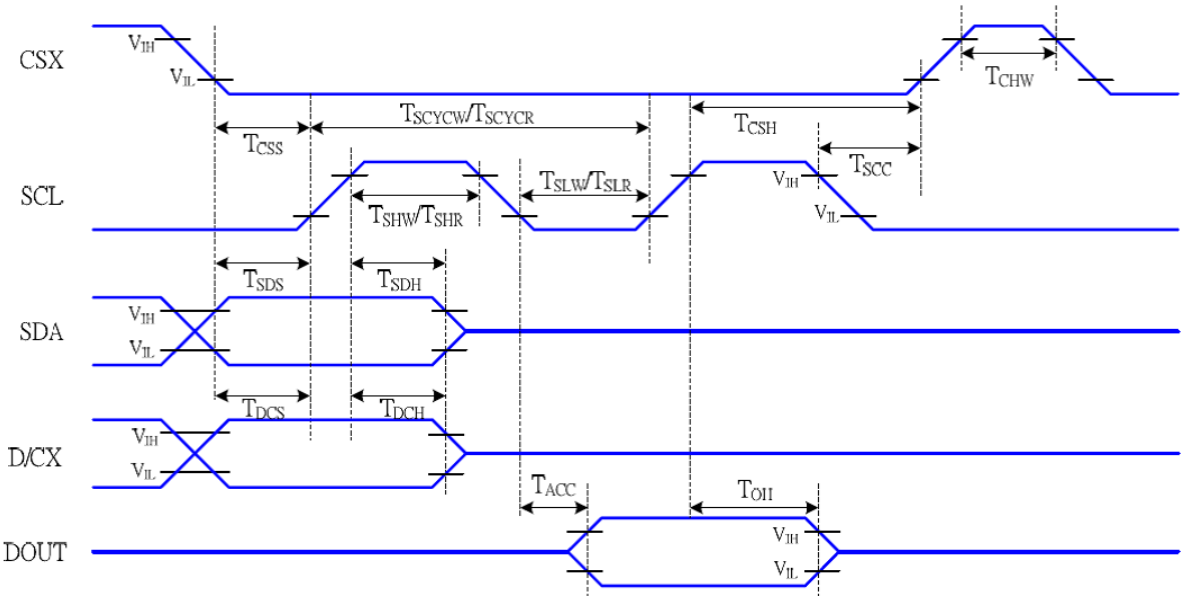
Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.2 Display Serial Interface Timing Characteristics (3-line SPI system)



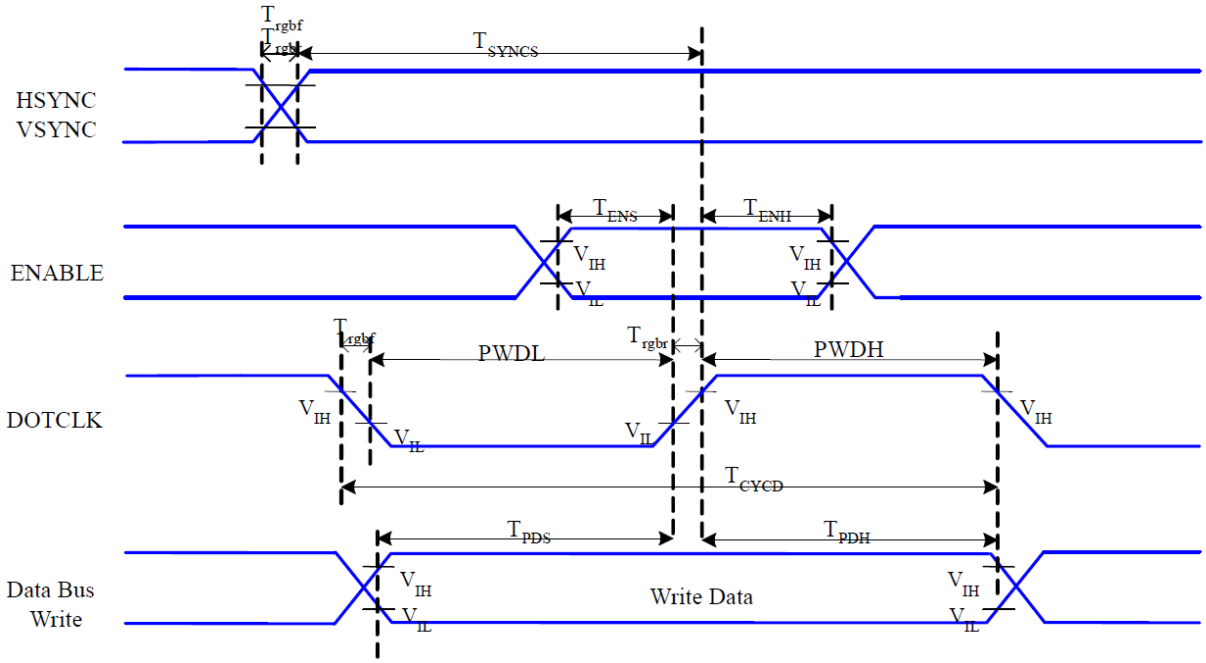
Item	Symbol	Min	Typ	Max	Unit
Chip select setup time (Write)	TCSS	15			ns
Chip select hold time (write)	TCSH	15			ns
Chip select setup time (read)	TCSS	60			ns
Chip select hold time (read)	TSCC	65			ns
Chip select “H” pulse width	TCHW	40			ns
Serial clock cycle (Write)	TSCYCW	66			ns
SCL “H” pulse width (Write)	TSHW	15			ns
SCL “L” pulse width (Write)	TSLW	15			ns
Serial clock cycle (Read)	TSCYCR	150			ns
SCL “H” pulse width (Read)	TSHR	60			ns
SCL “L” pulse width (Read)	TSLR	60			ns
Data setup time	TSDS	10			ns
Data hold time	TSDH	10			ns
Access time	TACC	10		50	ns
Output disable time	TOH	15		50	ns

7.3 Display Serial Interface Timing Characteristics (4-line SPI system)



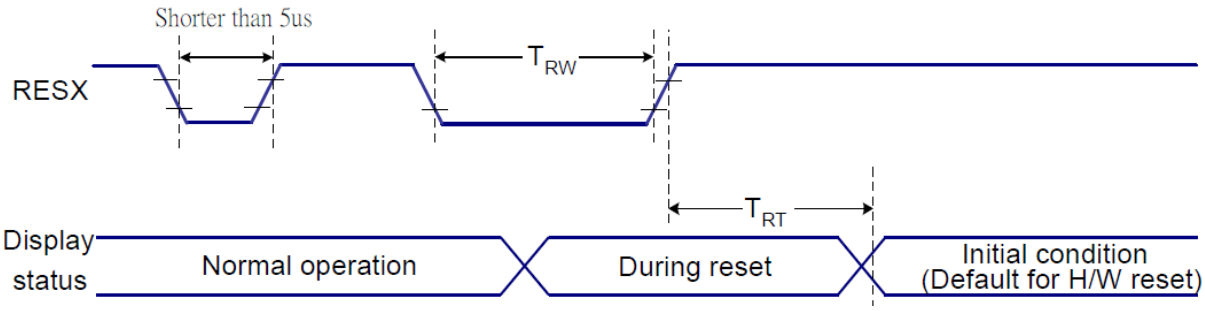
Item	Symbol	Min	Typ	Max	Unit
Chip select setup time (Write)	TCSS	15			ns
Chip select hold time (write)	TCSH	15			ns
Chip select setup time (read)	TCSS	60			ns
Chip select hold time (read)	TSCC	65			ns
Chip select “H” pulse width	TCHW	40			ns
Serial clock cycle (Write)	TSCYCW	66			ns
SCL “H” pulse width (Write)	TSHW	15			ns
SCL “L” pulse width (Write)	TSLW	15			ns
Serial clock cycle (Read)	TSCYCR	150			ns
SCL “H” pulse width (Read)	TSHR	60			ns
SCL “L” pulse width (Read)	TSLR	60			ns
D/CX setup time	TDCS	10			ns
D/CX hold time	TDCH	10			ns
Data setup time	TSDS	10			ns
Data hold time	TSDH	10			ns
Access time	TACC	10		50	ns
Output disable time	TOH	15		50	ns

7.4 Parallel RGB Interface Timing Characteristics



Item	Symbol	Min	Typ	Max	Unit
VSYNC, HSYNC Setup Time	TSYNCS	30			ns
Enable Setup Time	TENS	25			ns
Enable Hold Time	TENH	25			ns
DOTCLK High-level Pulse Width	PWDH	60			ns
DOTCLK Low-level Pulse Width	PWDL	60			ns
DOTCLK Cycle Time	TCYCD	120			ns
DOTCLK Rise/Fall time	Trghr/Trghf			20	ns
PD Data Setup Time	TPDS	50			ns
PD Data Hold Time	TPDH	50			ns

7.5 Reset Timing Characteristics



Item	Symbol	Min	Typ	Max	Unit
Reset pulse duration	TRW	10			us
Reset cancel	TRT			5(note 1,5)	ms
				120(note 1,6,7)	ms

Notes:

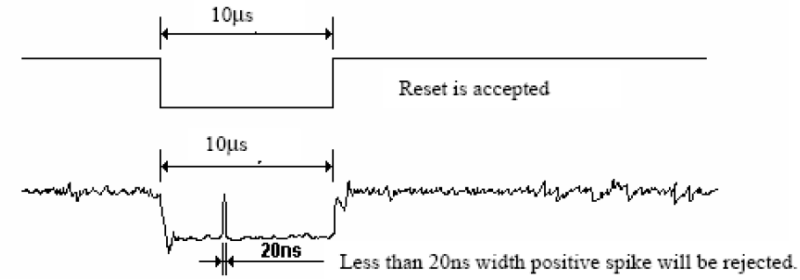
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 CTP Specification

8.1 Elective Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VDD		0.3	3.3	3.6	V
I/O Digital Voltage	VDDIO		1.8	-	3.6	V
Input Current	IDD			4		mA
Low Level Input Voltage	V_{IL}		-0.3		0.3VDDIO	V
High Level Input Voltage	V_{IH}		0.7 VDDIO		VDDIO	V
Low Level Output Voltage	V_{OL}		-		0.3VDDIO	V
High Level Output Voltage	V_{OH}		0.7 VDDIO		-	V
Operating Temperature	TOP	Absolute Max	-20		+70	℃
Storage Temperature	TST	Absolute Max	-30		+80	℃

8.2 Timing Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
OSC clock 1	Fosc 1	VDDA=2.8V; Ta=25℃	34.64	35	35.35	MHz

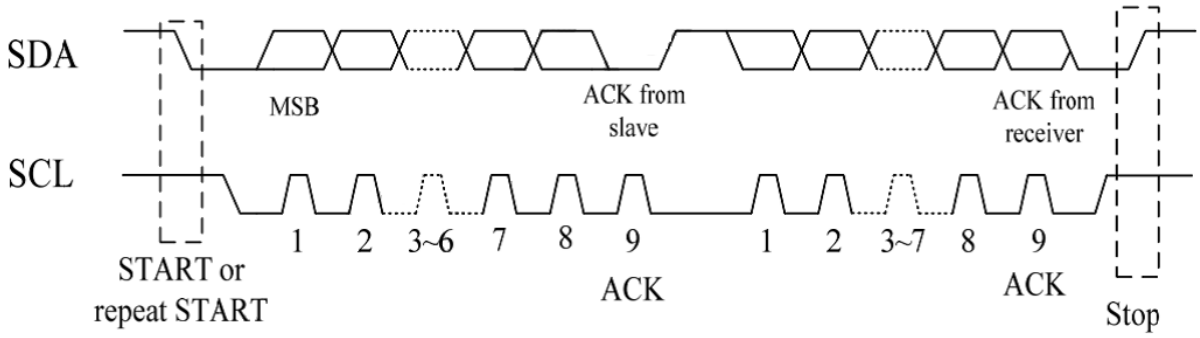
AC characteristics of Oscillators

Item	Symbol	Condition	Min	Typ	Max	Unit
Sensor acceptable clock	ftx	VDDA=2.8V; Ta=25℃	0	100	300	KHz
Sensor output rise time	Ttxr	VDDA=2.8V; Ta=25℃	-	100	-	nS
Sensor output fall time	Ttxf	VDDA=2.8V; Ta=25℃	-	80	-	nS
Sensor input voltage	Trxi	VDDA=2.8V; Ta=25℃	-	5	-	V

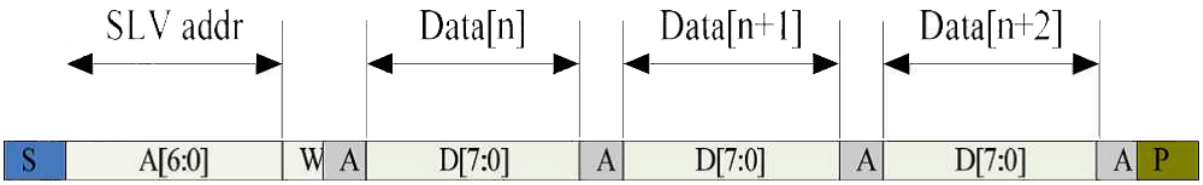
AC Characteristics of sensor

I2C Interface

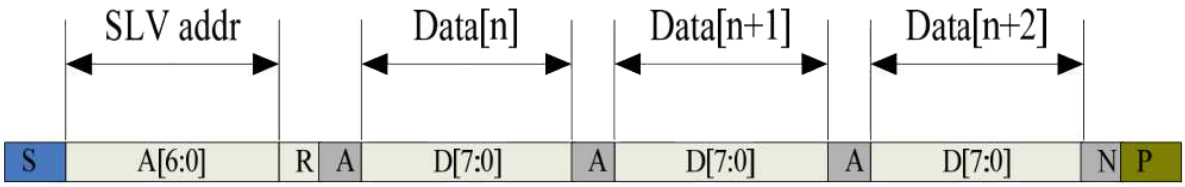
The I2C is always configured in the Slave mode.



I2C Serial Data Transfer Format



I2C master write, slave read



I2C master read, slave write

Mnemonics Description

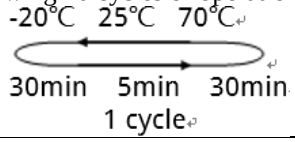
Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit; ‘1’ for read, ‘0’ for write
A(N)	ACK(NACK)
P	STOP:the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

Slave Address is 0x38;

I2C Interface Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup time for STOP condition	4.0	\	us

9 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation. 	-20℃/70℃ 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container

10 Warranty and Conditions

http://www.displaymodule.com/pages/faq